

## 40V N+P-Channel Enhancement Mode MOSFET

### Description

The AP15G04NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 21A$

$R_{DS(ON)} < 17m\Omega$  @  $V_{GS}=10V$

$V_{DS} = -40V$   $I_D = -18A$

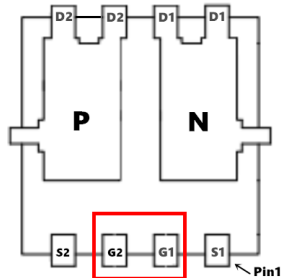
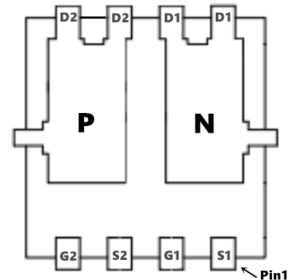
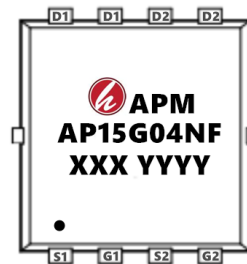
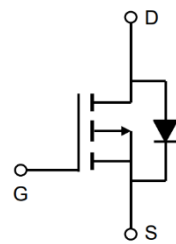
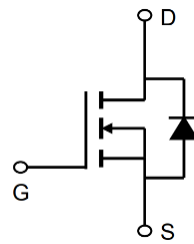
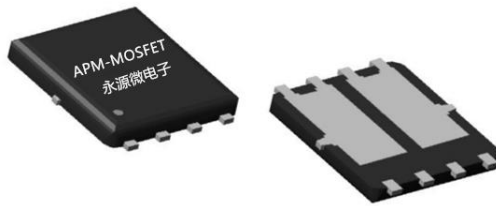
$R_{DS(ON)} < 45m\Omega$  @  $V_{GS}=-10V$

### Application

Wireless charging

Boost driver

Brushless motor



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15G04NF	PDFN5*6-8L	AP15G04NF XXX YYYY	5000
AP15G04NF-A	PDFN5*6-8L	AP15G04NF-A XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
$V_{DS}$	Drain-Source Voltage	40	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	21	-18	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	17.5	-14	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	38	-32	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	66	66	mJ
$I_{AS}$	Avalanche Current	28.8	-23.2	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	25	31.3	W
$T_{STG}$	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	5		$^\circ C/W$

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### Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	46	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=1mA$	---	0.032	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=15A$	---	13.5	17	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$	---	18.4	24	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.8	---	$mV/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=15A$	---	34	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.1	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=32V, V_{GS}=4.5V, I_D=15A$	---	10	---	nC
$Q_{gs}$	Gate-Source Charge		---	2.55	---	
$Q_{gd}$	Gate-Drain Charge		---	4.8	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=20V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	2.8	---	ns
$T_r$	Rise Time		---	12.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	21.2	---	
$T_f$	Fall Time		---	6.4	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	1013	---	pF
$C_{oss}$	Output Capacitance		---	107	---	
$C_{rss}$	Reverse Transfer Capacitance		---	76	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	40	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	85	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=15A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	10	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	3.1	---	nC

#### Note :

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=10A$
- 4、The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

## 40V N+P-Channel Enhancement Mode MOSFET

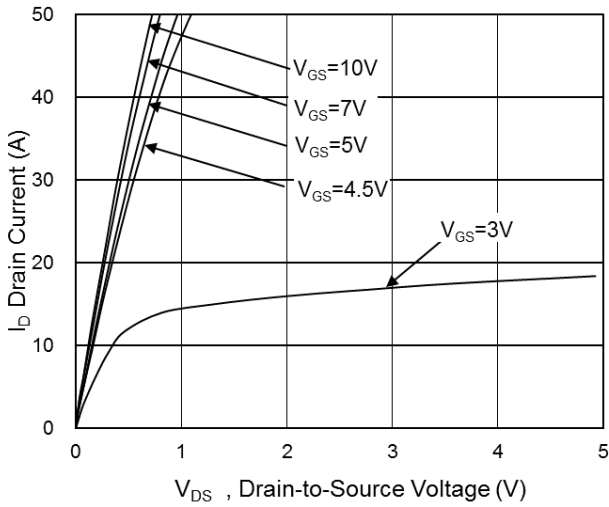
### Electrical Characteristics (T<sub>c</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-40	-46	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.012	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A	---	35	45	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	---	48	60	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	-1.6	-2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	4.32	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-8A	---	12.6	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	13	16	Ω
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-12A	---	9	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	2.54	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	3.1	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-1A	---	19.2	---	ns
T <sub>r</sub>	Rise Time		---	12.8	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	48.6	---	
T <sub>f</sub>	Fall Time		---	4.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	1004	---	pF
C <sub>oss</sub>	Output Capacitance		---	108	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	80	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current			-20	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>				-40	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C			-1	V

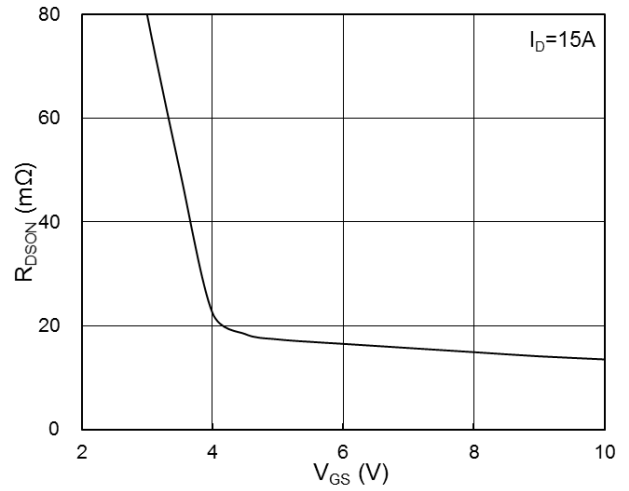
#### Note :

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%
- 3、The EAS data shows Max. rating. The test condition is V<sup>DD</sup>=-25V, V<sup>GS</sup>=-10V, L=0.1mH, I<sup>AS</sup>=-10A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

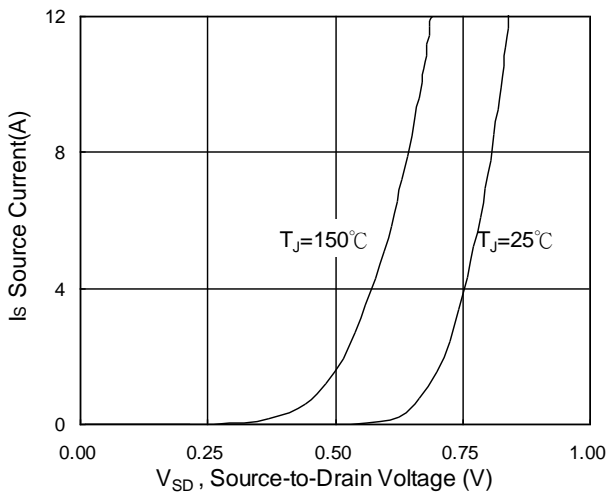
**N-Typical Characteristics**



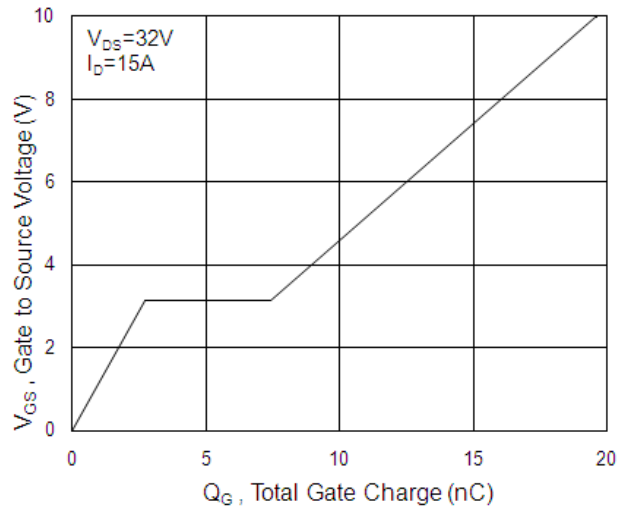
**Fig.1 Typical Output Characteristics**



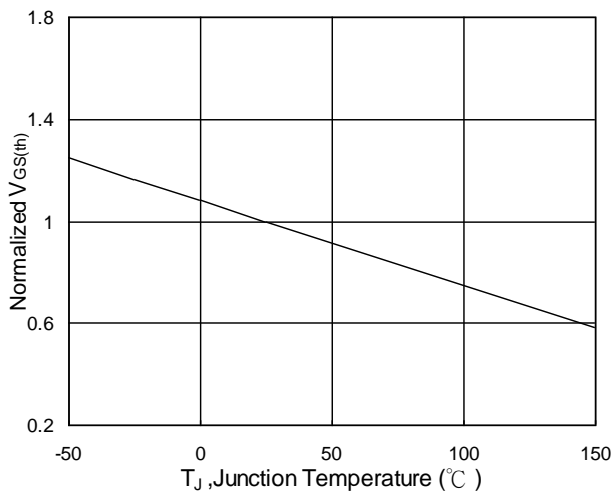
**Fig.2 On-Resistance vs. G-S Voltage**



**Fig.3 Forward Characteristics of Reverse**

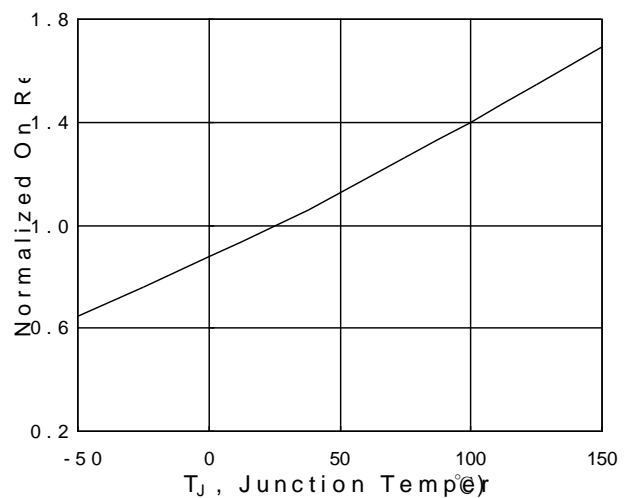


**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

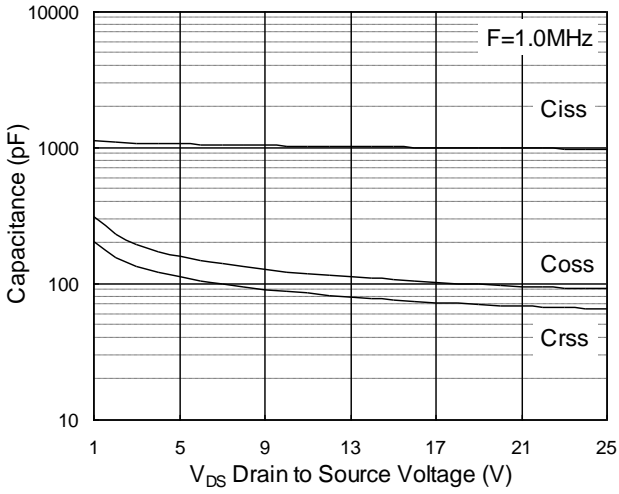
AP15G04NF RVE1.0



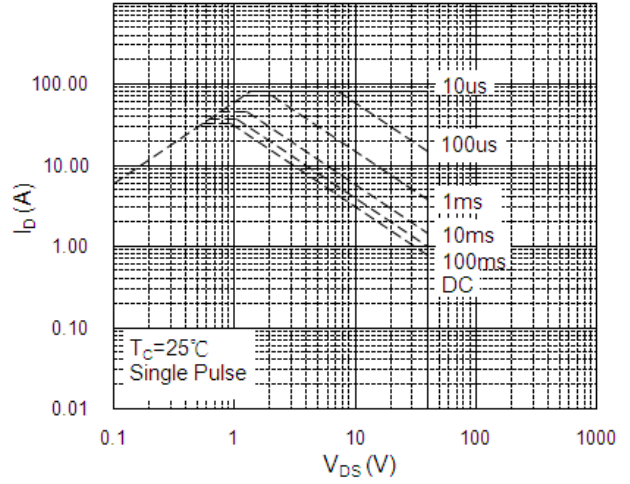
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

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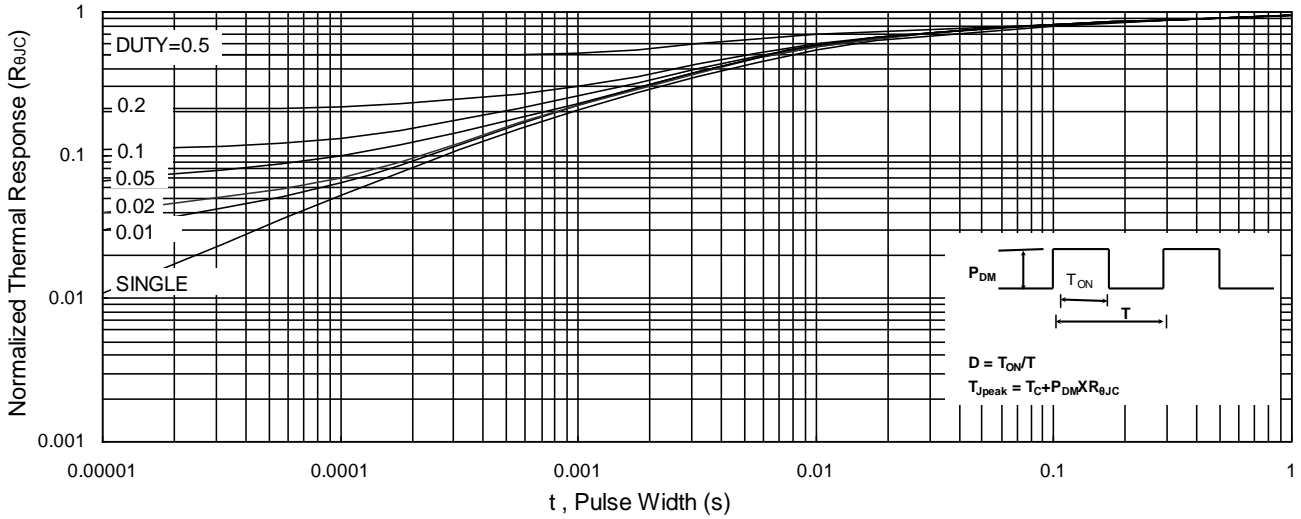
## 40V N+P-Channel Enhancement Mode MOSFET



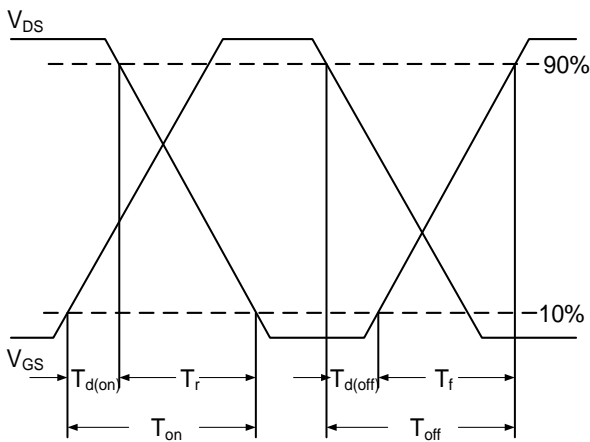
**Fig.7 Capacitance**



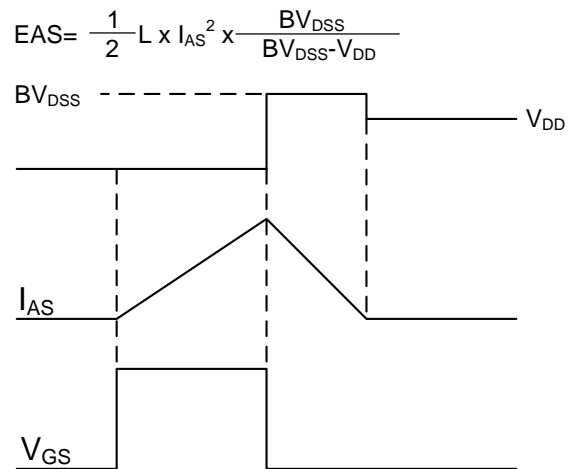
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

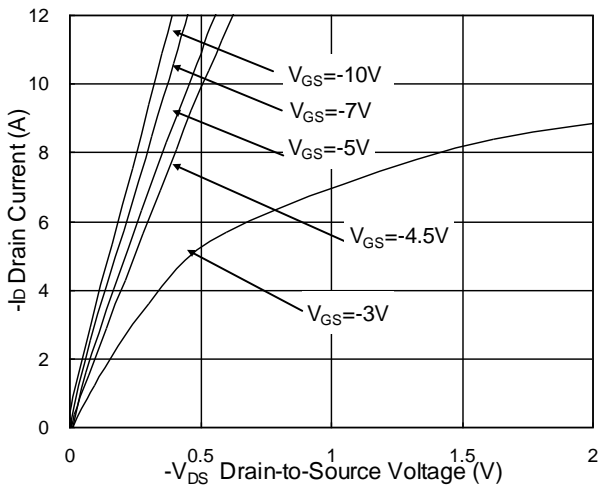


**Fig.10 Switching Time Waveform**

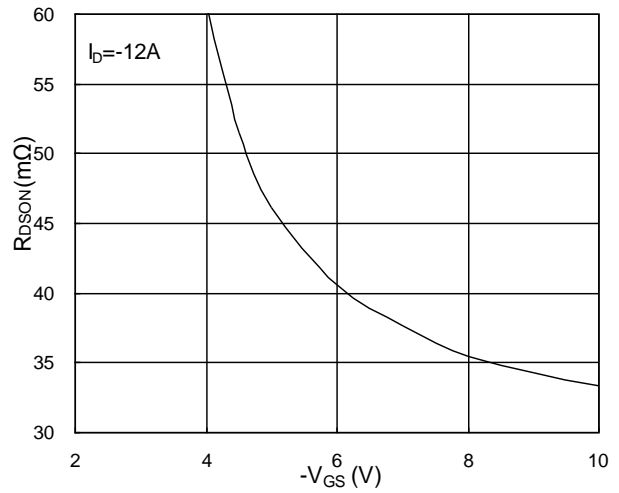


**Fig.11 Unclamped Inductive Switching Waveform**

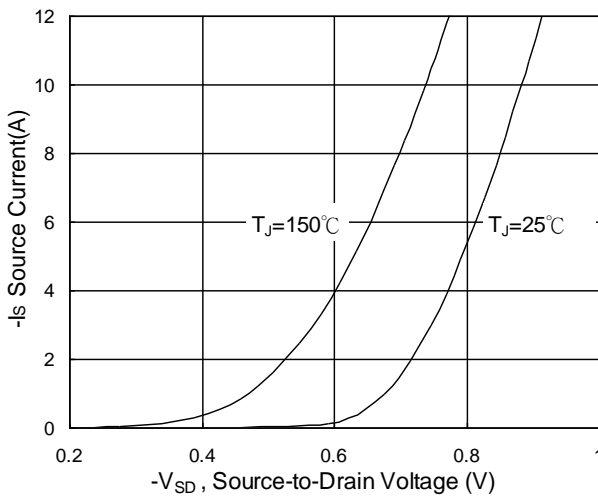
**P-Typical Characteristics**



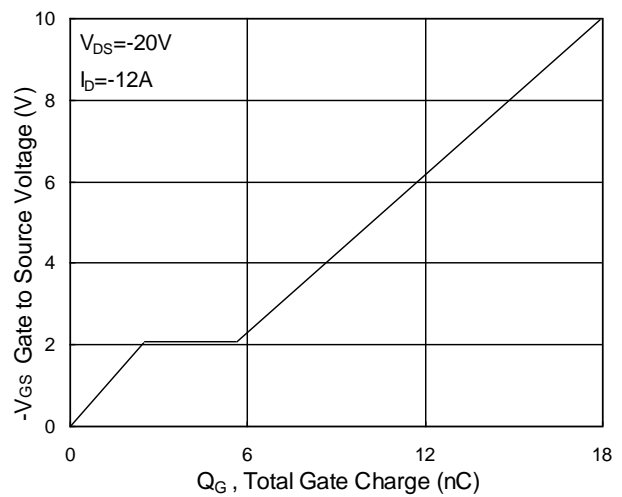
**Fig.1 Typical Output Characteristics**



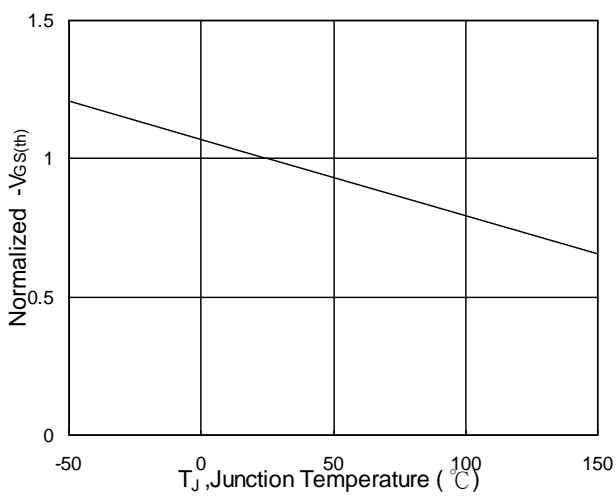
**Fig.2 On-Resistance v.s Gate-Source**



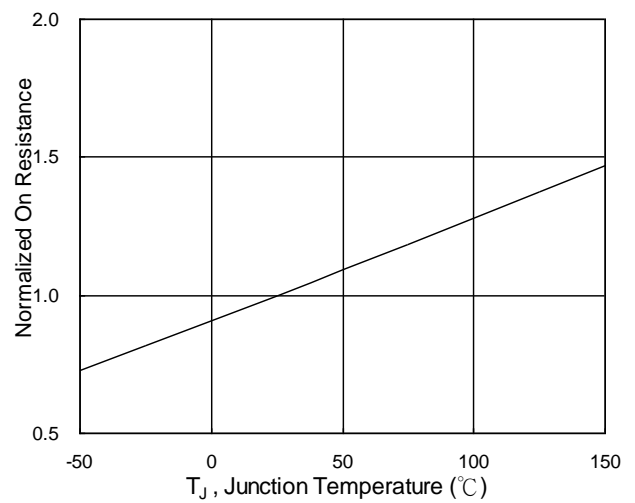
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

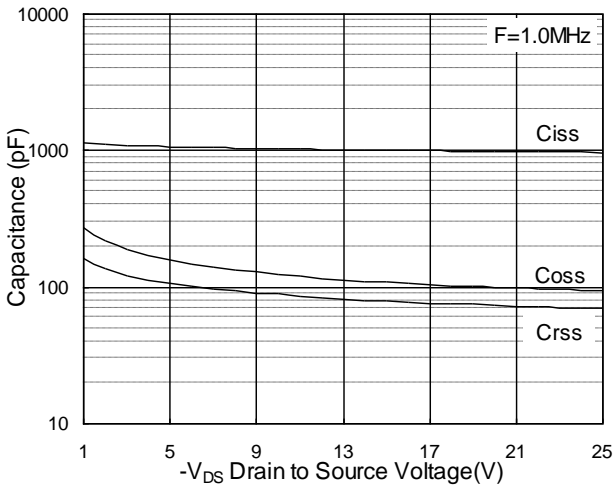


**Fig.5 Normalized V<sub>GS(th)</sub> v.s T<sub>J</sub>**

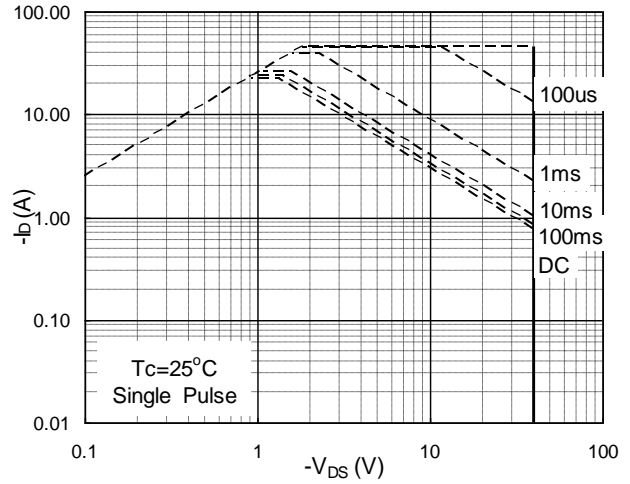


**Fig.6 Normalized R<sub>DS(on)</sub> v.s T<sub>J</sub>**

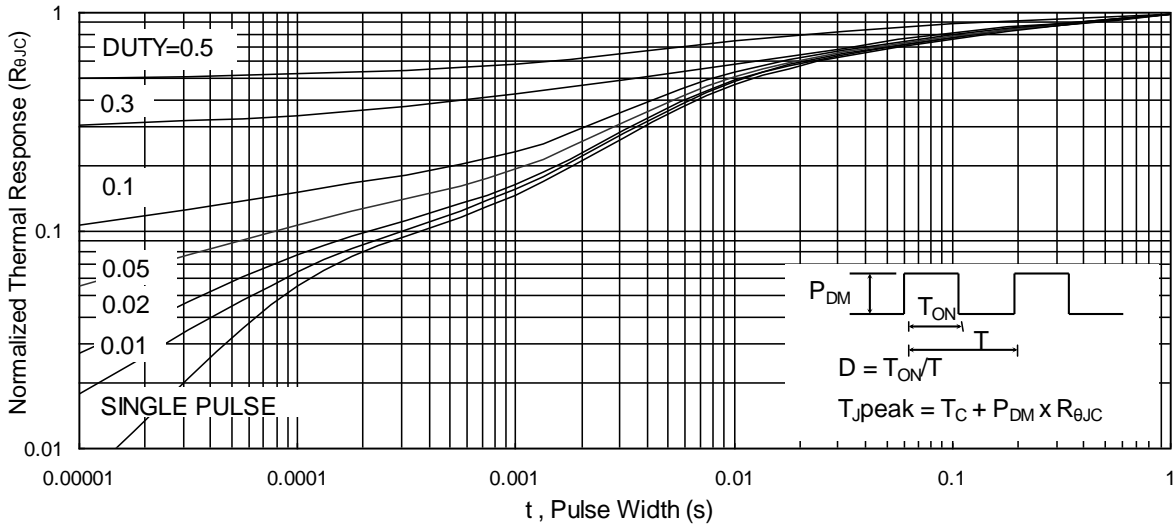
**40V N+P-Channel Enhancement Mode MOSFET**



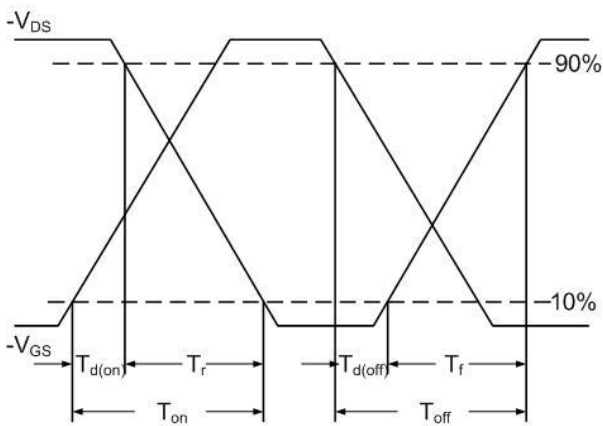
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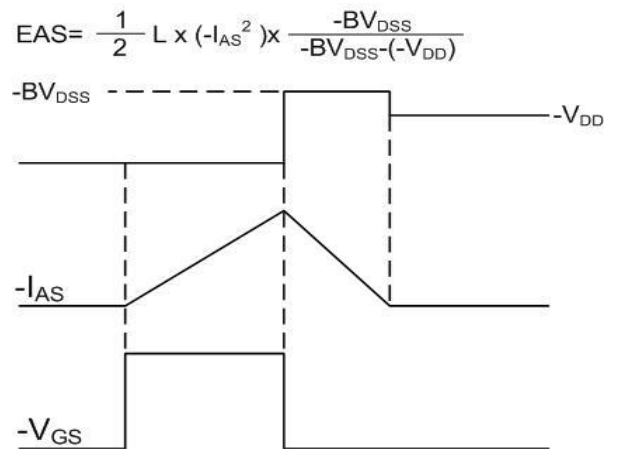
**Fig.8 Safe Operating Area**



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**Fig.10 Switching Time Waveform**

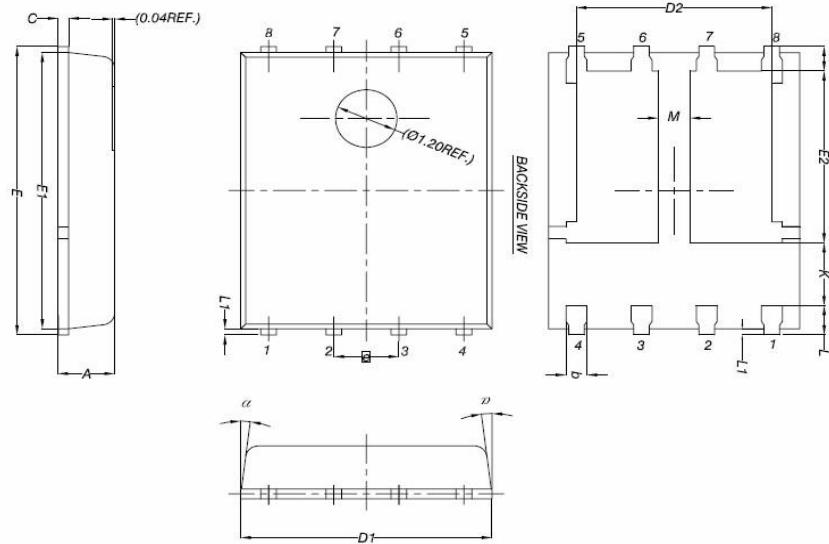


**Fig.11 Unclamped Inductive Waveform**



## 40V N+P-Channel Enhancement Mode MOSFET

### Package Mechanical Data-DFN5\*6-8L-JQ Double



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.66	5.76	5.83
E2	3.37	3.47	3.58
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°



**40V N+P-Channel Enhancement Mode MOSFET****Attention**

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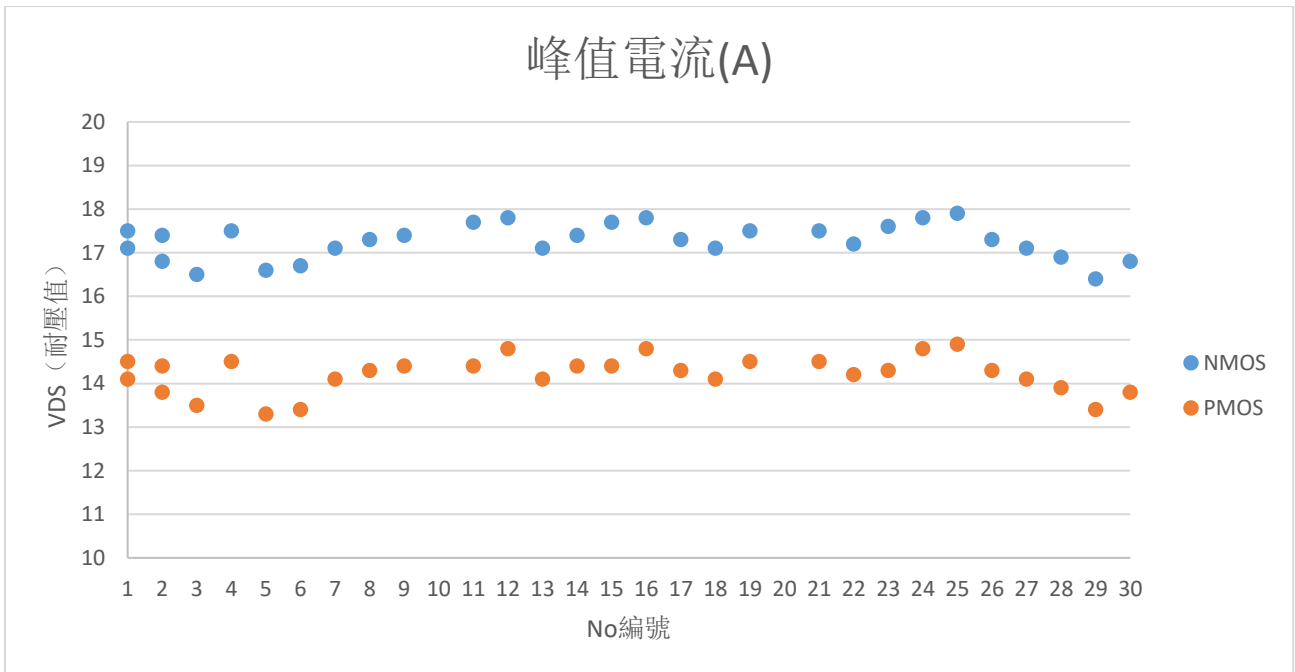
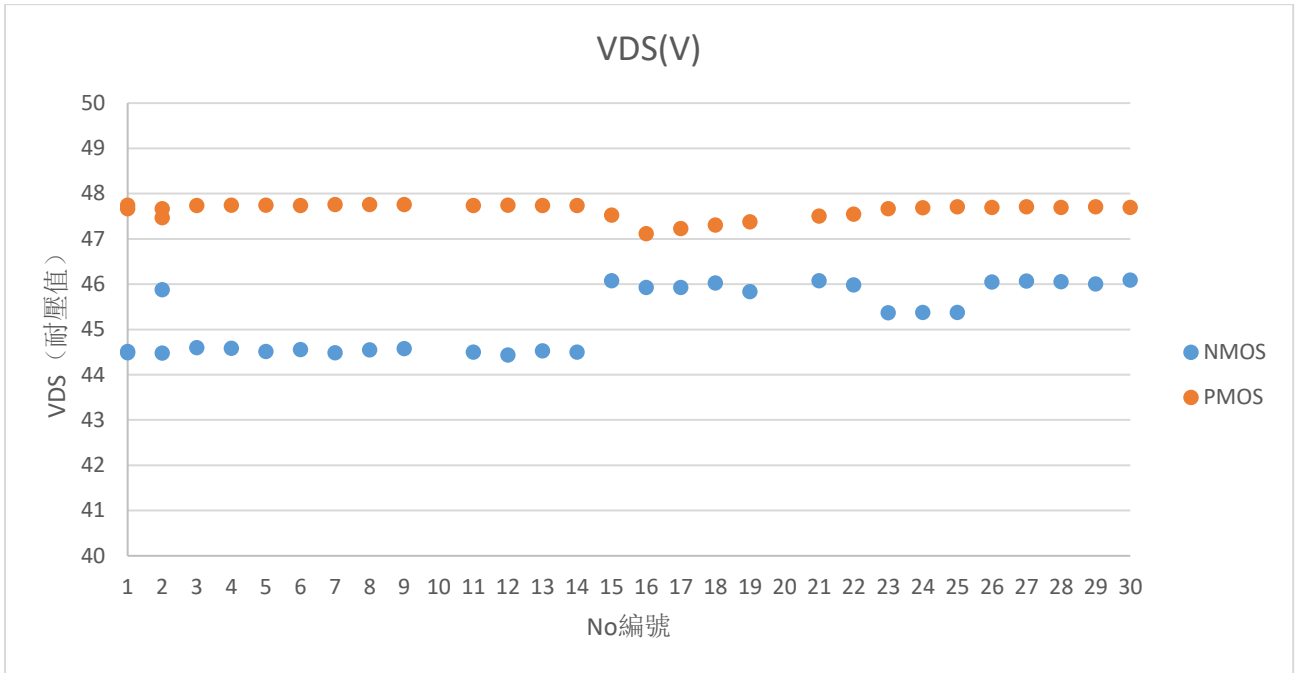
Edition	Date	Change
Rve1.0	2020/2/30	Initial release

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**40V N+P-Channel Enhancement Mode MOSFET**

Test Report For 30PCS (30pcs 典型測試報告)

Simulation 24V Brushless motor



測試條件：工作電壓：25V 驅動電壓：10V