

## 30V N+P-Channel Enhancement Mode MOSFET

### Description

The AP15G03NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

Battery protection or in other Switching application.

### General Features

$V_{DS} = 30V$   $I_D = 18A$

$R_{DS(ON)} < 22m\Omega$  @  $V_{GS}=10V$  (Type: 15m $\Omega$ )

$V_{DS} = -30V$   $I_D = -15A$

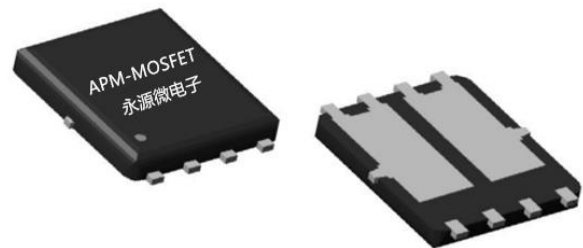
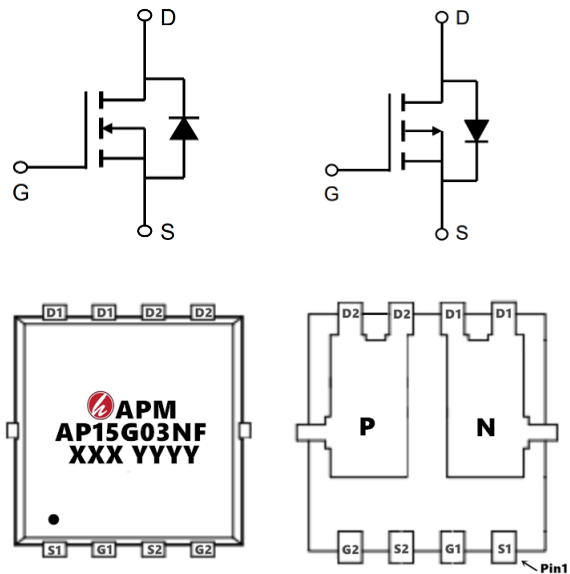
$R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=-10V$  (Type: 25m $\Omega$ )

### Application

Wireless charging

Boost driver

Brushless motor



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15G03NF	PDFN5*6-8L	AP15G03NF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	18	-15	A
$I_D@T_A=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	-8	A
IDM	Pulsed Drain Current <sup>2</sup>	52	-45	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	22	45	mJ
IAS	Avalanche Current	21	-30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	18	18	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	55		$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> ( $t \leq 10sec$ )	5		$^\circ C/W$

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### Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	32.5	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=10A$	---	15	22	m $\Omega$
		$V_{GS}=4.5V, I_D=5A$	---	20	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	16	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.5	5	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=10A$	---	7.2	---	nC
$Q_{gs}$	Gate-Source Charge		---	1.4	---	
$Q_{gd}$	Gate-Drain Charge		---	2.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=5A$	---	4.1	---	ns
$T_r$	Rise Time		---	9.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15.5	---	
$T_f$	Fall Time		---	6.0	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	572	---	pF
$C_{oss}$	Output Capacitance		---	81	---	
$C_{rss}$	Reverse Transfer Capacitance		---	65	---	
$I_s$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	10	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_s=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

#### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\cong 300\mu s$  , duty cycle  $\cong 2\%$
- 3、 The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=10A$
- 4、 The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5、 The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

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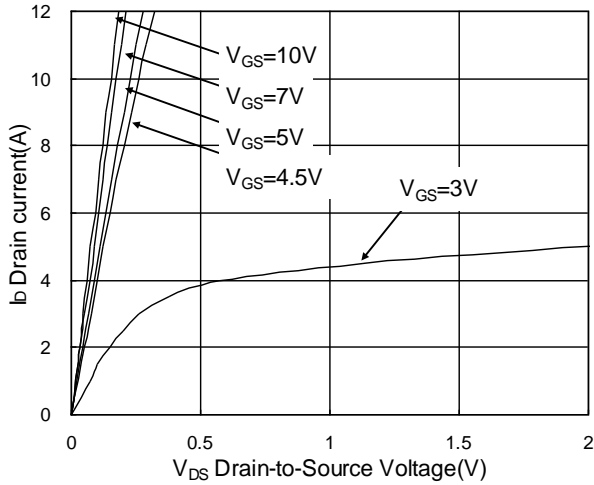
### Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-33	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-7A$	---	25	32	m $\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	---	37	54	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	---	-2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-7A$	---	15	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	15	30	
$Q_g$	Total Gate Charge (-4.5V)		---	9.8	---	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-7A$	---	2.2	---	
$Q_{gd}$	Gate-Drain Charge		---	3.4	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3, I_D=-5A$	---	16.4	---	ns
$T_r$	Rise Time		---	20.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
$T_f$	Fall Time		---	10	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	930	---	pF
$C_{oss}$	Output Capacitance		---	148	---	
$C_{rss}$	Reverse Transfer Capacitance		---	115	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	-8	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

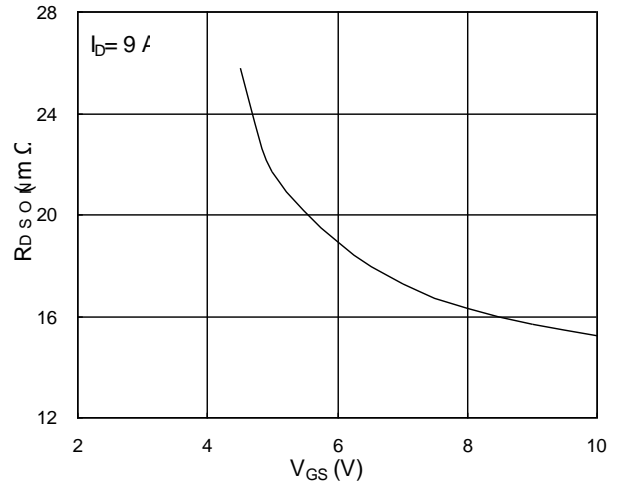
**Note :**

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\cong 300\mu s$  , duty cycle  $\cong 2\%$
- 3、 The EAS data shows Max. rating . The test condition is  $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-10A$
- 4、 The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
- 5、 The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

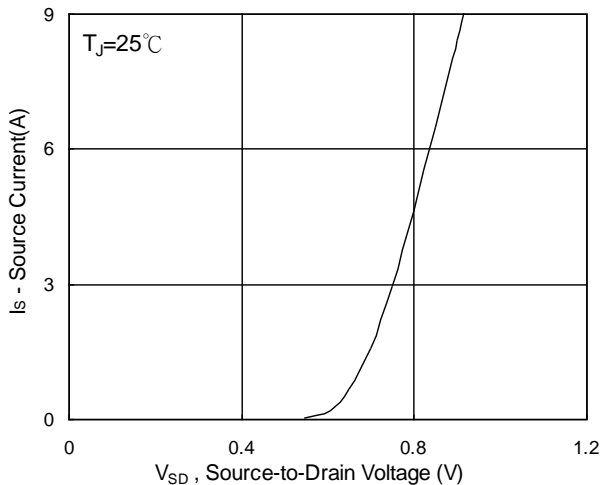
**N-Typical Characteristics**



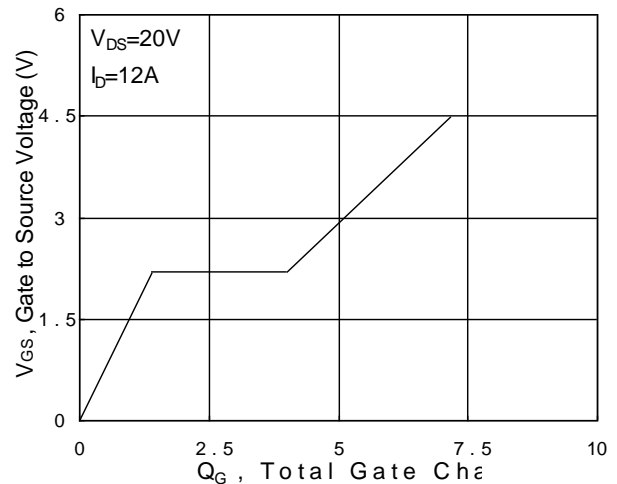
**Fig.1 Typical Output Characteristics**



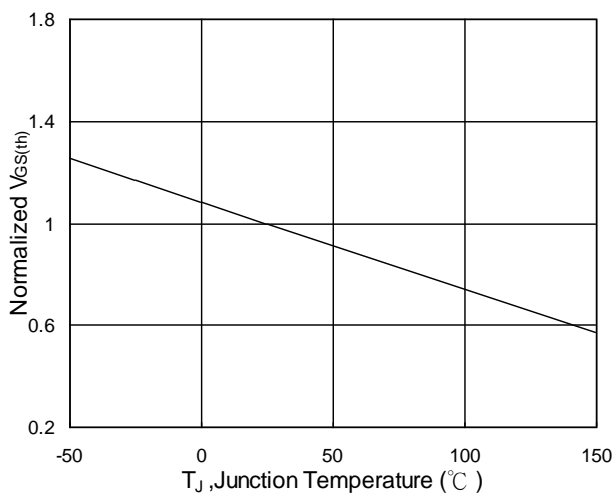
**Fig.2 On-Resistance v.s Gate-Source**



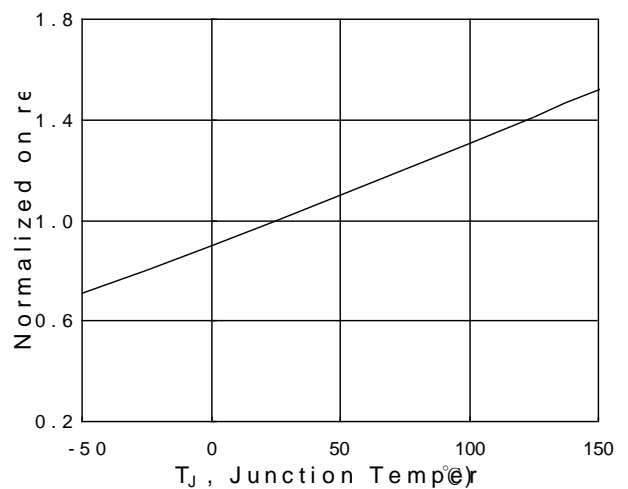
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge characteristics**



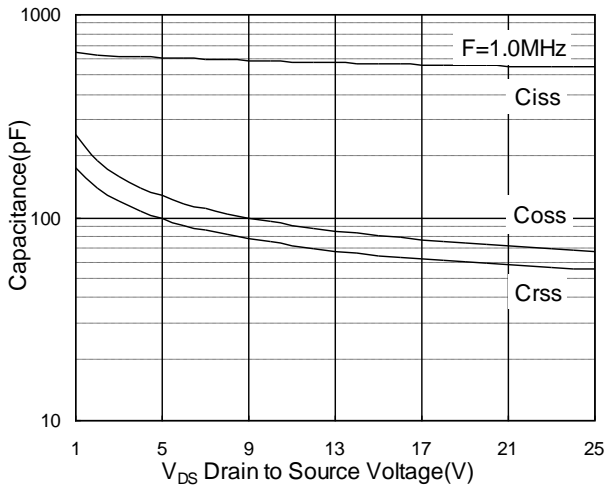
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



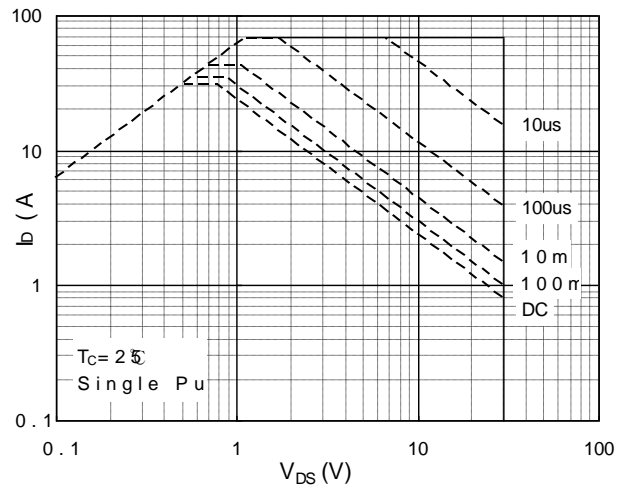
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



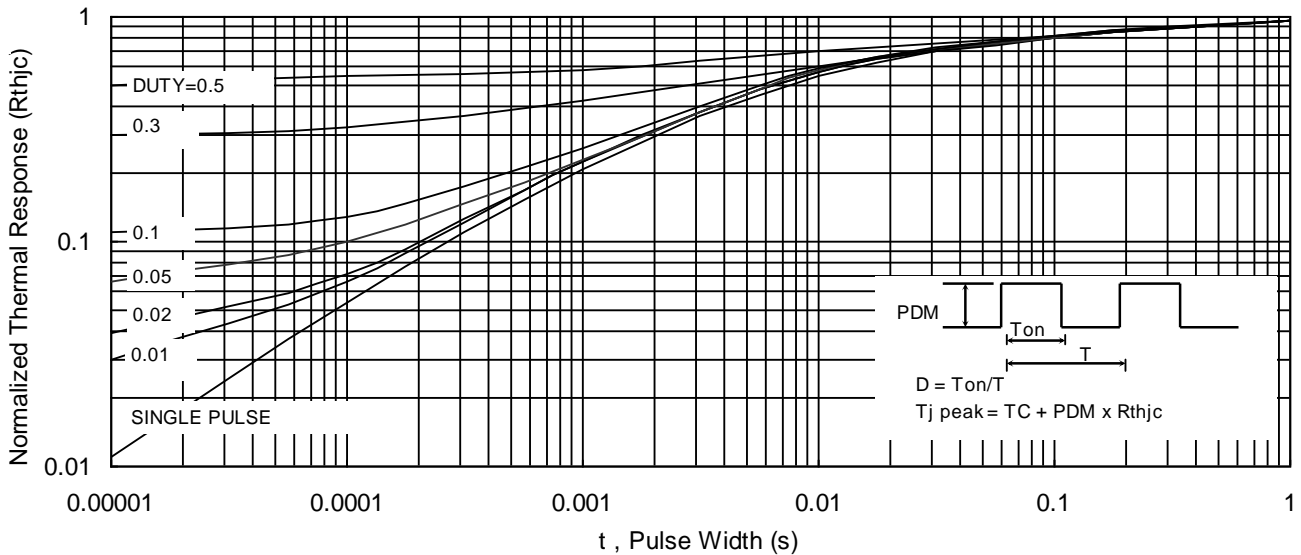
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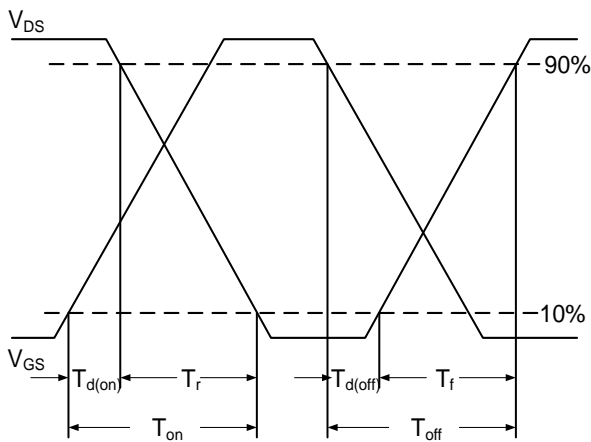
**Fig.7 Capacitance**



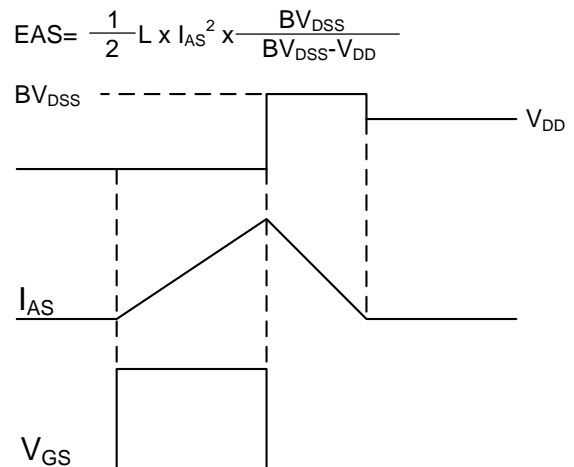
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

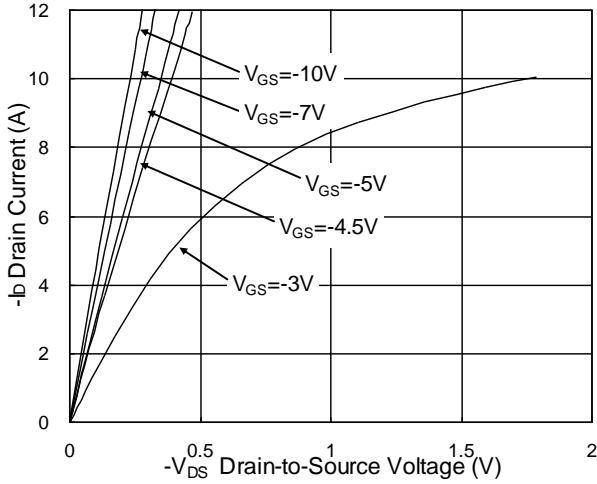


**Fig.10 Switching Time Waveform**

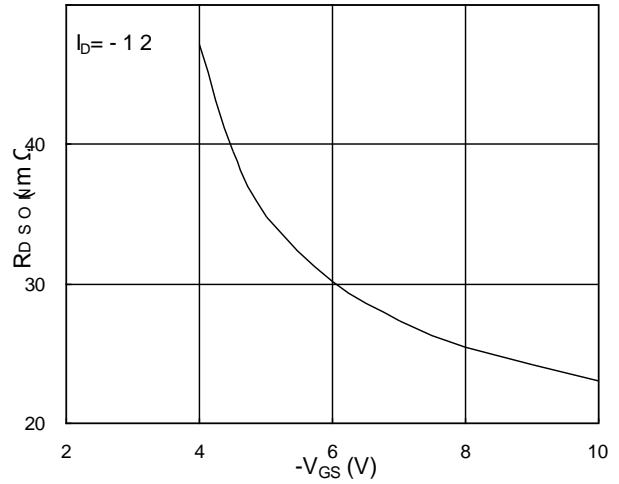


**Fig.11 Unclamped Inductive Waveform**

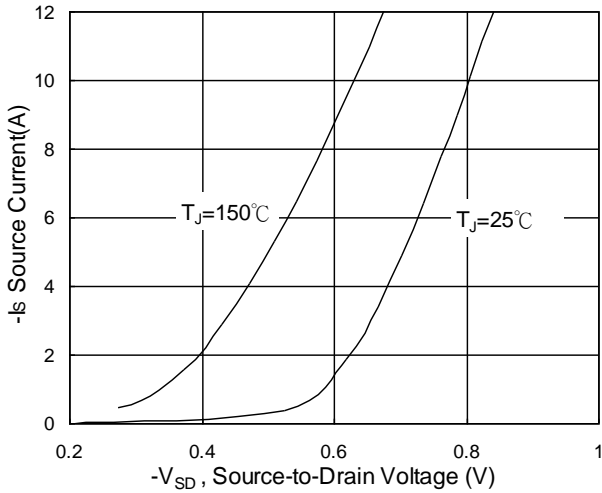
**P-Typical Characteristics**



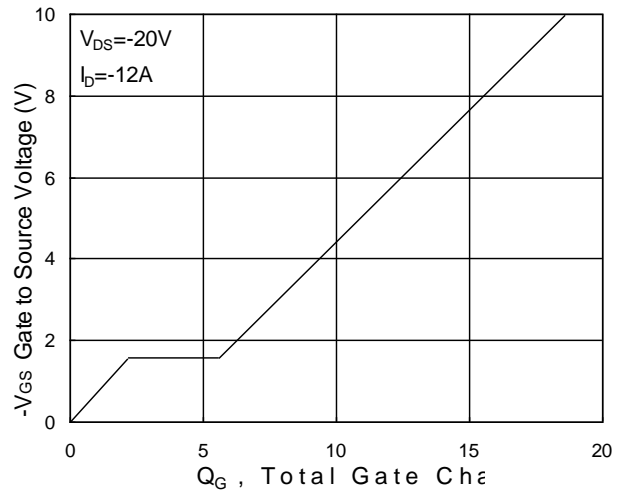
**Fig.1 Typical Output Characteristics**



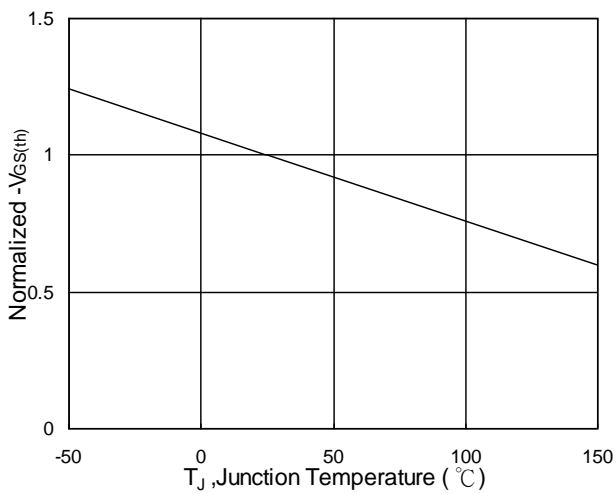
**Fig.2 On-Resistance v.s Gate-Source**



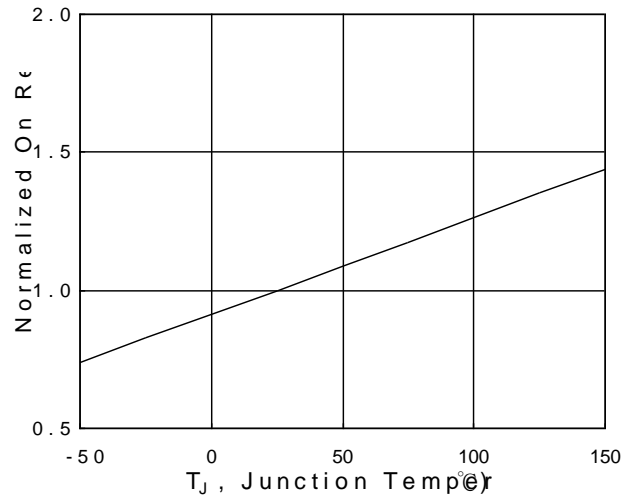
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**

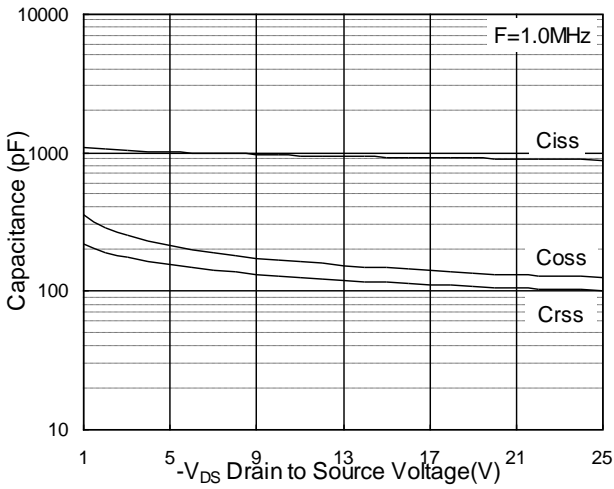


**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**

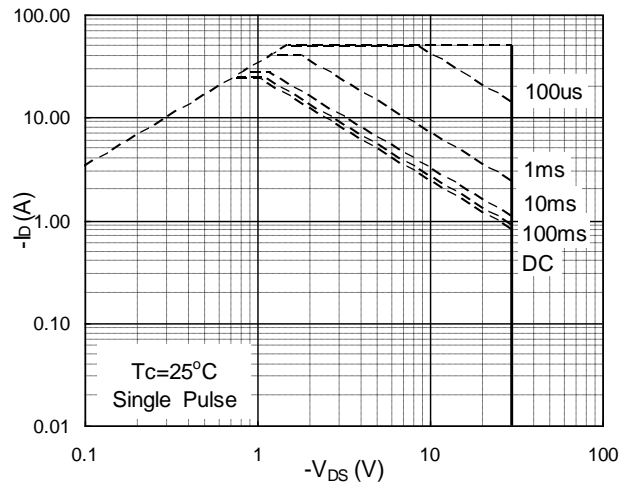


**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**

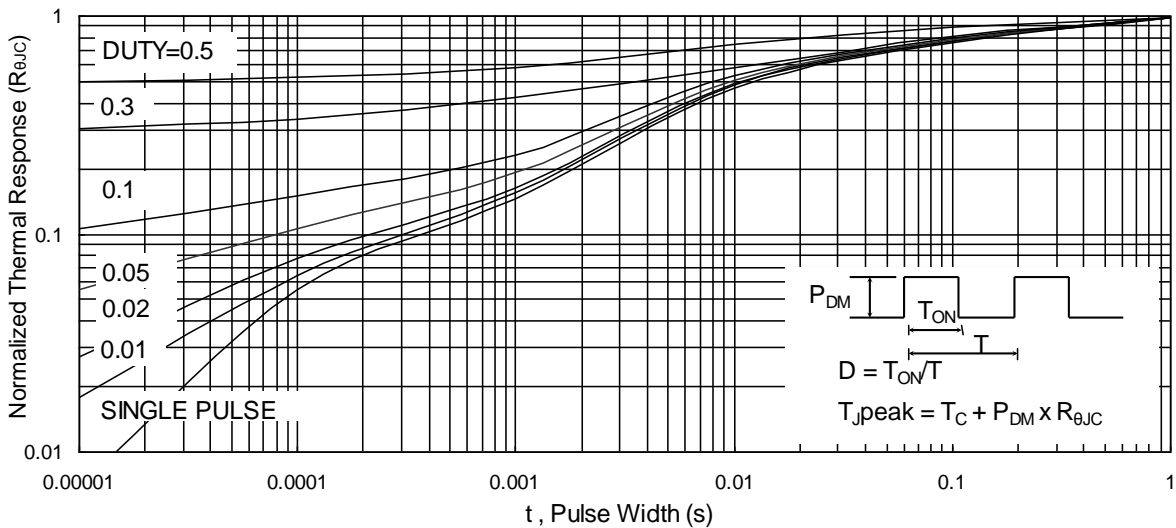
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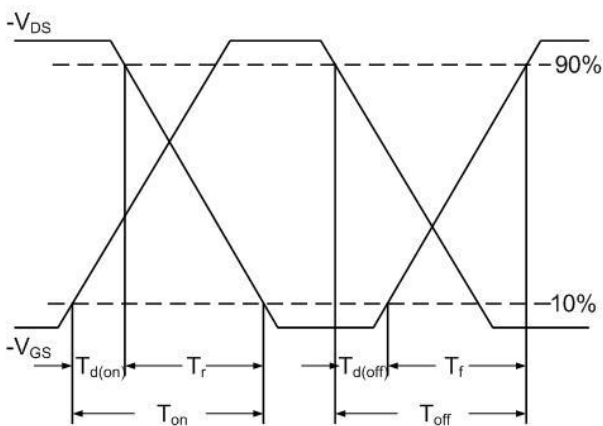
**Fig.7 Capacitance**



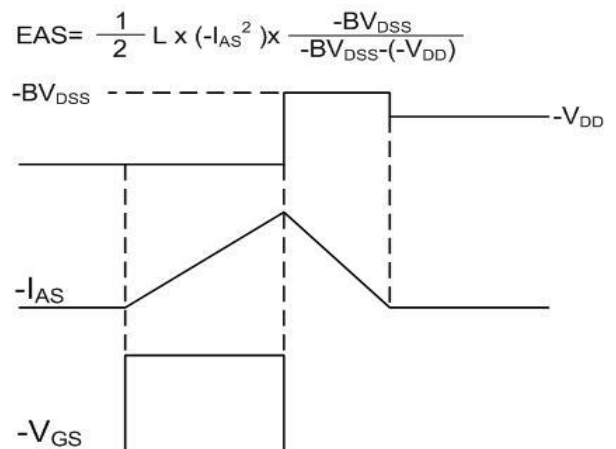
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



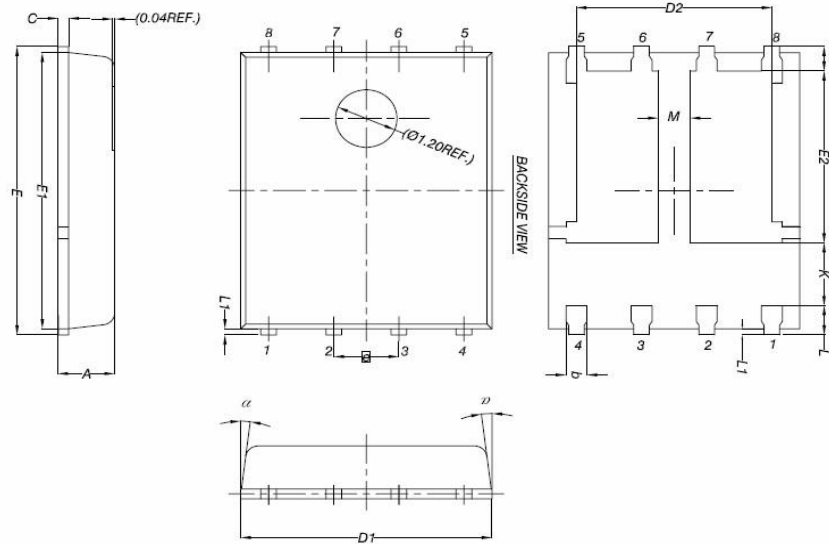
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**



### Package Mechanical Data-DFN5\*6-8L-JQ Double



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.66	5.76	5.83
E2	3.37	3.47	3.58
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°



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Edition	Date	Change
Rve1.0	2020/12/30	Initial release

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