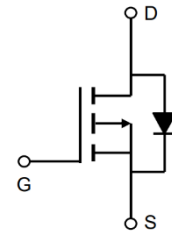


## -100V P-Channel Enhancement Mode MOSFET

### Description

The AP10P10D uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = -100V$   $I_D = -10A$

$R_{DS(ON)} < 400m\Omega$  @  $V_{GS} = -10V$

### Application

Auto Alarm Controller

POS

Brushless Motor

### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10P10D	TO-252-3L	AP10P10D XXX YYYY	2500

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-10	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-6.7	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-50	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>3</sup>	4.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	60	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	645	$^\circ C/W$

## -100V P-Channel Enhancement Mode MOSFET

### Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

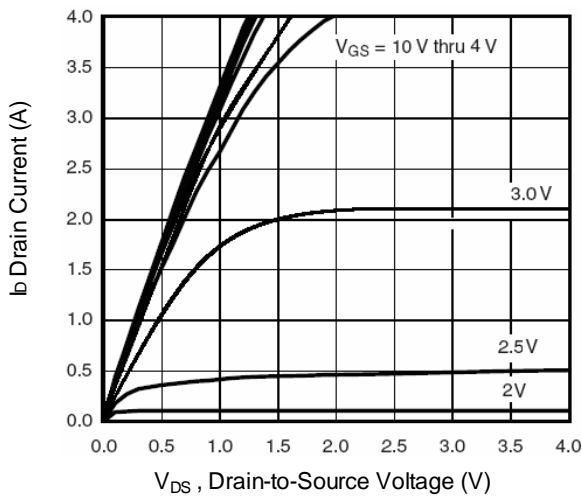
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-100	-116	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.0624	---	$V/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-3A$	---	325	400	m $\Omega$
		$V_{GS}=-4.5V, I_D=-2A$	---	320	420	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	-1.8	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.5	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-100V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu\text{A}$
		$V_{DS}=-100V, V_{GS}=0V, T_J=100^\circ\text{C}$	---	---	100	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-0.8A$	---	3	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	16	32	$\Omega$
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-0.5A$	---	4.5	---	nC
$Q_{gs}$	Gate-Source Charge		---	1.14	---	
$Q_{gd}$	Gate-Drain Charge		---	1.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-50V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-0.5A$	---	17.6	---	ns
$T_r$	Rise Time		---	2.7	---	
Td(off)	Turn-Off Delay Time		---	4.5	---	
$T_f$	Fall Time		---	3	---	
Ciss	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	550	---	pF
Coss	Output Capacitance		---	56	---	
Crss	Reverse Transfer Capacitance		---	35	---	
IS	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	-3	A
ISM	Pulsed Source Current <sup>2,4</sup>		---	---	-9	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.3	V

**Note :**

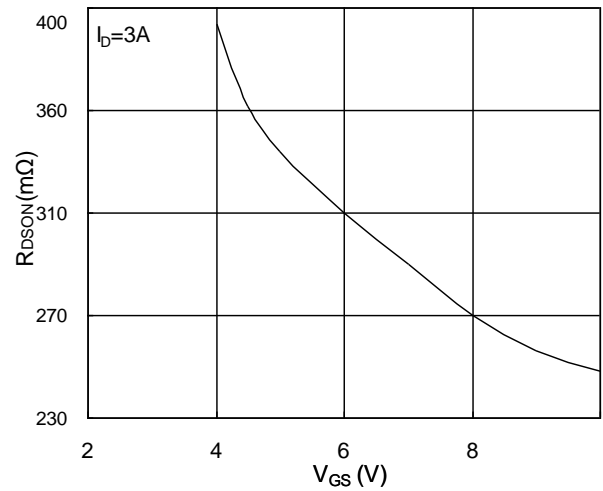
- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3、 The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4、 The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

## -100V P-Channel Enhancement Mode MOSFET

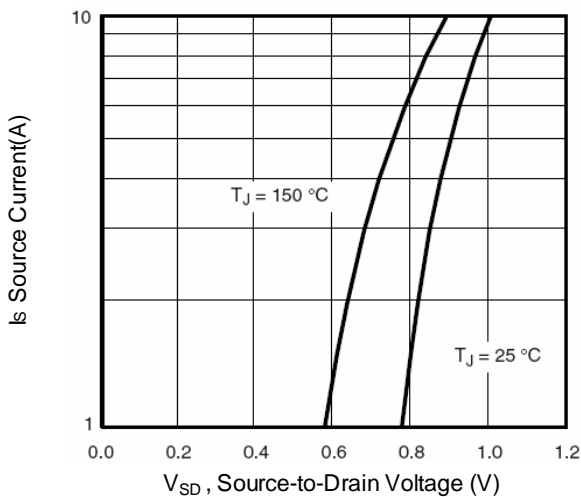
### Typical Characteristics



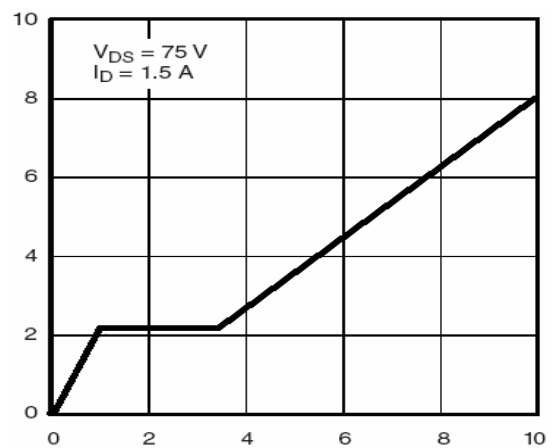
**Fig.1 Typical Output Characteristics**



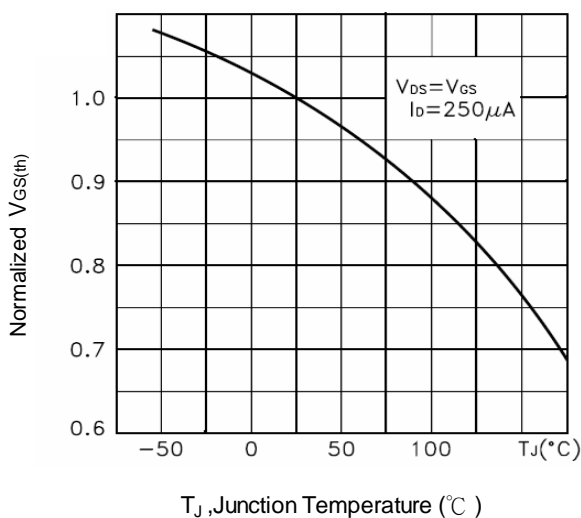
**Fig.2 On-Resistance vs. Gate-Source**



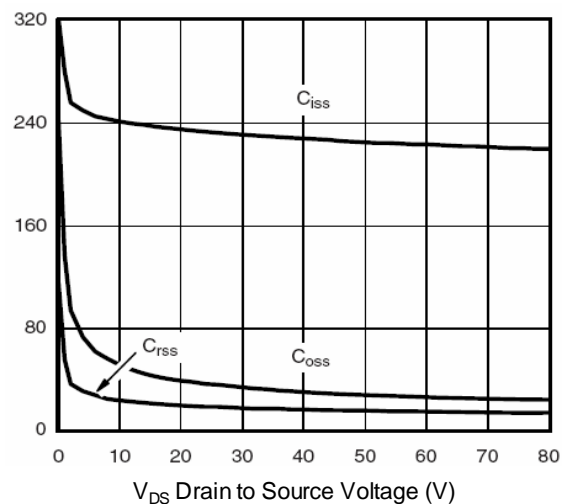
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



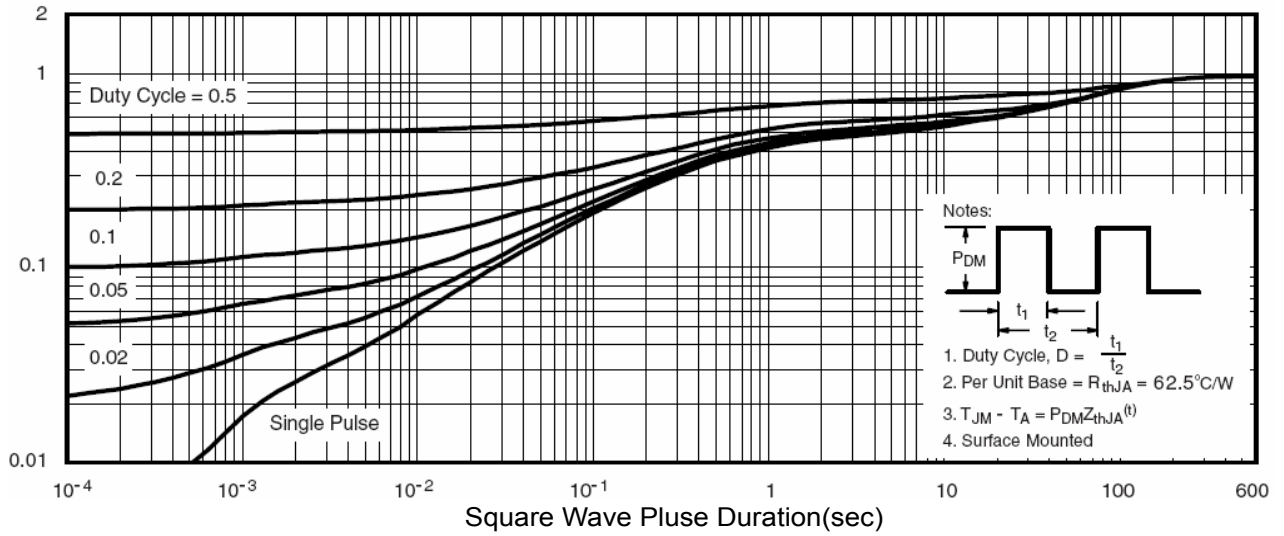
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



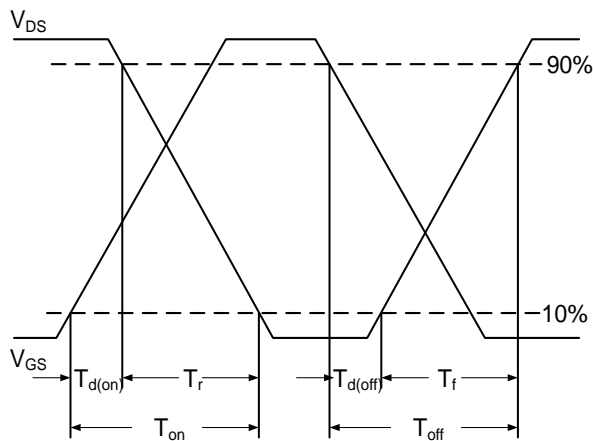
**Fig.6 Capacitance**



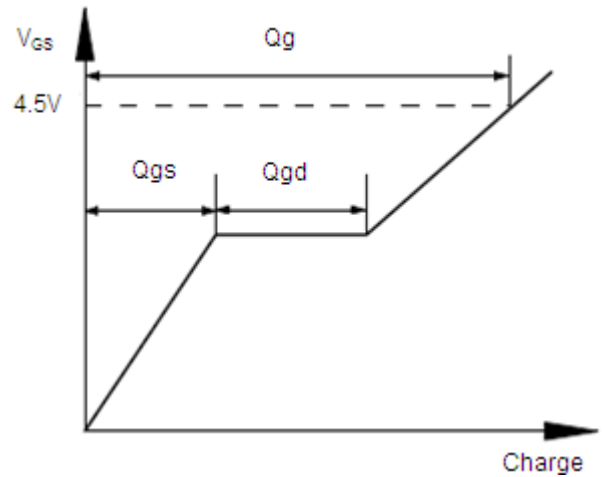
**-100V P-Channel Enhancement Mode MOSFET**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



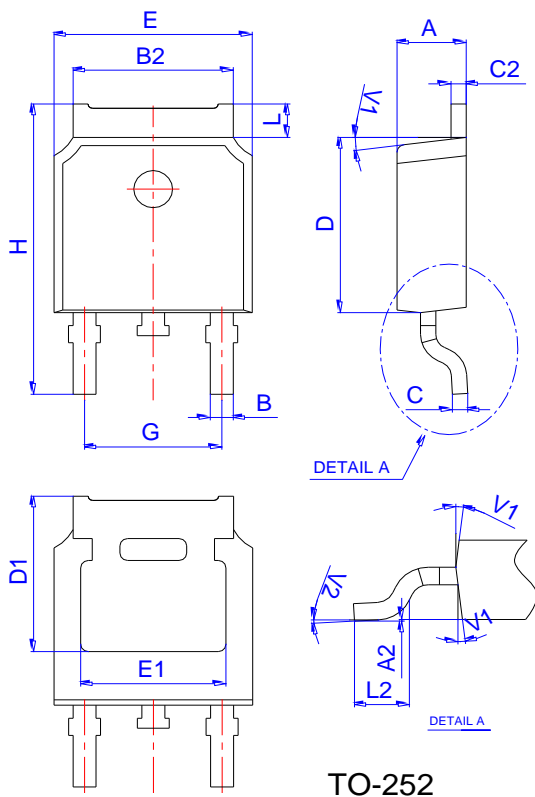
**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**

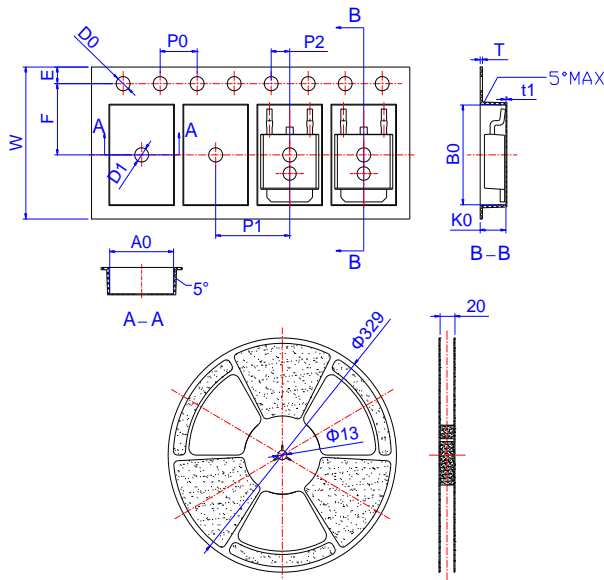
## -100V P-Channel Enhancement Mode MOSFET

### Package Mechanical Data



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

### Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

**-100V P-Channel Enhancement Mode MOSFET****Attention**

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## -100V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/8/11	Initial release

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