

60V N+P-Channel Enhancement Mode MOSFET

Description

The AP10G06NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 60V$ $I_D = 10A$

$R_{DS(ON)} < 40m\Omega$ @ $V_{GS} = 10V$

$V_{DS} = -60V$ $I_D = 9.5A$

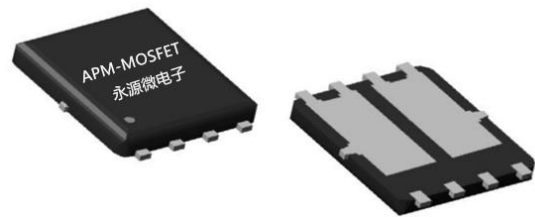
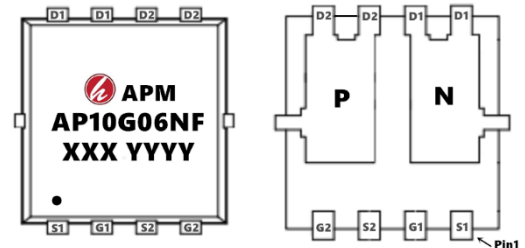
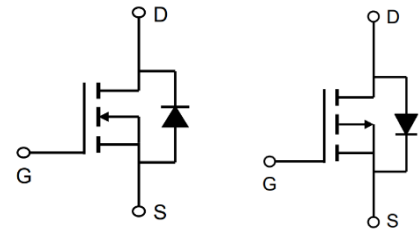
$R_{DS(ON)} < 70m\Omega$ @ $V_{GS} = 10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10G06NF	PDFN5*6-8L	AP10G06NF XXXX YYYYY	5000

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_{D@T_A=25^\circ\text{C}}$	Continuous Drain Current, $V_{GS} @ 10V^1$	10	-9.5	A
$I_{D@T_A=70^\circ\text{C}}$	Continuous Drain Current, $V_{GS} @ 10V^1$	5.2	-4.3	A
IDM	Pulsed Drain Current ²	30	-27	A
EAS	Single Pulse Avalanche Energy ³	25.5	35.3	mJ
IAS	Avalanche Current	22.6	-26.6	A
$P_{D@T_A=25^\circ\text{C}}$	Total Power Dissipation ⁴	1.5	1.5	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85	85	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	36	36	$^\circ\text{C/W}$

60V N+P-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	66	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.063	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =4A	---	35	40	mΩ
		V _{GS} =4.5V, I _D =2A	---	38	45	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250μA	1.2	1.6	2.5	V
VGS(th)	V _{GS(th)} Temperature Coefficient		---	-5.24	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V, T _J =25°C	---	---	1	μA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =4A	---	21	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	3.2	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =48V, V _{GS} =4.5V, I _D =4A	---	12.6	---	nC
Q _{gs}	Gate-Source Charge		---	3.2	---	
Q _{gd}	Gate-Drain Charge		---	6.3	---	
Td(on)	Turn-On Delay Time	V _{DD} =30V, V _{GS} =10V, R _G =3.3Ω, I _D =4A	---	8	---	ns
T _r	Rise Time		---	14.2	---	
Td(off)	Turn-Off Delay Time		---	24.4	---	
T _f	Fall Time		---	4.6	---	
Ciss	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1378	---	pF
Coss	Output Capacitance		---	86	---	
Crss	Reverse Transfer Capacitance		---	64	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	4.8	A
ISM	Pulsed Source Current ^{2,5}		---	---	9.6	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
- 3.The EAS data shows Max. rating . The test condition is VDD=-25V,VGS=-10V,L=0.1mH,IAS=-26.6A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-60	-66	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.03	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-3A	---	55	70	mΩ
		V _{GS} =-4.5V, I _D =-2A	---	75	105	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	-1.5	-2.5	V
V _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.56	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =-48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	15	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13.5	---	Ω
Q _g	Total Gate Charge (-4.5V)		---	9.86	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-48V, V _{GS} =-4.5V, I _D =-3A	---	3.1	---	
Q _{gd}	Gate-Drain Charge		---	2.95	---	
Td(on)	Turn-On Delay Time		---	28.8	---	ns
T _r	Rise Time	V _{DD} =-15V, V _{GS} =-10V R _G =3.3Ω, I _D =-1A	---	19.8	---	
Td(off)	Turn-Off Delay Time		---	60.8	---	
T _f	Fall Time		---	7.2	---	
Ciss	Input Capacitance		---	1447	---	pF
Coss	Output Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	97.3	---	
Crss	Reverse Transfer Capacitance		---	70	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-3.7	A
ISM	Pulsed Source Current ^{2,5}		---	---	-7.5	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
- 3.The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=22.6A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

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N-Channel Typical Characteristics

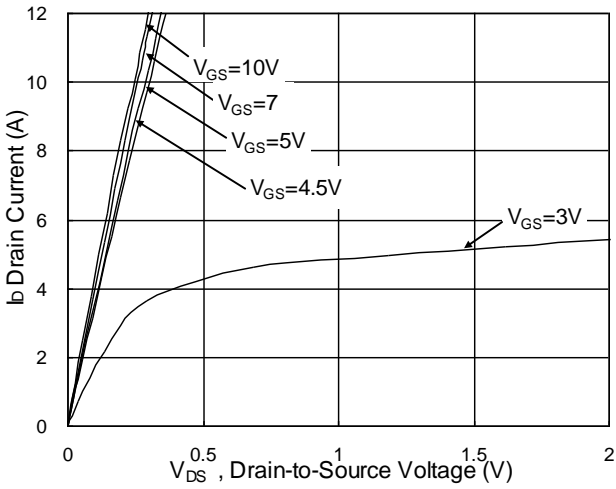


Fig.1 Typical Output Characteristics

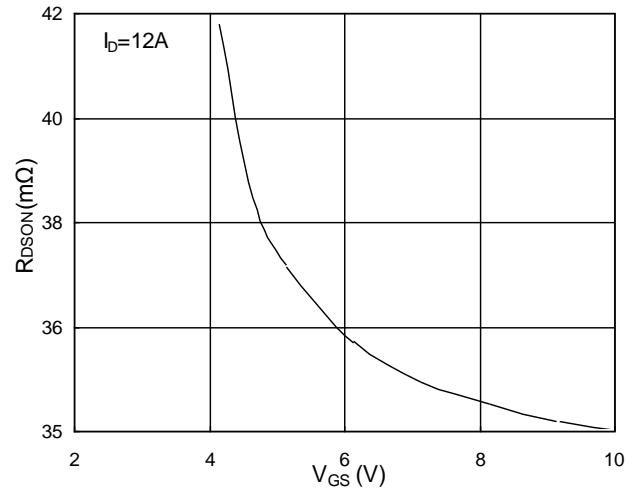


Fig.2 On-Resistance v.s Gate-Source

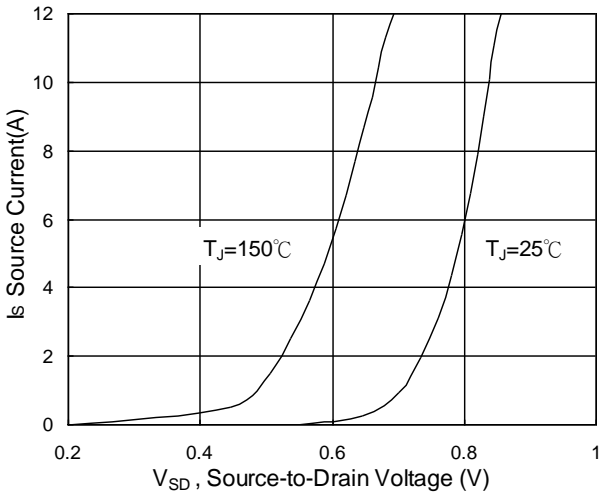


Fig.3 Forward Characteristics of Reverse

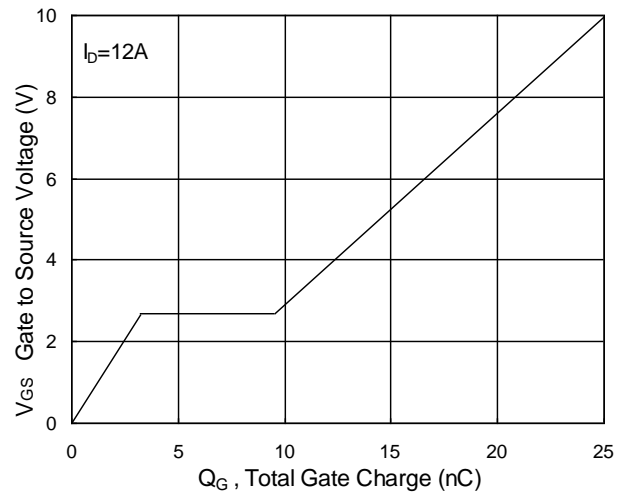


Fig.4 Gate-Charge Characteristics

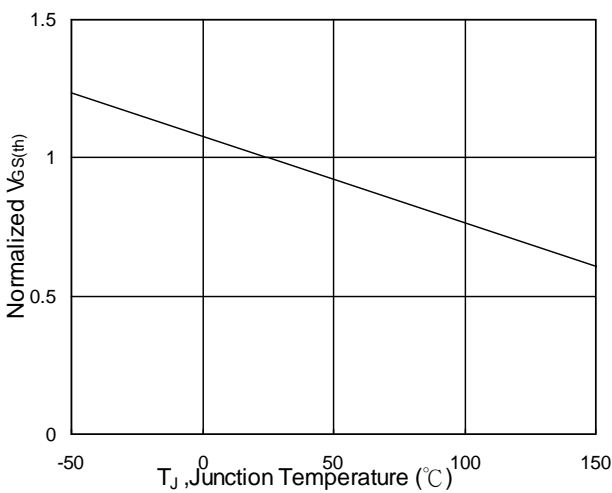


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

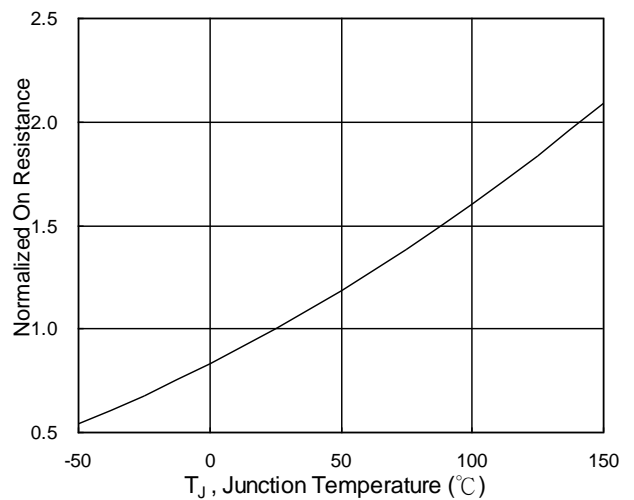


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

60V N+P-Channel Enhancement Mode MOSFET

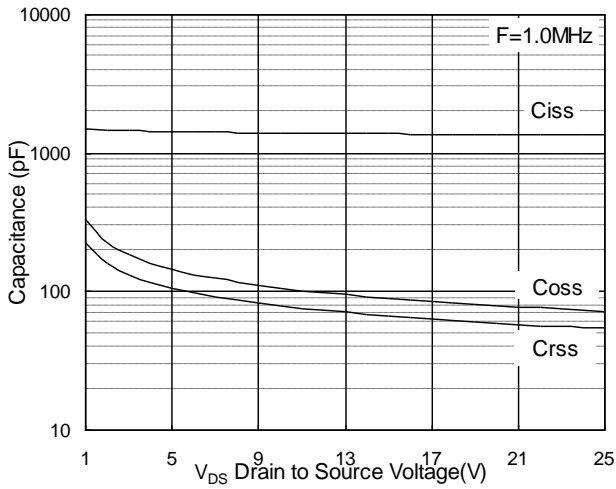


Fig.7 Capacitance

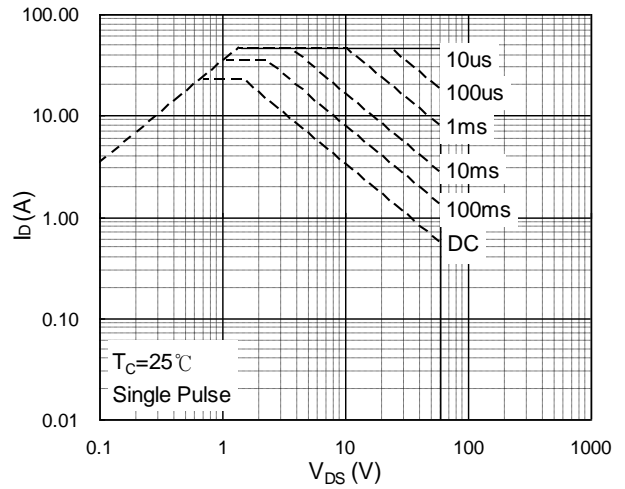


Fig.8 Safe Operating Area

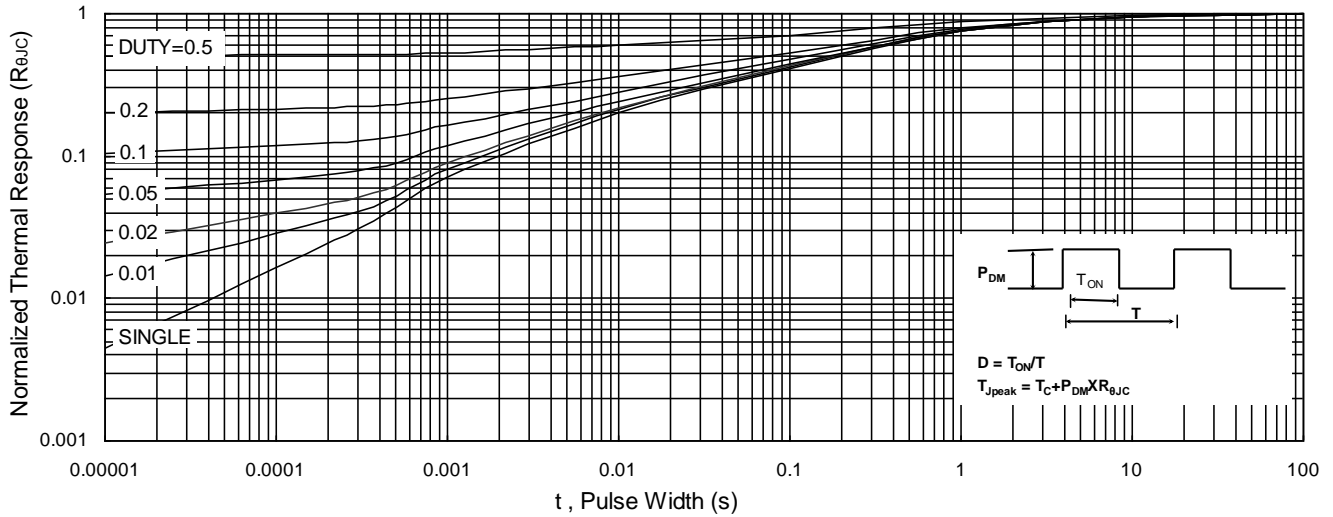


Fig.9 Normalized Maximum Transient Thermal Impedance

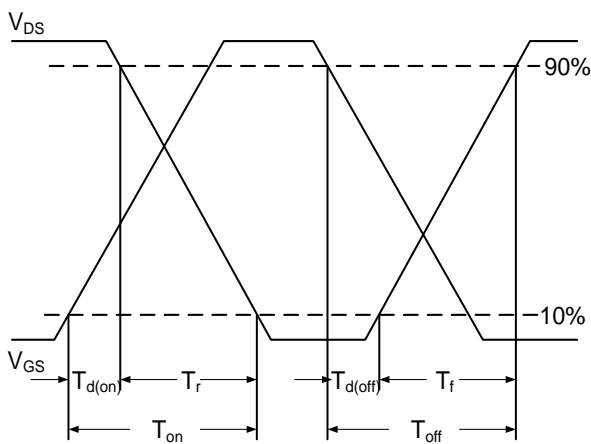


Fig.10 Switching Time Waveform

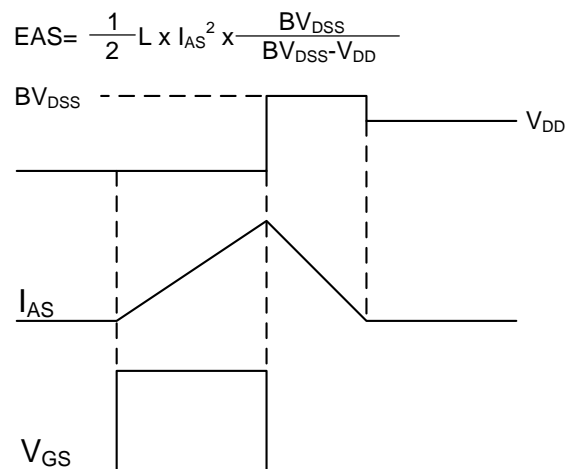


Fig.11 Unclamped Inductive Waveform

60V N+P-Channel Enhancement Mode MOSFET

P-Channel Typical Characteristics

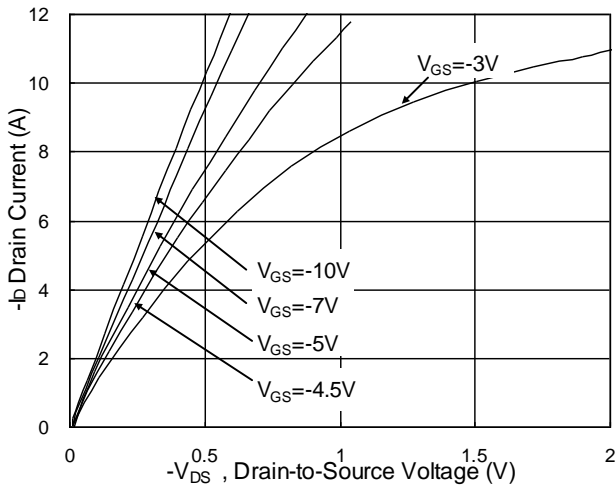


Fig.1 Typical Output Characteristics

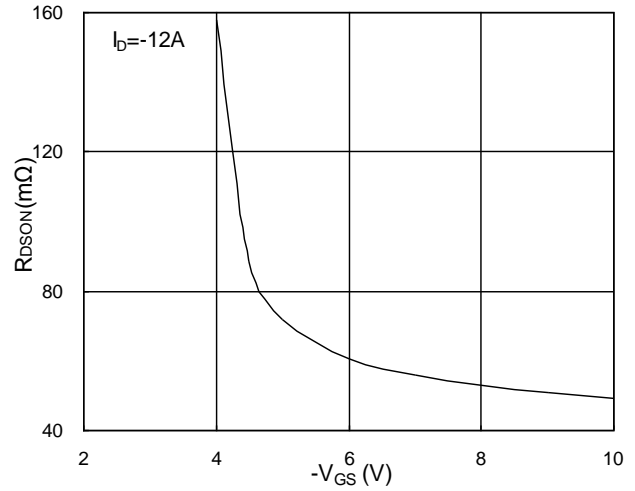


Fig.2 On-Resistance v.s Gate-Source

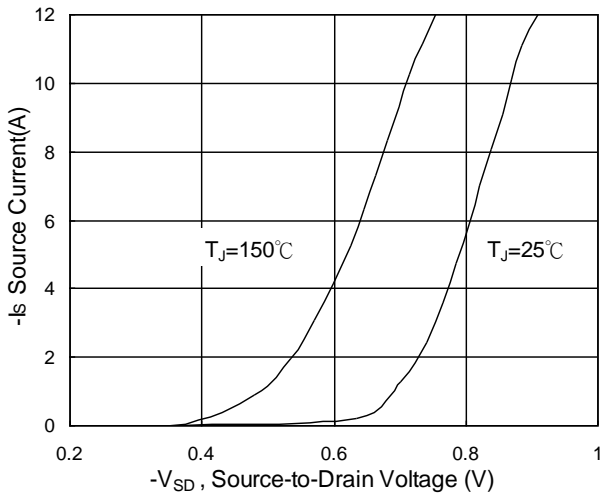


Fig.3 Forward Characteristics of Reverse

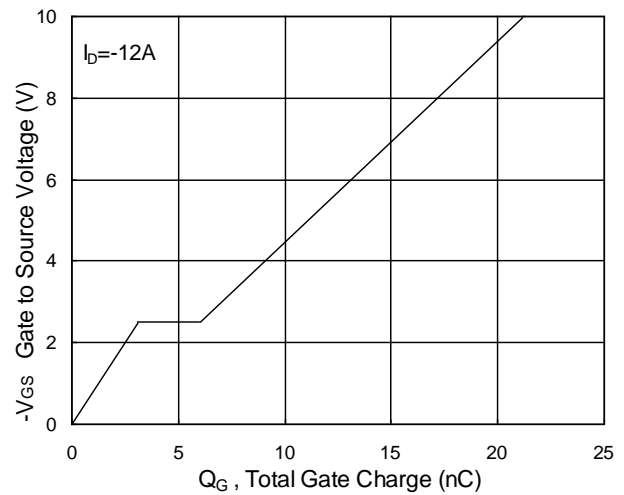


Fig.4 Gate-Charge Characteristics

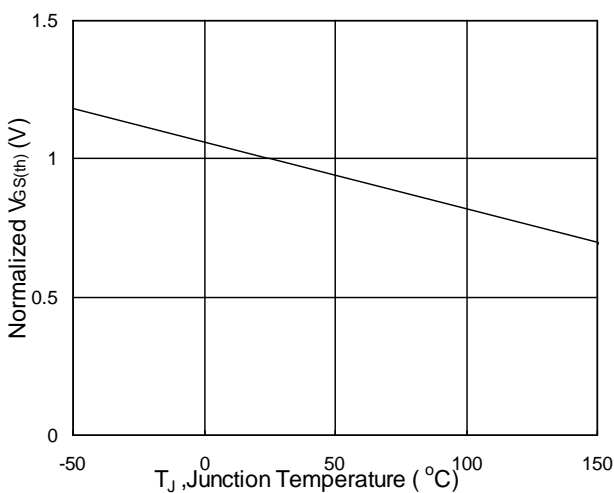


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

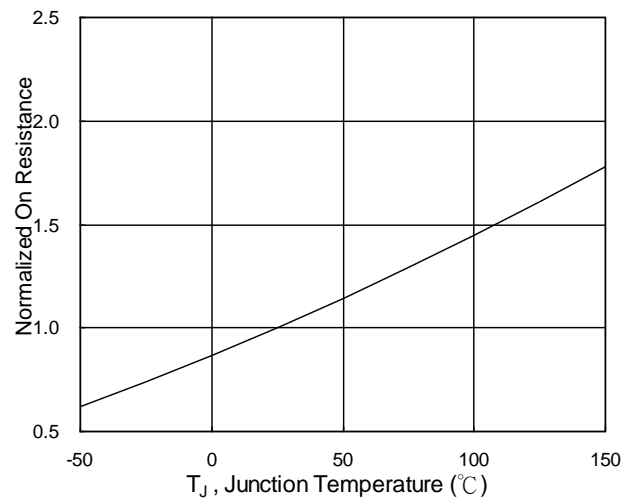


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

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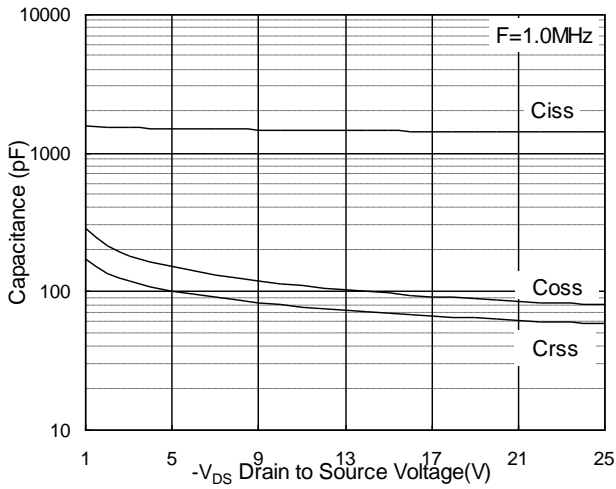


Fig.7 Capacitance

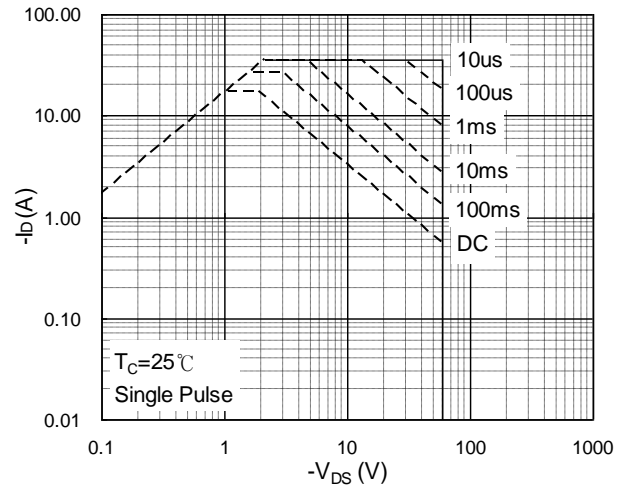


Fig.8 Safe Operating Area

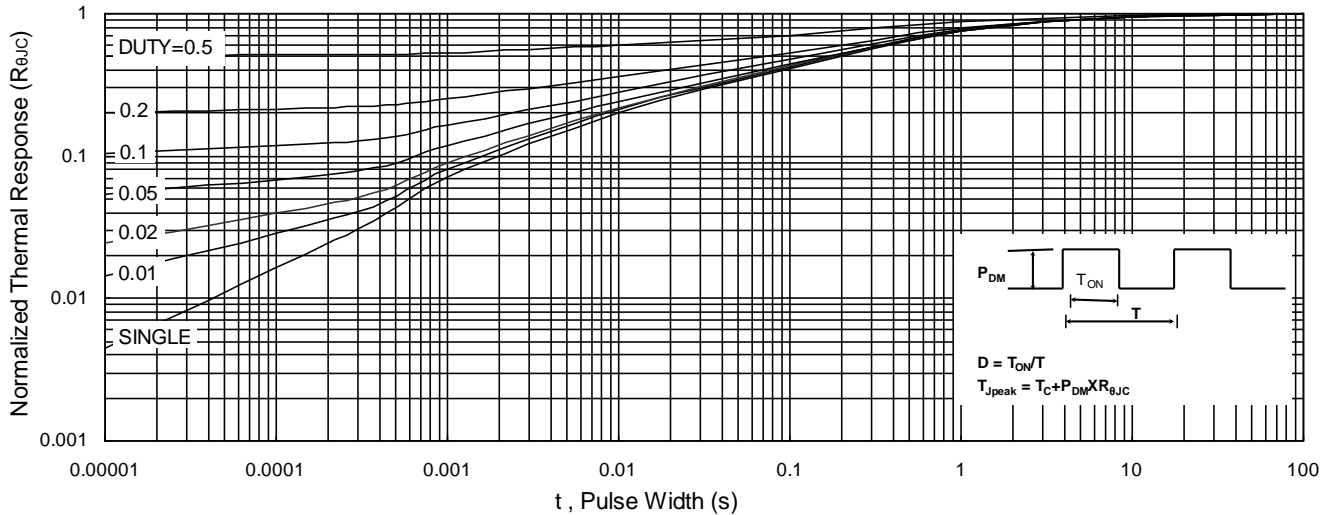


Fig.9 Normalized Maximum Transient Thermal Impedance

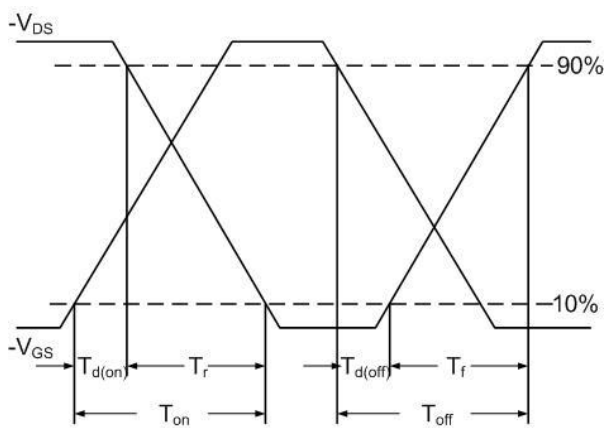


Fig.10 Switching Time Waveform

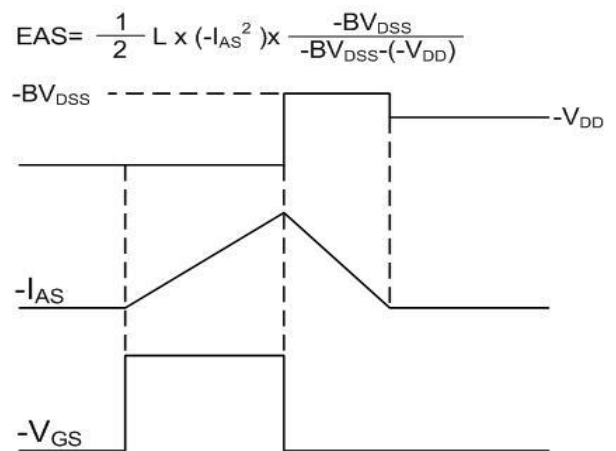
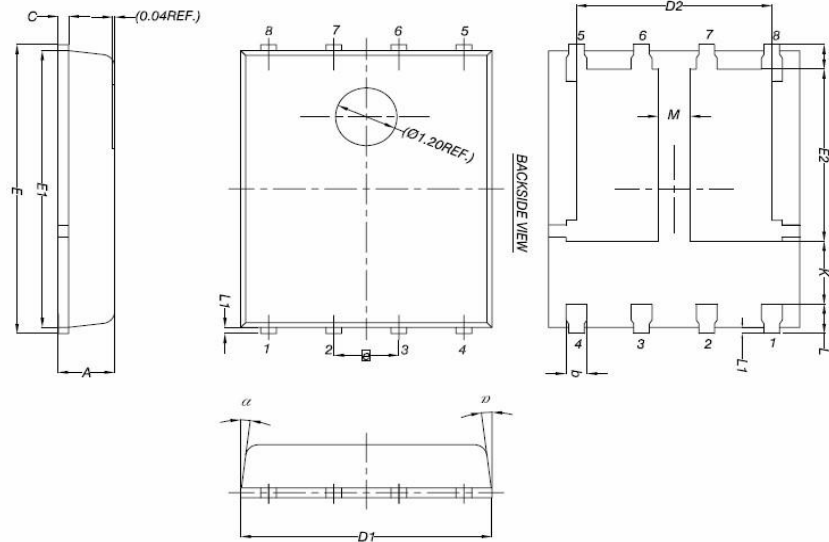


Fig.11 Unclamped Inductive Waveform



Package Mechanical Data-DFN5*6-8L-JQ Double



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.66	5.76	5.83
E2	3.37	3.47	3.58
e	1.27BSC		
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	--	--
a	0°	--	12°

60V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2019/5/31	Initial release

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