

Features

- Low Power Consumption: 8.0uA (Typ)
- Maximum Output Current: 300mA
- Small Dropout Voltage 200mV@100mA (Vout=3.3V)
- Input Voltage Range: 2.0V~6.5V
- Output Voltage Range: 1.2V~5.0V
- (customized on command in 0.1V steps)
- RoHS Compliant and Lead (Pb) Free

- High Accurate: ±2%
- Low temperature coefficient
- Output Current Limit
- Integrated Short-Circuit Protection
- Good Transient Response
- Stable with Ceramic Capacitor
- Available Package:
 SOT23、SOT23-3L、SOT89-3L

Application

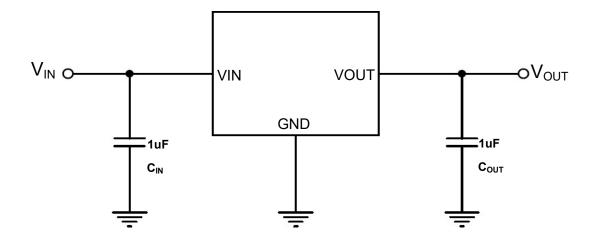
- Battery-powered equipment
- Reference voltage sources
- Mobile phones

- Cameras, video cameras
- Portable games
- Portable games

Description

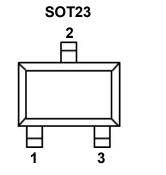
WL9002 series is a group, low power consumption, low dropout voltage, positive voltage regulators manufactured using CMOS and laser trimming technologies . It can provide 100mA output current when input / output voltage differential drops to 200mV (Vout=3.3V), The very low power consumption of WL9002 (Iq=8.0uA) can greatly improve natural life of batteries.WL9002 can provide output value in the range of 1.2V~5.0V in 0.1V steps. It also can customized on command.WL9002 includes high accuracy voltage reference, error amplifier, current limit circuit and output driver module.WL9002 has well load transient response and good temperature characteristic, And it uses trimming technique to guarantee output voltage accuracy within±2%.

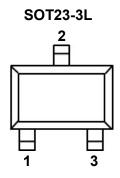
Application Circuits

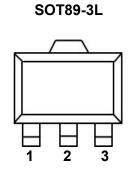




Pin Configuration







Pin Description

	Pin No.		Dia Nasa	Pin Function	
SOT23	SOT23-3L	SOT89-3L	Pin Name		
1	1	1	GND	Ground.	
2	2	2	VIN	Supply voltage input.	
3	3	3	VOUT	Voltage Output.	

Order Information

WL900212-34

Designator	Symbol	Description		
12	M3/S3/P3	SOT23 / SOT23-3L / SOT89-3L		
34	Integer	Output Voltage(12、15、18、25、28、30、33、36)		

Model*	Marking**	Description	Package	T/R Qty
WL9002M3-XX*	1234	WI 0002 200m \ Low	SOT23	3,000 PCS
WL9002S3-XX*	1234	WL9002 300mA Low- Dropout Linear voltage regulator	SOT23-3L	3,000 PCS
WL9002P3-XX*	1234	1	SOT89-3L	1,000 PCS

Note: (*) XX Represents the Output Voltage

(**) Please refer Page 3



Marking Information

①②Represents the product name

Mark ①	Product Series
6	WL9002 M3 / S3 / P3

③Represents the range of output voltage

Mar	·k ②	Product Series
VOUT: 1.2V-3.0V	VOUT: 3.1V-5.0V	WL9002 M3 / S3 / P3
5 6		VVL9002 IVI3 / 33 / F3

③Represents the Output Voltage

Mark3	Output Voltage(V)				Mark③	(Dutput Vo	Itage(V)	
0	-	3.1	ı	i	F	1.6	4.6	-	-
1	-	3.2	-	-	Н	1.7	4.7	-	-
2	-	3.3	ı	ı	K	1.8	4.8	ı	ı
3	-	3.4	-	-	L	1.9	4.9	-	-
4	-	3.5	-	-	М	2.0	5.0	-	-
5	-	3.6	-	-	N	2.1	-	-	-
6	-	3.7	ı	i	Р	2.2	ı	ı	ı
7	-	3.8	-	-	R	2.3	-	-	
8	-	3.9	1	ı	S	2.4	1	ı	-
9	-	4.0	ı	ı	Т	2.5	1	-	-
Α	-	4.1	ı	ı	U	2.6	ı	ı	ı
В	1.2	4.2	ı	ı	V	2.7	ı	ı	ı
С	1.3	4.3	-	-	X	2.8	-	-	-
D	1.4	4.4	-	-	Υ	2.9	-	-	-
E	1.5	4.5	ı	ı	Z	3.0	1	1	-

NOTE: 4 Represents the assembly lot no. 0~9, A~Z repeated (G, I, J, O, Q, W excepted)



Absolute Maximum Ratings (1)(2)

Paramete	er	Symbol	Maximum Rating	Unit	
Input Voltage		Vin	V _{SS} -0.3~V _{SS} +7.0	V	
Output Current		Іоит	350	mA	
Output Voltage		Vouт	V _{SS} -0.3~V _{IN} +0.3	V	
	SOT23		200		
	SOT23-3	Pd	250	mW	
Power Dissipation	SOT89-3		500		
	SOT23	(3)	500	°C/W	
Thermal Resistance	SOT23-3	R _{eJA} (3)	400	°C/W	
	SOT89-3 (Junction-to-ambient thermal resistance		200	°C/W	
Operating Temperature		Topr	-40~85	$^{\circ}\!\mathbb{C}$	
Storage Temperature		Tstg	-40~125	$^{\circ}\mathbb{C}$	
Soldering Temperatu	re & Time	Tsolder	260℃, 10s		

Note (1): Exceeding these ratings may damage the device.

ESD Ratings

Item	Description	Value	Unit
V(ESD-HBM)	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014	±4000	>
	Classification, Class: 2		
V(ESD-CDM)	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014	±400	V
	Classification, Class: C0b		
ILATCH-UP	JEDEC STANDARD NO.78E APRIL 2016	+400	mA
ILATOH-UP	Temperature Classification, Class: I	± 1 00	IIIA

ESD testing is performed according to the respective JESD22 JEDEC standard. The human body model is a 100 pF capacitor discharged through a $1.5k\Omega$ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Recommended Operating Conditions

Parameter	MIN.	MAX.	Units
Supply voltage at V _{IN}	2.0	6.5	V
Operating junction temperature range, Tj	-40	125	°C
Operating free air temperature range, TA	-40	85	°C

Note: All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note (2): The device is not guaranteed to function outside of its operating conditions

Note (3): The package thermal impedance is calculated in accordance to JESD 51-7.



Electrical Characteristics

(Test Conditions: CIN=1uF, COUT=1uF,TA=25°C, unless otherwise specified.)

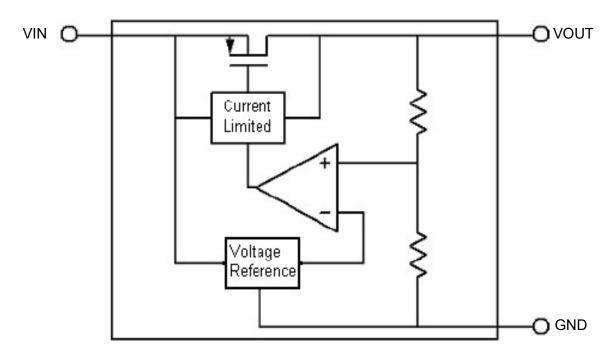
Parameter	Symbol	Conditions	Min	Тур	Max	Units
Input Voltage	Vin		-0.3		6.5	V
Quiescent Current	ΙQ	Vout≦Vin Iload=0mA ⁽²⁾		8.0		uA
Output Voltage	Vоит	V _{IN} =V _{set} +1.0V Iouт=30mA	Vset*0.98	Vset	Vset*1.02	V
Maximum Output Current	Іоит(Мах)	VIN=VOUT+1.0V	300 ⁽¹⁾			mA
Dropout Voltage	VDROP	Iouт=100mA Vouт=3.3V		200		mV
Line Regulation	ΔVout/ ΔVin•Vout	I _{OUT} =40mA (V _{set} +1.0v)≦V _{IN} ≦7.0V		0.05		%/V
Load Regulation	ΔVουτ	V _{IN} =V _{set} +1.0V 1mA≦Iouт≦100mA		30		mV
Short Current	Ishort	V _{IN} = V _{set} +1.0 V V _{OUT} =GND		10		mA
Current Limit	Ііміт		_	350	_	mA
Power Supply Rejection Rate	PSRR	V _{IN} =V _{set} +1.0V f=1KHz,I _{OUT} = 40mA		50		dB
Output Voltage Temperature Coefficient	ΔVουτ/ ΔΤ•Vουτ	Іоυт=10mA		100		ppm/℃

NOTE:(1) I_{OUT} =Pd I (V_{IN} - V_{OUT})

⁽²⁾ WL9002 keeps the chip low power when the input voltage is low



Function Block Diagram



Application Guideline

Input Capacitor

A $1\mu F$ ceramic capacitor is recommended to connect between V_{DD} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 1µF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage VDROP also can be expressed as the voltage drop on the pass-FET at specific output current (IRATED) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance RDS(ON). Thus the dropout voltage



can be defined as (VDROP = VIN - VOUT = RDS(ON) x IRATED). For normal operation, the suggested LDO operating range is (VIN > VOUT + VDROP) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: TA=25°C, PCB,

The max PD= (125°C - 25°C) / (Thermal Resistance °C/W)

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

 $PD = (VIN - VOUT) \times IOUT$

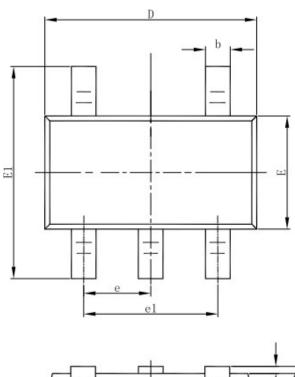
Layout Consideration

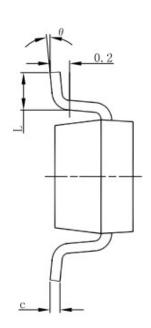
By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the WL9002 ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/ or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

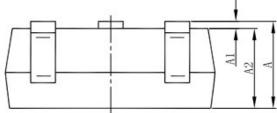


Packaging Information

SOT23





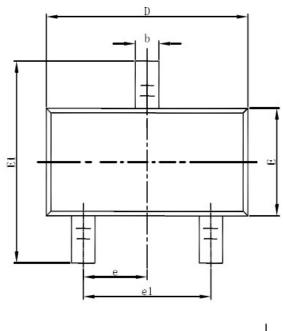


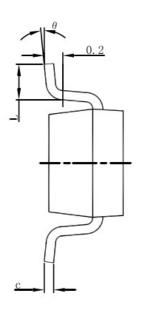
Cumb a l	Dimensions In	Millimeters	Dimensions	In Inches
Symbol	Min	Max	Min	Max
Α	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
С	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
е	0.950(BSC)	0.037(BSC)
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

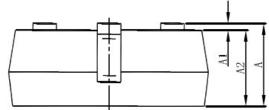


Packaging Information

SOT23-3L





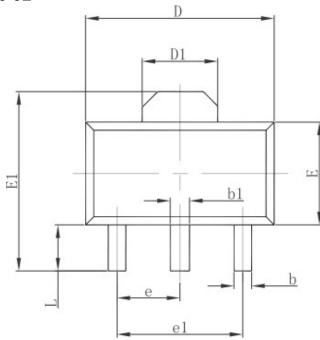


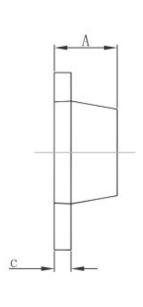
Cumbal	Dimensions In	n Millimeters	Dimensions	In Inches
Symbol	Min	Max	Min	Max
Α	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
С	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
Е	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
е	0.950	(BSC)	0.037(BSC)
e1	1.800	2.000	0.071	0.079
Ĺ	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



Packaging Information

SOT89-3L





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
Α	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
С	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
е	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047