500mA Adjustable High-Speed Low Power LDO

Features

- Programmable Output: Minimum can go to 0.8V
- Low Power Consumption: 28μA (Typ.)
- Low Voltage Drops: 0.15V@50mA
- Standby Mode: less than 0.1uA
- Low Temperature Coefficient
- Active Discharge Function
- High Ripple Rejection: 70dB@1KHz (Typ.)
- High Input Voltage (up to 8V)
- Output Voltage Accuracy: Tolerance ±2%
- Build-in Enable / Output Current Limit
- SOT23-5 Package

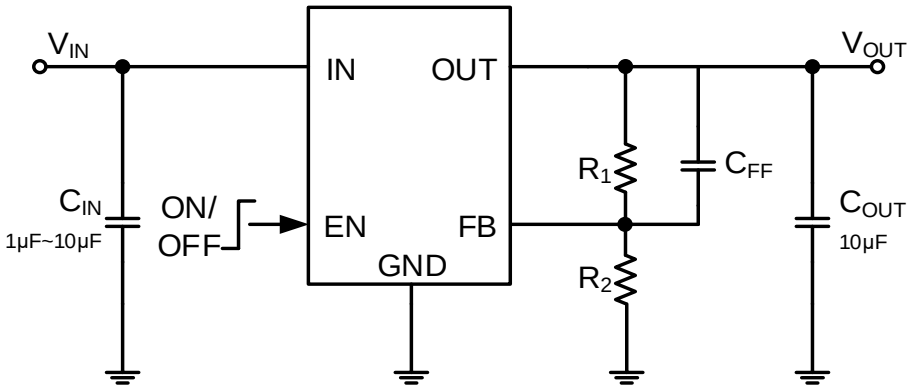
Applications

- Cellular Handsets
- Battery-Powered Equipment
- Wi-Fi Router
- Hand-Held Instruments
- Portable Information Application
- Adjustable power supply

General Description

The RY6050-ADJM5R is highly precise, low noise, positive voltage LDO regulators manufactured using CMOS processes. The RY6050-ADJM5R achieves high ripple rejection and low dropout and consists of a standard voltage source, an error correction, current limit, and a phase compensation circuit plus a driver transistor. External output feedback, customers can easily get the required voltage. In order to make the load current does not exceed the current capacity of the output transistor, built-in over-current protection, over temperature protection and short circuit protection. The internal op amp with advanced structure, the output capacitor can be omitted. The RY6050-ADJM5R is available in SOT23-5 package.

Typical Application Circuit



Typical Application Circuit with FB

V_{OUT}=0.8×(1+R1/R2)

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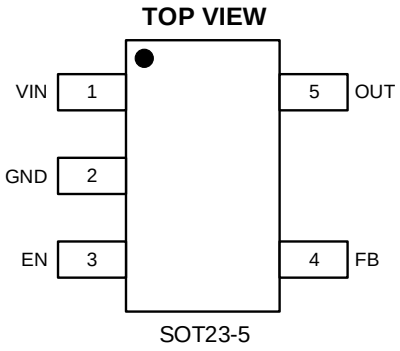
Pin Description

Pin Configuration



Top Marking: 4bLL (device code: 4b, LL= lot number code)

Pin Description

Pin No.	Pin Name	Function
1	VIN	Input voltage pin for the regulator.
2	GND	Ground pin.
3	EN	Enable Control (Active high), Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	FB	FB pin for adjustable output option.
5	OUT	Output voltage pin for the regulator.

Mark Rule

Mark	Part No.	Mode	Description	Package	T/R Qty
4bLL	70605021	RY6050-ADJM5R	RY6050-ADJM5R LDO, ADJ, 500mA, SOT23-5	SOT23-5	3000PCS

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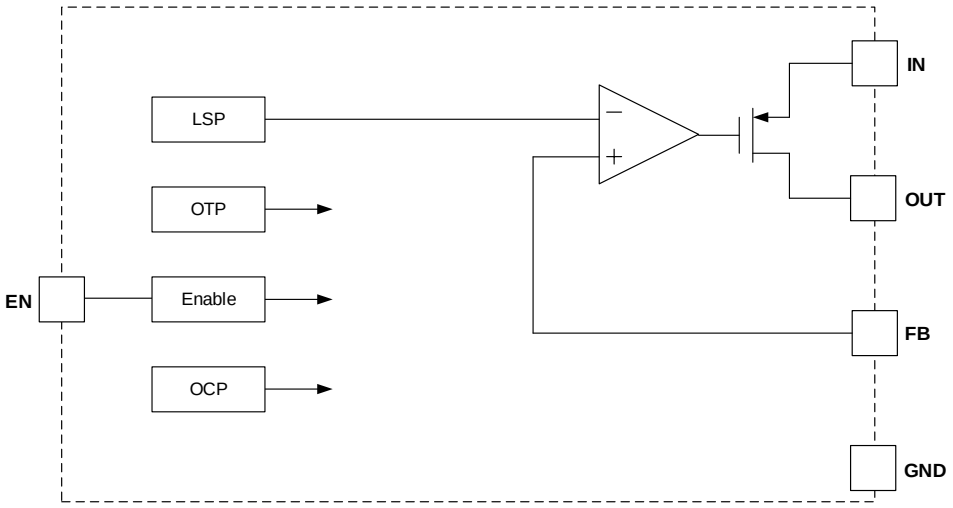
Functional Block Diagram



Functional Block Diagram

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} voltage	2.0	8.0	V
V_{OUT} voltage	1.0	3.3	V
Output Current (3)	600		mA
Power dissipation (4)	Internally Limited		
Operating Ambient Temperature	-40	85	°C
Maximum junction temperature		150	°C
Storage temperature, T_{stg}	–50	85	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): $I_{OUT}=P_D/(V_{IN}-V_{OUT})$

Note (4): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=155°C (typical) and disengages at T_J= 140°C (typical).

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Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	2	6.5	V
Output current	0	500	mA

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	230	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	152	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

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Electrical Characteristics

T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions			Min	Typ.	Max	Units
Input Voltage	V_{IN}				2		6.5	V
Feedback Voltage	V_{FB}				784	800	816	mV
Output Current	I_{OUT}	$V_{IN} \geq V_{OUT(S)}+1.0V$				500		mA
Dropout Voltage $V_{OUT}=0.98V_{OUT}$ (NOM)	V_{drop}	-40°C ≤ T_J ≤125°C	3.3V	100mA		60		mV
				300mA		230		
			2.5V	100mA		70		
				300mA		250		
			1.2V	100mA		430		
				300mA		700		
Line Regulations	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	$V_{OUT(S)}+0.5\ V \leq V_{IN} \leq 7V$, I_{OUT}=300mA			-	0.20	0.60	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	$V_{IN}=V_{OUT(S)}+1.0$ V			-	0.50	2	%
Supply Current	I_{SS1}	$V_{IN}=V_{OUT(S)}+1.0$ V			-	28		μA
Shutdown Current	I_{shut}	V_{IN}=5V, V_{EN}=0					0.1	μA
Power Supply Rejection Ratio	PSRR	V_{OUT}=2.5V, I_{OUT}=20mA	f = 1KHz		-	70	-	dB
			f = 10kHz			50	-	dB
Short-circuit Current	I_{short}	$V_{IN}=V_{OUT(S)}+1.0V$, ON/OFF Terminal is ON, V_{OUT}=0V			-	500	-	mA
EN “High Voltage	V_{ENH}				1			V
EN “Low” Voltage	V_{ENL}						0.5	V
EN “High Current	I_{ENH}	$V_{IN}=V_{EN}=V_{OUT(T)}+1V$			-0.1		0.1	μA
EN “Low” Current	I_{ENL}	$V_{IN}=V_{OUT(T)}+1V$, $V_{EN}=V_{SS}$			-0.1		0.1	μA
Thermal Shutdown Temperature	T_{SD}	I_{LOAD} =10mA				155		°C
Thermal Shutdown Hysteresis	ΔT_{SD}					15		°C

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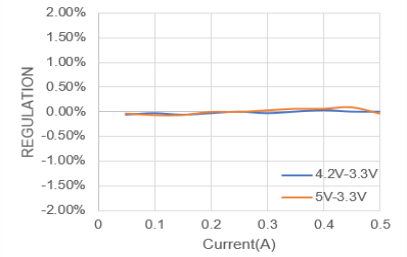
Typical Performance Characteristics (1)

Note (1): Typical performance characteristics below based on T_A = 25°C, unless otherwise noted.

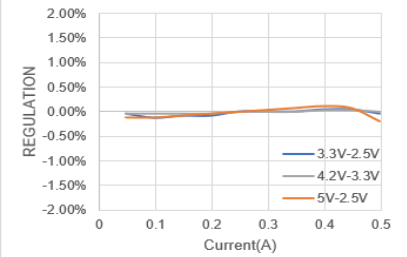
Load Regulation

V_{OUT}=3.3V



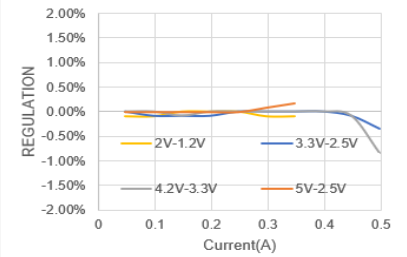
Load Regulation

V_{OUT}= 2.5V



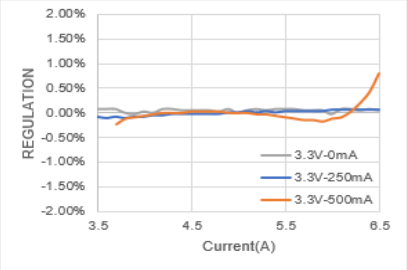
Load Regulation

V_{OUT}=1.2V



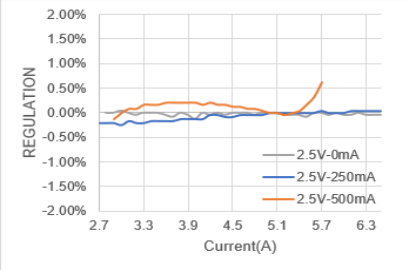
Line Regulation

V_{OUT}=3.3V



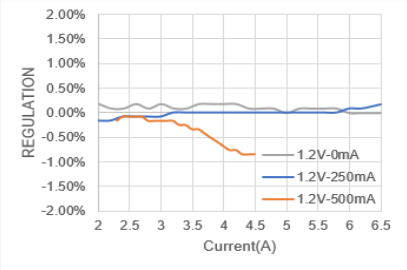
Line Regulation

V_{OUT}=2.5V



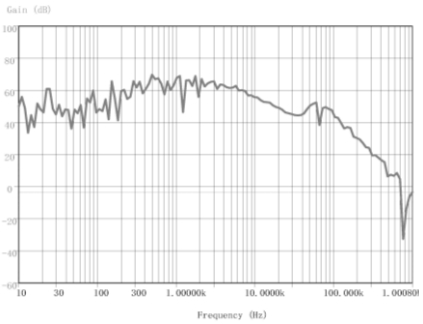
Line Regulation

V_{OUT}=1.2V



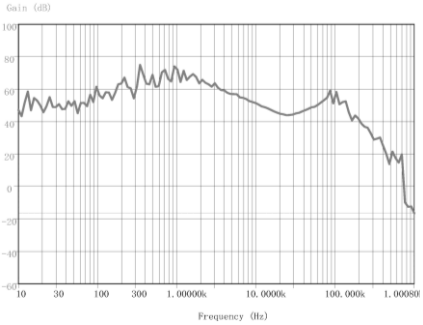
Power Supply Rejection Ration

V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=20mA



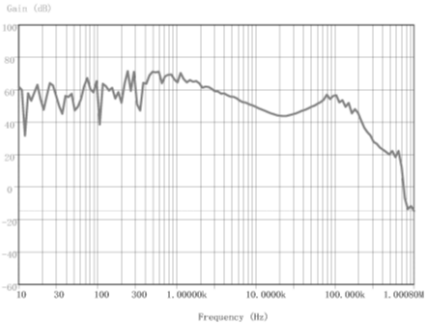
Power Supply Rejection Ration

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=20mA



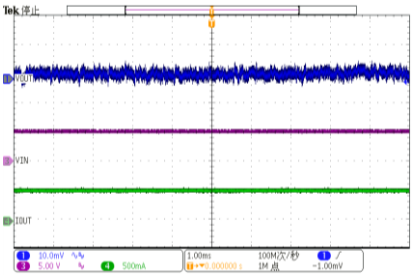
Power Supply Rejection Ration

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=20mA



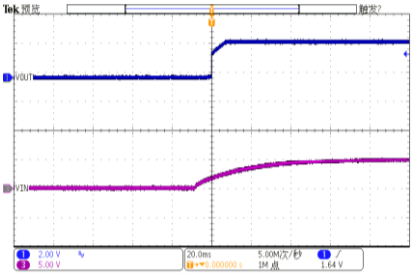
Steady State

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=350mA



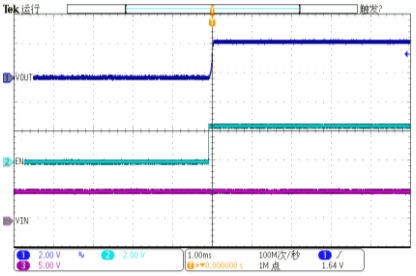
Vin Start Up

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=1mA



EN Start Up

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=1mA



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Applications Information

Setting the Output Voltage

RY6050-ADJM5R require an input capacitor and an output capacitor. These components are critical to the performance of the device. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF}
1	25.00	100	1~10	10	Opt.
1.05	31.25	100	1~10	10	Opt.
1.2	50.00	100	1~10	10	Opt.
1.5	87.50	100	1~10	10	Opt.
1.8	125.00	100	1~10	10	Opt.
2.5	212.50	100	1~10	10	Opt.
2.8	250.00	100	1~10	10	Opt.
3.3	312.50	100	1~10	10	Opt.

Low ESR Capacitors

With the RY6050-ADJM5R, a stable output voltage is achievable even if used with low ESR capacitors as a phase compensation circuit is built-in. In order to ensure the effectiveness of the phase compensation, we suggest that an output capacitor (C_{OUT}) is connected as close as possible to the output pin (V_{OUT}) and the GND pin. Please use an output capacitor with a capacitance value of 10uF. Also, please connect an input capacitor (C_{IN}) of 10uF between the V_{IN} pin and the GND pin in order to ensure a stable power input. Stable phase compensation may not be ensured if the capacitor runs out capacitance when depending on bias and temperature. In case the capacitor depends on the bias and temperature, please make sure the capacitor can ensure the actual capacitance.

Current Limiter, Short-Circuit Protection

The RY6050-ADJM5R includes a combination of a fixed current limiter circuit & a feedback circuit, which aid the operations of the current limiter and circuit protection. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. As a result of this drop-in output voltage, the feedback circuit operates, output voltage drops further and output current decreases.

EN pin

The IC's internal circuitry can be shutdown via the signal from the EN pin with the RY6050-ADJM5R. Driving EN over 1 V turns on the regulator. Driving EN below 0.5 V puts the regulator into shutdown mode. The operational logic of the IC's EN pin is selectable. Note that as the standard RY6050-ADJM5R type's regulator is 'High Active/No Pull-Down', operations will become unstable with the EN pin open. Although the EN pin is equal to an inverter input with CMOS hysteresis, with either the pull-up or pull-down options, the EN pin input current will increase when the IC is in operation. We suggest that you use this IC with either a V_{IN} voltage or a GND voltage input at the EN pin. If this IC is used with the correct specifications for the EN pin, the operational logic is fixed and the IC will

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operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry.

Notes on Use

1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between V_{IN} and GND wiring.
3. Please wire the input capacitor (C_{IN}) and the output capacitor (C_{OUT}) as close to the IC as possible.

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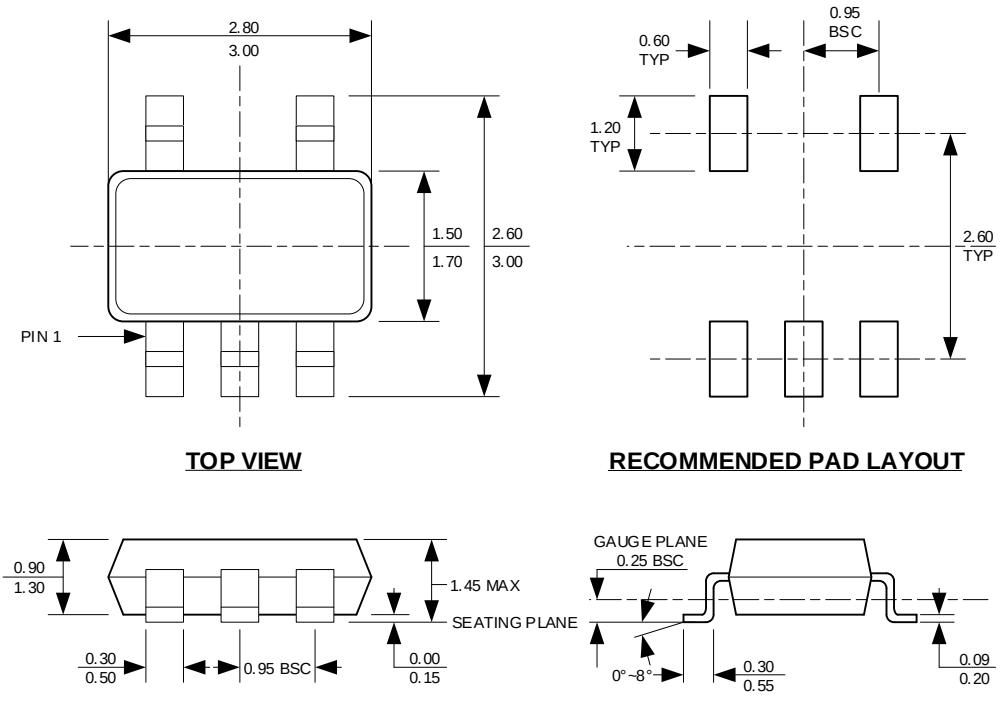
Packaging Information

5-Pin SOT23 Packaging Information

SOT23-5



NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.