Industrial Application
Battery Monitoring IC

KA49517A
Product Standards

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Characteristics

- Maximum support 17 battery cells in series
- 10mV measurement accuracy with 14 bits voltage ADC for cell voltage, and 5 channels analog input measurement for Thermistor
- Built-in 16 bits Low speed Current measurement ADC (Coulomb Counter) and 15 bits High speed Current measurement ADC
- Low–side Sense resistor Current measurement and monitoring
- Operation mode - Active, Standby/Low power; Sleep and Shutdown
- SPI serial communication interface up to 1MHz clock with CRC code correction and watchdog timer
- Built-in ALARM pins for overvoltage, undervoltage, overcurrent and short circuit detection and protection feature
- Built-in cell balancing MOSFET, support external cell balance MOSFET operation as well
- 3 channels General GPIO and 2 channels high voltage output GPOH
- Interrupt signal provision for MCU to notify state of operation as well as measurement cycle indication at the available GPIO pins
- High-side N-MOSFET driver: Charge (CHG) & Discharge (DIS) with built-in charge pump and FETOFF control pin
- Built in controllable fuse driver for cell OV and overcurrent monitoring algorithm to serve as secondary protection system
- Regulator (REG_EXT) for external circuit power provision with selectable output setting 5V/3.3V/2.5V, and 50mA drive ability
- Safety Diagnostic function for measurement related check and FET driver check to enhance the total diagnostic coverage of the chip
- Package : TQFP 64L (10x10x1mm^3, Lead Pitch 0.5mm)

Overview

KA49517A is a battery monitoring IC with protection function. With high resolution ADC built-in, KA49517A is capable to measure battery cell voltage and current level accurately.

Through SPI serial interface, microcontroller unit (MCU) is able to read the status and measured result by KA49517A.

The ALARM pins alert the MCU with the abnormal condition such as over voltage (OV), under voltage (UV),

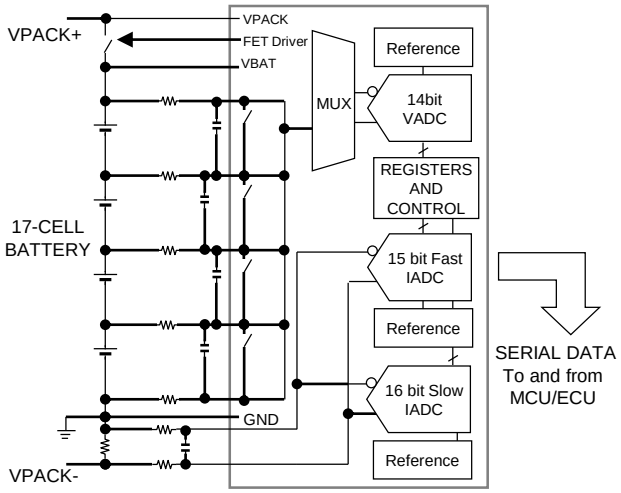
over current (OC) and short circuit (SC).

KA49517A can support an application with up to 17 batteries cells in series or a maximum voltage of 85V, it is suitable for application with high input voltage such as E-bike, UPS etc.

Applications

- Pedelec, e-Bike, UPS, Server Backup System, Power Tool, Energy Storage Systems etc

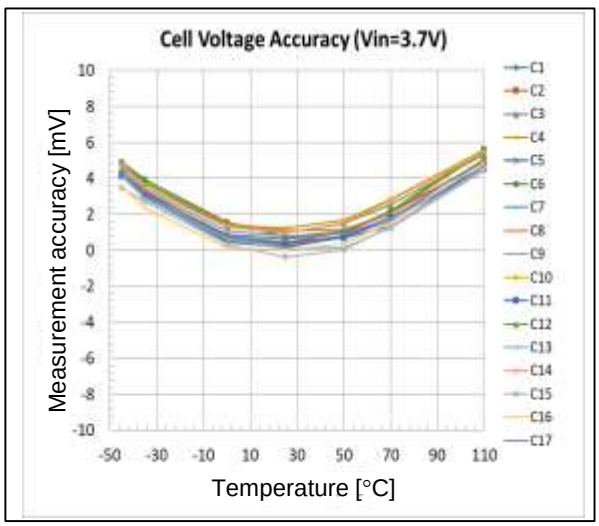
System Block Diagram



Notes: This is just an example of a circuit set: it is not guaranteed to function identically to the final production version. When designing a set for production, make sure to carefully evaluate and verify the circuitry.

Representation Characteristics

Measurement accuracy



Application circuit example (17cells connection), VBAT=62.9V , cell voltage ΔCn (C_n-C_{n-1}) = 3.7V

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Absolute Maximum Ratings

Parameter	Symbol *1	Rating	Unit	Notes
Supply voltage	V_{VBAT} to GND	-0.3 to 130	V	*5
	V_{CVDD} to GND	-0.3 to 6.4	V	*2
	V_{VDD55} to GND	-0.3 to 6.4	V	*2
	V_{VDD18} to GND	-0.3 to 2.3	V	*2
	V_{REGEXT} to GND	-0.3 to 6.4	V	*2
Input Voltage Range	Cn (n=10 ～17)	-0.3 to V_{VBAT}	V	
	Cn (n=1～9)	-0.3 to 38 + 11*(N-1)	V	
	C0	-0.3 to 38	V	
	SEN, SCL, SDI, FETOFF, GPIOn (n=1～3)	-0.3 to V_{CVDD}+0.3	V	*3
	TMONIn (n=1～5), REGSEL	–0.3 to V_{VDD55}+0.3	V	*3
	SRP.SRN	-0.5 to 2.0	V	
	VPC	-0.3 to 130	V	
	LDM	-0.3 to 130	V	
	SHDN	-0.3 to 6.4	V	
Output Voltage Range	ALARM1,SDO,NRST	-0.3 to V_{CVDD}+0.3	V	
	GPOHn (n=1～2)	-0.3 to 130	V	
	REGB	-0.3 to 14	V	
Output Current Range	ALARM1,SDO,NRST GPIOn (n=1～3)	-6.0 to +6.0 (-12.0 to +12.0)	mA	*4
	REGB	-3.5 to 3.5	mA	
	REGEXT	-50.0 to 0	mA	*6
Allowable Voltage Between Pins	C_n - C_{n-1} (n=1～17)	-0.3 to 11	V	
Operating junction temperature	T_j	-40 to 125	°C	*2
Storage temperature	T_{stg}	-55 to 125	°C	*2

Notes: Stresses that exceed the absolute maximum ratings may cause fatal damage to the product.
This specifies the maximum rating for stress.
It is NOT a guaranteed operating region because it exceeds the recommended operating conditions.
The reliability of the IC may be affected if it is kept under absolute maximum rating conditions for long periods.
Applied external current and voltage to pins should also not exceed the absolute maximum ratings listed here.

*1: GND is the voltage of pins GND1, GND2, and GND3 which are connected inside the device.
Connect these pins on the board and apply the same voltage.

*2: The maximum ratings are allowable unless the power consumption exceeds the power dissipation ratings.

*3: V_{CVDD} is the voltage of CVDD. V_{VDD55} is the voltage of VDD55. It should not exceed the rated 6.4 V.

*4: + Polarity is the direction in which current flows into the IC pins.
– Polarity is the direction in which current flows out from the IC pins.

*5: V_{VBAT} is the voltage of VBAT. It should not exceed the rated 130V.

*6: The output circuit consists of both external components and internal circuitry.
Refer to the application circuit diagram.

Power Dissipation Ratings

Package	θj-a	θj-c	P_D (Ta = 25°C)	P_D (Ta=105°C)	Note
TQFP 64L (10x10x1mm^3, Lead Pitch 0.5mm)	37.7 °C/W	2.7 °C/W	2.65 W	0.53 W	*1

Notes: These characteristics are the reference values for design.
Refer to the PD-Ta characteristics diagram in the package specifications. Thermal design with a sufficient margin is recommended based on the conditions of supply voltage, load, and ambient temperature.

*1: Mounting board: Glass epoxy 4-layer board without soldered heat spreader measuring 50 mm x 50 mm x 0.8 mm
Wiring layer thickness: all layers 0.035 mm, proportion of copper foil: 57% / 100% / 100% / 57%

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

Recommended Operating Conditions

Below items must be within the range of Recommended Operating Conditions.

Parameter	Symbol *1	Min.	Typ.	Max.	Unit	Note
Supply voltage range	V_{VBAT}	12.5	62.9	85	V	*2
	V_{CVDD}	3.0	5.0	5.5	V	
Input Voltage Range	C_n - C_{n-1} (n=1～17)	1.0	—	4.8	V	*3
	SEN, SCL, SDI	0	—	V_{CVDD}	V	
	TMONIn (n=1～5)	0	—	V_{VDD55}	V	
	GPIOn (n=1～3)	0	—	V_{CVDD}	V	
	REGSEL	0	—	V_{VDD55}	V	
	SRP,SRN	-0.18	—	0.18	V	
	VPC	0	—	85	V	
	LDM	0	—	85	V	
	SHDN	0	—	V_{VDD55}	V	
Operating Ambient Temperature	Ta_{opr}	–40	25	105	℃	

*1: GND is the voltage of pins GND1, GND2, and GND3, which are connected inside the device.
Connect these pins on the board and apply the same voltage.

*2 : The recommended operating supply range varies due to the characteristics of the external Nch BJT connected to VDD55. Use the parts described in the recommended circuit.

*3: The C_n - C_{n-1} voltage measurement accuracy is not guaranteed if input is less than 2.0 V or more than 4.3 V. Moreover, the measurement accuracy is not guaranteed unless the following conditions are fulfilled.
C2 > 2.0 V, C17 > 12 V, VBAT – C17 > –2 V, VBAT - C16 > 1 V
* Cn (n = 1 to 17) and VBAT voltage in this conditions are in reference to GND.
* Similarly for the monitoring system, replace the above condition Cn (n = 1 to 17) with CBn (n = 1 to 17).

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SUPPLY CURRENT*1							
VBAT Active Mode	I_{BAT1}		—	3.6	4.5	mA	
VBAT Low Power Mode	I_{BAT2}	INTMSEL=10 20ms intermittent mode	—	1.35	1.75	mA	*2
VBAT Standby Mode	I_{BAT3}	VDD55=Low Power, REGEXT=Low Power Coulomb Counter=off FDRV=power reduction mode INTMSEL=00 Communication=off	—	0.22	0.30	mA	
VBAT Sleep Mode	I_{BAT4}	VDD55=Low Power, REG18=Low Power, REGEXT=off, Communication=off	—	80	130	μA	
VBAT Shutdown Mode	I_{BAT5}		—	0	1	μA	
VDD55							
VDD55 Output Voltage	V_{VDD55}		5.3	5.5	5.8	V	
VDD55 Base Current1	IB_{VDD551}	High Power mode; Temp=25ºC; VBAT=62.9V	0.75	1.025	1.30	mA	
VDD55 Base Current2	IB_{VDD552}	Low Power mode; Temp=25ºC; VBAT=62.9V	0.4	0.65	0.9	mA	
REGEXT							
REGEXT Output Voltage1	V_{EXT1}	REGSEL pin=L	4.75	5	5.25	V	
REGEXT Output Voltage2	V_{EXT2}	REGSEL pin=H	3.05	3.3	3.55	V	
REGEXT Output Voltage3	V_{EXT3}	REGSEL pin=Float	2.3	2.5	2.7	V	
REGEXT Output Current1	I_{EXT1}	Normal mode	0	—	50	mA	
REGEXT Output Current2	I_{EXT2}	Low Power mode	0	—	10	mA	
REG18							
REG18 output Voltage	V_{REG18}	No load condition	1.78	1.85	1.92	V	

*1 : Current consumption is based on the following settings.
- Consumption current is measured based total current from VBAT pin (pin 14) and VDD55 pin (pin 28).
- LDM pin is HIZ condition unless specified ;All pins no load ;SEN, SCL, and SDI = Low
- Unless otherwise specified, all registers are in the default setting.
  If VDD55 and CVDD are supplying an external load, this extra current should be included additionally .

*2 : Design reference value not tested during final production inspection.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN1}	C_n - C_{n-1} (n=1～17)	0	—	5	V	*4
Voltage Resolution	V_{RES1}	14bits $V_{RES1} = 5 / 2^{14}$	-—	0.3	—	mV	*4
Voltage Accuracy1	V_{ACC_VC1}	ΔCn = 2.0V ～ 4.3 V	–5	—	5	mV	*1 to *3
Voltage Accuracy2	V_{ACC_VC2}	ΔCn = 2.0V ～ 4.3 V Ta = –30℃ ～ 75℃	–10	—	10	mV	*4
Voltage Accuracy3	V_{ACC_VC3}	ΔCn = 2.0V ～ 4.3 V Ta = –40℃ ～ 85℃	–15	—	15	mV	*4
Conversion Time	t_{conv}	time/cell	—	50	—	μs	*4
Cell Measurement Input Current	I_{IN}	Active mode	–5	—	5	μA	
Input Leakage Current	I_{LK}	Shutdown mode	–1	—	1	μA	
OVER / UNDER VOLTAGE DETECTOR (OV / UV)							
OV detection threshold step	V_{ACC_OV}	2.0～4.5V@6bit	—	50	—	mV	*4
UV detection threshold step	V_{ACC_UV}	0.5～3.0V@6bit	—	50	—	mV	*4
VPACK CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN2}		0	—	110	V	*4
Voltage Resolution	V_{RES2}	14bits	—	6.7	—	mV	*4
Voltage Accuracy1	V_{ACC_VPACK1}	V_{VPACK} = 12.5V ～ 76.5V	–1	—	1	V	*1 to *3
Voltage Accuracy2	V_{ACC_VPACK2}	V_{VPACK} = 12.5V ～ 76.5V T_a = –30℃ ～ 75℃	–1	—	1	V	*4

*1 : The C_n - C_{n-1} voltage measurement accuracy is not guaranteed if input is less than 2.0 V or more than 4.3 V. Moreover, the measurement accuracy is not guaranteed unless the following conditions are fulfilled.
C2 > 2.0 V, C17 > 12 V, VBAT – C17 > –2 V, VBAT - C16 >1 V
* Cn (n = 1 to 17) and VBAT voltage in this conditions are in reference to GND.

*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting. The value in the parenthesis is the accuracy after soldering and aging.

*3 : Measurement accuracy value including consideration of input average current and input leakage current.

*4 : Design reference value not tested during final production inspection.

*5 : Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
Cell (Monitoring) voltage resolution, $V_{RES1} = V_{IN1} / 2^{14} = 5 / 2^{14}$ = 0.3mV approx.
Vpack voltage resolution, $V_{RES2} = V_{IN2} / 2^{14} = 110 / 2^{14}$ = 6.7mV approx

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TMONI1-5 VOLTAGE MONITOR							
Input Voltage Range	V_{IN3}		0	—	5	V	*1
Voltage Resolution	V_{RES3}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_TMONI1}	VIN = 0.4V～4.7V Not use Pull-up Resistance	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_TMONI2}	VIN = 0.4V～4.7V Not use Pull-up Resistance T_a = –30℃ ～ 75℃	–10	—	10	mV	*1
Voltage Accuracy3	V_{ACC_TMONI3}	VIN = 0.4V～4.7V Not use Pull-up Resistance T_a = –40℃ ～ 85℃	–15	—	15	mV	*1
Input Pull-up Resistance	R_{PU}		7	10	13	kΩ	
Input Pull-up Resistance Temperature coefficient	RT_{PU}	T_a = –30℃ ～ 75℃ (with reference to 25℃)	–1.0	—	1.0	%	*1
GPIO1-2 VOLTAGE MONITOR							
Input Voltage Range	V_{IN4}		0	—	5	V	*1
Voltage Resolution	V_{RES4}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_GPIO1}	VIN = 0.4V～4.7V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_GPIO2}	VIN = 0.4V～4.7V T_a = –30℃ ～ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	V_{ACC_GPIO3}	VIN = 0.4V～4.7V T_a = –40℃ ～ 85℃	–20	—	20	mV	*1

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
TMONI voltage resolution, $V_{RES3} = V_{IN3}(Max.) / 2^{14} =$ 5 / 2^{14} = 0.3mV approx.
GPIO voltage resolution, $V_{RES4} = V_{IN4}(Max.) / 2^{14} =$ 5 / 2^{14} = 0.3mV approx.
*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.
*3 : Measurement accuracy value including consideration of input average current and input leakage current.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VDD55 VOLTAGE MONITOR							
Input Voltage Range	V_{IN5}		0	—	7.5	V	*1
Voltage Resolution	V_{RES5}	14bits	—	0.5	—	mV	*1
Voltage Accuracy1	V_{ACC_VDD551}	VIN = 5.5V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_VDD552}	VIN = 5.5V T_a = –30℃ ~ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	V_{ACC_VDD553}	VIN = 5.5V T_a = –40℃ ~ 85℃	–20	—	20	mV	*1
REGEXT VOLTAGE MONITOR							
Input Voltage Range	V_{IN6}		0	—	7.5	V	*1
Voltage Resolution	V_{RES6}	14bits	—	0.5	—	mV	*1
Voltage Accuracy1	$V_{ACC\_REGEXT1}$	VIN = 5V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	$V_{ACC\_REGEXT2}$	VIN = 5V T_a = –30℃ ~ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	$V_{ACC\_REGEXT3}$	VIN = 5V T_a = –40℃ ~ 85℃	–20	—	20	mV	*1

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
VDD55 voltage resolution, $V_{RES5} = V_{IN5}(Max.) / 2^{14} =$ 7.5 / 2^{14} = 0.5mV approx.
REGEXT voltage resolution, $V_{RES6} = V_{IN6}(Max.) / 2^{14} =$ 7.5 / 2^{14} = 0.5mV approx.

*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.

*3 : Measurement accuracy value including consideration of input average current and input leakage current.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
VDD18 VOLTAGE MONITOR							
Input Voltage Range	V_{IN7}		0	—	5	V	*1
Voltage Resolution	V_{RES7}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_VDD181}	VIN = 1.85V	–10	—	10	mV	*2 to *3
Voltage Accuracy2	V_{ACC_VDD182}	VIN = 1.85V T_a = –30℃ ~ 75℃	–15	—	15	mV	*1
Voltage Accuracy3	V_{ACC_VDD183}	VIN = 1.85V T_a = –40℃ ~ 85℃	–20	—	20	mV	*1
CELL BALANCING CONTROL OUTPUT (CBn)							
Output Impedance	Z_{CB}	⊿Cn = 3.0V ~ 5.0V	—	12.5	20	Ω	
THERMAL SHUTDOWN							
Shutdown Threshold	T_{SD2}	Tj	150	175	200	°C	*1

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
VDD18 voltage resolution, $V_{RES7} = V_{IN7}(Max.) / 2^{14} = 5 / 2^{14} = 0.3mV$ approx.
*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.
*3 : Measurement accuracy value including consideration of input average current and input leakage current.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LOW SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN8}		-180	—	180	mV	*1
Voltage Resolution	V_{RES8}	16bits	—	5.493	—	μV	
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	*2
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*1
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-25	—	25	μV	
HIGH SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN9}		-180	—	180	mV	*1
Voltage Resolution	V_{RES9}	15bits	—	10.99	—	μV	*3
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	*2 *3
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*1
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-50	—	50	μV	*3
CURRENT PROTECTION (SRP,SRN)							
Over Current in Charge Detection Accuracy1	V_{CP_OCC}	Detection Threshold 5mV & 10mV	-4	—	4	mV	*1
Over Current in Charge Detection Accuracy2	V_{CP_OCC}	Detection Threshold from 15mV to 120mV	–10	—	10	mV	
Over Current in Discharge Detection Accuracy1	V_{CP_OCD}	Detection Threshold from 10mV to 100mV	–10	—	10	mV	
Over Current in Discharge Detection Accuracy2	V_{CP_OCD}	Detection Threshold from 100mV to 320mV	–10	—	10	%	
Short Circuit in Discharge Detection Accuracy1	V_{CP_SCD}	Detection Threshold from 20mV to 100mV	–10	—	10	mV	
Short Circuit in Discharge Detection Accuracy2	V_{CP_SCD}	Detection Threshold from 100mV to 640mV	–10	—	10	%	

*1 : Design reference value not tested during final production inspection.
Voltage resolution Typ. value is an approximate value derived from the Input voltage range Max. value and the number of bits.
$V_{RES8} = V_{IN8}(max.) / 2^{16} = 360mV / 2^{16} = 5.493\mu V$ approx. ; $V_{RES9} = V_{IN9}(max.) / 2^{15} = 360mV / 2^{15} = 10.99\mu V$ approx.
*2 : This is the final inspection value before shipping out. The value does not include variations caused by stress applied during board mounting or after board mounting.
*3 : Values are for normal measurement mode only (not in V-I sync mode)

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
GENERAL PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage “H”	V_{IH1}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL1}		0	—	V_{CVDD} ×0.2	V	
Output Voltage “H”	V_{OH1}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL1}	I_{OL} = +1mA	–0.3	—	0.4	V	
GENERAL PURPOSE HV OUTPUT (GPO)							
Output Voltage “L”	V_{HVOL1}	I_{OL} = +1mA	–0.3	—	7.0	V	
DIGITAL INPUT(1) VPC							
Input Voltage “H”	V_{IH2}		4.0	—	—	V	
Input Voltage “L”	V_{IL2}		—	—	0.3	V	
Pull-down resistance	R_{IL2}		6	28	55	MΩ	
DIGITAL INPUT(2) LDM							
Input Voltage “H”	V_{IH3}	LDM pin voltage rising for load release detection	—	2.2	2.3	V	
Input Voltage “L”	V_{IL3}	LDM pin voltage falling for load current detection	1.9	2	—	V	
Pull-Up current source 1	I_{IL3_1}	LDM pin=2V ILDM setting=50uA	30	50	70	μA	
Pull-Up current source 2	I_{IL3_2}	LDM pin=2.2V ILDM setting =400uA	200	400	600	μA	
DIGITAL INPUT(3) SHDN							
Input Voltage “H”	V_{IH4}		3.0	—	—	V	
Input Voltage “L”	V_{IL4}		—	—	0.1	V	
Pull-down resistance	R_{IL4}		200	820	1500	kΩ	

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DIGITAL INPUT(4) SDI,SCL,SEN,FETOFF							
Input Voltage “H”	V_{IH5}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL5}		0	—	V_{CVDD} ×0.2	V	
Input Leakage Current	I_{LK5}		-1	0	1	μA	
DIGITAL INPUT(5) REGSEL							
Input Voltage “H”	V_{IH6}	REGSEL pin=H For REGEXT=3.3V output settings	V_{VDD55} –0.3	—	—	V	
Input Voltage “L”	V_{IL6}	REGSEL pin=L For REGEXT=5V output settings	—	—	0.3	V	
Input Voltage Float	V_{FLT6}	REGSEL pin=Float For REGEXT=2.5V output settings	2	2.75	3.5	V	
DIGITAL OUTPUT(1) ALARM1,SDO							
Output Voltage “H”	V_{OH7}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL7}	I_{OL} = +1mA	–0.3	—	0.4	V	
DIGITAL OUTPUT(2) NRST							
Output voltage “L”	V_{OL8}	I_{OL} = 0 mA	–0.3	—	0.5	V	
Pull-up resistance	R_{IL8}	—	50	100	200	kΩ	

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
REGEXT UVLO							
UV detection voltage	V_{IL_UV1}	REGSEL pin=L	—	4	—	V	*1
UV release voltage	V_{IH_UV1}	REGSEL pin=L	—	4.2	—	V	*1
VDD55 UVLO							
UVLO detection voltage	V_{IL_UV2}		—	4.5	—	V	*1
UVLO release voltage	V_{IH_UV2}		—	4.75	—	V	*1
Nch. FET DRIVER							
Drive voltage (DIS=“H”)	V_{ON_DIS}	$V_{ON\_DIS} = V_{DIS} – V_{VPACK}$ VGS connect 10MΩ	9	11	13	V	
Drive voltage (CHG="H”)	V_{ON_CHG}	$V_{ON\_CHG} = V_{CHG} – V_{VBAT}$ VGS connect 10MΩ	9	11	13	V	
Drive voltage (DIS=“L”)	V_{OFF_DIS}	$V_{OFF\_DIS} = V_{DIS} – V_{VPACK}$ VGS connect 10MΩ	—	—	0.2	V	
Drive voltage (CHG=“L”)	V_{OFF_CHG}	$V_{OFF\_CHG} = V_{CHG} – V_{VBAT}$ VGS connect 10MΩ	—	—	0.2	V	
Rise time (DIS=“L” to ”H”)	tr	V_{DIS} = 0 to 4V C_L = 20nF	—	20	50	μs	*1
Rise time (CHG=“L” to ”H”)	tr	V_{CHG} = 0 to 4V C_L = 20nF	—	20	50	μs	*1
Fall time (DIS =“H” to ”L”)	tf	V_{DIS} = 90% to 10% C_L = 20nF	—	20	30	μs	*1
Fall time (CHG=“H” to ”L”)	tf	V_{CHG} = 90% to 10% C_L = 20nF	—	20	30	μs	*1

*1 :Design reference value not tested during final production inspection.

Electrical Characteristics (continued)

Unless otherwise noted, the characteristics are specified under the recommended operating condition:
VBAT = 62.9 V, CVDD = 5.0V, ambient temperature, T_a = 25℃±2℃ and test circuit reference.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI Interface Timing (SEN, SDI, SCL, SDO)							
SCL Frequency	f_{SCL}	—	—	—	1	MHz	
SCL Duty Cycle	t_{DUTY}	—	45	50	55	%	
SEN Rising to SCL Rising	t_{SEN_LD}	—	100	—	—	ns	
SCL Falling to SEN Falling	t_{SEN_LG}	—	100	—	—	ns	
SEN "L" Width	t_{SEN_LO}	—	500	—	—	ns	
SDI Setup Time	t_{SDI_SU}	SDI valid to SCL falling	100	—	—	ns	
SDI Hold Time	t_{SDI_HD}	SCL falling to SDI valid	100	—	—	ns	
SDO Valid Time	t_{SDO_VD}	SCL rising to SDO valid $C_L \leqq 50$ pF	—	—	400	ns	
SDO Disable Time	t_{SDO_DIS}	SEN falling to SDO disable	—	—	400	ns	

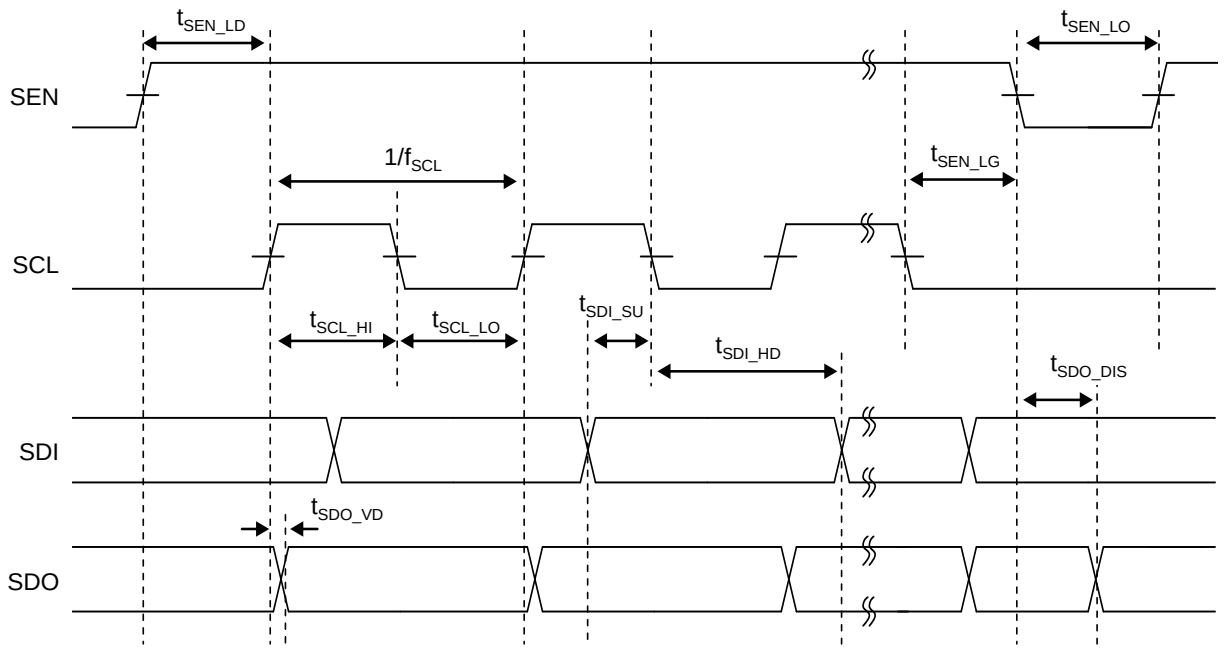
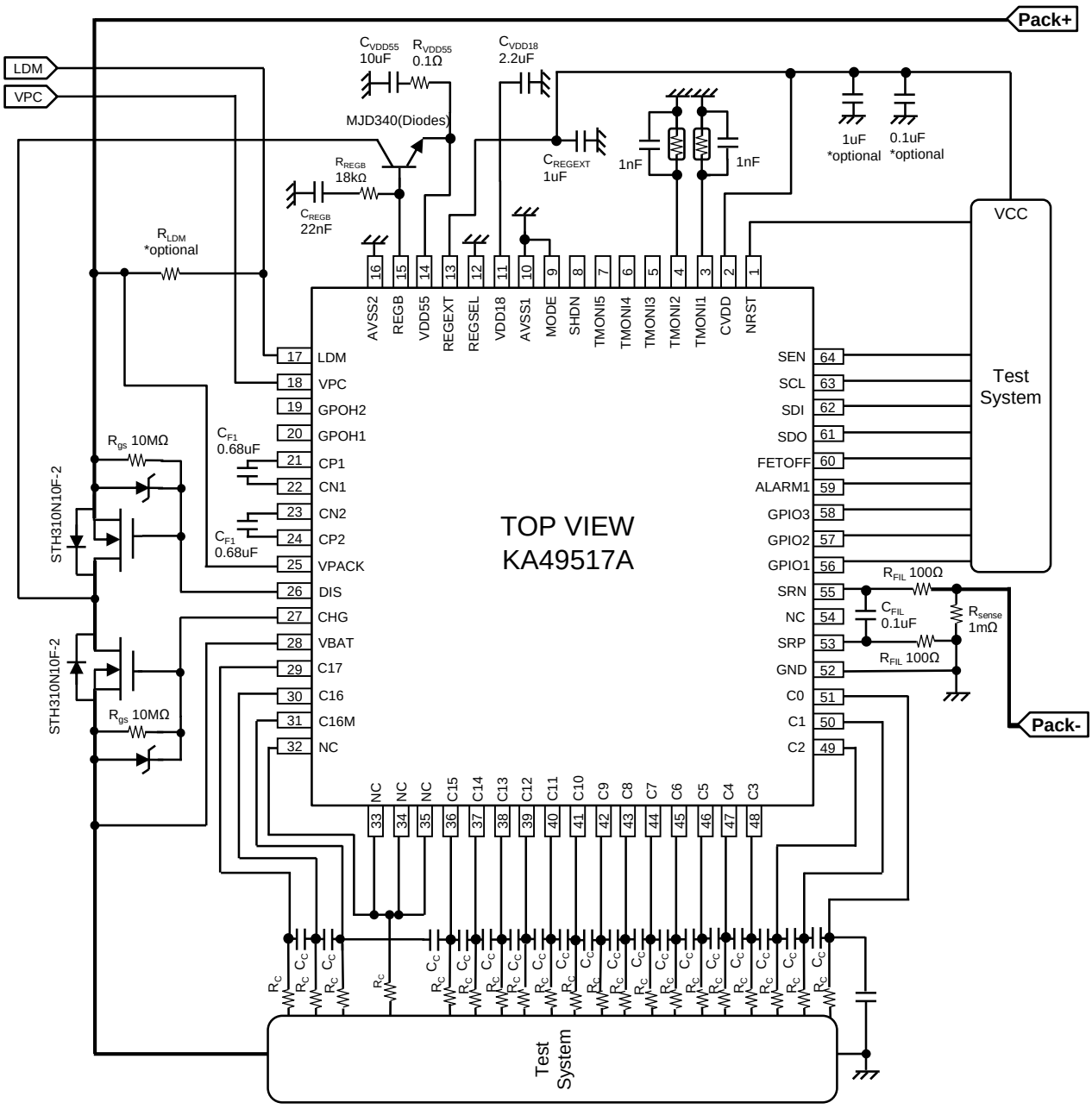


Fig.2.4.1 SPI Timing

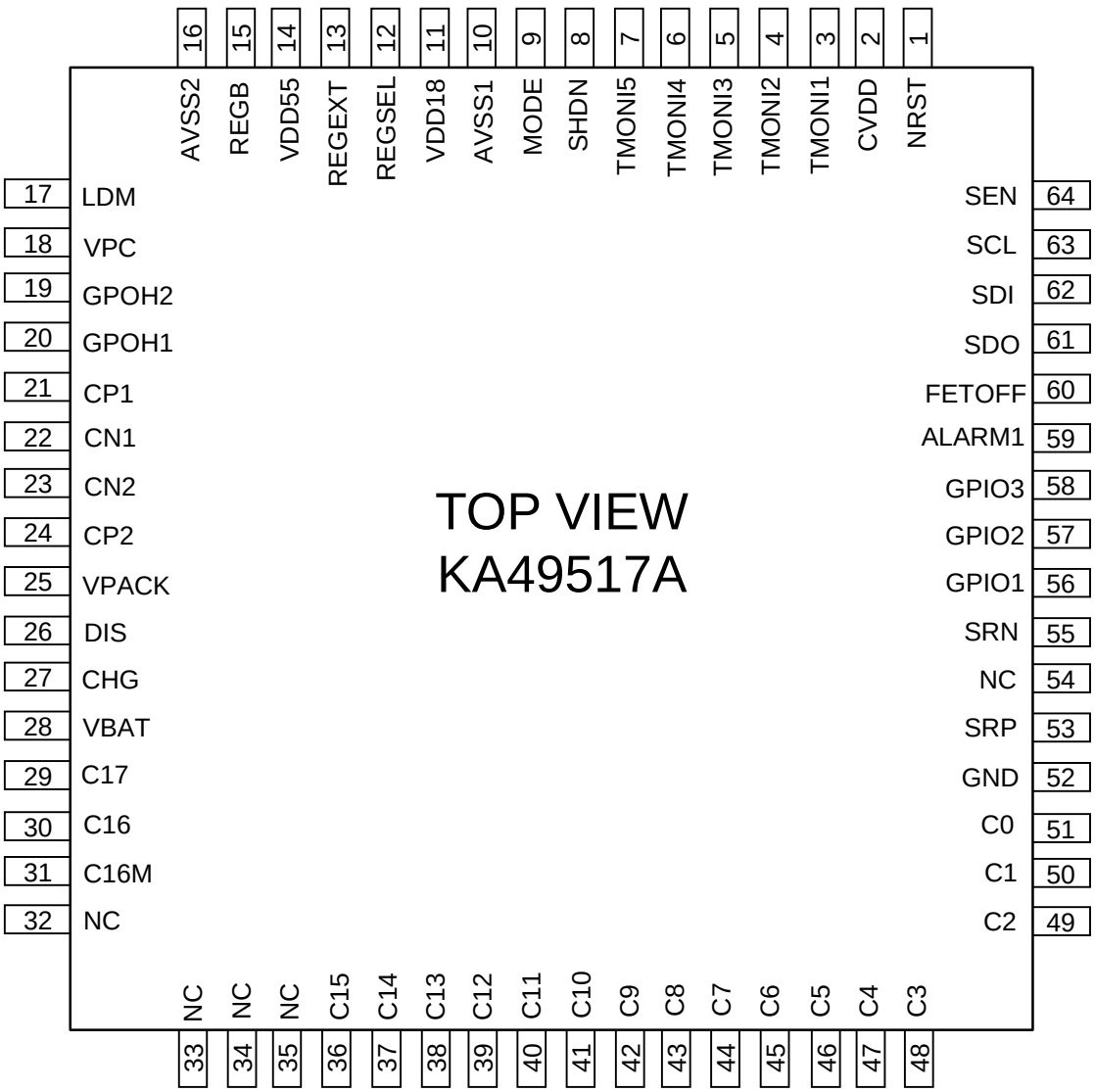
Electrical Characteristics (continued)

■Test Circuit

Electrical characteristics are tested under our recommended 17cell RC filter condition below.



*1: REGEXT voltage setting can only be set to 5V or 3.3V when using as direct connection with CVDD.
There is a requirement for the usage of REGEXT and CVDD total capacitor value.
Please refer to page 23 bottom note (*3) for more detail.


TOP VIEW
KA49517A
1 CVDD
2 NRST
3 TMONI1
4 TMONI2
5 TMONI3
6 TMONI4
7 TMONI5
8 SHDN
9 MODE
10 AVSS1
11 VDD18
12 REGSEL
13 REGEXT
14 VDD55
15 REGB
16 AVSS2
17 LDM
18 VPC
19 GPOH2
20 GPOH1
21 CP1
22 CN1
23 CN2
24 CP2
25 VPACK
26 DIS
27 CHG
28 VBAT
29 C17
30 C16
31 C16M
32 NC
33 NC
34 NC
35 NC
36 C15
37 C14
38 C13
39 C12
40 C11
41 C10
42 C9
43 C8
44 C7
45 C6
46 C5
47 C4
48 C3
49 C2
50 C1
51 C0
52 GND
53 SRP
54 NC
55 SRN
56 GPIO1
57 GPIO2
58 GPIO3
59 ALARM1
60 FETOFF
61 SDO
62 SDI
63 SCL
64 SEN

Pin Description

Pin	Pin name	Type	Description
1	NRST	O	Power Reset Output Pin（Open Drain）
2	CVDD	I (Supply)	Digital Voltage Supply
3	TMONI1	I	Analog Input Pin
4	TMONI2	I	Analog Input Pin
5	TMONI3	I	Analog Input Pin
6	TMONI4	I	Analog Input Pin
7	TMONI5	I	Analog Input Pin
8	SHDN	I	Shutdown Control “L”: Active / “H”: Shutdown
9	MODE	I	Test Mode pin for Manufacturer Use Only (Connect to DVSS always) *1
10	AVSS1	GND	Analog Ground
11	VDD18	O	1.85V LDO Output Pin for Internal Use
12	REGSEL	I	External 5V/3.3V/2.5V REGEXT output selection Pin
13	REGEXT	O	External 5V/3.3V/2.5V LDO Output Pin
14	VDD55	O	5.5V Regulator Output Pin
15	REGB	O	Base Pin for 5.5V Pre-regulator
16	AVSS2	GND	Analog Ground
17	LDM	I	Load Detect Pin
18	VPC	I	Wake Up Signal Pin - “L” Active / “H” Wake Up. Also for Charger Detect.
19	GPOH2	O	High Voltage General Purpose Output Pin 2 (Open Drain)
20	GPOH1	O	High Voltage General Purpose Output Pin 1 (Open Drain)

*1 An external pull-down resistor should be connected to MODE pin and it is internally connected to GND through a 1 kΩ resistor.

Pin Description (continued)

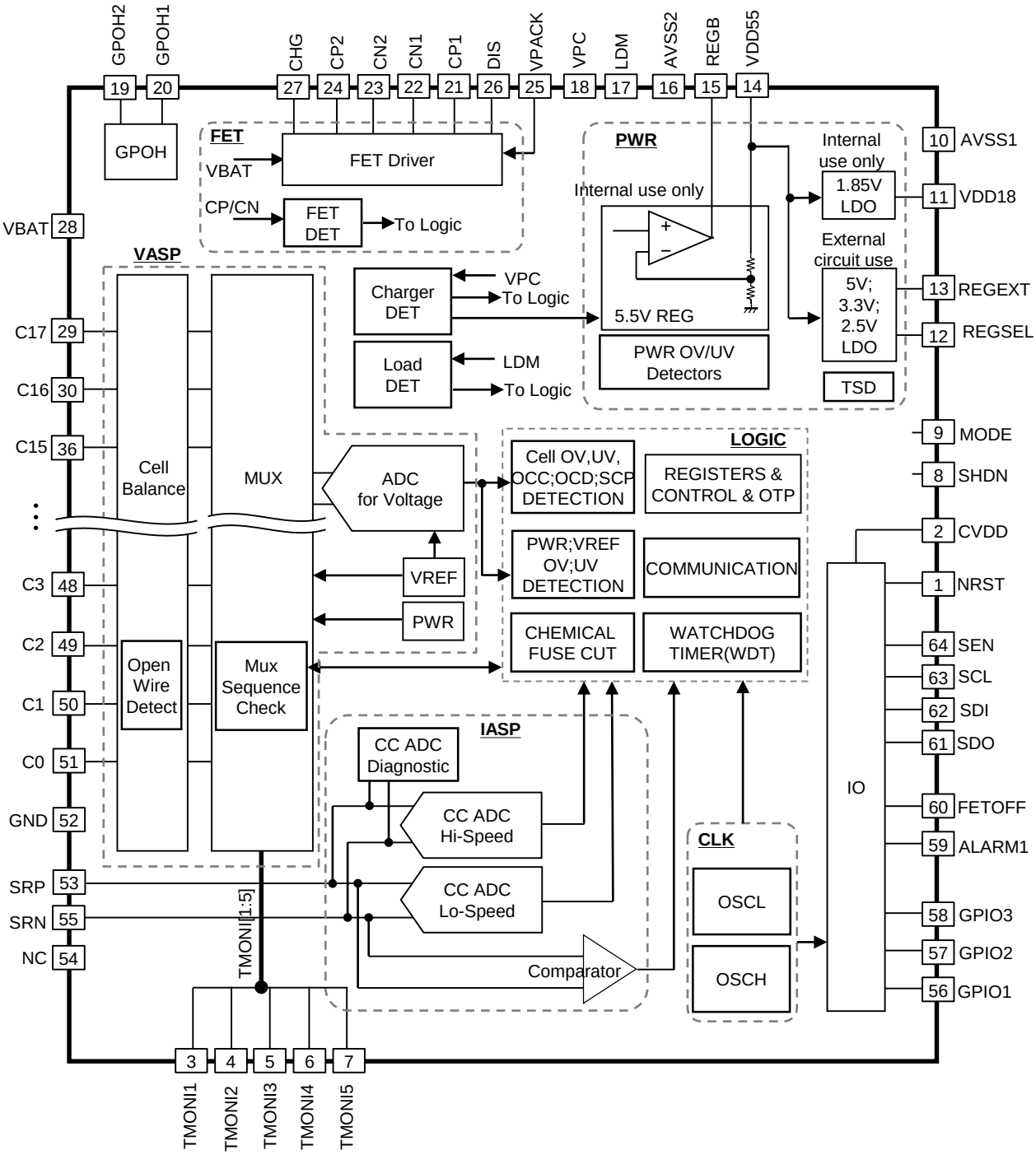
Pin	Pin name	Type	Description
21	CP1	O	Charge Pump Capacitor Pin (Positive Terminal for VPACK)
22	CN1	O	Charge Pump Capacitor Pin (Negative Terminal for VPACK)
23	CN2	O	Charge Pump Capacitor Pin (Negative Terminal for VBAT)
24	CP2	O	Charge Pump Capacitor Pin (Positive Terminal for VBAT)
25	VPACK	I (Supply)	Positive Terminal of Battery Pack to load or charger.
26	DIS	O	Discharge NMOSFET Gate Drive Pin
27	CHG	O	Charge NMOSFET Gate Drive Pin
28	VBAT	I (Supply)	Stacked Cells Highest Voltage Pin
29	C17	I	Cell 17 Input Pin (+ve)
30	C16	I	Cell 16 Input Pin (+ve) / Cell 17 Input Pin (-ve)
31	C16M	I	Cell 16 Input Pin (-ve)
32	NC	I	N.C. Pin
33	NC	I	N.C. Pin
34	NC	I	N.C. Pin
35	NC	I	N.C. Pin
36	C15	I	Cell 15 Input Pin (+ve) / Cell 16 Input Pin (-ve)
37	C14	I	Cell 14 Input Pin (+ve) / Cell 15 Input Pin (-ve)
38	C13	I	Cell 13 Input Pin (+ve) / Cell 14 Input Pin (-ve)
39	C12	I	Cell 12 Input Pin (+ve) / Cell 13 Input Pin (-ve)
40	C11	I	Cell 11 Input Pin (+ve) / Cell 12 Input Pin (-ve)

Pin Description (continued)

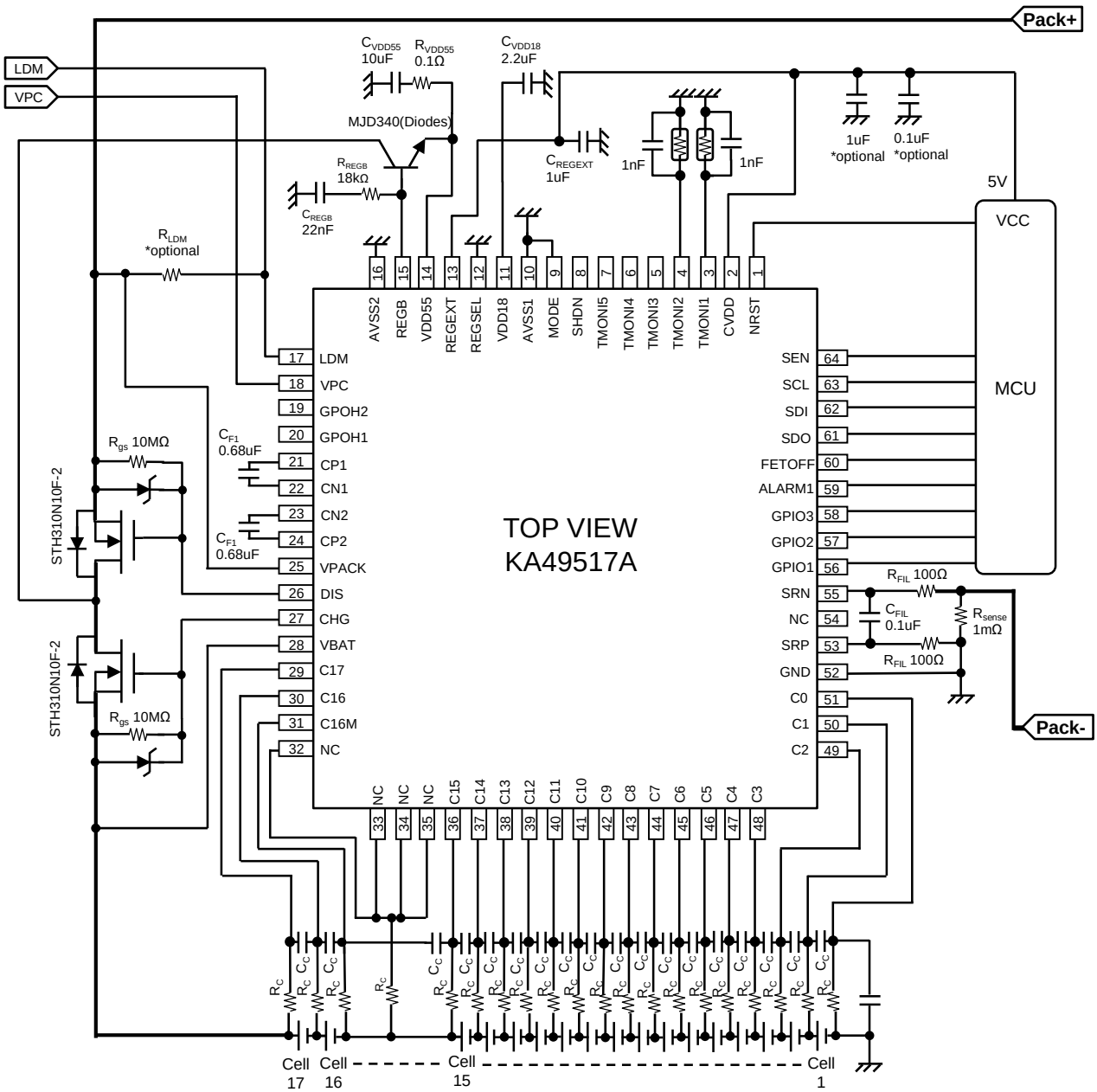
Pin	Pin name	Type	Description
41	C10	I	Cell 10 Input Pin (+ve) / Cell 11 Input Pin (-ve)
42	C9	I	Cell 9 Input Pin (+ve) / Cell 10 Input Pin (-ve)
43	C8	I	Cell 8 Input Pin (+ve) / Cell 9 Input Pin (-ve)
44	C7	I	Cell 7 Input Pin (+ve) / Cell 8 Input Pin (-ve)
45	C6	I	Cell 6 Input Pin (+ve) / Cell 7 Input Pin (-ve)
46	C5	I	Cell 5 Input Pin (+ve) / Cell 6 Input Pin (-ve)
47	C4	I	Cell 4 Input Pin (+ve) / Cell 5 Input Pin (-ve)
48	C3	I	Cell 3 Input Pin (+ve) / Cell 4 Input Pin (-ve)
49	C2	I	Cell 2 Input Pin (+ve) / Cell 3 Input Pin (-ve)
50	C1	I	Cell 1 Input Pin (+ve) / Cell 2 Input Pin (-ve)
51	C0	I	Cell 1 Input Pin (-ve)
52	GND	GND	Analog Ground
53	SRP	I	Shunt Resistor Positive Pin
54	NC	-	N.C. Pin
55	SRN	I	Shunt Resistor Negative Pin
56	GPIO1	I/O	General Purpose I/O Pin 1
57	GPIO2	I/O	General Purpose I/O Pin 2
58	GPIO3	I/O	General Purpose I/O Pin 3
59	ALARM1	O	ALARM1 Pin
60	FETOFF	I	CHG/DIS FET Control Pin - “L” Normal / “H” FET Forced OFF
61	SDO	O	SPI Interface Pin – Data Out *1
62	SDI	I	SPI Interface Pin – Data In *1
63	SCL	I	SPI Interface Pin – Clock *1
64	SEN	I	SPI Interface Pin – Enable *1

*1: An external capacitor may be required near the unused open pin to increase noise immunity.

Block Diagram



B. Application Circuit Example



*1: REGEXT voltage setting can only be set to 5V or 3.3V when using as direct connection with CVDD.
There is a requirement for the usage of REGEXT and CVDD total capacitor value.
Please refer to page 23 bottom note (*3) for more detail.

Recommended Constant of External Component

Item	Symbol	Constant				Note
		Min.	Typ.	Max.	Unit	
Constant of components connected to pins	C_{REGB}	—	22	—	nF	*1, *2
	R_{REGB}	—	18	—	kΩ	*2
	C_{VDD55}	—	10	—	μF	*1, *2
	R_{VDD55}	—	0.1	—	Ω	*2
	C_{VDD18}	—	2.2	—	μF	*1
	C_{REGEXT}	—	1	—	μF	*1,*3
	R_{GS}	—	10	—	MΩ	*2
	C_{F1}	—	0.68	—	μF	*1
	C_{F2}	—	0.68	—	μF	*1
	R_C	—	1	—	kΩ	*5
	C_C	—	1	—	μF	*1,*4
	R_{sense}	—	100	—	mΩ	*6
	R_{FIL}	—	100	—	Ω	
	C_{FIL}	—	0.1	—	μF	*1
	R_{LDM}	—	32.4	—	kΩ	*7

*1: Use of a ceramic capacitor is recommended.

*2: The parameters are applicable for system using an external NPN BJT (Diodes Inc MJD340), as shown in the recommended circuit.

*3: REGEXT can be used for as power supply for CVDD pin and external circuit. 1uF capacitor (C_{REGEXT}) is necessary at REGEXT output. It is recommended to connect a maximum of 1uF capacitor for CVDD pin and external circuit, which is compatible with default C_{VDD55} and VDD55 NPN device (Diodes Inc MJD340)

If it is necessary to increase these total capacitor value at CVDD pin and external circuit, the capacitor C_{VDD55} must be increased proportionally with about 5 times ratio to ensure stability. Please note start-up time of VDD55 and REGEXT would increase proportionally by doing this.

*4: Usage of C_n pin input filter Capacitor or Resistor of different value other than the recommended values, or, RC filter connection other than the 17 cells testing circuitry indicated in the Electrical Characteristics, will cause a shift in voltage accuracy.

*5: R_C can be selected based on the required internal MOS Cell Balance function.

It is important to maintain the current below its rated value.

*6: R_{sense} resistor design is based on actual load current needed. This value should not cause SRP and SRN pin to generate voltage out of the sensing range which will affect measurement accuracy.

*7: R_{LDM} allow user to adjust Load detector threshold based on system requirement.
By using R_{LDM} of 32.4k, it is possible to detect LDM threshold of 0.4V when load current of minimum 70uA is drawn at the pin in the case FET is open case.

Description of Functions

1. Battery Connection

The minimum required VBAT pin voltage is 12.5V to guarantee normal operation.

For application using less than 17 cells, all unused cells Cn pins should be connected as shown in figure below, user shall use cells connect to C17, C16, C1 and C2 pins first and followed by battery from lower cell. Please also note that although pin 32 ~ pin 35 are NC pins, they are to be connected as shown in the diagram below to ensure the best measurement performance of other cell pins

Battery cells connection sequence:

Connect the GND pin followed by VBAT pin. After that, it should be connected from the lower cell in turn.

GND → VBAT → Cell between C0-C1 → Cell between C1-C2 → incrementally

Figures below are some system example. Minimum VBAT for 4 cells system must be higher than 12.5V.

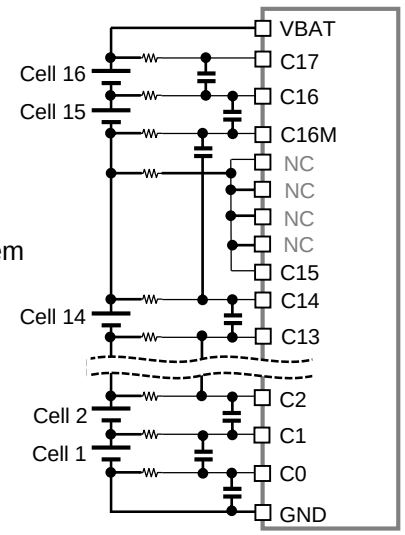


Fig.1.1.1
Example of
16 Cell System

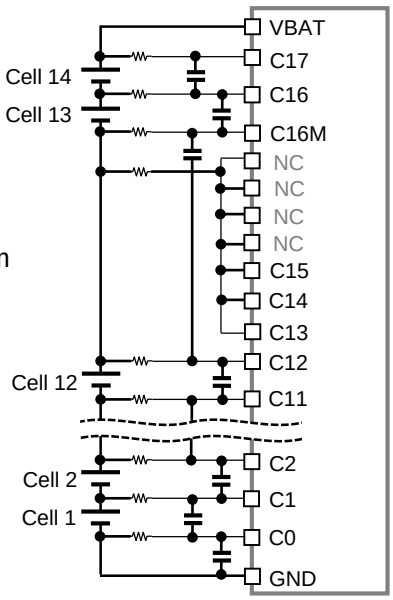


Fig.1.1.2
Example of
14 Cell System

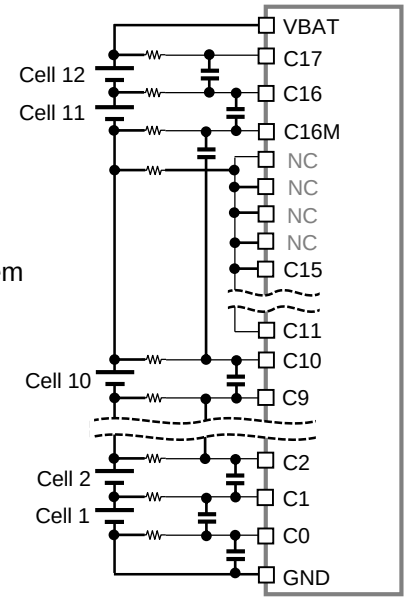


Fig.1.1.3
Example of
12 Cell System

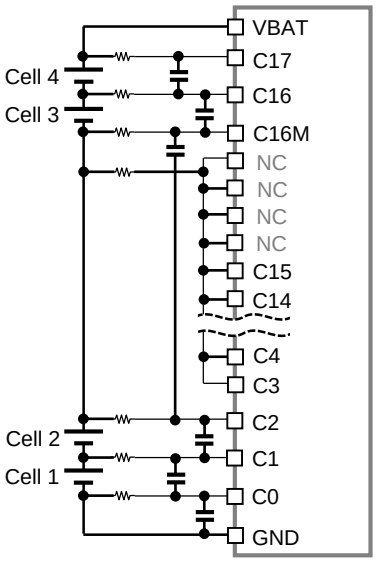


Fig.1.1.4
Example of
4 Cell System

Description of Functions

2. Operation Mode

2.1 Overview of Operation Mode

KA49517A supports the following operating mode:

Active Mode, Low Power/Standby intermittent Mode, Sleep mode and Shutdown Mode.

The operating mode can be determined by reading back register ST_ACT, ST_LP, ST_STBY, ST_INTM, ST_SDWN at address 0x1C[4:0]:

2.2 Active Mode

KA49517A will always operate in Active mode of operation after first power ON from shutdown mode.
In Active Mode, voltage measurement; high speed (HS) and Low speed(LS) current measurement can be performed. Full measurement and protection functions are also available in this mode of operation.

From shut down mode, with VPACK or VBAT pins voltage higher than 12.5V and VPC pin at “H” condition, KA49517A will enter Active Mode of operation. After wake up, NRST pin will change from “L” to “H” indicating the SPI communication is ready. After wake up, it is recommended to fix VPC pin to "L". Refer to typical startup waveform shown in Fig 2.2.1a and Fig 2.2.1b below.
For CVDD=REGEXT use case, it is recommended to perform a soft reset as the first command which can be sent either after NRST pin goes High, or after MCU active mode initialization completes. After receiving a valid SPI soft reset command, SDO pin will change from “L” to “H”. Soft Reset, NPD_RST can be set by writing address 01h [0] = “0”. This is for system to start at correct default settings regardless of the startup timing at REGEXT/CVDD pin due to different system capacitor loading at the pins.

When watchdog timer is set to enabled, KA49517A will shutdown when no communication between MCU and the IC is made in a set duration (initial value:1 minute) and VPC pin is “L”. For watchdog timer operation, refer to Chapter 13.7.

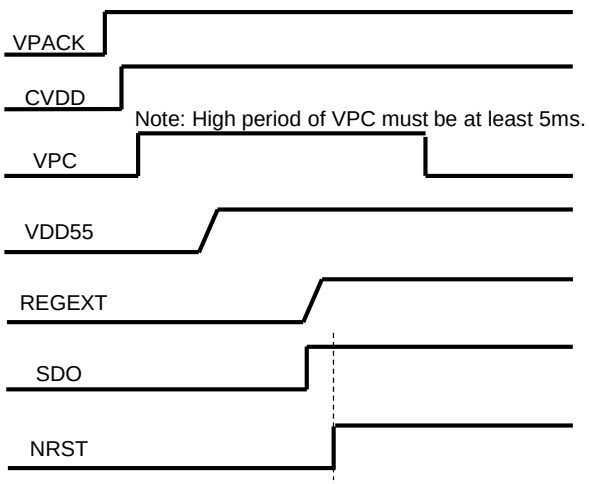


Fig. 2.2.1a Wake up waveform
(CVDD applied externally before IC startup case)

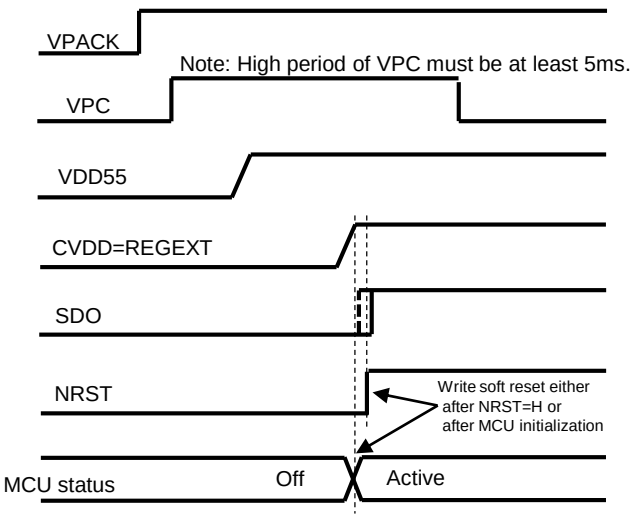


Fig. 2.2.1b Wake up waveform
(CVDD=REGEXT case)

Description of Functions

2. Operation Mode

2.3 Low Power / Standby Mode

From Active mode, user can select KA49517A to enter either Low Power mode or Standby mode of operation. This can be done by writing into registers MSET_STB and MSET_LP at address 0x01[4:3] respectively. Low Power and Standby mode are basically the same operating state. The only difference is that in Standby mode, communication between MCU and KA49517A is stopped to allow greater amount of power saving whereas In Low Power mode, communication between MCU and KA49517A is maintained. Other functions remained the same in both Low power mode and Standby mode.

In both Low Power and Standby Mode, current consumption can be reduced. Voltage and high speed (HS) current measurement ADC will not be performed in this mode. Low speed (LS) current measurement ADC, however, can still be set to operate. From Active Mode, IC enter Standby Mode by setting MSET_STB register at address 0x01[4] to be “1”. IC can return to Active mode by holding SEN pin to be “H” for a period of more than 3ms. From Active Mode, IC enter Low Power Mode by writing MSET_LP register at address 0x01[3] to be “1”. IC can return to Active mode by re-writing the same bit to be “L”.

2.4 Low Power / Standby Mode with intermittent operation

At Low power and Standby Mode, it is possible to automatically switch back to Active Mode and measure the cell voltage by setting intermittent operation using register INTMSEL at address 0x01[12:11].
KA49517A will toggle back to Active mode periodically from Low power/Standby mode to perform voltage and current measurement at a reduce power consumption level as compared to normal Active mode of operation. After Voltage and HS current measurement is completed, the state will return to Low Power or Standby Mode to reduce current consumption. Refer to table 2.4.1 and 2.4.2 for the settings.

Register: MSET_LP Address= 0x01[3]	Register: INTMSEL[1:0] Address= 0x01[12:11]	Register: INTM_TIM[1:0] / AUTO_TIM[1:0] Address=0x01[14:13]/ Address 0x01[6:5]	Current detect compare registers AUTO_ITHL[14:0] Address=0x55[14:0]	Mode description
MSET_LP = H	INTMSEL=00	--	--	Fixed Low Power mode: There is no cell voltage/HS current measurement.
MSET_LP = H	INTMSEL=01	--	--	Intermittent Low Power Mode1: Periodic Cell voltage/HS current measurement when there is no SPI communication for 1s
MSET_LP = H	INTMSEL=10	INTM_TIM=00=20ms INTM_TIM=01=40ms INTM_TIM=10=80ms INTM_TIM=11=160ms	--	Intermittent Low Power Mode2: Periodic Cell voltage/HS current measurement is possible according to the time set by INTM_TIM timer.
MSET_LP = H	INTMSEL=11	AUTO_TIM=00=10ms AUTO_TIM=01=20ms AUTO_TIM=10=40ms AUTO_TIM=11=80ms	HS current measurement is < AUTO_ITHL register settings	Intermittent Low Power Mode3: Low power mode is entered by current detection method.(HS current < AUTO_ITHL) Upon expiry of AUTO_TIM timer, IC will move from Low power mode to Active mode to perform voltage/HS current measurement. If HS current>AUTO_ITHL, IC stays in Active mode. If HS current<AUTO_ITHL, IC will return to Low power mode again and this operation repeats.

Table.2.4.1 Low power and intermittent mode setting

Description of Functions

2. Operation Mode

Register: MSET_STB Address= 0x01[4]	Register: INTMSEL[1:0] Address= 0x01[12:11]	Register: INTM_TIM[1:0] / AUTO_TIM[1:0] Address=0x01[14:13]/ Address 0x01[6:5]	Current detect compare registers AUTO_ITHL[14:0] Address= 0x55h[14:0]	Remarks
MSET_STB= H	INTMSEL=00	--	--	Fixed STB mode: There is no cell voltage/HS current measurement. SPI communication is stopped
MSET_STB= H	INTMSEL=01	--	--	Intermittent STB Mode1: Periodic Cell voltage/HS current measurement when there is no SPI communication for 1s
MSET_STB= H	INTMSEL=10	INTM_TIM=00=20ms INTM_TIM=01=40ms INTM_TIM=10=80ms INTM_TIM=11=160ms	--	Intermittent STB Mode2: Periodic Cell voltage/HS current measurement is possible according to the time set by INTM_TIM timer.
MSET_STB= H	INTMSEL=11	AUTO_TIM=00=10ms AUTO_TIM=01=20ms AUTO_TIM=10=40ms AUTO_TIM=11=80ms	HS current measurement is < AUTO_ITHL settings	Intermittent STB Mode3: STB mode is entered by current detection method.(HS current < AUTO_ITHL) Upon expiry of AUTO_TIM timer, IC will move from STB mode to Active mode to perform voltage/HS current measurement. If HS current>AUTO_ITHL, IC stays in Active mode. If HS current<AUTO_ITHL, IC will return to STB mode again and this operation repeats. Please note that after returning to active mode, SEN="H" for >3ms is necessary to re-establish back communication.

Table.2.4.2 Standby and intermittent mode setting

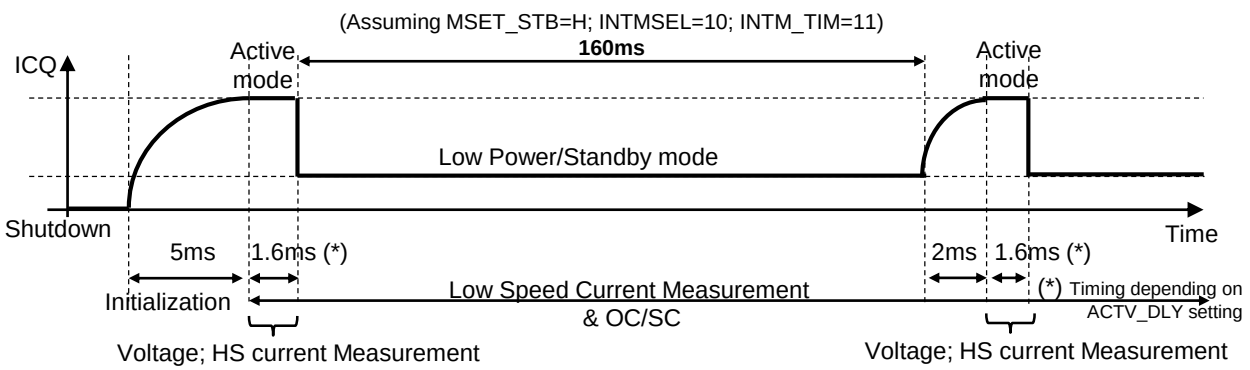


Fig. 2.4.1 Example of operation on intermittent operation (Active Mode → Standby Mode and repeating)

In summary, it is possible to reduce the current consumption by operating the IC in intermittent operation, MCU can control the IC to operate from Active Mode to Low Power/Standby Mode at periodic interval. Alternatively, Automatic intermittent operation timing and using current detection method can be set by INTMSEL;INTM_TIM; AUTO_TIM and AUTO_ITHL registers for automatic intermittent mode in KA49517A. It requires a minimum of 5ms for initialization wake up from Shutdown Mode before IC start voltage measurement and minimum of 2ms for initialization when returning to Active Mode from Low Power/Standby mode before starting voltage measurement.

Description of Functions

2. Operation Mode

To enter Low Power or Standby mode:
MCU need to write into registers; MSET_LP or MSET_STB at address 0x01[4:3] to be “1” to shift it into this state.
*When both MSET_LP and MSET_STB are written as “1” at the same time, higher priority is given to Low power mode.

To exit from Low Power or Standby mode back to active mode, there are a few ways:
(1) By setting MSET_LP=0 (from Low Power mode); or by pulling SEN pin high for 3ms(from Standby mode)
(2) Or When VPC* pin receive a high signal pulse of minimum 2ms (to signify charger detected condition in KA49517A) (This detection function can be disabled from address 0x01[7], VPC_STB_EN=“0” ; By default this function is ON)
(3) Or When LDM* pin receive a low signal pulse of minimum 2ms (to signify a load detected condition; in KA49517A) (This detection function can be disabled from address 0x01[8], LDM_STB_EN=“0”; By default this function is ON)

*Refer to VPC and LDM pin operation from chapter 3 for more details.
**Refer to state movement diagram from chapter 2.7 for more details.

2.5 Sleep Mode

KA49517A can enter Sleep mode from Active mode by writing into MSET_SLP register at address 0x01[2]=“1”
In Sleep Mode, IC current consumption is Low and there is no measurement or protection function.
FET between VPACK and VBAT will also be turned OFF in this mode. This mode helps to conserve energy by reducing current consumption and can be used when system battery pack has been unplugged making all measurement function unnecessary.

In the event of MSET_LP; MSET_STB and MSET_SLP are all written as “1” at the same time, higher priority is given to Low power mode followed by STB mode and lastly by Sleep mode.

To exit from Sleep mode back to active mode, there are a few ways:
(1) When VPC* pin receive a high signal pulse of minimum 2ms.(to signify as charger detected condition in KA49517A) This detection function can be disabled from register address 0x01[9], VPC_SLP_EN=“0” ; By default this function is ON.
(2) Or When LDM* pin receive a low signal of minimum 2ms. (to signify a load detected condition in KA49517A)This detection function can be disabled from register address 0x01[10], LDM_SLP_EN=“0”;
By default this function is ON.

Upon returning to Active mode, IC will remember its all previous register setting prior to when it enter Sleep mode. Setting both VPC_SLP_EN and LDM_SLP_EN=“0” is prohibited. If both are set to “0”, KA49517A allow VPC detection to move IC from Sleep mode back to Active mode by default.

*Refer to VPC and LDM pin operation from chapter 3 for more details.
**Refer to state movement diagram from chapter 2.7 for more details.

Description of Functions

2. Operation Mode

2.6 Shutdown Mode

The current consumption is minimized at Shutdown Mode when all circuits stopped operation.
The IC can be shutdown by setting SHDN pin to “H” (at least 1ms.) or by setting MSET_SHDN register at address 0x01[1] to “1” with VPC pin at “L”.

When Watchdog Timer, Thermal Shutdown or VDD55 UVLO are detected, KA49517A will also enter Shutdown Mode automatically while VPC pin is "L“.

Refer to table 2.6.1 below for the different condition that could shift the KA49517A into shutdown mode.

Mode	SHDN pin ”H”	MSET_SHDN "1"	Watchdog Timer	Thermal Shutdown	OVP VDD55/VDD18 /REGEXT	UVLO VDD55 /REGEXT
Active Mode	Available	Available	Available	Available	Available	Available
Low Power Mode Or Low Power intermittent Mode (Communication ON)	Available	Available	Available	Available	Available	Available
Standby Mode Or Standby intermittent Mode (Communication OFF)	Available	Not available	Available	Available	Available	Available
Sleep Mode	Available	Not available	Not available	*Available	*Available	Available

Table.2.6.1 Condition of moving to Shutdown Mode (VPC pin “L”)

Please note that:

For Watchdog Timer to shutdown the IC, COMTIMON bit at address 0x03[12] must be set to “1”.
For Watchdog Timer to shutdown the IC when in STB mode, WDT_STB_EN bit at address 0x03[14] must be set to “1”.

For Thermal shutdown detection to shutdown the IC, TSD_F_SET register at address 0x11[13] must be set to “0”.

For Over Voltage Protection of VDD55/VDD18 to shutdown the IC, OVP_F_SET bit at address 0x11[14] must be set to “0”. For Over Voltage Protection of REGEXT to shutdown the IC, OVP_F_SET_REGEXT bit at address 0x20h[2] must be set to “0”.

For Under Voltage protection of VDD55, IC will shutdown when detected. For under voltage protection of REGEXT to shutdown the IC, UVP_F_SET bit at address 0x20h[1] must be set to “0”

*In order for this function to work in Sleep mode, user will need to set the bit: DIS_OSC_OFF at address 17h[14] to be “1”. By default this function is OFF during SLEEP mode.

Description of Functions

2. Operation Mode

2.7 State Diagram

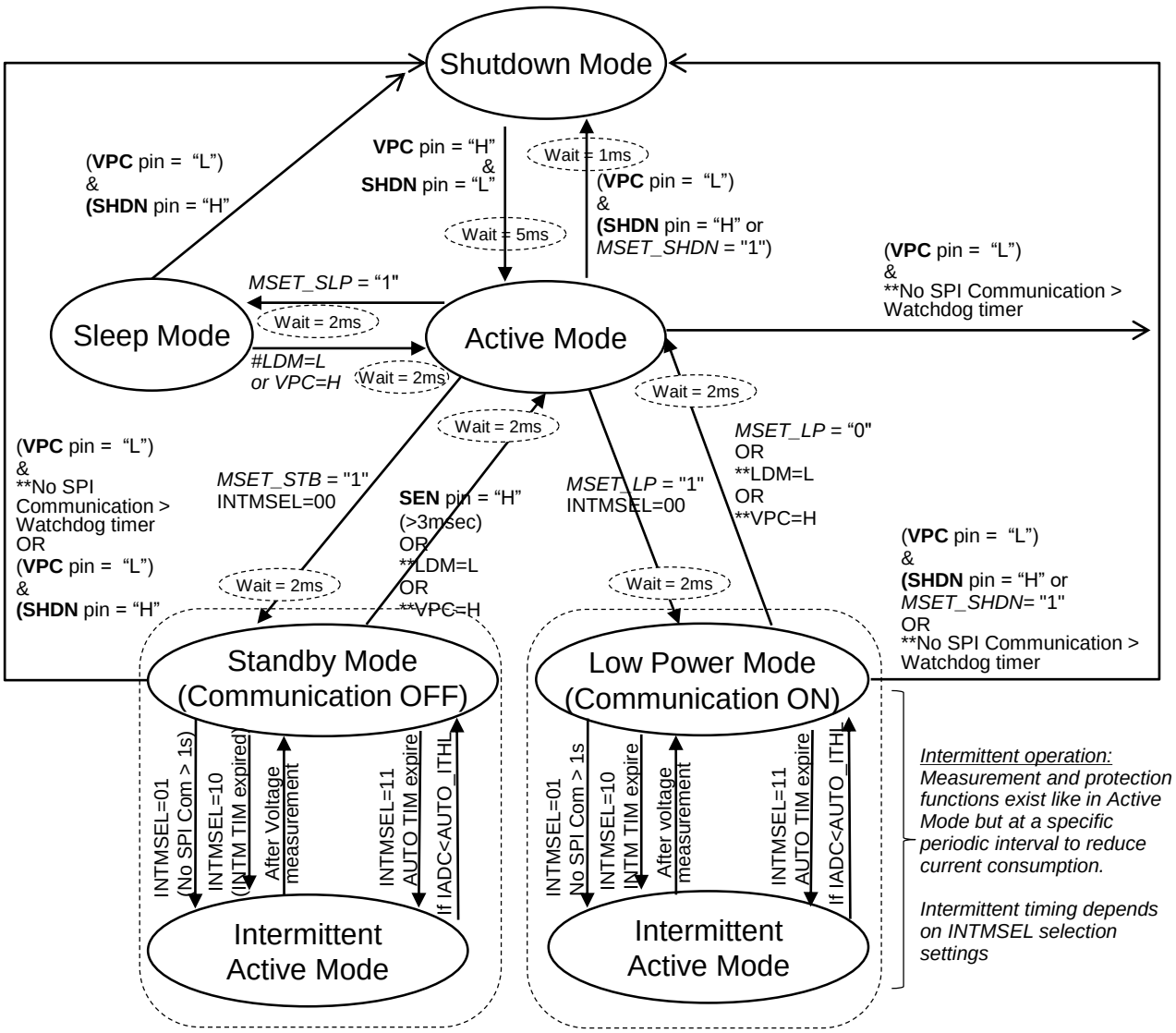


Fig.2.7.1 State Diagram

** This function can be selectable to be ON/OFF by registers.

This function can be selectable to be ON/OFF by registers.
In the event both LDM and VPC detection are set to OFF, the system will automatically select VPC as detection to return from Sleep to Active mode

Description of Functions

2. Operation Mode

Table.2.7.1 Operation Mode Summary

FUNCTION	ACTIVE (Full measurement function)	LOW POWER (Intermittent measurement selectable)	STANDBY (Intermittent measurement selectable)	SLEEP (Battery pack unplug)	SHUTDOWN (Storage / Shipment)
FET SW Control	Yes	Yes *1		OFF	OFF
Voltage ADC	Yes	Intermittent selectable		OFF	OFF
Current ADC (Fast)	Yes	Intermittent selectable		OFF	OFF
Current ADC (Slow)	Yes	Yes		OFF	OFF
Cell balance	Yes *2	Yes *2		OFF	OFF
OV/UV protection	Yes	Yes (intermittent)		OFF	OFF
TSD protection	Yes	Yes		Yes *3	OFF
SCD (discharge short)	Yes	Yes		OFF	OFF
OCD/OCC	Yes	Yes		OFF	OFF
Watchdog WDT	Yes	Yes	Yes* (register selectable ON/OFF)	OFF	OFF
SPI communication	ON	ON	OFF	OFF	OFF
External Regulator for MCU (REGEXT)	Yes (Hi Power=50mA Drive)	Yes (High Power= 50mA drive /Low Power=10mA drive)		Yes (High Power= 50mA drive /Low Power=10mA drive)	OFF
Current detect by Hi speed IADC	OFF	Yes (Selectable ON/OFF) (Provide Interrupt at selected GPIO pin when detected)	Yes (Selectable ON/OFF) (Provide Interrupt at selected GPIO pin when detected)	OFF	OFF
Charger detect @ VPC	Provide Interrupt When detected			Yes (Selectable ON/OFF)	Yes
Load detect @ LDM				Yes (Selectable ON/OFF)	OFF
Current consumption estimated	~ 3.6mA	~ 1.35mA (intermittent) ~1mA (non intermittent)	~ 0.7mA (intermittent) ~0.22 (non-intermittent)	~ 80uA	~ 1uA

Note:
The External regulator for MCU drivability, coulomb counter (CC), FET control, cell balance control can be set by respective register.

*1 DIS and CHG FET setting is kept when operation mode change from Active Mode to Standby Mode, FET control is available in Low Power Mode (Communication ON) except when register FDRV_STBY = “1”. During Standby Mode (Communication OFF), it can only be turned OFF by FETOFF pin.

*2 Cell balance can be turned ON during Active Mode/Low power/Standby mode, however it could cause wrong abnormal detection, user should not enable UV/OV detection at the same time.

*3 In order for this function to work in Sleep mode, user will need to set DIS_OSC_OFF at address 17h[14] to be “1”. By default this function is OFF during SLEEP mode.

Description of Functions

2. Operation Mode

2.8 Operation Mode control register

Table.2.7.2 Operation Mode Control Register (For Intermittent mode setting)

Register	Address [bit]	Function
INTM_TIM[1:0]	0x01 [14:13]	2 Bits programmable Delay to return from STB mode to ACT mode to check Cell voltage in intermittent mode 00: 20ms (Default) 01: 40ms 10: 80ms 11: 160ms
INTMSEL[1:0]	0x01 [12:11]	Intermittent mode selection 00: No intermittent; stay at STB or Low Power mode (Default) 01: Intermittent mode using no SPI>1s; intermittent mode of previous IC AN49503 10: Intermittent mode using INTM_TIM; lower power active mode 11: Intermittent mode using AUTO_TIM; sense current auto mode
AUTO_TIM[1:0]	0x01 [6:5]	2 Bits programmable Delay to return to Active mode by checking sense current using Fast ADC vs ITH_L in AUTO current detection mode 00: 10ms (Default) 01: 20ms 10: 40ms 11: 80ms
AUTO_ITHL[14:0]	0x55 [14:0]	15 bit to set detection current level to enter Low power auto mode (compare by IADC_fast) Use only when INTMSEL[1:0] = 11 Value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V Voltage/step = 0.005493mV
ACTV_DLY	0x11 [1:0]	Number of ADC scan cycles after returning back to Active when INTSEL==2'b11 (intermittent auto current detection mode) 00: 1 cycle 01: 2 cycles (Default) 10: 3 cycles 11: 4 cycles

Description of Functions

2. Operation Mode

2.8 Operation Mode control register

Table.2.7.3 Operation Mode Control Register
(Selectable LDM and VPC return to Active mode in STB/Low Power and Sleep mode)

Register	Address [bit]	Function
LDM_SLP_EN	0x01 [10]	Enable control by LDM pin 1: Enable return to active mode from SLP mode when LDM is high (Default) 0: No control
VPC_SLP_EN	0x01 [9]	Enable control by VPC pin 1: Enable return to active mode from SLP mode when VPC is high (Default) 0: No control
LDM_STB_EN	0x01 [8]	Enable control by LDM pin 1: Enable return to active mode from LP/STB mode when LDM is high (Default) 0: No control
VPC_STB_EN	0x01 [7]	Enable control by VPC pin 1: Enable return to active mode from LP/STB mode when VPC is high (Default) 0: No control

* VPC_SLP_EN and LDM_SLP_EN cannot be set both ‘0”.
If both “0” are set, VPC_SLP_EN will be selected automatically by the system.

*In order for LDM function to move IC state machine from Sleep or STB or Low Power back to Active, the LDM function must first be turned ON first using NPD_LDM bit at register 20h[3]=1. Refer to section 4.4 for LDM function powering up sequence.

Description of Functions

2. Operation Mode

2.8 Operation Mode control register

Table.2.7.4 Operation Mode Control Register (mode setting registers)

Register	Address [bit]	Function
MSET_STB	0x01 [4]	Standby mode control 1: Standby mode 0: Normal operation (Default)
MSET_LP	0x01 [3]	Low Power mode control 1: Low Power mode 0: Normal operation (Default)
MSET_SLP	0x01 [2]	Sleep mode control 1: Sleep mode 0: Normal operation (Default)
MSET_SHDN	0x01 [1]	Shutdown control 1: Shutdown Mode 0: Normal operation (Default)

Description of Functions

3. Power Supply Operation

3.1 Regulators Summary

KA49517A has 3 built in regulators.

(1) VDD18 regulator is for internal IC devices supply only.

(2) REGEXT is designed as supply for system external circuitries. (Eg: MCU supply)

(3) VDD55 regulator utilizes external NPN BJT transistor as power devices and it can be used for internal IC or external circuitries load driving.

Table 3.1.1 below show the summary of each regulator specification.

Table 3.1.1 Regulator functions Summary

Regulator Type	Pin	Output Voltage (V)	Output Power Devices	Output Drive in High Power (HP) Mode (mA)	Output Drive in Low Power (LP) Mode (mA)
VDD18	Pin 11	1.85	PMOS (Internal)	--	--
	Note: For internal circuit use only.				
REGEXT	Pin 13	5/ 3.3/ 2.5 (selectable)	PMOS (Internal)	50	10
	Note: For external circuit use only. Output voltage depends on REGSEL pin setting. Only 5V or 3.3V should be set for system using direct connection with CVDD.				
VDD55	Pin 14	5.5	NPN (External)	>60mA collector current drive is recommended	>10mA collector current drive is recommended
	Note: For both internal and external circuit use. Select a BJT with suitable Beta and together with the IC base current drive setting to obtain the required output current drive. (Refer to page35 for the base current design) Please verify external NPN power dissipation thoroughly. NPN power dissipation should be verified according to the system maximum operating temperature, VBAT supply and load current of REGEXT regulator. Type of NPN with low thermal resistance and optimum PCB heat pad size are recommended for the system. In case there is a need to further reduce NPN power dissipation, it is possible to connect power resistor or power Zener serially at the collector of the NPN. Verify the value of resistor or Zener in all operating condition.				

Description of Functions

3. Power Supply Operation

3.2 Regulators Mode settings

VDD55 and REGEXT regulators can be set to high power(HP) or low power (LP) setting.
LP setting can only be set when the IC operates in modes other than Active mode of operation.
During Active mode of operation, VDD55 and REGEXT will always operate in high power (HP) mode.
Refer to table 3.2.1 below for this settings.

Table 3.2.1 Regulator registers settings

Register	Address [bit]	Function
REGEXT_EN	0x02 [8]	Use to select whether REGEXT is to be used in the system or not. 1: REGEXT ON (default) 0: REGEXT OFF
STB_REGEXT_LPEN	0x02 [6]	Enable REGEXT to enter Low Power mode during Standby/Low Power mode 1: Select LP mode 0: Select HP Mode (Default)
SLP_REGEXT_LPEN	0x02 [5]	Enable REGEXT to enter Low Power during Sleep mode 1: Select LP mode 0: Select HP Mode (Default)
INTM_REGEXT_LPEN	0x02 [4]	Enable REGEXT to enter Low Power during Intermittent mode 1: Select LP mode 0: Select HP Mode (Default)
STB_VDD55_LPEN	0x02 [3]	Enable VDD55 to enter Low Power mode during Standby/Low Power mode 1: Select LP mode 0: Select HP Mode (Default)
SLP_VDD55_LPEN	0x02 [2]	Enable VDD55 to enter Low Power during Sleep mode 1: Select LP mode 0: Select HP Mode (Default)
INTM_VDD55_LPEN	0x02 [1]	Enable VDD55 to enter Low Power during Intermittent mode 1: Select LP mode 0: Select HP Mode (Default)
PD_REG	0x17 [6]	VDD55 regulator power down 1: Power down 0: Normal (Default). *For Power down condition, it is necessary to force 5.5V/5V at VDD55 pin. In the case 5V is forced externally at the pin, REGEXT (5V) output setting will not be able to function.

Description of Functions

3. Power Supply Operation

3.3 VDD55 Regulator settings (Base Current Gain Selection)

KA49517A VDD55 regulator uses an external NPN as its power transistor. The output driving ability of VDD55 depends on the selection of NPN Beta. Output current driving ability (Iout_VDD55) will be set by the selected base current (IB) in KA49517A, multiply by the selected external NPN Beta, β. (Iout_VDD55= IB * β).

Please refer to Table 3.3.1 below to select the required base current for output current generation with the selected NPN β value. Please note that base current adjustment function is only possible when KA49517A is operating in Active mode. In Standby; Low power or Sleep Mode, base current is fixed at around 0.65mA if VDD55 regulator is selected to operate in Low power operation.

NPN Minimum β selection consideration:

User will need to ensure there is sufficient drive needed for the system when selecting Lower Beta NPN.

Please note that load current needed for VDD55 include internal IC current (~10mA) as well as REGEXT output drive (~50mA). It is recommended to maintain at least 60mA drive ability for VDD55 regulator to ensure proper operation under all conditions.

NPN Maximum β selection consideration:

It is recommended to select NPN with β < 150 (@ VCE=10V condition) and β < 300 (@ VCE=80V condition)

For β higher than this recommended level, evaluation with the NPN will need to be performed on bench to ensure stability by changing external BOM from the recommended BOM list. This is to ensure stability of VDD55 output.

It is also necessary to consider package thermal performance of the selected NPN to ensure heat can be dissipated properly and SOA criteria is met using the selected Base current setting and NPN device.

Table 3.3.1 VDD55 Base current output setting

Register	Address [bit]	Base current (IB) setting
R55GAIN [2:0]	0x56 [9:7]	NPN Hfe(Gain) β Adjustment (Set the output Base current drive based on external NPN β specs) 000: IB = 1.01mA (Default) 001: IB = 0.89mA 010: IB = 0.78mA 011: IB = 0.70mA 100: IB = 2.60mA 101: IB = 1.94mA 110: IB = 1.53mA 111: IB = 1.27mA

Description of Functions

3. Power Supply Operation

3.4 VDD55 Regulator settings (β vs Temperature compensation selection)

Beta of NPN BJT tends to have tendency to vary with temperature. It tends to increase at higher temperature and reduce at lower temperature.

With this variation, output current drive of VDD55 regulator will also varies with temperature.

KA49517A comes with β Temperature compensation selection function. This allows user to select the suitable base current that changes with temperature level to cancel out the effect of Beta variation with temperature.

With this function, it will ensure output current drive ability remains relatively constant with respect to the entire range of operating temperature. Selection of this temperature compensation can be set in register address 0x56[6:4]. Based on the selected NPN Beta vs temperature profile, it is possible to select the nearest suitable base current to cancel this variation. For example, if a given NPN beta drops by 30% at low temp and increase by 30% at high temp, it is recommended to set Register R55TC[2:0] at address 0x56[6:4] to be “000” to cancel out this Beta variation. This is to achieve the best possible temperature curve vs base current trend for the selected NPN device.

Refer to below table 3.4.1 for setting details. Evaluation on actual Bench with the selected BJT part is recommended to confirm this selection setting before fixing the design.

Table 3.4.1 VDD55 Base current output setting

Register	Address [bit]	Base current (IB) setting
R55TC [2:0]	0x56 [6:4]	Setting for external NPN beta Temperature variation 000: IB% change = +33% (Lower temperature region) -40% (Higher temperature region) (Default) 001: IB% change = +28% (Lower temperature region) -35% (Higher temperature region) 010: IB% change = +23% (Lower temperature region) -30% (Higher temperature region) 011: IB% change = +18% (Lower temperature region) -25% (Higher temperature region) 100: IB% change = +50% (Lower temperature region) -57% (Higher temperature region) 101: IB% change = +46% (Lower temperature region) -53% (Higher temperature region) 110: IB% change = +42% (Lower temperature region) -49% (Higher temperature region) 111: IB% change = +38% (Lower temperature region) -44% (Higher temperature region) Lower temperature region : -25°C to 25°C Higher temperature region : 25°C to 125°C

Description of Functions

3. Power Supply Operation

3.5 VDD55 Regulator settings (β vs VCE compensation selection)

Beta of NPN BJT tends to have tendency to vary with VCE(supply). It tends to increase at higher VCE(supply) and reduce at lower VCE(supply).

With this variation, output current drive of VDD55 regulator will also varies with VCE(supply).

KA49517A comes with β VCE(supply) compensation selection function. This allows user to select the suitable base current that changes with VCE(supply) level to cancel out the effect of Beta variation with VCE(supply).

With this function, it will ensure output current drive ability remains relatively constant with respect to entire range of VCE(supply) operating range. Selection of this VCE(supply) compensation can be set in register address 0x56[3:1]. Based on the selected NPN Beta vs VCE profile, it is possible to select the nearest suitable base current to cancel this variation. For example, if a given NPN beta rise by 50% from 30V to 85V operation, it is recommended to set Register R55VC[2:0] at address 0x56[3:1] to be “000” to cancel out this Beta variation.

Refer to below table 3.5.1 for setting details.

Evaluation on actual Bench with the selected BJT part is recommended to confirm this selection setting before fixing the design.

Table 3.5.1 VDD55 Base current output setting

Register	Address [bit]	Base current (IB) setting
R55VC[2:0]	0x56 [3:1]	NPN VCE (Supply) coefficient adjustment against external NPN beta supply variation 000: IB% change from 30V to 62.9V = -16.5% (Default) IB% change from 62.9V to 85V = -10.4% 001: IB% change from 30V to 62.9V = -20.7% IB% change from 62.9V to 85V = -13.4% 010: IB% change from 30V to 62.9V = -25.4% IB% change from 62.9V to 85V = -16.9% 011: IB% change from 30V to 62.9V = -30.5% IB% change from 62.9V to 85V = -20.6% 100: IB% change from 30V to 62.9V = -2.7% IB% change from 62.9V to 85V = -2.3% 101: IB% change from 30V to 62.9V = -5.1% IB% change from 62.9V to 85V = -4.3% 110: IB% change from 30V to 62.9V = -10.0% IB% change from 62.9V to 85V = -6.6% 111: IB% change from 30V to 62.9V = -16.5% IB% change from 62.9V to 85V = -10.4%

Description of Functions

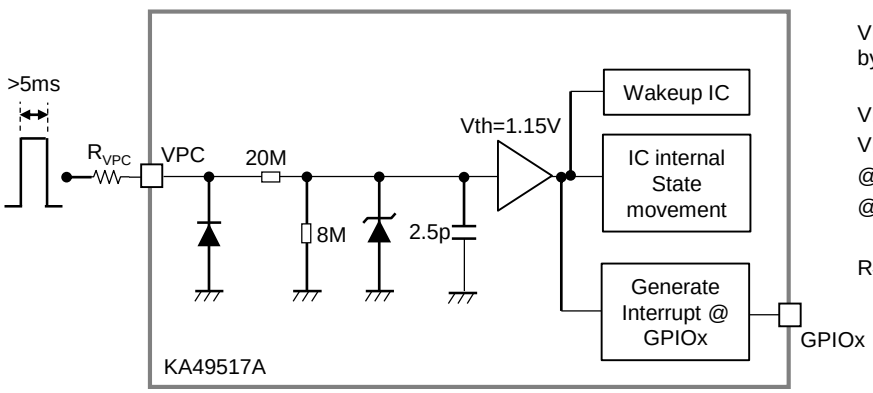
4. VPC and LDM detection Function

4.1 VPC Function description

VPC pin serves as the following functions for KA49517A.
Refer to Table 4.1.1 for the function of VPC and Fig 4.1.1 for VPC simplified design circuit.

Table.4.1.1 Function table for VPC

No.	VPC Pin Function	Remarks	Related Registers
1	Wakeup IC from Shutdown to Active mode of operation	VPC Pin >4V (R_{VPC} =0Ω) with minimum 5ms high pulse width is needed in order to complete startup action. Refer to state machine at section 2.7 for this detail.	ST_ACT Address 0x1C[0] To check Active status register after startup is completed
2	Shift IC state from either Sleep mode or Standby(STB)/ Low Power(LP) mode back to Active mode	VPC Pin >4V (R_{VPC} =0Ω) with minimum 2ms high pulse. Refer to state machine at section 2.7 for this detail.	Address 0x01[7]; 0x01[9]. To enable VPC detection to shift IC internal state from either STB/LP or Sleep mode back to Active Mode respectively. ST_ACT Address 0x1C[0] can be read again to check IC has return to Active mode
3a	Generate interrupt via GPIOx pin with VPC detection	VPC Pin >4V (R_{VPC} =0Ω) to signify Charger plug in. It can be used to wakeup MCU in STB. Interrupt need to be set by register to GPIO pin. Refer to section 7.5 for interrupt details.	Refer to table 7.5.1 for interrupt setting registers. VPC detection status register can be read from: Address 0x27[14]; VPC_DET_F or address 0x27[9:8] VPC_L_F and VPC_H_F
3b		VPC Pin <0.3V (R_{VPC} =0Ω) to signify Charger plug out info for MCU. Interrupt need to be set by register to GPIO pin. Refer to section 7.5 for interrupt details.	



VPC Threshold (VPCDET) Adjustment by external resistor R_{VPC}

$VPCDET = [(R_{VPC} + 28M) / 8M] \times Vth$
$VPCDET = (0.144u \times R_{VPC}) + 4$
@ R_{VPC} = 0Ω, VPCDET = 4V
@ R_{VPC} = 75MΩ, VPCDET = 14.8V

$R_{VPC} = [(VPCDET/Vth) \times 8M] – 28M$

Fig 4.1.1 VPC simplified circuit

Description of Functions

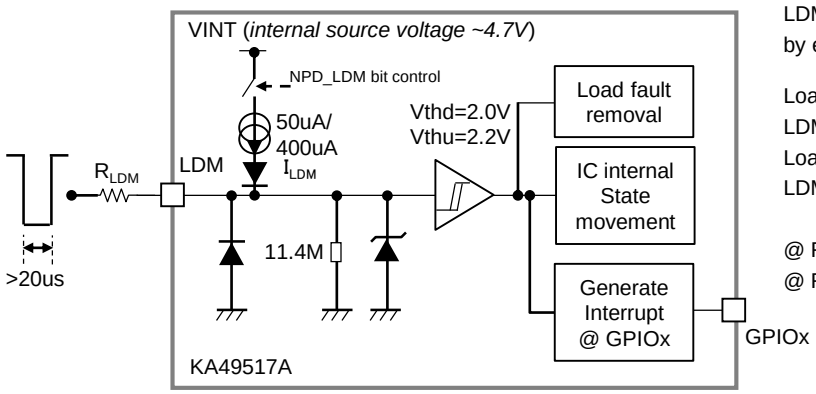
4. VPC and LDM detection Function

4.2 LDM Function description

LDM pin serves as the following functions for KA49517A.
Refer to Table 4.2.1 for the function of VPC and Fig 4.2.1 for LDM simplified design circuit.

Table.4.2.1 Function table for LDM

No.	LDM Pin Function	Remarks	Related Registers
1	Use to check that load is removed prior to turning ON external FETs after a discharge overcurrent or short-circuit current condition	When external FETs are OFF, and Load current of >400uA is drawn at LDM pin causing LDM pin voltage to drop <1.9V, this can serve as an indication for MCU to judge that FETs cannot be turned ON.	LDM detection status register can be read from: Address 0x27[15]; LDM_DET_F or Address 0x27[11:10] LDM_H_F; LDM_L_F
2	Shift IC state from either Sleep mode or Standby(STB)/ Low Power(LP) mode back to Active mode	When Load current of >50uA is drawn at LDM pin causing LDM pin voltage to drop <1.9V, it signifies Load is detected when FET is OFF condition. Refer to state machine at section 2.7 for the details.	Address 0x01[8]; 0x01[10] To enable LDM detection to shift IC internal state from either STB/LP or Sleep mode back to Active mode respectively
3a	Generate interrupt via GPIOx pin with LDM pin detection	When Load of >50uA is drawn at LDM pin causing LDM Pin voltage to drop <1.9V, it signifies Load is detected when FET is OFF condition. It can be used to wakeup MCU in STB. Interrupt need to be set by register to GPIOx pin. Refer to section 7.5 for interrupt details.	Refer to table 7.5.1 for interrupt setting registers. LDM detection status register can be read from Address 0x27[15]; LDM_DET_F or Address 0x27[11:10] LDM_H_F; LDM_L_F
3b		When Load is released from LDM pin causing LDM Pin >2.3V, it signifies Load is released when FET is OFF condition. It can be used to inform MCU that Load is being released so as to decide if FET is to be turned ON or not. Interrupt need to be set by register to GPIOx pin. Refer to section 7.5 for interrupt details.	



LDM Thresholds Adjustment
by external resistor R_{LDM}

Load Detection (LDMDET)
LDMDET = Vthd - (50u x R_{LDM})
Load Release (LDMREL)
LDMREL = Vthu - (50u x R_{LDM})

@ R_{LDM} = 0Ω, LDMDET=2.0V, LDMREL=2.2V
@ R_{LDM} = 30kΩ, LDMDET=0.5V, LDMREL=0.7V

Fig 4.2.1 LDM simplified circuit

Description of Functions

4. VPC and LDM detection Function

4.3 VPC and LDM Function description (Connections and detection)

There are two ways to connect LDM and VPC pins to operate KA49517A.
One way is to control these pins separately as shown in Fig 4.3.1. In this case, there is no need to put external R_{VPC} and R_{LDM} for the system to function. Second way is when charger input pin (VPC) and load detection pin(LDM) are both connect to the same VPACK port as shown in Fig 4.3.2.
In this case, resistor R_{VPC} is recommended to be used. R_{VPC} increases VPC pin detection threshold so that LDM pin internal biasing voltage will not be detected as a Charger detection. R_{LDM} is optional for both type of system connection depending on the required LDM pin detection voltage preferred.
Refer to table 4.3.1 below for recommendation and threshold computation consideration

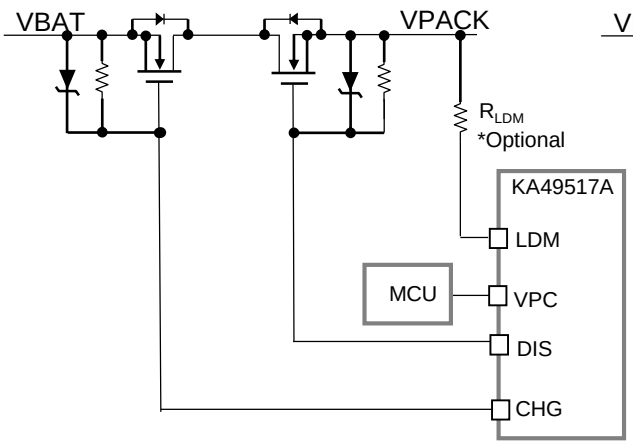


Fig 4.3.1 LDM & VPC separate connection (Case 1)

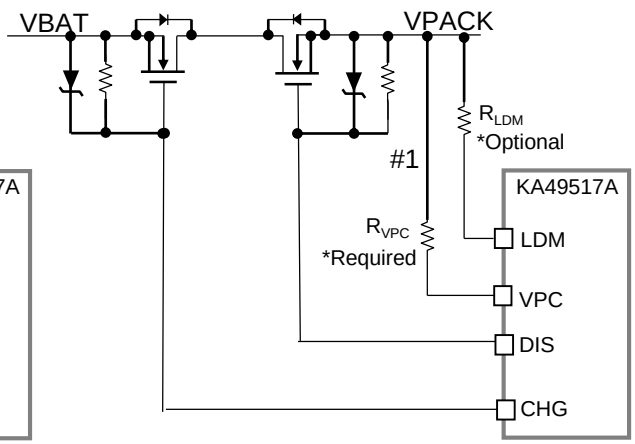


Fig 4.3.2 LDM & VPC common connection (Case 2)

Table 4.3.1 VPC and LDM pin resistors and typical detection threshold

Case No.	R_{LDM} and R_{VPC} Values	VPC Threshold (Charger Detect)	LDM Threshold (Load Detect)	Remark
1	Recommended: R_{VPC} = 0Ω R_{LDM} = 0Ω	2.3V	2.0V (Detect) 2.2V (Release)	Refer to Fig 4.3.1 It is not necessary to connect R_{LDM} and R_{VPC} resistors when both LDM and VPC are controlled separately. However, these can still be inserted depending on desired threshold.
2	Recommended: R_{VPC} = 75MΩ R_{LDM} = 30kΩ	8.5V	0.5V (Detect) 0.7V (Release)	Refer to Fig 4.3.2 R_{VPC} resistor is necessary when both LDM and VPC are shorted to VPACK to sense charger and load. This is to make sure IC will not mis-detect charger plug in condition. R_{LDM} can still be inserted depending on desired LDM threshold. #1: For this case, VPC is always at “high” state when charger is connected or NMOS FET is turned On. IC cannot be moved to Shutdown mode unless charger is removed and NMOS FET is turned Off.

Description of Functions

4. VPC and LDM detection Function

4.4 LDM Function description (Powering ON the function)

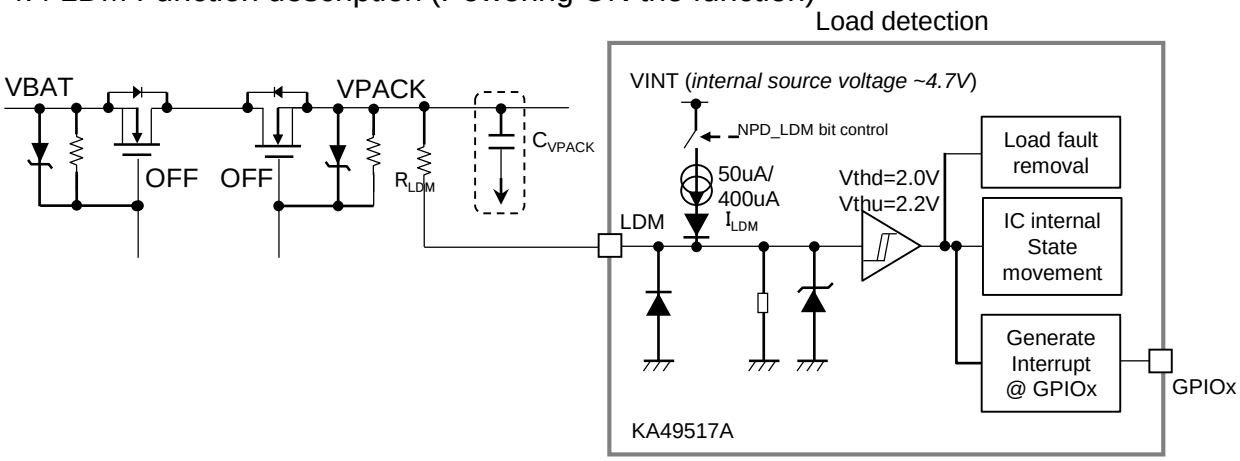


Fig 4.4.1 LDM connection to VPACK (LDM function Power ON sequence)

It is recommended to follow the following flow chart when turning ON and OFF the LDM function

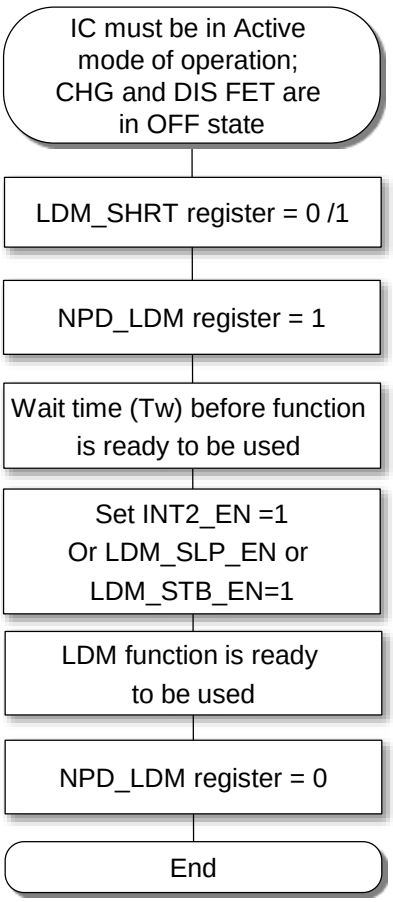


Fig 4.4.2 LDM turn ON sequence

■ IC must be in Active mode of operation and CHG and DIS FET are in OFF state before the LDM function is turned ON.

■ Decide the LDM pin current (I_{LDM}) required for detection.
Set LDM_SHRT register at address 0x20h[0] = 0 or 1.
When LDM_SHRT=0 →50uA load detection current is set. (Default)
When LDM_SHRT=1→400uA load detection current is set.

■ Turn ON LDM function.
Set NPD_LDM register to be "1"(address 0x20h[3]="1')

■ Set wait time after NPD_LDM=1 before the function is ready to be used. Wait time depend on load capacitance on VPACK line as well as the load detection current (I_{LDM}) used.
Wait time is approximately: Tw = (C_{VPACK} * Vthu) / I_{LDM}
Vthu=2.2V typical, I_{LDM}=50uA/400uA typical, C_{VPACK} depend on system capacitance at VPACK line.

■ Set INT2_EN at Address 0x02h[12]= "1" if load detection interrupt signal at GPIO and LDM_H_F (load detection latched flag) is needed to be used. Refer to section 7.4 for the interrupt setting instruction.

■ Set LDM_SLP_EN (address 0x01h[10]=1) or LDM_STB_EN (address 0x01h[8] =1) if using LDM function to move IC state machine from Sleep/STB/LP to active mode.

■ LDM function is ready to be used. For operation usage, please refer to the next 3 pages. After using LDM function, it can be turned OFF(NPD_LDM= 0) when IC is in Active mode.

Description of Functions

4. VPC and LDM detection Function

4.4 LDM Function description (Resistive Loading detection)

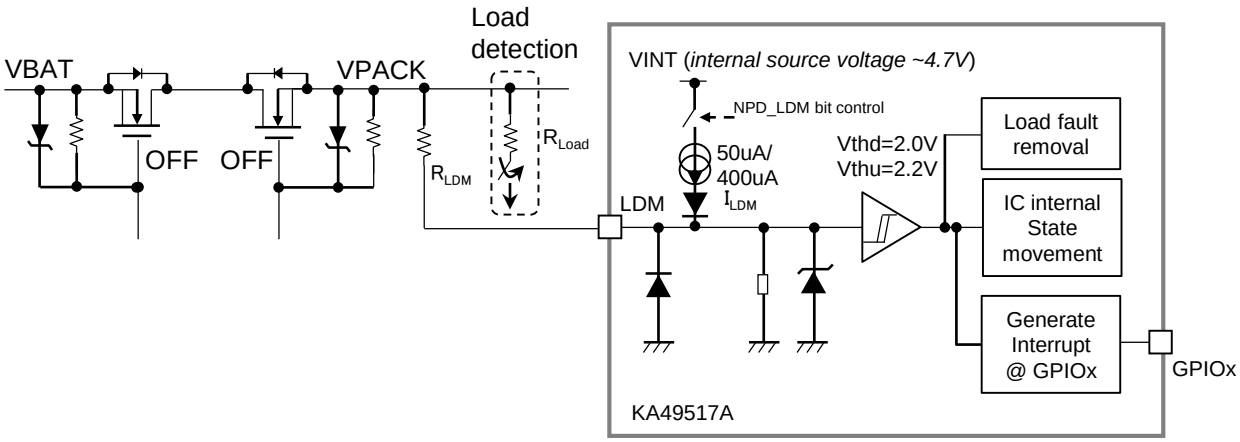


Fig 4.4.3 LDM connection to VPACK (Resistive Load detection)

For normal load detection, 50uA setting can be used after enable LDM by setting NPD_LDM bit = 1. In the case when resistive loading of more than 50uA current is drawn at LDM pin, this will cause LDM pin voltage to be pull down when FET is in OFF state. When LDM pin voltage cross the detection level as stated in Table 4.3.1, KA49517A will detect this condition as presence of Load. IC internal state movement (from STB/LP/Sleep mode to Active mode) can be carried out together with GPIOx pin interruption and Load detection register flag update. Refer to Fig 4.4.2 below for typical waveforms for LDM load detection.

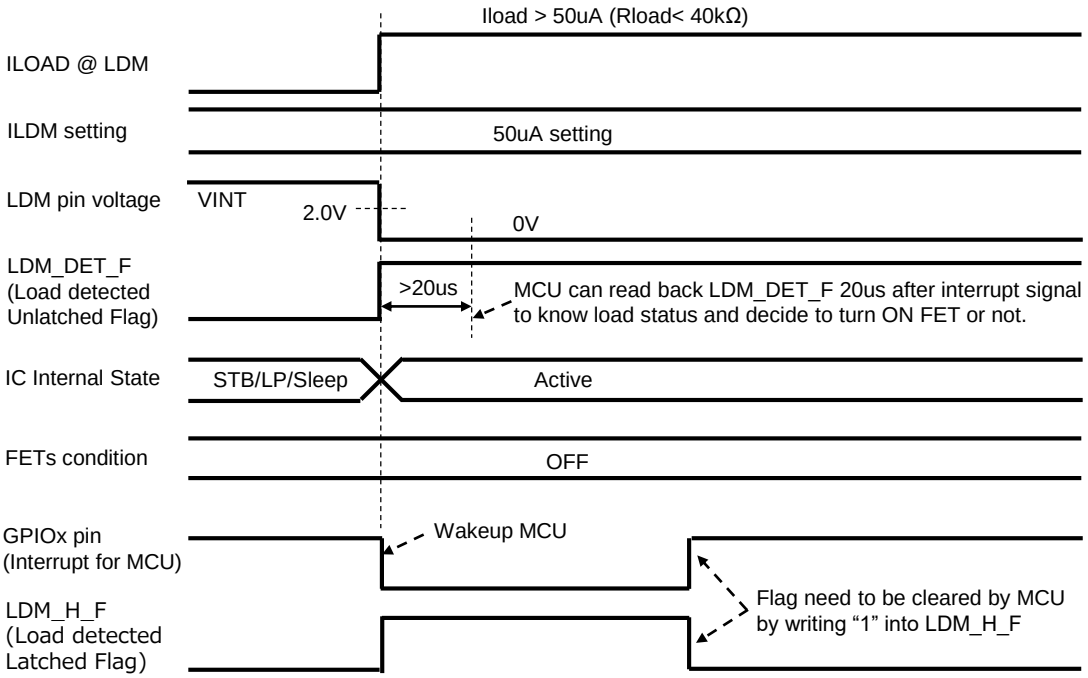


Fig 4.4.4 LDM Resistive load detection waveform example

Description of Functions

4. VPC and LDM detection Function

4.4 LDM Function description (Resistive Load short removal)

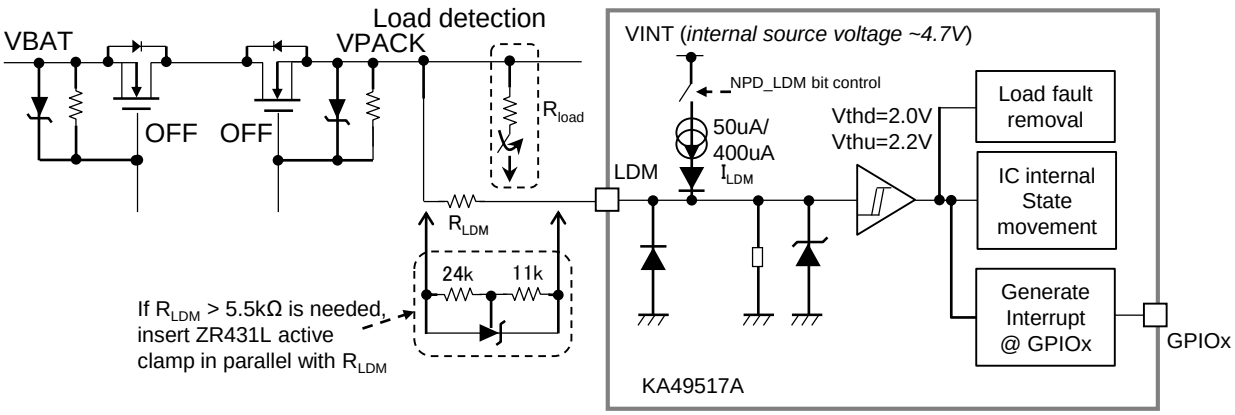


Fig 4.4.5 LDM connection to VPACK (Load Short detection)

For load short detection, MCU can turn on 400uA setting anytime by writing "1" to 0x20[0] bit register, after enable LDM by setting NPD_LDM bit = 1.
If LDM pin voltage is <2.2V for 20us, LDM_DET_F is set high to indicate load short (Rshort<5.5kΩ) condition.
If LDM pin voltage is >2.2V for 20us, LDM_DET_F is set low to indicate load short is removed or Rload>5.5kΩ.

It is possible to lower Rshort detection with external R_{LDM} resistor as shown below:

$$Rshort < \frac{2.2V - 400uA \times RLDM}{400uA} = 5.5k\Omega - RLDM \quad ; \ R_{LDM}<5.5k\Omega$$

If R_{LDM}>5.5kohm is required to lower normal load detection, active clamp is recommended (Fig 4.4.3)

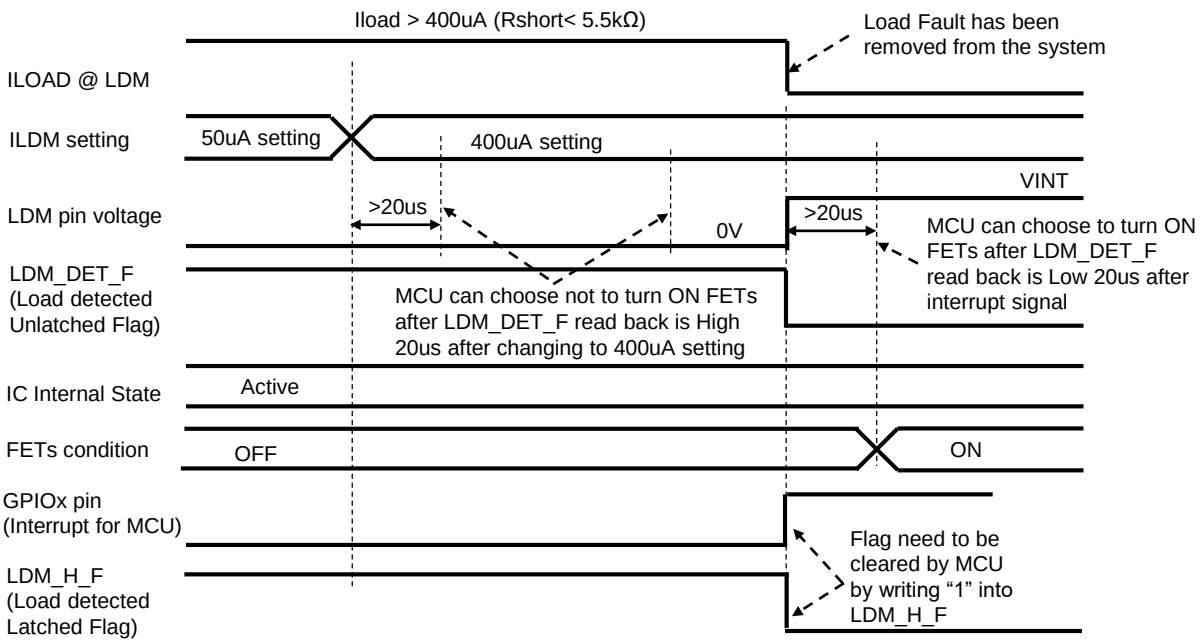


Fig 4.4.6 LDM Load Short detection waveform example

Description of Functions

4. VPC and LDM detection Function

4.4 LDM Function description (Capacitive Loading)

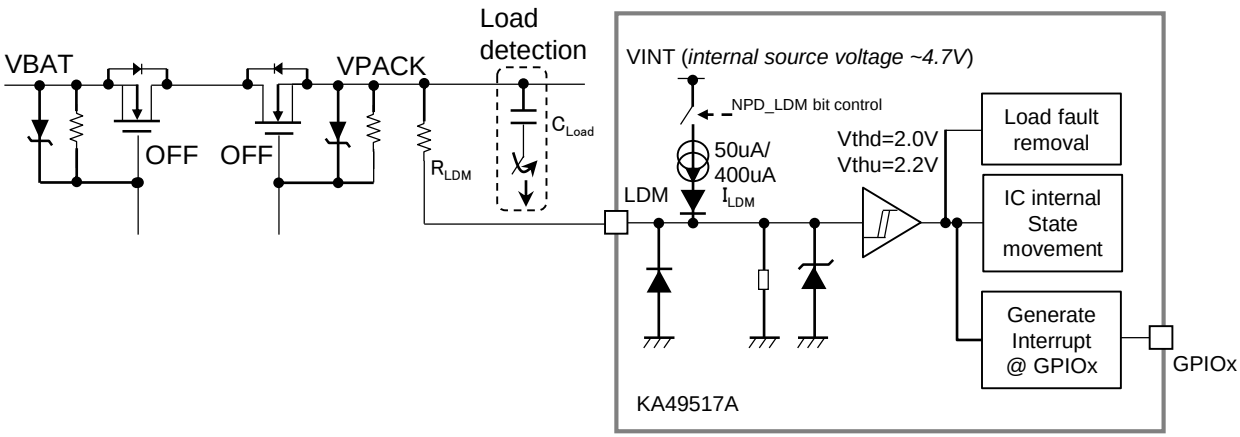


Fig 4.4.7 LDM connection to VPACK (Capacitive Load detection)

In the event when there is capacitive loading, for example when battery pack is plugged on to load system, this capacitive loading will cause a dip in LDM pin voltage. If voltage drop crosses the LDM pin detection threshold set by R_{LDM} value, it is possible to detect this load and when FET is in OFF state. When LDM pin voltage crosses the detection threshold level as stated in Table 4.3.1, KA49517A will detect this condition as presence of Load and LDM_DET_F flag will go from Low to High. IC internal state movement can be carried out as well. Refer to Fig 4.4.6 below for typical waveforms for LDM pin detection.

C_{Load} must be more than 10nF to ensure there is enough response time for proper detection by KA49517A.

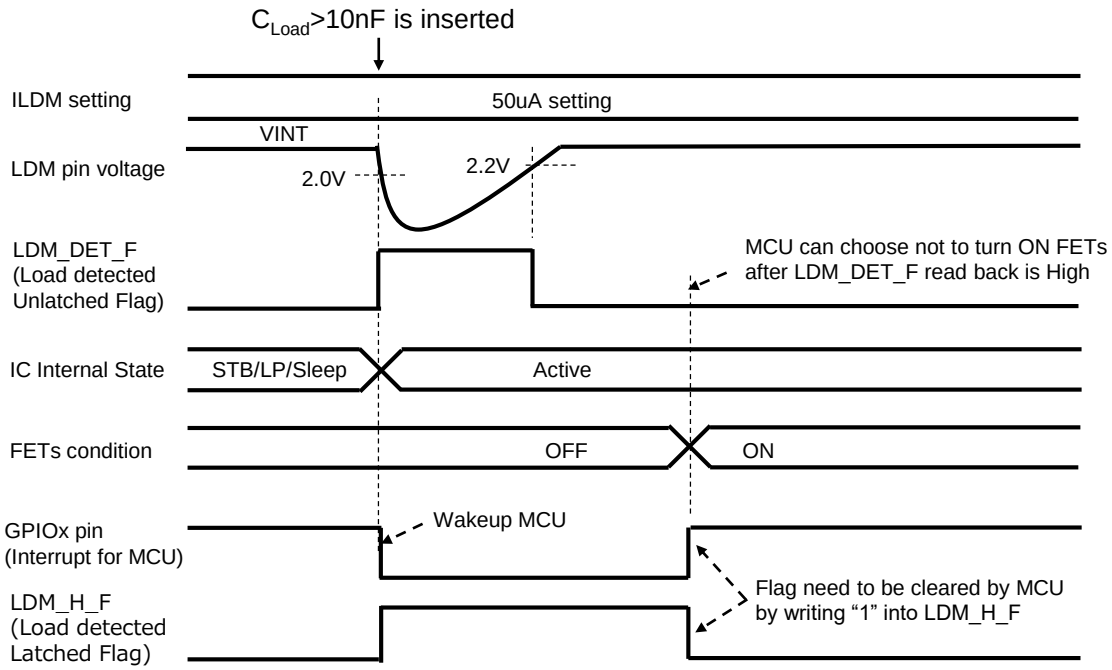


Fig 4.4.8 LDM Capacitive load detection waveform example

Description of Functions

5. CHG / DIS / Charge pump High side FET control

5.1 Description of external high side NMOS FET drive function by CHG/DIS/Charge pump

KA49517A has built-in function to drive external high side NMOS FET switches. The driving circuit consists of CHG pin, DIS pin and Charge pump(CP1-CN1 and CP2-CN2). Generally, each CHG and DIS pin is driving one external NMOS FET separately, and they are connected back to back serially to avoid current leakage through body diode during OFF state. Occasionally for some higher current application, CHG and DIS pins may drive multiple parallel NMOS FET with proper design verification. The NMOS FETs are controlled by connecting CHG and DIS pins to the gate pin of the NMOS FETs as shown, this control can be done in both Active and Standby Mode.

For CHG and DIS pin to drive properly, the Charge pump operation shall be activated first by applying wakeup signal to the VPC pin. Wait time is required for the flying capacitor at pins CP1-CN1 and CP2-CN2 to be fully charged up, which is depending on the capacitance. The Charge pump operating frequency is about 2kHz. The flying capacitance is usually at least 5 to 10 times of NMOS FET gate capacitance, in order for CHG and DIS to have sufficient charge to turn ON the gate instantly. The 680nF flying capacitors shown in Fig.5.1.1 have typical charge up time of around 10ms.

The turning ON of NMOS FETs is controlled by setting register FDRV_CHG_FET (address 0x04[10]) and FDRV_DIS_FET (address 0x04[9]) to “1” respectively. When it is turned ON, the VGS overdrive voltage of NMOS FET is 11V typically (default setting). The VGS overdrive voltage can be set by flag FDRV_LEVEL (address 0x04[4:2]). Higher overdrive voltage reduces ON resistance which can minimize NMOS FET power dissipation. Lower overdrive voltage can be used for NMOS FET with lower VGS threshold.

The turning OFF of NMOS FETs is controlled by setting the flags FDRV_CHG_FET (address 0x04[10]) and FDRV_DIS_FET (address 0x04[9]) to “0” respectively. It can also be turned OFF through setting FETOFF pin to “H”. CHG pin is pulled down to VBAT and DIS pin is pulled down to VPACK by dedicated internal low impedance switches so that NMOS FETs can be turned off fast. Therefore, the external routing paths for both VBAT pin and VPACK pin must have a low impedance.

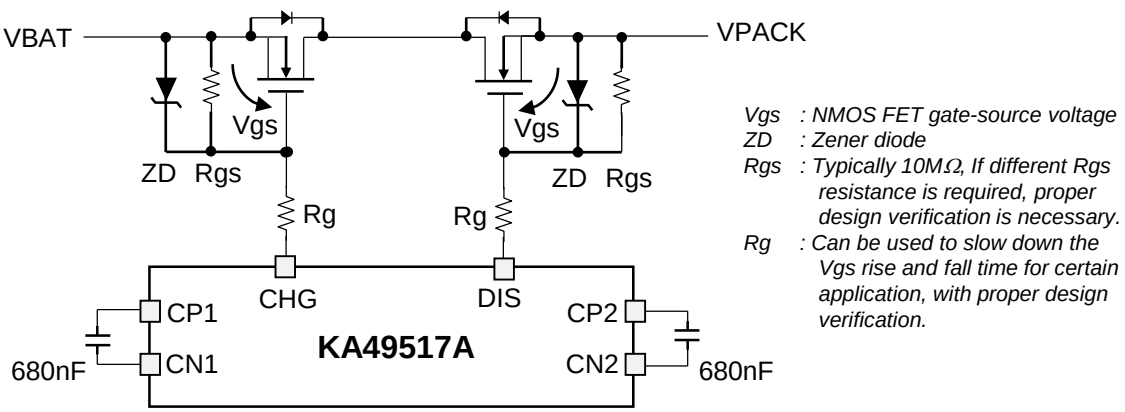


Fig.5.1.1 CHG / DIS / Charge pump driving FET circuit

Description of Functions

5. CHG / DIS / Charge pump High side FET control

5.1 Description of external high side NMOS FET drive function by CHG/DIS/Charge pump

When NMOS FET gate capacitance shown in Fig.5.1.1 is 20nF, the typical rise time of the control signal is around 20us (measured when Vgs rises from 0V to 4V) and the typical fall time is 20us (measured till Vgs drops from 90% to 10% of original setting).

For general application, CHG/DIS can instantly turn ON the NMOS FET gate (when Vgs rises from 0V to 4V) within the first cycle of enable pulse signal (based on default Charge pump operating at 2kHz). Some application that have big or multiple NMOS FET (if typical total gate capacitance more than 80nF), more than one cycle of pulse signal is required, which will cause longer turn ON time.

By setting FDRV_SEL_CLK (address 0x04[11]) to “1”, the first enable pulse signal can be extended from 500us to 2ms (Charge pump frequency becomes 500Hz) which is suitable to drive big gate capacitance. This extended pulse feature is applicable for gate capacitance up to about 600nF. Please note this function of FDRV_SEL_CLK, should be turned on first before the FET on command is sent to ensure the first FET on pulse is correct. After the NMOS FET turn ON, it is recommended to set back FDRV_SEL_CLK back to “0” for Charge pump to operate at normal 2kHz frequency.

During Standby or Low Power Mode, register FDRV_STBY(address 0x04[8]) can be set to “1” prior to entering Standby or Low power Mode. The Charge pump circuit operates in power reduction mode with lower frequency and charge timing, while maintaining the FET ON/OFF state. When user wants to change FET state, user should first change register FDRV_STBY to “0” first before changing FDRV_CHG_FET and FDRV_DIS_FET setting.

Under ALARM condition, the control of NMOS FETs could be set to response to the ALARM condition. Refer to Chapter 11 Monitoring and Protection for more information.

Description of Functions

5. CHG / DIS / Charge pump High side FET control

5.1 CHG/DIS/Charge pump FET Control Registers

Table.5.2.1 shows the related registers for the control of CHG / DIS / Charge pump..

Table.5.2.1 CHG/DIS/Charge pump FET Control Registers

Register	Address [bit]	Function
FDRV_CHG_FET	0x04[10]	External CHGFET control 1: FET ON 0: FET OFF (Default)
FDRV_DIS_FET	0x04[9]	External DISFET control 1: FET ON 0: FET OFF (Default)
FDRV_STBY	0x04[8]	FET driver's standby mode switch 1: power reduction mode (Standby) 0: Normal (Default)
FDRV_LEVEL [2:0]	0x04[4:2]	Setting of external NMOS FET V_{GS} overdrive voltage (typical value). 111: V_{GS} overdrive = 4V 110: V_{GS} overdrive = 5V 101: V_{GS} overdrive = 6V 100: V_{GS} overdrive = 7V 011: V_{GS} overdrive = 8V 010: V_{GS} overdrive = 9V 001: V_{GS} overdrive = 10V 000: V_{GS} overdrive = 11V (Default)
FDRV_SEL_CLK	0x04[11]	Charge Pump clock frequency adjustment 1: FDRV clock is 500Hz 0: FDRV clock is 2kHz (Default)

Description of Functions

6. General Purpose High Voltage Output (GPOH1 and GPOH2)

6.1 Description of General-Purpose High Voltage Output

KA49517A has built-in with two high voltage open drain GPOH pins (GPOH1/GPOH2). These two pins can sustain voltage up to VBAT level. When used, pull up resistors of more than 100kΩ are needed.

These pins could be used to drive high side PMOS FET and set to response to ALARM condition. Refer to Chapter 11 for Monitoring and Protection.

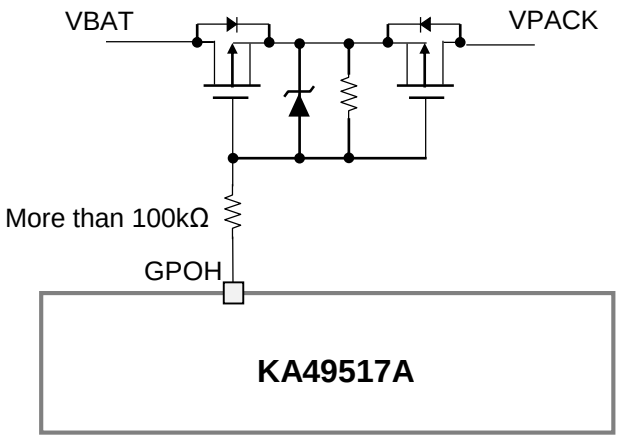


Fig.6.1.1 Circuit example using GPOH1/2

Description of Functions

6. General Purpose High Voltage Output (GPOH1 and GPOH2)

6.2 Description of GPOH control Registers

Table.6.2.1 shows the registers that control GPOH pins.

Table.6.2.1 GPOH Control Registers

Register	Address [bit]	Function
GPOH1_EN	0x10 [0]	GPOH1 output data 1: Low output 0: Hi-Z (Default)
GPOH2_EN	0x10 [1]	GPOH2 output data 1: Low output 0: Hi-Z (Default)
GPOH_FET	0x10 [2]	FET control settings of GPOH Pin 1: FET control used Control of FET driver ON/OFF by FDRV_CTL(0x04). 0: FET control not in use (Default)
GPOH1_ALM_ST	0x10 [4]	If using FET at GPOH1 pin, set GPOH1 pin data to output during ALARM. Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 . 1: Low output 0: Hi-Z (Default)
GPOH2_ALM_ST	0x10 [5]	If using FET at GPOH2 pin, to set GPOH2 pin data to output during ALARM. Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 . 1: Low output 0: Hi-Z (Default)
GPOH1_ST	0x1C [8]	GPOH1 state 1: Output “L” 0: Hi-Z
GPOH2_ST	0x1C [9]	GPOH2 state 1: Output “L” 0: Hi-Z

Description of Functions

6. General Purpose High Voltage Output (GPOH1 and GPOH2)

6.3 Operation at the time of ALARM occurrence

KA49517A is possible to control the GPOH1 / 2 pins in accordance with the state of the ALARM.
This function can be activated by writing GPOH_FET register at address 0x10, bit 2 to be =“1”.
Refer to table 6.3.1 below for the control operation when GPOH_FET is set to “1” condition.
Refer to Chapter 11 Monitoring and Protection for details of Alarm event operation.

Table.6.3.1 GPOH Pins control at the time of the alarm (when flag GPOH_FET = “1”)

	Detecting abnormality	GPOH1	GPOH2
Abnormal	OV/UV OCC/OCD SCD	Control flag GPOH1_ALM_ST (address 0x10[4])	Control flag GPOH2_ALM_ST (address 0x10[5])
Normal	-	Control flag GPOH1_EN (address 0x10[0])	Control flag GPOH2_EN (address 0x10[1])

6.4 GPOH state flag

The status of GPOH1/2 can be checked by a state flag.

Table.6.4.1 GPOH Pin state flag

GPOH	State Flag
GPOH1	GPOH1_ST flag (address 0x1C[8])
GPOH2	GPOH2_ST flag (address 0x1C[9])

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.1 Description of General-Purpose Input Output

KA49517A has built-in with three low voltage GPIO pins (GPIO1~3) .
The power bias of GPIO is supplied from CVDD.
Possible operating mode of GPIO can be selected based on GPIOnSEL register at address 0D[11:8]; 0E[11:8]; 0F[11:8], for GPIO1, 2 and 3 respectively.
Refer table below for possible configuration for each pin that can be output from GPIO pins.

Table.7.1.1 GPIO Pins Configuration

Pin	GPIOnSEL	Functions
GPIO1 GPIO2 GPIO3	0000	GPIO (General)
	0001	GPOH1 Data Output
	0010	GPOH2 Data Output
	0011	ADIRQ1 Output
	0100	ADIRQ2 Output
	0101	High Speed Oscillator Clock Divided Output
	0110	Low Speed Oscillator
	0111	Active mode state Output
	1000	Standby mode state Output
	1001	Low Power mode state Output
	1010	FUSE FET Output (For Chemical Fuse burn output drive)
	1011	Alarm2 Output
	1101	All Possible MCU Interrupt “OR” Output *See page 53-57 for Interrupt functions

Note:
When GPIO pin is configured as output, it shall not be set with pull down resistor. (ie. flag GPIO[n]_PD = “1”)
When GPIO pin is configured as Analog Input, flag GPIO[n]_IE shall be set to “0”.
By outputting GPOH data to GPIO1/GPIO2, it can be used to drive a low-side NMOS FET (responding to the ALARM condition).

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.2 GPIO Pins Input and Output Configuration

Each GPIO Pin can be set as the various configuration by control register.

Table.7.2.1 GPIO pin setting Register

Flag	Pin Configuration	Description
GPIO*_NOE	Output Enable	1: Disabled (Default) 0: Enabled
GPIO*_IE	Input Enable	1: Enabled 0: Disable (Default)
GPIO*_OD	Output Configuration	1: Nch Open Drain 0: Push Pull (Default)
GPIO*_PD	Pull-Down Register	1: Pull-down resistor ON 0: Pull-down resistor OFF(Default)
ST_GPIO*	Input Data	State of GPIOn pin input (It is effective only at GPIOn_IE=1). 1: Input level “H” 0: Input level “L” (Default)
GPIO*_OUT	Output Data	GPIOn_OD = 0 (push pull) 1: Output “H” 0: Output “L” (Default)
GPIO*_CHDRV	Output Drivability	1: 4mA 0: 2mA (Default)

Note:
When GPIOn pin is configured as GPOH1/2 , GPIOn_OD should be set to “0”.
It is required to change other registers accordingly when setting GPIO[n]SEL.
e.g. GPIO3 is set to ALARM2,
User shall set:
GPIO3SEL[3:0] : 1011 (ALARM 2)
GPIO3_NOE: 0 (Output enable)
GPIO3_IE: 0 (Input disable)

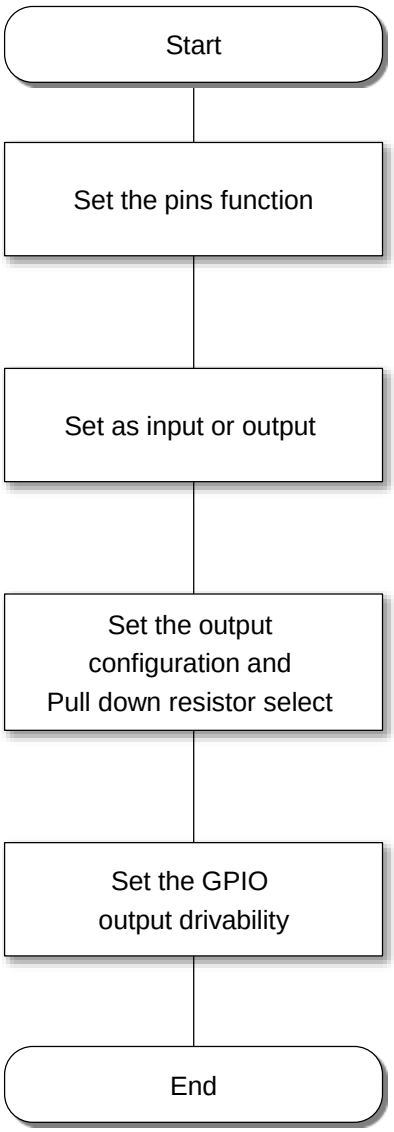
When GPIO pin is configured as output , GPIO[n]_PD shall not be set to “1” at the same time.
When GPIO pin is configured as Analog Input , GPIO[n]_IE shall not be set to “1” at the same time.

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.3 GPIO Pins Setup Example

For example, GPIO Pins use the following settings
GPIO1 : Analog Input
GPIO2 : Output Configuration Push Pull, output Drivability 4mA
GPIO3 : Low Speed Oscillator Clock Divided Output,
Clock Divider 4kHz with a description of each step is shown below.



■ Set the Pins function
Set the GPIO*SEL[3:0] flag of GPIOSEL register.
GPIO3SEL[3:0] =0110, GPIO2SEL[3:0] =0000, GPIO1SEL[3:0] =0000
OSCL_DIV flag(address 11, bit 8) set to “1” to 4 kHz.

■ Set the input or output
Set GPIO*_NOE flag(address 0x0E[1] and 0x0F[1])
set to ”0” to GPIO2 & 3 output.
Set the GPIO*_IE flag(address 0x0D[0])
set to ”0” to GPIO1 as analog input.
Set GPIO*_NOE flag(address 0x0D[1])
set to ”1” to GPIO1 as analog input.

■ Set the Output configuration and Pull-down resistor select
Set the GPIO*_OD flag(address 0x0E[3], 0x0F[3])
set to ”0” at GPIO2 and 3 to push-pull.
Set the GPIO*_PD flag(address 0x0E[2], 0x0F[2])
set to ”0” at GPIO2 and 3 to pull down resistor OFF.

■ Set the GPIO Output drivability
Set the GPIO*_CHDRV flag(address 0x0E[5]) set to ”1” to GPIO2 output drivability to 4mA.

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

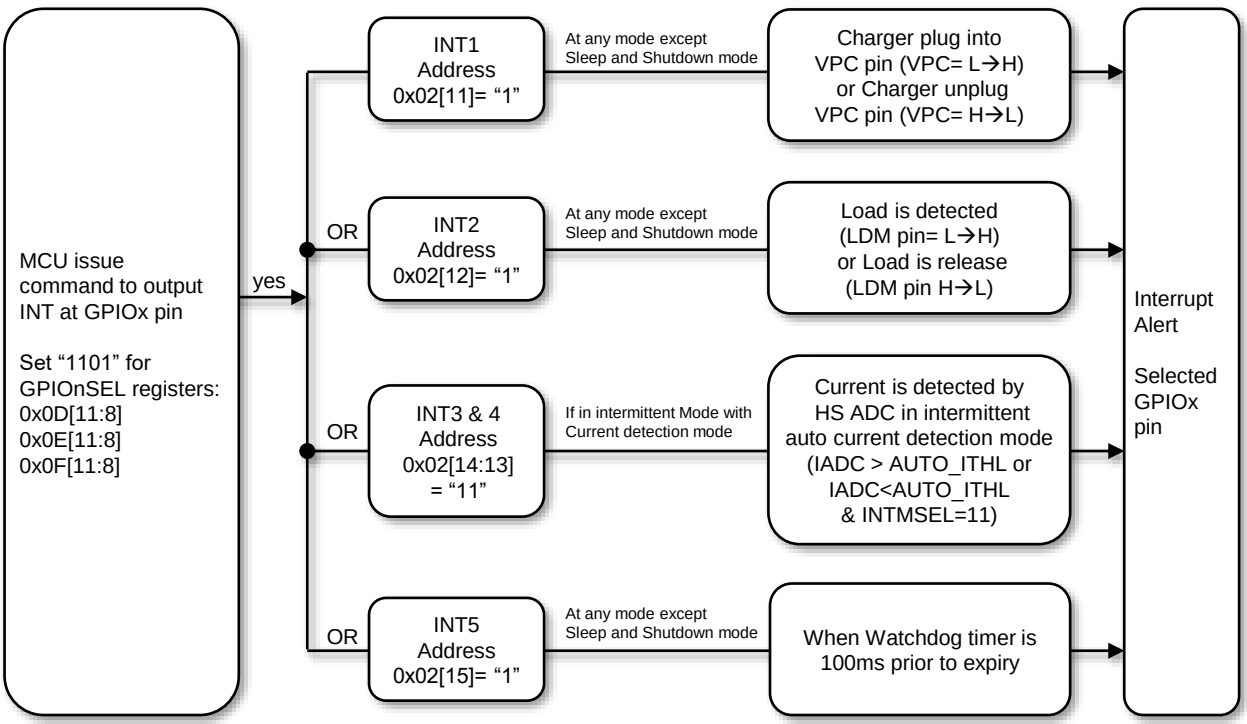
7.4 Types and Method of Interrupt

There are 5 types of interrupt (INT) from KA49517A to MCU during normal operation.
The 5 events are Charger Detection, Load Detection, Current Detection, Current release as well as Watchdog timer pre expiry (as shown in Fig.7.4.1)

In order to receive the INT signal from KA49517A to MCU, user will need to issue an interrupt command to any of the 3 GPIO pins. This can be set by address 0x0D[11:8], 0x0E[11:8] and 0x0F[11:8] to “1101”
Each of the five INT function can be enabled individually by control bit at address 0x02[15 :11]

Refer to Fig.7.4.1 for the event that trigger interrupt control method. Detail information about each interrupt usage is explained in the subsequent pages.

Fig.7.4.1 Possible events that trigger interrupt to MCU



Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.4 Types and Method of Interrupt

Interrupt event 1 (INT1): Charger Detection

In the event INT is output to GPIOx pin and INT1 function is enabled, MCU can be notified via interrupt signal when Charger is plugged into the system through VPC pin going from L→H.
IC will detect this rising edge at VPC pin as charger plug in condition and issue a ”H” to “L” interrupt through the assigned GPIO pin. VPC_H_F flag (address 0x27[9]) will be set to “1”.

During the event that charger is plugged out, IC will detect the falling edge at VPC pin and issue another “H” to “L” interrupt through the assigned GPIO pin. VPC_L_F flag (address 0x27[8]) will be set to “1”.

MCU can make use of this interrupt signal to wake itself as a form of power saving.
Refer to Fig.7.4.1 for waveform example.

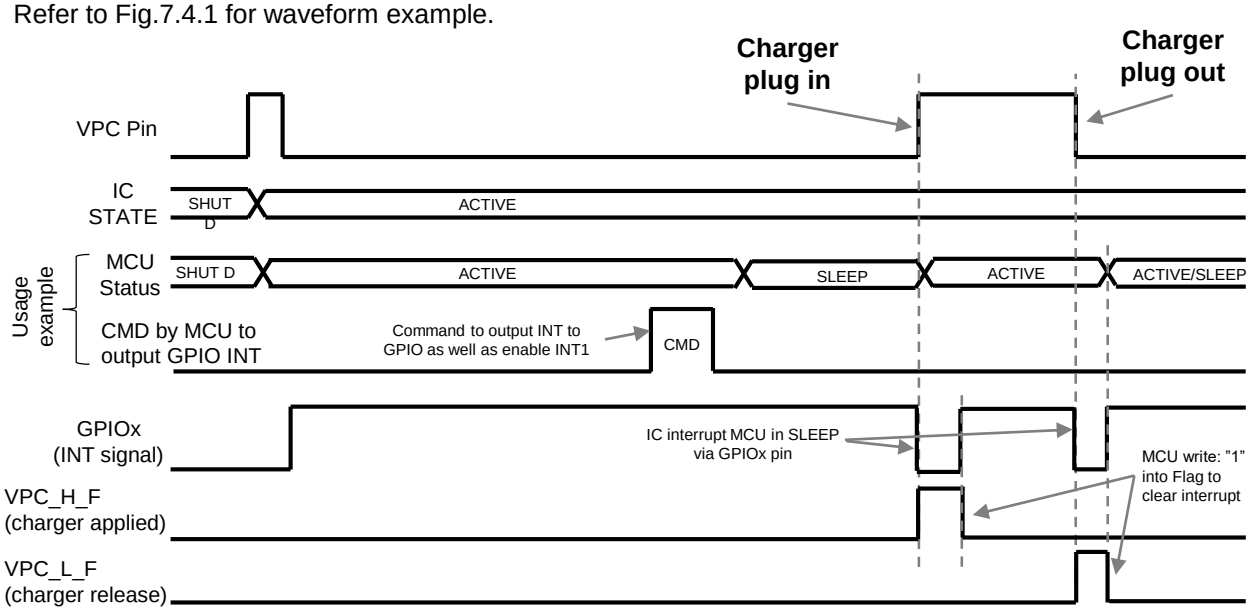


Fig.7.4.1 Waveforms of interrupt function(Eg: Charger Detector input)

VPC_H_F and VPC_L_F as well as INT signal at GPIO pin need to be cleared by MCU before it can be released. MCU need to write a bit “1” into VPC_H_F or VPC_L_F flag. After receiving the clear signal from MCU, KA49517A will pull this flag Low and INT signal at GPIO pin will also return High after a delay time of 12us. Refer to clearing waveform shown in Fig,7.4.2

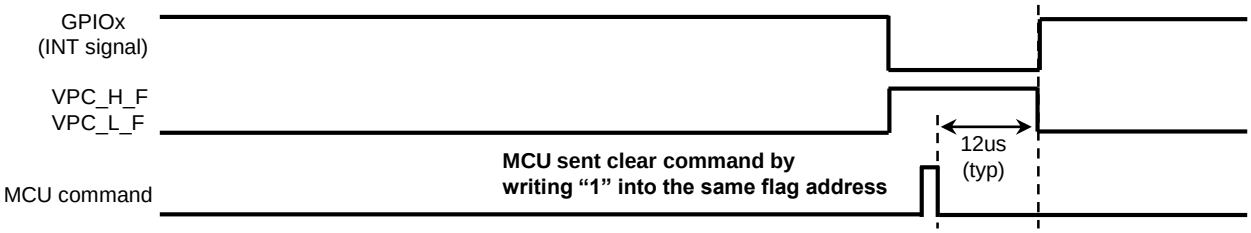


Fig.7.4.2 Waveforms of interrupt flag clearance

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.4 Types and Method of Interrupt

Interrupt event 2 (INT2): Load Detection

In the event INT is output to GPIOx pin and INT2 function is enabled, MCU can be notified via interrupt signal when Load is detected by LDM pin H□L during CHG and DIS FET off condition.
IC will detect this falling edge at LDM pin condition and issue a ”H” to “L” interrupt through the assigned GPIO pin. Concurrently KA49517A will set the LDM_H_F flag (address 0x27[11]) to “1”.

During the event that Load is released, IC will detect the rising edge at LDM pin and issue another “H” to “L” interrupt through the assigned GPIO pin. Concurrently, KA49517A will set the LDM_L_F flag (address 0x27[10]) to “1”

MCU can make use of this interrupt signal to wake itself as a form of power saving.
Refer to Fig.7.4.3 for waveform example

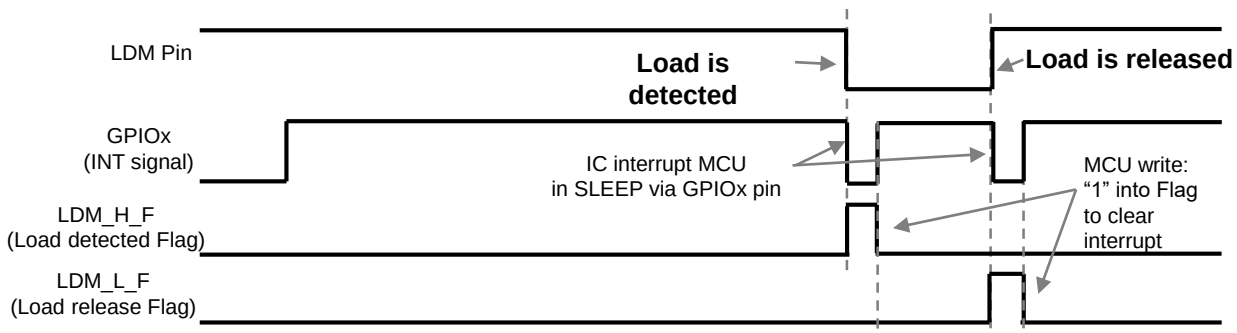


Fig.7.4.3 Waveforms of MCU SLEEP Alert function (Load Detector input)

LDM_H_F and LDM_L_F and INT pin signal at GPIO pin need to be cleared by MCU before it can be released. MCU write a bit “1” into LDM_H_F or LDM_L_F flags. After receiving the clear signal from MCU, KA49517A will pull this flags Low and INT pin signal at GPIO pin will also be return High after a delay time of 12us. Refer to clearing waveform shown in Fig.7.4.4

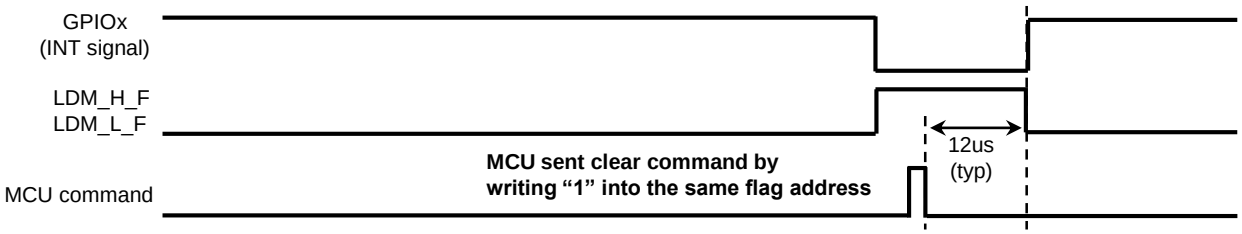


Fig.7.4.4 Waveforms of interrupt flag clearance

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.4 Types and Method of Interrupt

Interrupt event 3 & 4 (INT3; INT4): Auto Current Detection

In the event INT is output to GPIOx pin and INT3 function is enabled, MCU can be notified via interrupt signal when the IC detects that current is lower than the set threshold current (IADC < ITHL). IC will then issue a “H” to “L” interrupt through the assigned GPIO pin. There is no flag signal for this detection.

In the event INT is output to GPIOx pin and INT4 function is enabled, MCU can be notified via interrupt signal when high current through the battery cells is detected by the internal High-Speed current ADC measurement. (IADC > ITHL). IC will then issue a “H” to “L” interrupt through the assigned GPIO pin. Concurrently KA49517A will set the CUR_H_F flag (address 0x27[12]) to “1”.

*This function is only available when IC is operating in Low power/Standby intermittent mode of operation with auto current detection mode enable. (Refer to mode of operation page 29 for this operation state machine)
MCU can make use of this interrupt signal to wake itself as a form of power saving.
Refer to Fig.7.4.5 for waveform example

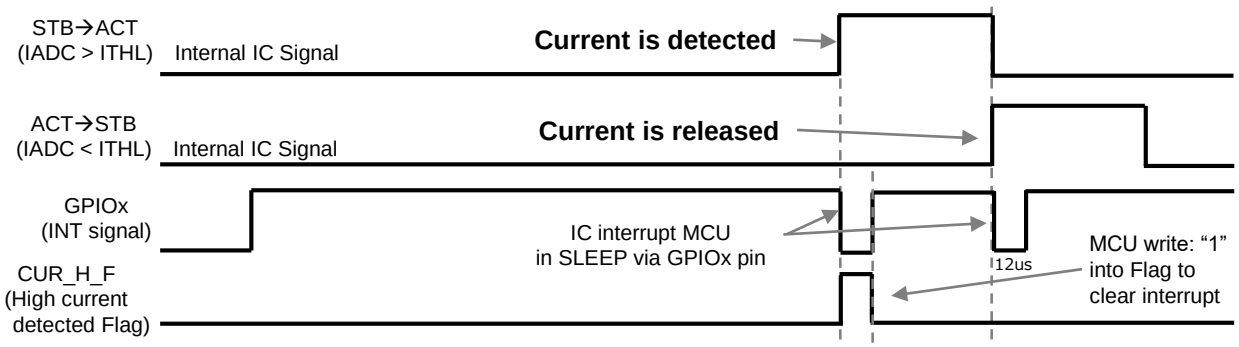


Fig.7.4.5 Waveforms of Auto Current Detection mode

CUR_H_F and INT signal at GPIO pin for current detection event need to be cleared by MCU before it can be released. MCU need to write a bit “1” into CUR_H_F flag. After receiving the clear signal from MCU, KA49517A will pull this flag Low and INT pin signal at GPIO will also be return High after a delay time of 12us. Refer to clearing waveform shown in Fig.7.4.6.

Please note that current release event has only interrupt and no flag. The interrupt for current release is automatically cleared after 12us from interrupt event

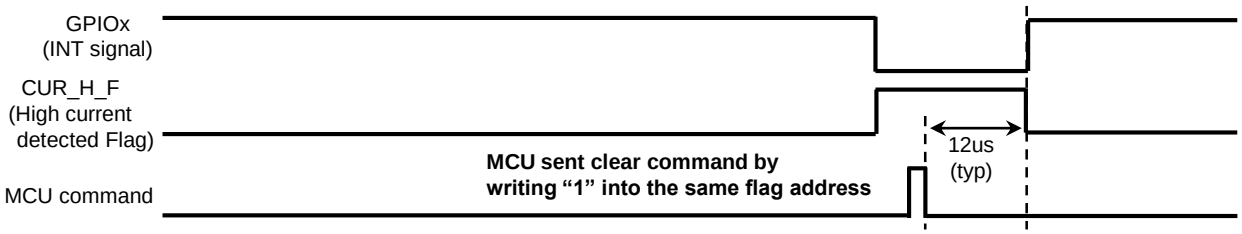


Fig.7.4.6 Waveforms of interrupt flag clearance

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.4 Types and Method of Interrupt

Interrupt event 5 (INT5): WDT prior expiry Detection

In the event INT signal is output to GPIOx pin and INT5 function is enabled, MCU can be notified via interrupt signal when Watch Dog Timer (WDT) is going to be expired. KA49517A will issue an interrupt at the assigned GPIO pin, 100ms prior to WDT expiry. This serves as a warning to MCU in case WDT protection is turned ON and no communication has been done from MCU to KA49517A.

MCU can make use of this interrupt signal to check if MCU communication is working correctly or not before the event of WDT expiry. Refer to Fig.7.4.7 for waveform example

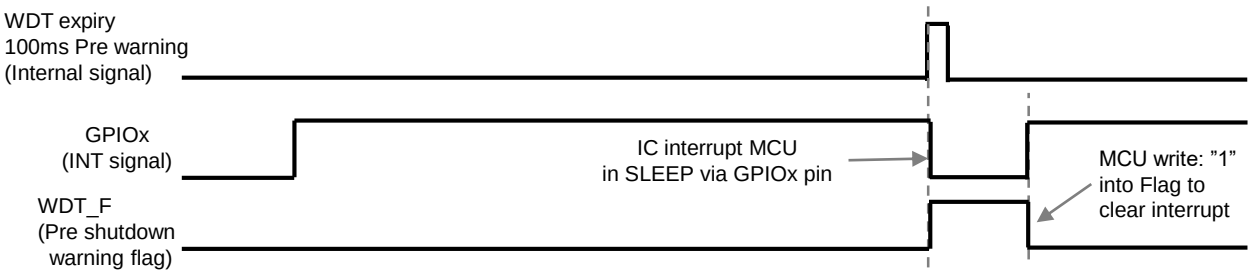


Fig.7.4.7 Waveforms of WDT prior expiry detection mode

WDT_F and INT signal at GPIO pin need to be cleared by MCU before it can be released. MCU need to write a bit "1" into WDT_F flag. After receiving the clear signal from MCU, KA49517A will pull this flag Low and INT pin signal at GPIO will also be return High after a delay time of 12us. Refer to clearing waveform shown in Fig,7.4.8

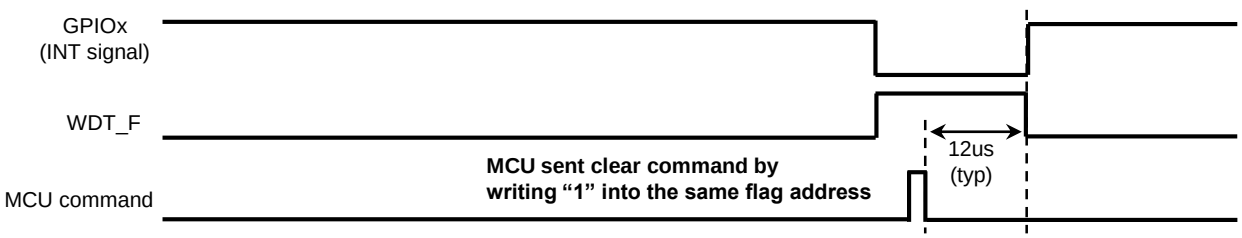


Fig.7.4.8 Waveforms of interrupt flag clearance

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.5 Interrupt related Registers

Table.7.5.1 shows the registers that control GPIO.

Table.7.5.1 Interrupt Control Registers

Register	Address [bit]	Function
GPIO1SEL[3:0]	0x0D [11:8]	To output the selected interrupt signal to GPIO1 pin Refer to Table.7.1.1 GPIO Pins Configuration
GPIO2SEL[3:0]	0x0E [11:8]	To output the selected interrupt signal to GPIO2 pin Refer to Table.7.1.1 GPIO Pins Configuration
GPIO3SEL[3:0]	0x0F [11:8]	To output the selected interrupt signal to GPIO3 pin Refer to Table.7.1.1 GPIO Pins Configuration
INT1_EN	0x02 [11]	To enable VPC detection interrupt at GPIOx pin 1: Enable VPC_L_F & VPC_H_F flag as well as GPIO pin interrupt to be triggered when VPC is falling/rising 0: No status indication (Default)
INT2_EN	0x02 [12]	To enable LDM detection interrupt at GPIOx pin 1: Enable LDM_L_F & LDM_H_F flag as well as GPIO pin interrupt to be triggered when LDM is falling/rising 0: No status indication (Default)
INT3_EN	0x02 [13]	To enable Load release for auto current detection mode at GPIOx pin 1: Enable GPIO pin interrupt to be triggered when Sense current has reduced; IADC<ITHL 0: No status indication (Default)
INT4_EN	0x02 [14]	To enable Load detection for auto current detection mode at GPIOx pin 1: Enable CUR_H_F flag as well as GPIO pin interrupt to be triggered when Sense current has increase; IADC>ITHL 0: No status indication (Default)
INT5_EN	0x02 [15]	To enable Pre watch dog timer expiry warning at GPIOx pin 1: Enable WDT_F flag as well as GPIO pin interrupt to be triggered when WDT is 100ms before expiry time 0: No status indication (Default)
VPC_L_F	0x27 [8]	Latched type output flag for VPC H→ L event (Charger release detection) 1: Event is detected 0: Event is not detected (Default) It is cleared by writing "1".
VPC_H_F	0x27 [9]	Latched type output flag for VPC L→ H event (Charger input detection) 1: Event is detected 0: Event is not detected (Default) It is cleared by writing "1".

Description of Functions

7. General Purpose Input Output (GPIO1, GPIO2 and GPIO3)

7.5 Interrupt related Registers

Table.7.5.1 shows the registers that control GPIO.

Table.7.5.1 Interrupt Control Registers

Register	Address [bit]	Function
LDM_L_F	0x27 [10]	Latched type output flag for LDM L→ H event (Load release detection) 1: Event is detected 0: Event is not detected (Default) It is cleared by writing “1”.
LDM_H_F	0x27 [11]	Latched type output flag for LDM H→ L event (Load input detection) 1: Event is detected (AFE return to Active mode) 0: Event is not detected (Default) It is cleared by writing “1”.
CUR_H_F	0x27 [12]	Latched type output flag for current detection event (Current detection: IADC>ITHL) 1: Event is detected 0: Event is not detected (Default) It is cleared by writing "1".
WDT_F	0x27 [13]	Latched type output flag for Watch Dog Timer pre expiry warning (100ms prior to WDT expiry) 1: WDT will be timeout in 100ms 0: WDT timeout is not detected (Default) It is cleared by writing "1".
VPC_DET_F	0x27 [14]	Non-Latch type output flag for VPC detection Status of VPC 1: VPC pin is "H" 0: VPC pin is "L"
LDM_DET_F	0x27 [15]	Non-Latch type output flag for LDM detection Status of Load 1: Load is detected 0: No load
AUTO_ITHL [14:0]	0x55 [14:0]	15 bit to set detection current level to enter Low power auto mode (compare by IADC_fast) Use only when INTMSEL[1:0] = 11 Value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V Voltage/step = 0.005493mV

Description of Functions

8. Cell Balance

8.1 Description of Cell Balance

KA49517A has Cell balance function. This function can be turned ON during Active Mode, and Standby Mode, and can be done by using an external MOSFET or the built-in MOSFET.

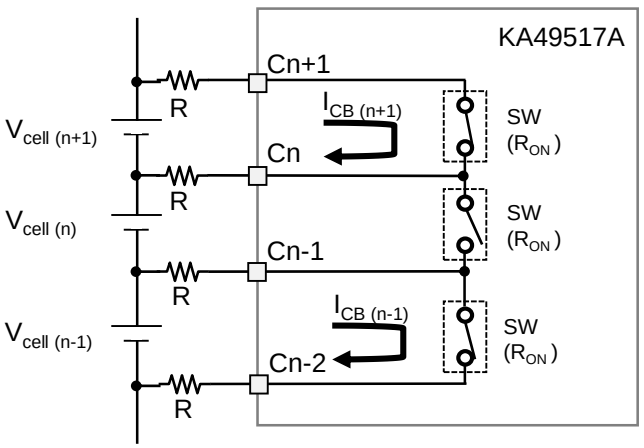
Please note the following points.

- When using cell balance, user shall set 5.5V regulator to normal operation.(See Chapter 3: 5.5V regulator)
- Adjacent cell ($V_{cell\ (n+1)}$ and $V_{cell(n)}$ shown in Fig.8.1.1) should not be operated in cell balance at the same time.
- When cell balance is turned ON, the OV/UV detection will not operate correctly. Therefore, user shall turn OFF OV/UV detection when using cell balance. (See Chapter 11 Monitoring and Protection)
- In using the cell balance function, the power consumption of the IC increases. Then user shall do the thermal design with enough margin for the actual usage. Please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions.
  (See 1.4.2 POWER DISSIPATION RATING)

How to design cell balance with built-in MOSFET (See Fig.8.1.1)

- Cell balance can be done by turning ON the SW made of built-in MOSFET.
- ON resistance of built-in MOSFET (SW) is Max.20Ω.
- For either single cell or multi-cells balance, user shall set the external resistor (R) value so that current flowing through the built-in MOSFET ($I_{CB\ (n)}$) does not exceed 50mA.

If more discharge current flowing through the built-in MOSFET is required, it is recommended to use external FET for cell balance shown in Fig.8.1.2 .



SW : Built-in MOSFET

R_{ON} : ON resistance of built-in MOSFET (Max.20Ω)

$I_{CB(n+1)} = V_{cell(n+1)} / (2R + R_{ON})$

$I_{CB(n-1)} = V_{cell(n-1)} / (2R + R_{ON})$

Fig.8.1.1 Circuit example in using the built-in MOSFET

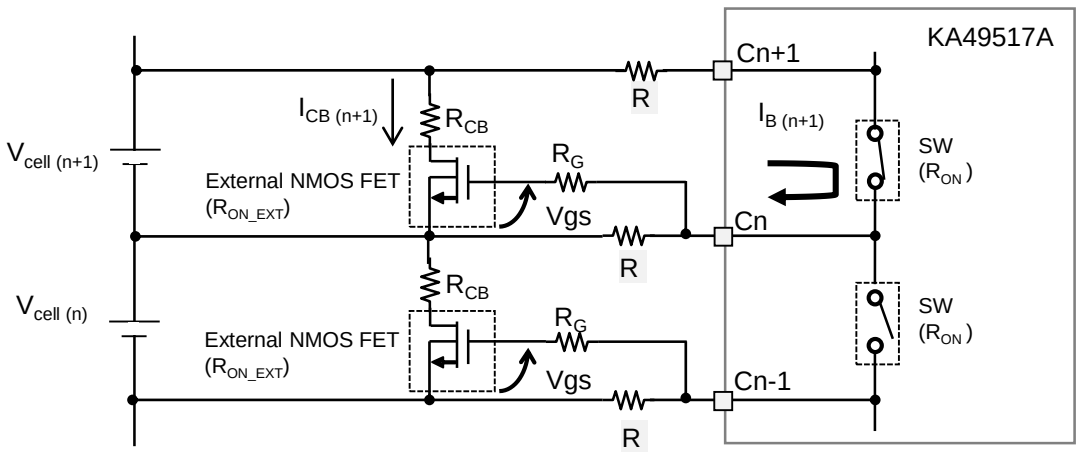
Description of Functions

8. Cell Balance

8.1 Description of Cell Balance

How to design cell balance with external NMOS FET (See Fig.8.1.2)

- Cell balance can be done by turning ON the external NMOS FET with the Vgs, the Vgs is generated by the discharge current ($I_{B\ (n)}$) when the built-in MOSFET SW is ON and the external resistor (R) .
- ON resistance of built-in MOSFET (SW) is Max.20Ω.
- Cell balance current in the external MOSFET ($I_{CB\ (n)}$) can be obtained by the cell voltage ($V_{cell\ (n)}$) and the resistance value (R_{CB} + R_{ONext})
- User shall set the external resistor (R) value so that current flowing through the built-in MOSFET ($I_{CB\ (n)}$) does not exceed 50mA.



Vgs : Gate-Source voltage of external NMOS FET

R_{ON_EXT} : ON resistance of external NMOS FET

SW : Built-in MOSFET

R_{ON} : ON resistance of built-in MOSFET (Max.20Ω)

R_G : MOSFET Gate Resistor

$I_{B(n+1)}$ = $V_{cell(n+1)}$ / (2R + R_{ON})

Vgs = R x $I_{B(n+1)}$

= $V_{cell(n+1)}$ / 2 ($R_{ON} \ll R$)

$I_{CB(n+1)}$ = $V_{cell(n+1)}$ / (R_{CB} + R_{ONext})

Fig.8.1.2 Circuit example in using the external MOSFET

Description of Functions

8. Cell Balance

8.2 Control Registers of Cell Balance

Table.8.2.1 shows the registers that control Cell Balance.

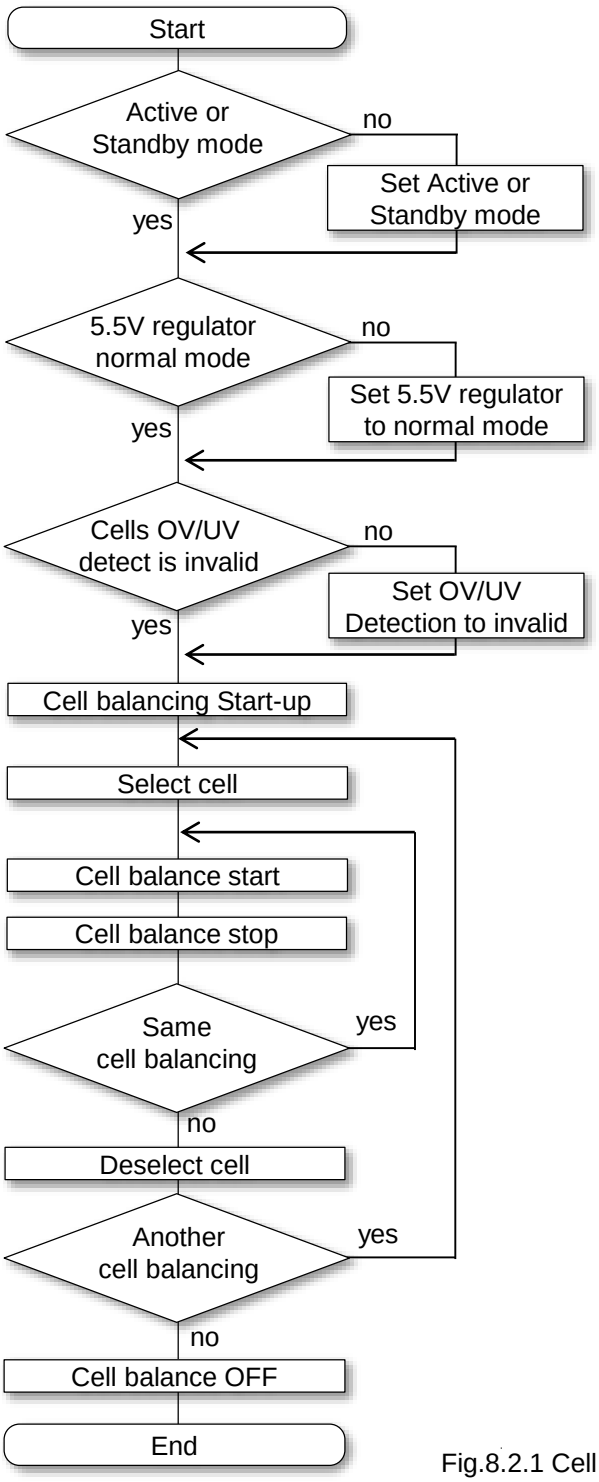
Table.8.2.1 Cell Balance Control Registers

Register	Address [bit]	Function
CB_SET	0x0C [8]	Cell Balance ON/OFF control register 1: Cell balance operation ON 0: Cell balance operation OFF (Default)
DI_CBSEL	0x15 [15:0]	Selection of cell for balancing (Channels 1-16) 1: Cell balance selected 0: Cell balance not selected (Default)
DI_CBSEL	0x16 [0]	Selection of cell for balancing (Channel 17) 1: Cell balance selected 0: Cell balance not selected (Default)
CB_ST	0x51 [15:0]	Individual cell balance control status display (Channels 1-16) 1: Cell balance ON 0: Cell balance OFF
CB_ST	0x52 [0]	Individual cell balance control status display (Channels 17) 1: Cell balance ON 0: Cell balance OFF
NPD_CB	0x17 [0]	Cell balance control power down 1: Normal. 0: Power down (Default).

Description of Functions

8. Cell Balance

8.3 Cell Balance Flow



■Prior confirmation
Set to Active mode or Standby mode and set the 5.5V regulator to normal mode. Disable OV/UV detection of cell voltage.

■Cell balancing Start-up
Set NPD_CB flag (address 0x17[0]) to “1” to turn ON cell balance circuit.

■Select cell
Set DI_CBSEL flag (address 0x15[15:0] and address 0x16[0]) to “1” for cell to be cell balanced.

DI_CBSELn is corresponding to VCELL (n) (e.g. if DI_CBSEL[1] is selected, VCELL (1) (between C1-C0) is cell balanced.)
Please do not select adjacent cells at the same time.

■Cell balance start
Set CB_SET flag (address 0x0C[8]) to ”1” to start cell balancing operation.

■Cell balance stop
Set CB_SET flag (address 0x0C[8]) to “0” to stop cell balancing operation.

■Deselect cell
Set DI_CBSEL flag (address 0x15[15:0] and address 0x16[0]) to “0” to deselect cell.

■Another cell balancing
When doing another cell balancing, repeat step from “select cell “ to “deselect cell”.

■Cell balance OFF
Set NPD_CB flag (address 0x17[0]) to “0” to turn OFF cell balance circuit.

Fig.8.2.1 Cell Balance Flow

Description of Functions

9. Voltage Measurement

9.1 Voltage Measurement

Voltage data is measured by the built-in 14 bits ADC in both Active Mode and Intermittent Active Mode. Figure.9.1.1 below shows the sequence of data measured by ADC. The voltage measurement is done in the following sequence, VREF2; VDD18; REGEXT, GPIO1~2 pin, VPACK, TMONI1~5 pin, VDD55, and Cells Voltage.

The measurement cycle time, including the Reset period, is about 1.5ms (50us per slot × 30 slots).

The voltage measurement can be set to continuous measurement or 1-shot measurement with respective registers which will be explained in this chapter.

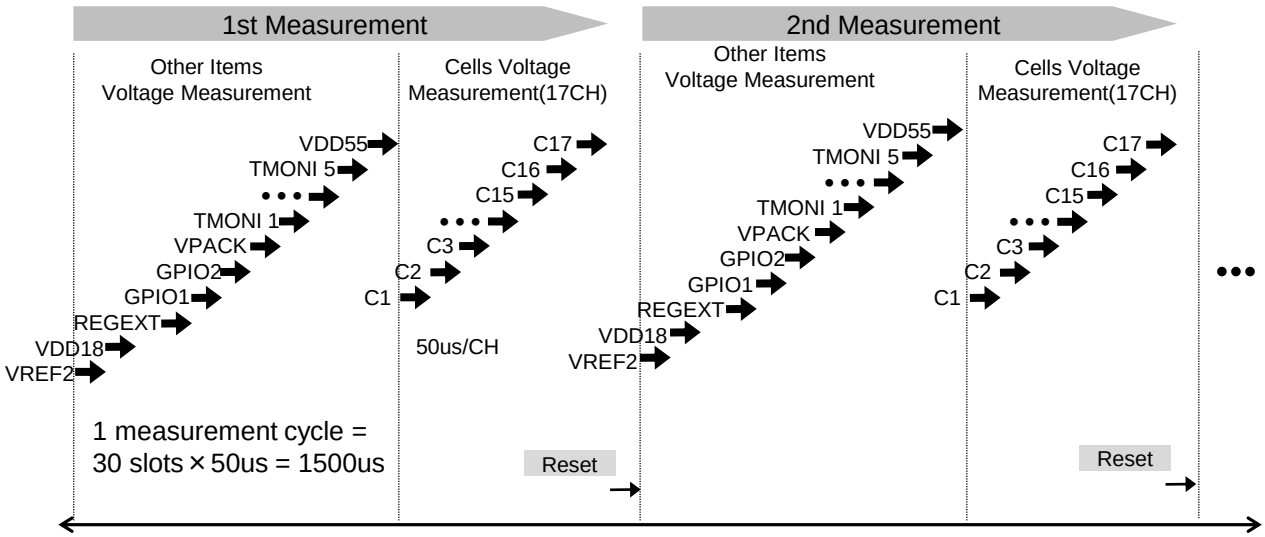


Fig.9.1.1 Measurement sequence (Continuous measurement)

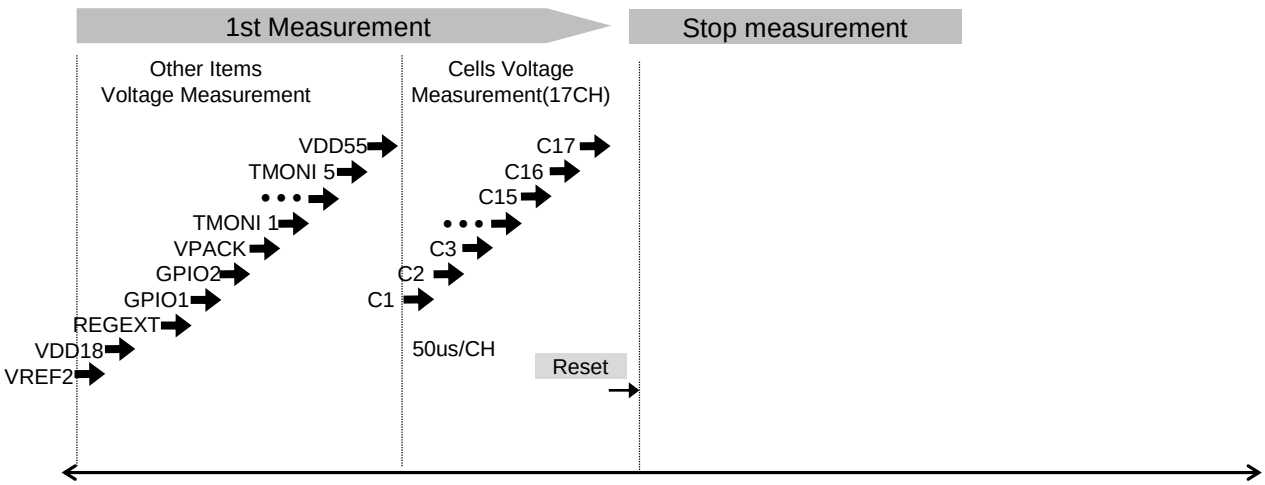


Fig.9.1.2 Measurement sequence (1-Shot measurement)

Description of Functions

9. Voltage Measurement

9.1 Voltage Measurement

The block diagram of the ADC for voltage measurement is shown in Fig.9.1.3.
Cell voltage measurement is measured the differential voltage of both cell ends, for example both ends of Cell17 are C17 and C16),
For TMONI pin, GPIO pin, VPACK voltage and VDD55, the voltage measurement is measured the voltage between the pin and GND.

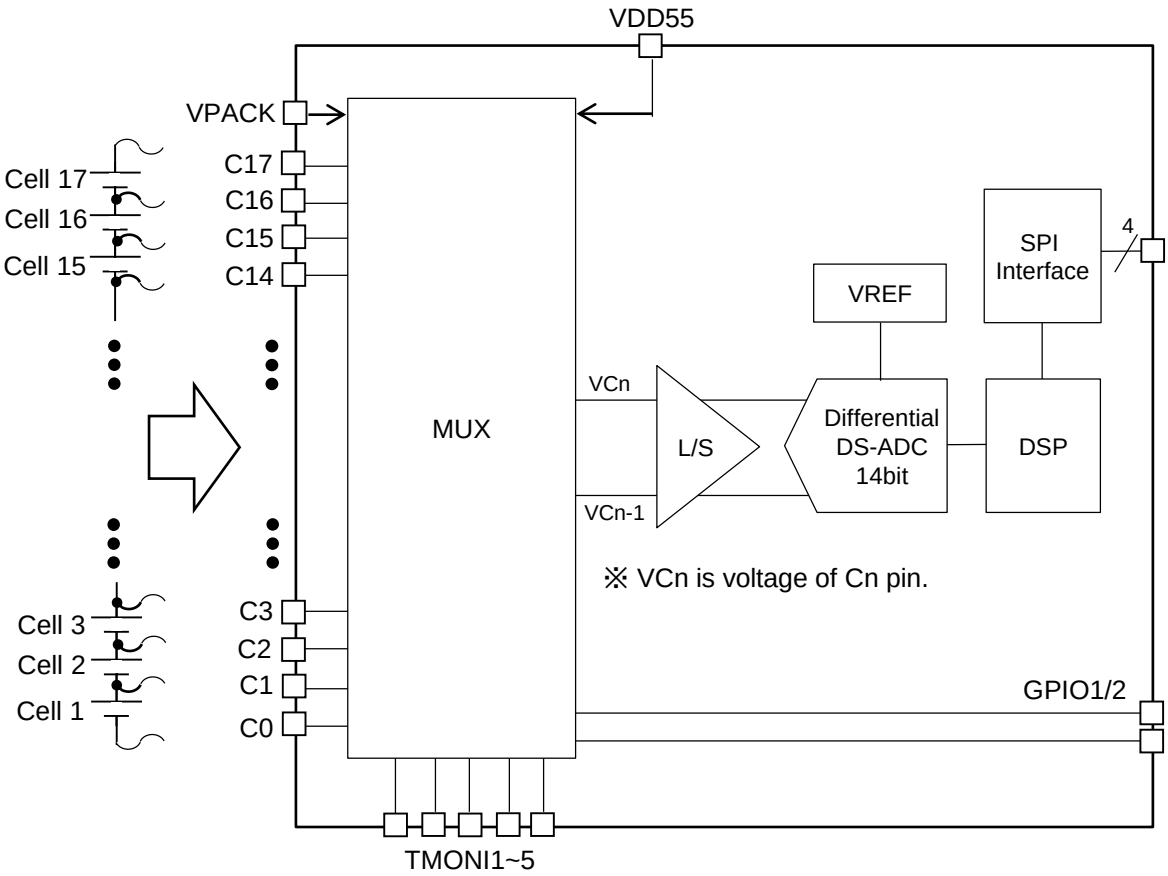


Fig.9.1.3 block diagram of the ADC for voltage measurement

Description of Functions

9. Voltage Measurement

9.1.1 Voltage Measurement Timing

Voltage measurement is operated during active mode only. There are two measurement operation, continuous measurement (when ADC_CONT flag (address 0x01[15] = “1”) and 1shot operation (when ADC_CONT flag (address 0x01[15] =“0”). During continuous measurement, the voltage measurement cycle is repeating. While 1-shot measurement is done once when ADC_TRG flag (address 0x0C[4]) is set to “1”. This flag is automatically cleared to “0” after measurement.

When each measurement cycle is completed, ADIRQ1 signal output through GPIO pin will be triggered to “H” and register VAD_DONE flag (address 0x1C[5]) will be set to “1”. The measured data will be latched to data register 0x28~0x4B by setting ADV_LATCH flag (address 0x0C[0]) to “1”, ADIRQ1 signal will be reset to “L” and ADV_LATCH flag (address 0x0C[0]) become “0” after completion. VAD_DONE flag (address 0x1C[5]) is cleared by writing “1” to it.

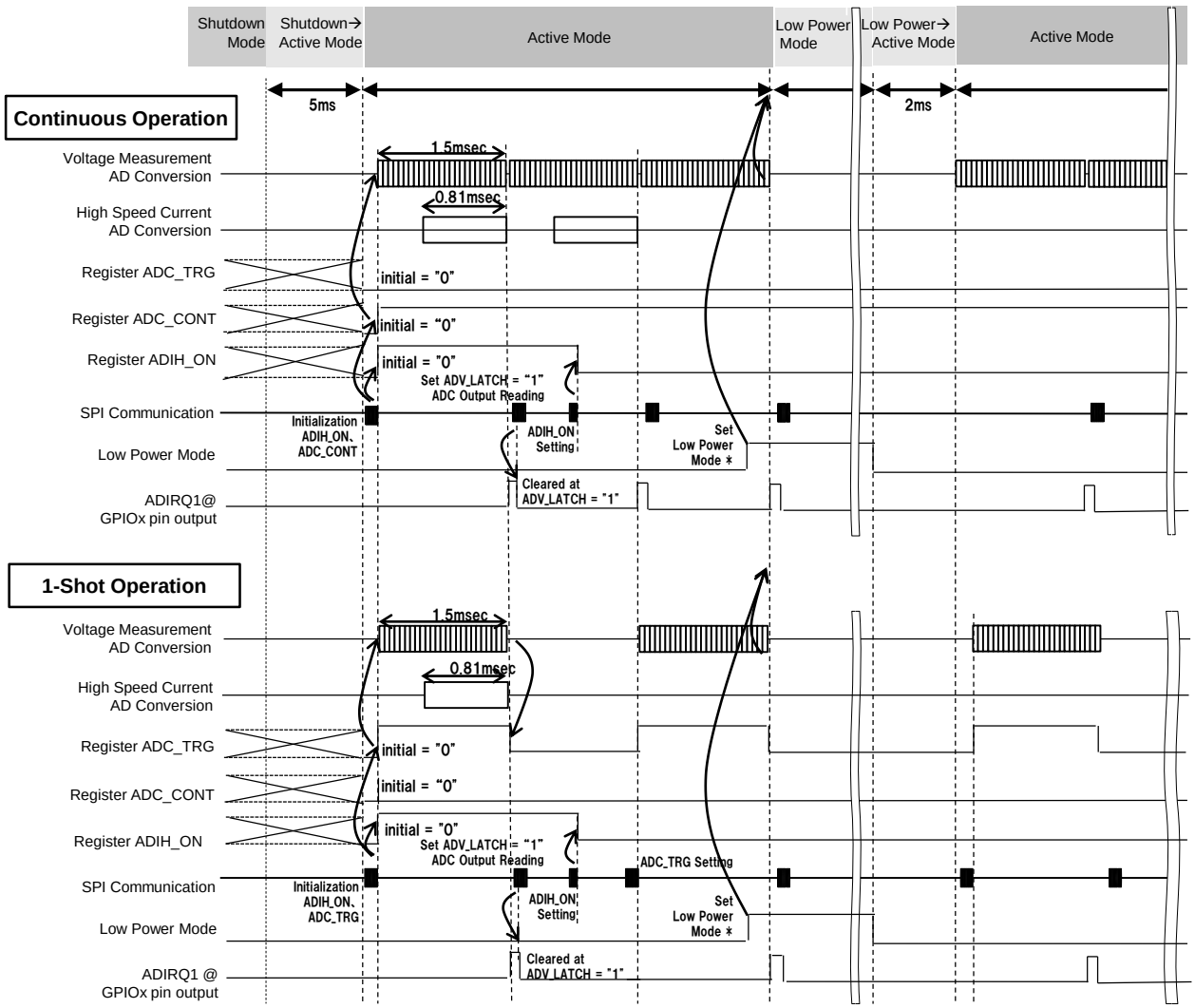


Fig.9.1.4 Example of Voltage and Current Measurement Timing Diagram

Description of Functions

9. Voltage Measurement

9.2 Control Registers of Voltage Measurement

Table.9.2.1 Voltage Measurement Control Registers1

Register	Address [bit]	Function
CVSEL	0x05, 0x06	Respective cell voltage measurement ON/OFF setting register
GVSEL	0x07	Other voltage measurement ON/OFF setting register
OP_MODE	0x0C	ADC Operation register
GPIO_CTL1	0x0D	GPIO control 1 register
GPIO_CTL2	0x0E	GPIO control 2 register
GPIO_CTL3	0x0F	GPIO control 3 register
ADCTL1	0x18	ADC control register1
TMONI1	0x57	FUSE setting for TMONI1 pull up R measurement
TMONI23	0x58	FUSE setting for TMONI2 & 3 pull up R differential from TMONI1 measurement
TMONI45	0x59	FUSE setting for TMONI4 & 5 pull up R differential from TMONI1 measurement
OVSTAT1 OVSTAT2	0x22 0x23	ADC/ALARM Status register
UVSTAT1 UVSTAT2	0x24 0x25	ADC/ALARM Status register
STAT5	0x27	ADC/ALARM Status register
CV01_AD	0x28	Voltage measurement result for cell 1 register
CV02_AD	0x29	Voltage measurement result for cell 2 register
CV03_AD	0x2A	Voltage measurement result for cell 3 register
CV04_AD	0x2B	Voltage measurement result for cell 4 register
CV05_AD	0x2C	Voltage measurement result for cell 5 register
CV06_AD	0x2D	Voltage measurement result for cell 6 register
CV07_AD	0x2E	Voltage measurement result for cell 7 register
CV08_AD	0x2F	Voltage measurement result for cell 8 register
CV09_AD	0x30	Voltage measurement result for cell 9 register
CV10_AD	0x31	Voltage measurement result for cell 10 register

Description of Functions

9. Voltage Measurement

9.2 Control Registers of Voltage Measurement

Table.9.2.2 Voltage Measurement Control Registers 2

Register	Address [bit]	Function
CV11_AD	0x32	Voltage measurement result for cell 11 register
CV12_AD	0x33	Voltage measurement result for cell 12 register
CV13_AD	0x34	Voltage measurement result for cell 13 register
CV14_AD	0x35	Voltage measurement result for cell 14 register
CV15_AD	0x36	Voltage measurement result for cell 15 register
CV16_AD	0x37	Voltage measurement result for cell 16 register
CV17_AD	0x38	Voltage measurement result for cell 17 register
VPACK_AD	0x3E	Voltage measurement result for VPACK register
TMONI1_AD	0x3F	Voltage measurement result for TMONI1 register
TMONI2_AD	0x40	Voltage measurement result for TMONI2 register
TMONI3_AD	0x41	Voltage measurement result for TMONI3 register
TMONI4_AD	0x42	Voltage measurement result for TMONI4 register
TMONI5_AD	0x43	Voltage measurement result for TMONI5 register
VDD55_AD	0x44	Voltage measurement result for VDD55 register
GPIO1_AD	0x45	Voltage measurement result for GPIO1 register
GPIO2_AD	0x46	Voltage measurement result for GPIO2 register
VDD18_AD	0x49	Voltage measurement result for VDD18 register
REGEXT_AD	0x4A	Voltage measurement result for REGEXT register
VREF2_AD	0x4B	Voltage measurement result for VREF2 register

Description of Functions

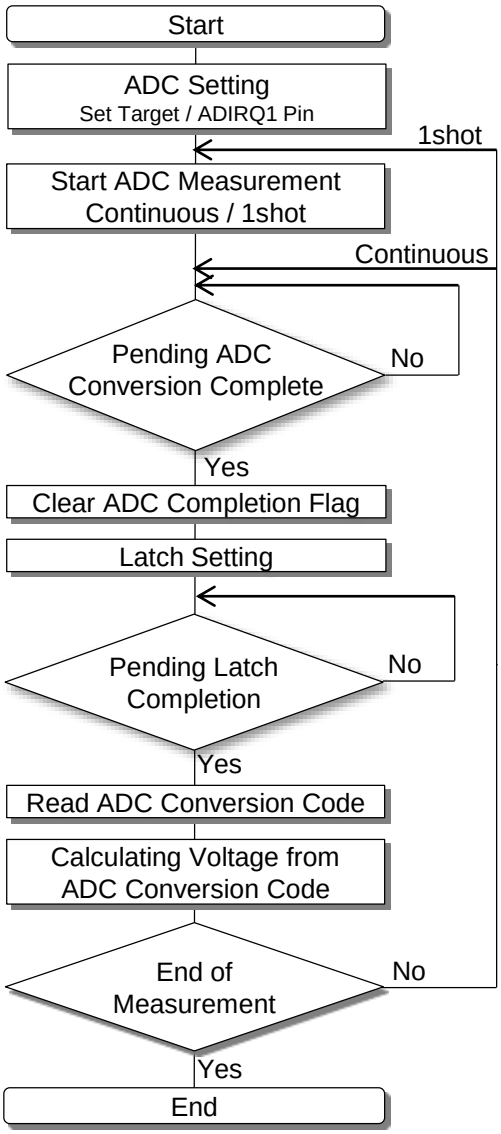
9. Voltage Measurement

9.3 Cell Voltage Measurement

Voltage across each cell (C1, C2 … C17) will be measured during voltage measurement cycle.

9.3.1 Cell Voltage Measurement Setting Procedure

Cell Voltage use the following settings
- Set Measurement Target: Cell 1~17
- ADIQR1 Pin Setting



■ADC Setting
Set the CV[n]SEL flag (address 0x05[15:0] and address 0x06[0] to 0xFFFF, 0x0001 respectively to set measurement target.
Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1.
Set the GPIO1_NOE flag (address 0x0D[1]) to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output : ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for CVn_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read CVn_AD register (address: 0x28-0x38)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from Cell voltage conversion table.9.3.1.

Description of Functions

9. Voltage Measurement

9.3 Cell Voltage Measurement

9.3.2 Cell Voltage Conversion Table

The full range and resolution of cell voltage measurement is shown below and listed in Table.9.3.1.

- Maximum input voltage : 4.999695V = 5.0V × (2^{14}-1) / 2^{14}
- Minimum Input Voltage : 0V
- Resolution : 0.000305V = 5.0V/2^{14}

Table.9.3.1 Cell Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (CV01_AD[13:0] ～ CV17_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Functions

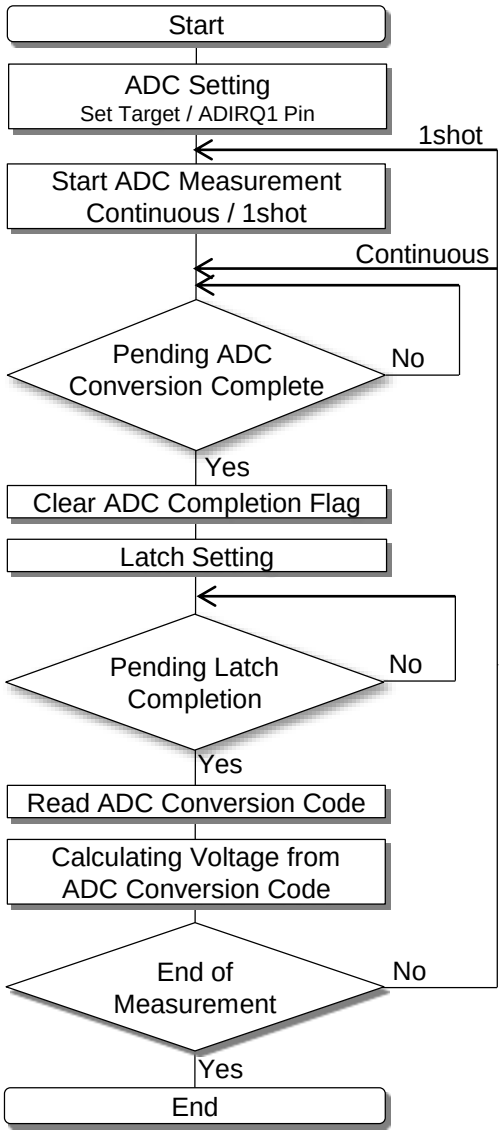
9. Voltage Measurement

9.4 VPACK Voltage Measurement

Voltage at VPACK pin is measured during voltage measurement cycle.

9.4.1 VPACK Voltage Measurement Setting Procedure

VPACK Voltage use the following settings
- Set Measurement Target: VPACK
- ADIQR1 Pin Setting



■ADC Setting
Set the VPACK_SEL flag (address 0x07[0]) to “1” to set measurement target. Set the GPIO1SEL flag (address 0x0D[11:8] to “0011” to output ADIRQ1.
Set the GPIO1_NOE flag (address 0x0D[1] to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output :
ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for VPACK_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read VPACK_AD register (address 0x3E)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from VPACK voltage conversion table.9.4.1.

Description of Functions

9. Voltage Measurement

9.4 VPACK Voltage Measurement

9.4.2 VPACK Voltage Conversion Table

The full range and resolution of cell voltage measurement is shown below and listed in table below.

- Maximum input voltage : 109.9933V = 110.0V × $(2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : 0.006714V = $110.0V/2^{14}$

Table.9.4.1 VPACK Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VPACK_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
109.9933	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
55.007802	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
55.001088	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
54.994374	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.006714	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Functions

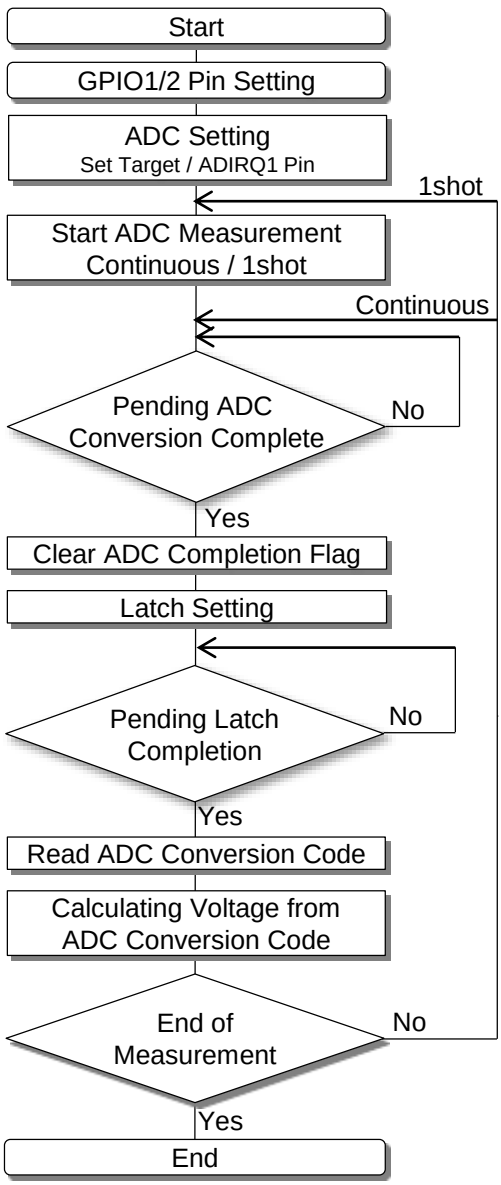
9. Voltage Measurement

9.5 GPIO1/2 Voltage Measurement

GPIO1/2 pins set as analog input and the voltage will be measured during voltage measurement cycle.

9.5.1 GPIO1/2 Voltage Measurement Setting Procedure

GPIO1/2 Voltage use the following settings
- Set Measurement Target: GPIO1,2
- ADIQR1 Pin Setting



■GPIO1/2 Pin Setting
Set GPIO1/2 Pin as Table 9.5.1.

■ADC Setting
Set the GPAD2SEL and GPAD1SEL flag (address 0x07[8:7]) to "11" to set measurement target.
Set GPIO3SEL flag (address 0x0F[11:8]) to "0011" to output ADIRQ1.
Set GPIO3_NOE flag (address 0x0F[1]) to "0" for GPIO3 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to "1" to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to "1" to start ADC Measurement, this flag is auto cleared to "0" after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO3 pin :
ADIRQ1 → "H" when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become "1" when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to "1" to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to "1", latch Voltage measurement result for GPIO1/2_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become "0" or ADIRQ1 pin become "L". Or wait for 315ns.

■Reading ADC Conversion Code
Read GPIO1/2_AD register (address 0x45~0x46)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from GPIO1/2 voltage conversion table.9.5.2.

Description of Functions

9. Voltage Measurement

9.5 GPIO1/2 Voltage Measurement

9.5.2 GPIO1 Pin Registers setting of Voltage Measurement

Table.9.5.1 GPIO1 pin setting of GPIO Voltage Measurement

Address [Bit]	Flag	Pin Configuration	Description
0x0D [1]	GPIO1_NOE	Output Enable	1:Disabled（default）
0x0D [0]	GPIO1_IE	Input Enable	1:Enabled
0x0D [3]	GPIO1_OD	Output Configuration	0:Push Pull(default)
0x0D [2]	GPIO1_PD	Pull-Down Register	0:No（default）
0x1C [13]	ST_GPIO1	Input Data	0:LO (VSS) （default）
0x0D [4]	GPIO1_OUT	Output Data	0:LO （default）
0x0D [5]	GPIO1_CHDRV	Output Drivability	0:2mA （default）
0x0D [11:8]	GPIO1SEL[1:0]	Function	0011:Analog Input

9.5.3 GPIO1/2 Voltage Conversion Table

The full range and resolution of GPIO1/2 voltage measurement is shown below and listed in table below.

- Maximum input voltage : $4.999695V = 5.0V \times (2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : $0.000305V = 5.0V/2^{14}$

Table.9.5.2 GPIO1/2 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (GPIO1_AD[13:0] / GPIO2_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Functions

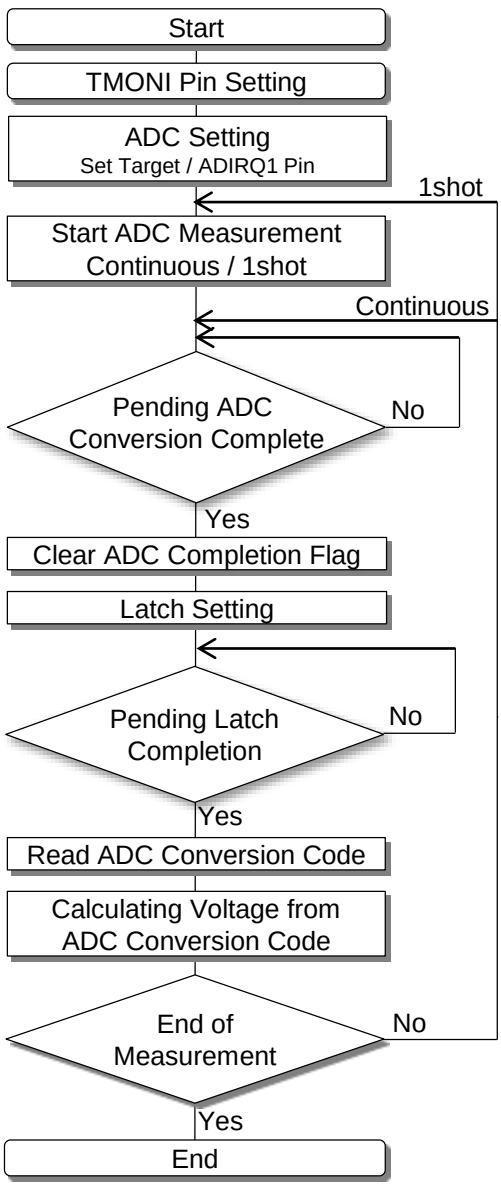
9. Voltage Measurement

9.6 TMONI 1~5 Voltage Measurement

TMONI 1~5 pins are designed as temperature measurement input.
To used these pins, connect thermistor externally to GND and set registers accordingly as below.

9.6.1 TMONI 1~5 Voltage Measurement Setting Procedure

TMONI Voltage use the following settings
- Set Measurement Target: TMONI1~5
- ADIQR1 Pin Setting



■TMONI Pin Setting
Set PULLUP_SEL flag (address 0x11[7:3]) to “11111” to add the pull-up resistance in ADC measurement. Pull-up resistor is only connected during voltage measurement for respective pin.

■ADC Setting
Set the TMONInSEL flag (address 0x07[5:1]) to “11111” to set measurement target. Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1. Set the GPIO1_NOE flag (address 0x0D[1] to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output :
ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for TMONIn_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read TMONIn_AD register (0x3F-0x43)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from TMONI voltage conversion table.9.6.1.

Description of Functions

9. Voltage Measurement

9.6 TMONI 1~5 Voltage Measurement

9.6.2 TMONI 1~5 Voltage Conversion Table

The full range and resolution of TMONI voltage measurement is shown below and listed in table below.

- Maximum input voltage : 4.999695V = 5.0V × $(2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : 0.000305V = $5.0V/2^{14}$

Table.9.6.1 TMONI Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (TMONI1_AD[13:0]～TMONI5_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Functions

9. Voltage Measurement

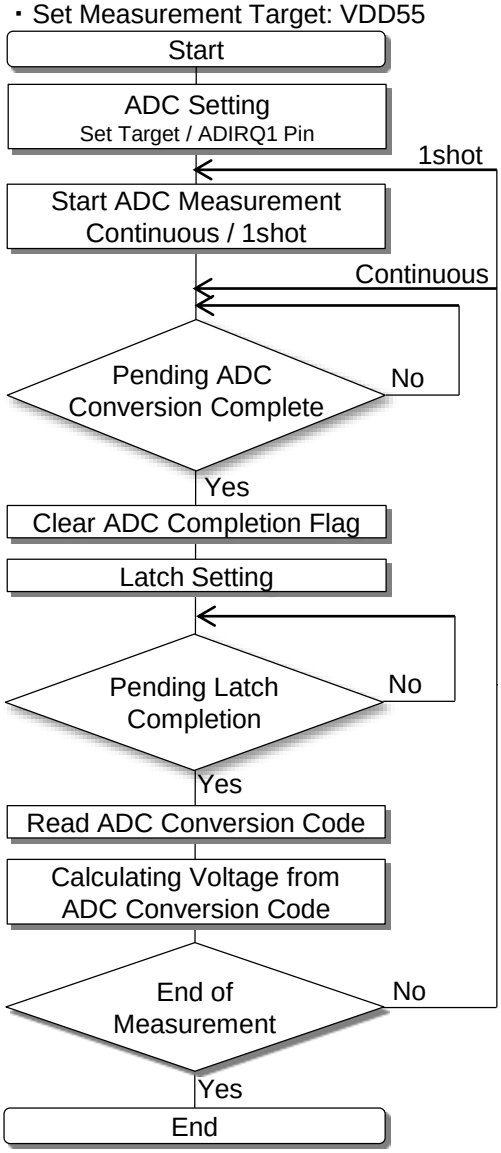
9.7 VDD55 Voltage Measurement

VDD55 is measured during voltage measurement cycle. As VDD55 is used as supply voltage for internal pull up resistor for TMONI 1~5 pins, VDD55 voltage affect the TMONI 1~5 pin voltage measurement.

9.7.1 VDD55 Voltage Measurement Setting Procedure

VDD55 Voltage use the following settings

・Set Measurement Target: VDD55



■ADC Setting
Set the VDD55SEL flag (address 0x07[6]) to “1” to set measurement target.
Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1. Set the GPIO1_NOE flag (address 0x0D[1]) to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output :
ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for VDD55_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read VDD55_AD register (address 0x44)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from VDD55 voltage conversion table.9.7.1.

Description of Functions

9. Voltage Measurement

9.7 VDD55 Voltage Measurement

9.7.2 VDD55 Voltage Conversion Table

The full range and resolution of VDD55 voltage measurement is shown below and listed in table below.

- Maximum input voltage : 7.499542V = 7.5V × $(2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : 0.000458V = $7.5V/2^{14}$

Table.9.7.1 VDD55 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VDD55_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7.499542	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪	▪
3.750458	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
3.750000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3.749542	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Description of Functions

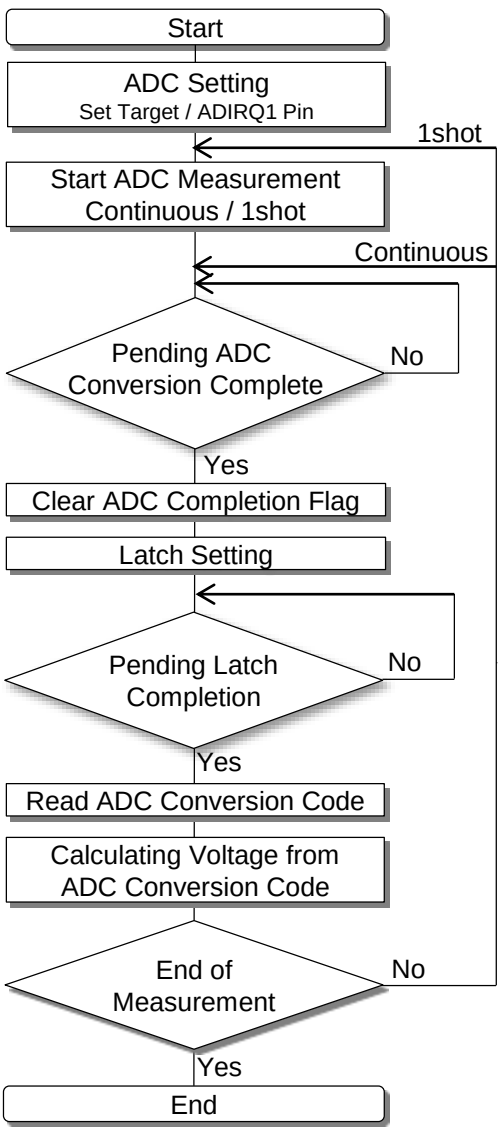
9. Voltage Measurement

9.8 REGEXT Voltage Measurement

REGEXT, regulator for external circuit is measured during voltage measurement cycle.

9.8.1 REGEXT Voltage Measurement Setting Procedure

REGEXT Voltage use the following settings
・Set Measurement Target: REGEXT



■ADC Setting
Set the REGEXTSEL flag (address 0x07[13]) to “1” to set measurement target.
Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1. Set the GPIO1_NOE flag (address 0x0D[1]) to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output :
ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for VDD55_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read REGEXT_AD register (address 0x4A)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from REGEXT voltage conversion table.9.8.1.

Description of Functions

9. Voltage Measurement

9.8 REGEXT Voltage Measurement

9.8.2 REGEXT Voltage Conversion Table

The full range and resolution of REGEXT voltage measurement is shown below and listed in table below.

・Maximum input voltage : 7.499542V = 7.5V × $(2^{14}-1)/2^{14}$

・Minimum Input Voltage : 0V

・Resolution : 0.000458V = $7.5V/2^{14}$

Table.9.8.1 REGEXT Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (REGEXT_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
7.499542	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
3.750458	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
3.750000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
3.749542	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Description of Functions

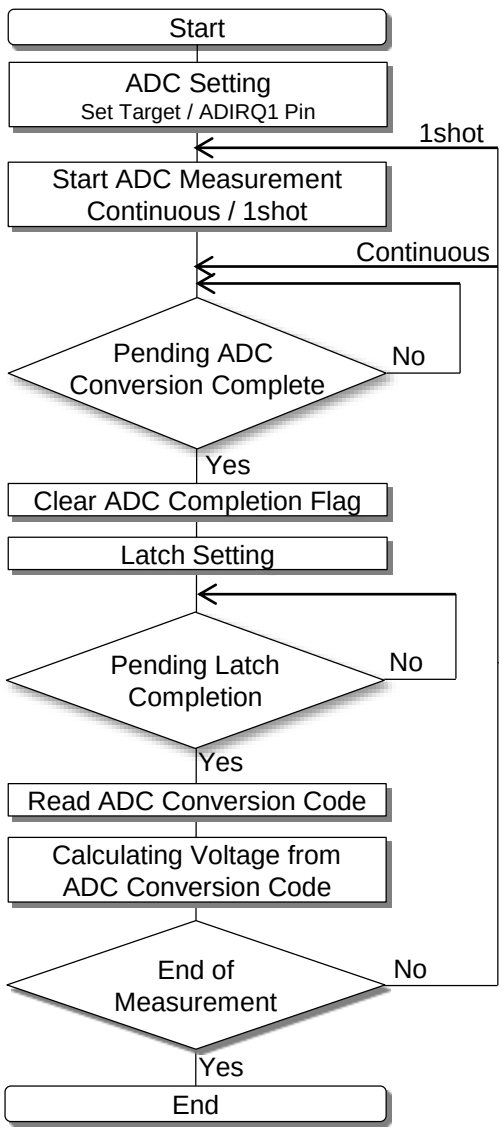
9. Voltage Measurement

9.9 VDD18 Voltage Measurement

VDD18, internal regulator is measured during voltage measurement cycle.

9.9.1 VDD18 Voltage Measurement Setting Procedure

VDD18 Voltage use the following settings
・Set Measurement Target: VDD18



■ADC Setting
Set the VDD18SEL flag (address 0x07[12]) to “1” to set measurement target.
Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1. Set the GPIO1_NOE flag (address 0x0D[1]) to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output :
ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for VDD55_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read VDD18_AD register (address 0x49)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from VDD18 voltage conversion table.9.9.1.

Description of Functions

9. Voltage Measurement

9.9 VDD18 Voltage Measurement

9.9.2 VDD18 Voltage Conversion Table

The full range and resolution of VDD18 voltage measurement is shown below and listed in table below.

- Maximum input voltage : $4.999695V = 5.0V \times (2^{14}-1)/2^{14}$
- Minimum Input Voltage : 0V
- Resolution : $0.000305V = 5.0V/2^{14}$

Table.9.9.1 REG18 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VDD18_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Functions

9. Voltage Measurement

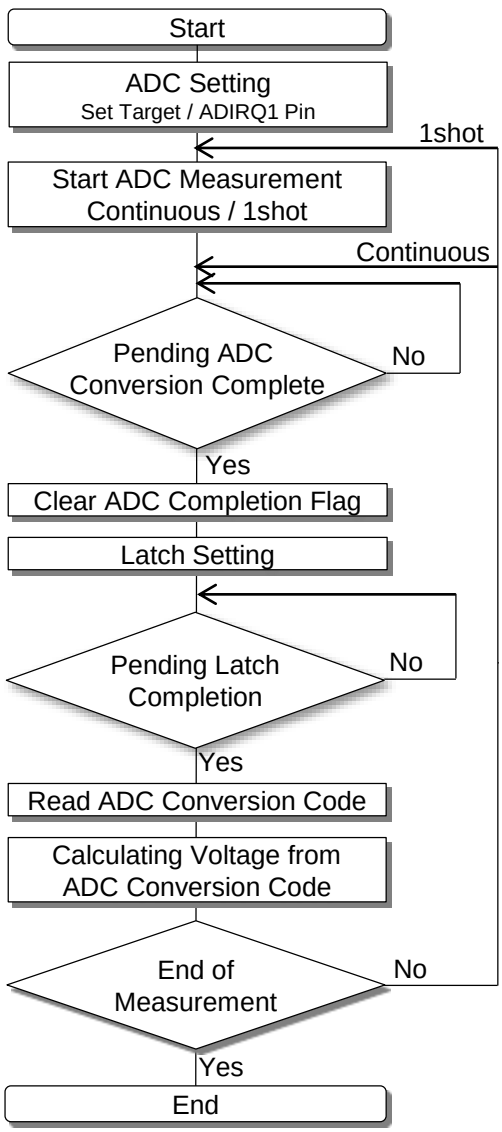
9.10 VREF2 Voltage Measurement

VREF2 is internal reference voltage for slow speed current ADC. The voltage measure of VREF2 is done by voltage ADC which is using reference voltage of VREF1. By measuring VREF2 using VREF1 as ADC reference, it provides a ratio check of VREF2 and VREF1 which should stay relatively constant. This can be used as a diagnostic check if 1 reference changes against the other.

9.10.1 VREF2 Voltage Measurement Setting Procedure

VREF2 Voltage use the following settings

・Set Measurement Target: VREF2



■ADC Setting
Set the VREF2SEL flag (address 0x07[14]) to “1” to set measurement target.
Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1. Set the GPIO1_NOE flag (address 0x0D[1]) to “0” to set GPIO1 as output.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin output :
ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for VDD55_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read VREF2_AD register (address 0x4B)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from VREF2 voltage conversion table.9.10.1.

Description of Functions

9. Voltage Measurement

9.10 VREF2 Voltage Measurement

9.10.2 VREF2 Voltage Conversion Table

The full range and resolution of VREF2 voltage measurement is shown below and listed in table below.

・Maximum input voltage : 4.999695V = 5.0V × $(2^{14}-1)/2^{14}$

・Minimum Input Voltage : 0V

・Resolution : 0.000305V = $5.0V/2^{14}$

Table.9.10.1 VREF2 Voltage Conversion Table

Analog level [V] (typ)	Code	Digital output (VREF2_AD[13:0])													
		MSB													LSB
		b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
4.999695	0x3FFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
2.500305	0x2001	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2.500000	0x2000	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2.499695	0x1FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1
・	・	・	・	・	・	・	・	・	・	・	・	・	・	・	・
0.000305	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Description of Functions

9. Voltage Measurement

9.11 Temperature Measurement with TMONI1~5 pins

9.11.1 Temperature Measurement Procedure with TMONI1~5 pins

TMONI1~5 is designed for temperature measurement, with external thermistor connected from each pin to ground. For each pin, there is an internal pull up resistor of 10kΩ to VDD55 connected with a switch. User may choose to use the internal pull up resistor or external pull up resistor by register.

Due to the process tolerance, the internal pull up resistors may be deviated from the typical value, the actual resistor values are measured during the production test and stored in PULLUP_TMONIn registers, user should use these registers data in temperature calculation. These are explained in more details from the following section. By connecting the pull-up resistor and a thermistor externally in series, it is possible to measure the resistance of the thermistor externally.

The connection example at TMONI1~5 with thermistor and internal pull up resistor is given in Fig 9.11.1.

The temperature could be derived from the TMONI1~5 reading, VDD55 with the consideration of thermistor characteristic, and pull up resistor. The capacitor at TMONI1~5 should not exceed 1nF.

Please note that maximum input voltage of TMONI that can be measured by ADC is 5V and the built-in 10k resistor (R''_{PUx}) are pull-up to 5.5V internally. Therefore, the maximum resistance of the selected thermistor should be less than 50kohm. If the resistance of thermistor at the measured temperature range exceed 50khom, pull-down resistor ($R''_{PDx.}$) in parallel with thermistor is recommended.

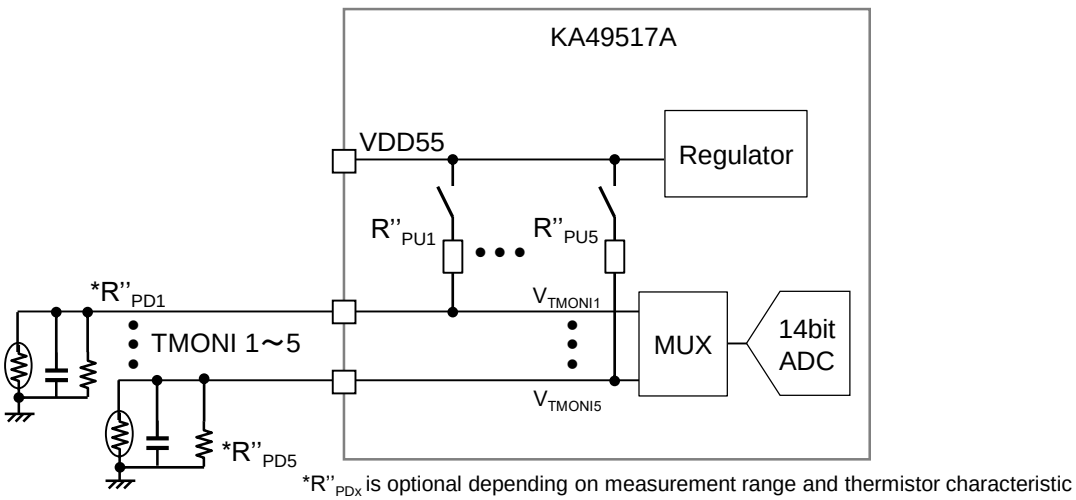


Fig.9.11.1 Thermistor Connection (Internal pull up resistor)

Description of Functions

9. Voltage Measurement

9.11 Temperature Measurement with TMONI1~5 pins

9.11.1 Temperature Measurement Procedure with TMONI1~5 pins

The temperature calculation procedure by TMONI pin is shown in Fig 9.11.2.

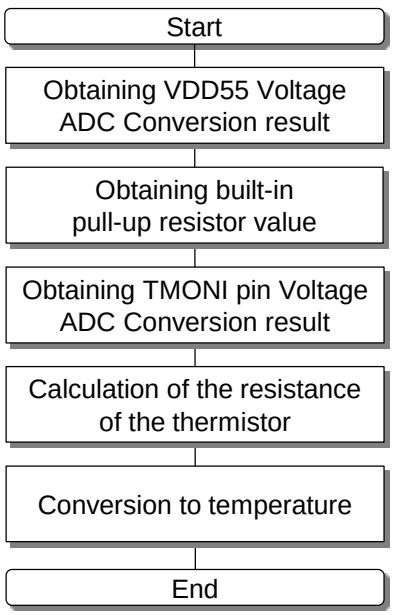


Fig.9.11.2 Temperature Measurement Procedure with TMONI1~5 pins

■Obtaining VDD55 Voltage
Obtain the VDD55 voltage [V_{VDD55}] by the ADC conversion as explained in 9.7.

■Obtaining internal pull-up resistor value
Obtain internal pull-up resistor [R_{PU}], by reading the pre-measured data from the built-FUSE register and convert into the resistance value following steps in 9.11.2.

■Obtaining TMONI pin Voltage
Obtain voltage at each TMONI1~5 [V_{TMONI}] pins as explained in 9.6.

■Calculation of the resistance of the thermistor
Effective resistance of the thermistor [R_S] (kohm) can be calculated as [R_S] = (V_{TMONI} × R_{PU}) / (V_{VDD55} - V_{TMONI})

■Conversion to temperature
From the effective resistance of thermistor [R_S], the temperature can be obtained from the temperature characteristic of the thermistor, an example of the thermistor is shown in Fig.9.11.3.
Depending on whether R_{PDx} parallel pull-down resistor is connected or not, the value of temperature can be obtained from the corresponding Resistance-Temperature characteristic of the thermistor.

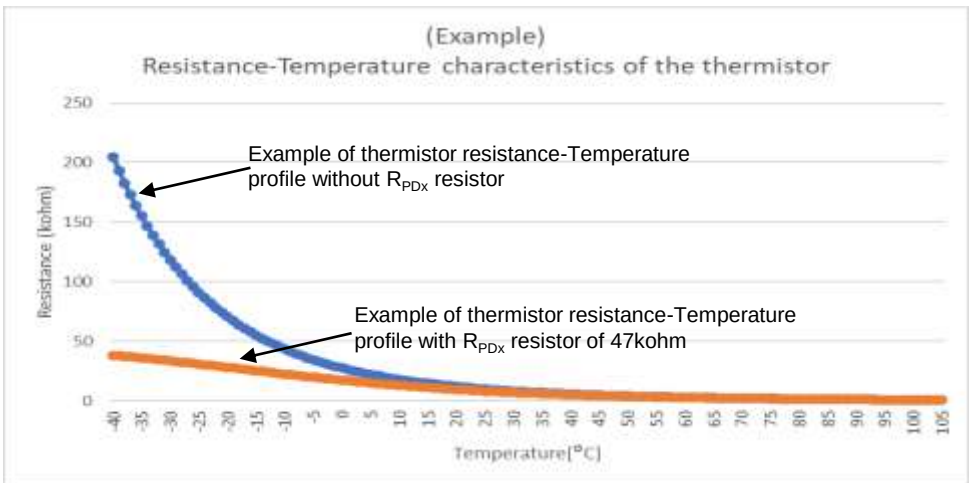


Fig.9.11.3 Resistance-Temperature characteristics of the thermistor (example)

Description of Functions

9. Voltage Measurement

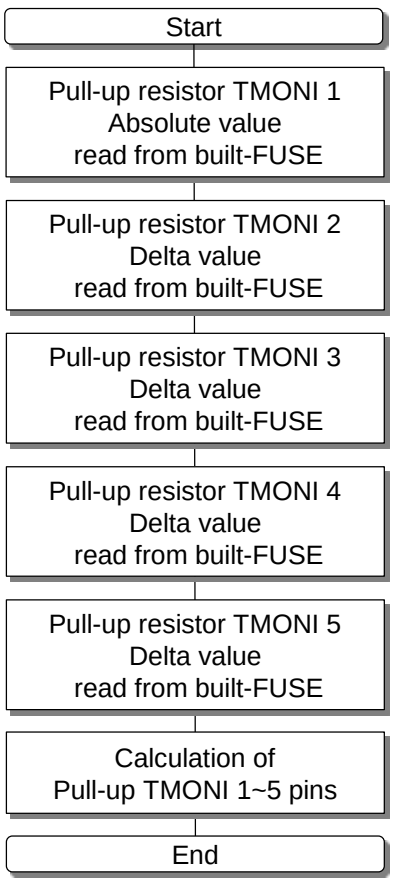
9.11 Temperature Measurement with TMONI 1~5 pins

9.11.2 Internal Pull-up Resistor of TMONI pin calculation procedure

The information for pre-measured pull up resistor of TMONI 1~5 is stored in the built-FUSE, it can be used to calculate the resistance value. The address map of the built-FUSE is shown in Table.9.11.1. Internal pull-up resistor value of TMONI 1 pin is absolute value, internal pull-up resistor value of TMONI 2 ~ 5 pins are stored as delta from TMONI 1 pin resistor.
The procedure to calculate the TMONI 1 ~ 5 internal pull-up resistor value is shown in Fig.9.11.4.

Fig.9.11.1 Address map for built in FUSE of TMONI Resistor

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x57							Pull-up resistor of TMONI 1 (absolute) [9:0]									
0x58	Pull-up resistor of TMONI 3 (delta) [7:0]								Pull-up resistor of TMONI 2 (delta) [7:0]							
0x59	Pull-up resistor of TMONI 5 (delta) [7:0]								Pull-up resistor of TMONI 4 (delta) [7:0]							



■Pull-up resistor of TMONI1 (absolute value)
Read back data from register address 0x57 [9:0]

■Pull-up resistor of TMONI2 (difference with TMON1 reading)
Read back data from register address 0x58 [7:0]

■Pull-up resistor of TMONI3 (difference with TMON1 reading)
Read back data from register address 0x58 [15:8]

■Pull-up resistor of TMONI4 (difference with TMON1 reading)
Read back data from register address 0x59 [7:0]

■Pull-up resistor of TMONI5 (difference with TMON1 reading)
Read back data from register address 0x59 [15:8]

■Calculation of Pull-up TMONI1~5 pins
TMONI1 is calculated resistance in accordance with TMONI1 pin pull-up resistor conversion table.9.11.2,
TMONI2 is calculated resistance in accordance with TMONI2 pin pull-up resistor conversion table.9.11.3.
TMONI3 ~ 5 pins are the same calculation formula as TMONI2 pin.

Fig.9.11.4 Internal pull-up resistor of TMONI pin calculation procedure

Description of Functions

9. Voltage Measurement

9.11 Temperature Measurement with TMONI 1~5 pins

9.11.2 Internal Pull-up Resistor of TMONI pin calculation procedure

■TMONI 1 pin

Refer to the table below to obtain pull up resistance from data read (from previous page)

- Max : 12.99414kΩ = 6kΩ X (2^9 – 1) / 2^{10} +10kΩ
- Min : 7kΩ
- Resolution : 5.86Ω = 6kΩ / 2^{10} (2's complement data)

■TMONI 2 pin

For TMONI2 pin, the delta from TMONI1 pin is determined from the table below using data read (from previous page)

- Max : 0.74414kΩ = 1.5kΩ X (2^7 – 1) / 2^8
- Min : - 0.75kΩ
- Resolution : 5.86Ω = 1.5kΩ / 2^8 (2's complement data)

Resistance of TMONI2 is calculated by : delta read in this step + TMONI 1 resistance

■TMONI 3/4/5 pins

TMONI 3~5 resistance can be determined similarly as TMONI 2 calculation.

Table.9.11.2 TMONI 1 pin pull up resistance conversion

Resistance [kΩ] (typ)	Code	Fuse Digital output (0x57[9:0])									
		MSB									LSB
		0x57									
		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
12.99414	0x1FF	0	1	1	1	1	1	1	1	1	1
·	·	·	·	·	·	·	·	·	·	·	·
10.00586	0x001	0	0	0	0	0	0	0	0	0	1
10.00000	0x000	0	0	0	0	0	0	0	0	0	0
9.99414	0x3FF	1	1	1	1	1	1	1	1	1	1
·	·	·	·	·	·	·	·	·	·	·	·
7.00586	0x201	1	0	0	0	0	0	0	0	0	1
7.00000	0x200	1	0	0	0	0	0	0	0	0	0

Table.9.11.3 TMONI 2 pin pull up resistance conversion

Resistance (Delta from TMONI1) [kΩ] (typ)	Code	Fuse Digital output (0x58[7:0])							
		MSB							LSB
		b7	b6	b5	b4	b3	b2	b1	b0
0.74414	0x7F	0	1	1	1	1	1	1	1
·	·	·	·	·	·	·	·	·	·
0.00586	0x01	0	0	0	0	0	0	0	1
0.00000	0x00	0	0	0	0	0	0	0	0
-0.00586	0xFF	1	1	1	1	1	1	1	1
·	·	·	·	·	·	·	·	·	·
-0.74414	0x81	1	0	0	0	0	0	0	1
-0.75000	0x80	1	0	0	0	0	0	0	0

Description of Functions

10. Current Measurement of SRP / SRN

10.1 SRP / SRN Sensing Current Measurement (High Speed / Low Speed)

KA49517A measures the voltage across the shunt resistor connected between SRP / SRN pins with ADC. For current measurement, different ADCs from voltage measurement are used as shown system block diagram. Current across the shunt resistor can be calculated by dividing the measured voltage with shunt resistor value used.
There are two current measurement modes, High Speed current measurement and Low Speed current measurement which uses two different ADCs. High Speed current measurement mode measured current in synchronize with the voltage measurement with a short measurement time. While Low Speed current measurement mode integrates the measured current, which can be used such as Coulomb Counter,
It is possible to be selected depending on the application.
The measured voltage is output as 16-bit data.

High Speed current measurement operates only during the Active mode.
Low Speed current measurements can operate in Active mode and Standby mode.

Conversion time of the ADC for High Speed current measurement mode is about 0.81ms while conversion time for Low Speed current measurement mode is about 250ms.

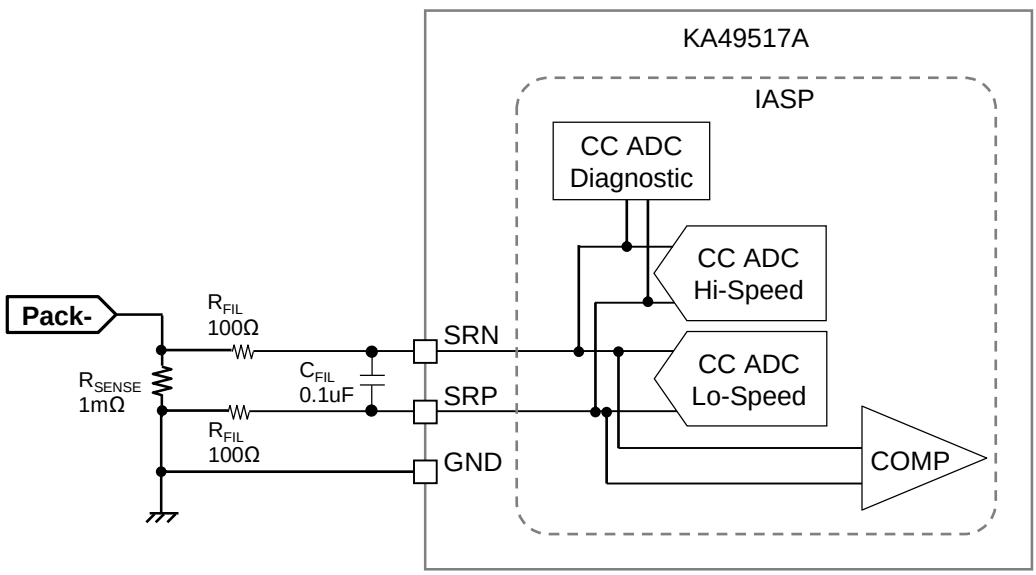


Fig.10.1.1 Block diagram of SRP / SRN Current Measurement (High Speed / Low Speed)

Description of Functions

10. Current Measurement of SRP / SRN

10.1 SRP / SRN Sensing Current Measurement (High Speed / Low Speed)

10.1.1 High Speed (HS) Current Measurement Timing

HS current measurement only operates during active mode which can be set by ADIH_ON flag (address 0x18[0]) and ADSWHY_EN flag (address 0x18[13]) to “1”. HS current measurement will start at next cell voltage measurement. The current is measured at the same time cell voltage is being measured, which is about 0.81ms for each measurement.

When current measurement completed, IADH_DONE flag (address 0x1C[6]) will be set to “1”, and the measured data is latched to CVIH_AD flag (address 0x47[15:0]) when ADIH_LATCH flag (address 0x0C[1]) is set to “1”, this flag is cleared to “0” after completion. IADH_DONE flag (address 0x1C[6]) is cleared by writing “1” to it.

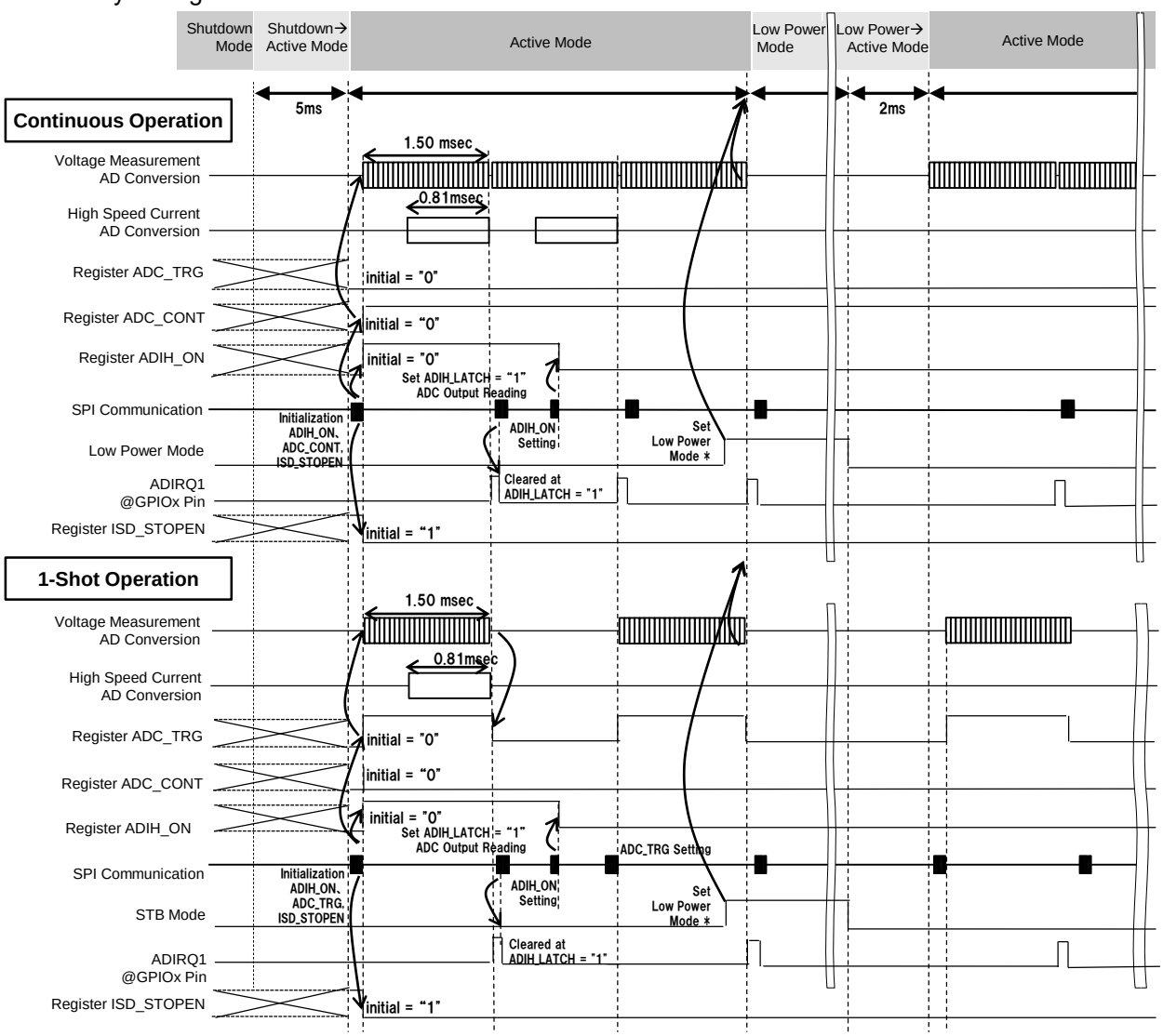


Fig.10.1.2 Example of Voltage and Current Measurement Timing Diagram

Description of Functions

10. Current Measurement of SRP / SRN

10.1 SRP / SRN Sensing Current Measurement (High Speed / Low Speed)

10.1.2 Low Speed (LS) Current Measurement Timing

Coulomb Counter can be operated during Active, Low Power and Standby Mode. The measurement starts when ADIL_ON flag (address 0x18[1]) and ADSWSD_EN flag (address 0x18[12]) set to “1” and accumulating the current for a period of 250ms. When each measurement cycle has completed, ADIRQ2 pin will be triggered to “H” and IADS_DONE flag (address 0x1C[7]) will be set to “1”. The measured data will be updated to CVIL_AD flag (address 0x48[15:0]) when ADIL_LATCH flag (address 0x0C[2]) is set to “1”. ADIRQ2 pin is cleared when ADIL_LATCH flag (address 0x0C[2]) is set to “1”. This flag is cleared to “0” after completion. IADS_DONE flag (address 0x1C[7]) is cleared by writing “1” to it.

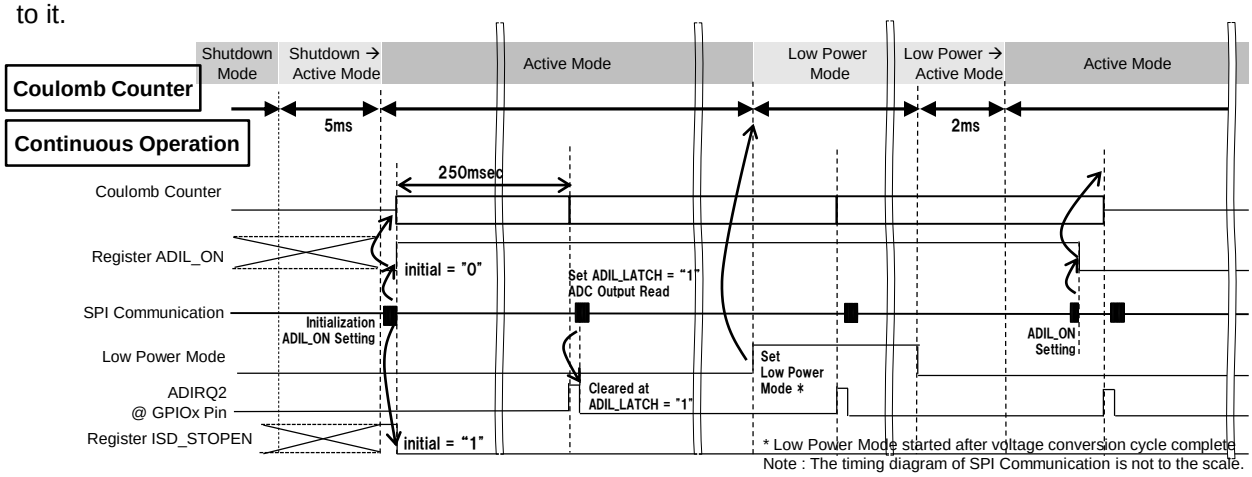


Fig.10.1.3 Example Coulomb Counter Timing Diagram

10.1.3 Enable HS and LS Current Simultaneous Measurement

In 1 Shot mode, when ISD_STOPEN at address 0x18[4] is set to “1”, LS current ADC cannot operate simultaneously when HS current ADC is in operation but instead sequentially after HS current ADC has completed. LS current ADC will reset when HS current ADC is in operation. When ISD_STOPEN at address 0x18[4] is set to “0”, LS current ADC can operate simultaneously with HS current ADC.

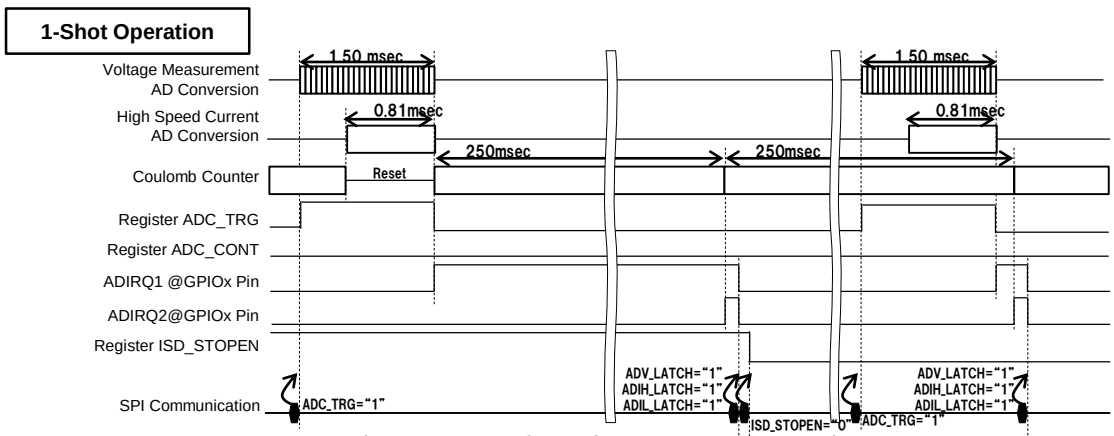


Fig.10.1.4 Waveform of ISD_STOPEN operation

Description of Functions

10. Current Measurement of SRP / SRN

10.2 Control Registers of Current Measurement

Table.10.2.1 shows the registers that control Current Measurement.

Table.10.2.1 Current Measurement Control Registers

Address	Function
0x01	Mode of Operation control related registers
0x04	FET Driver Operation Control registers
0x0C	ADC Operation registers
0x0D 0x0E 0x0F	GPIO1;2;3 control registers GPIO1;2;3 output control registers
0x18	ADC control register1
0x21	ADC/ALARM Status register
0x47	High speed current ADC measurement result register
0x48	Low speed current ADC measurement result register

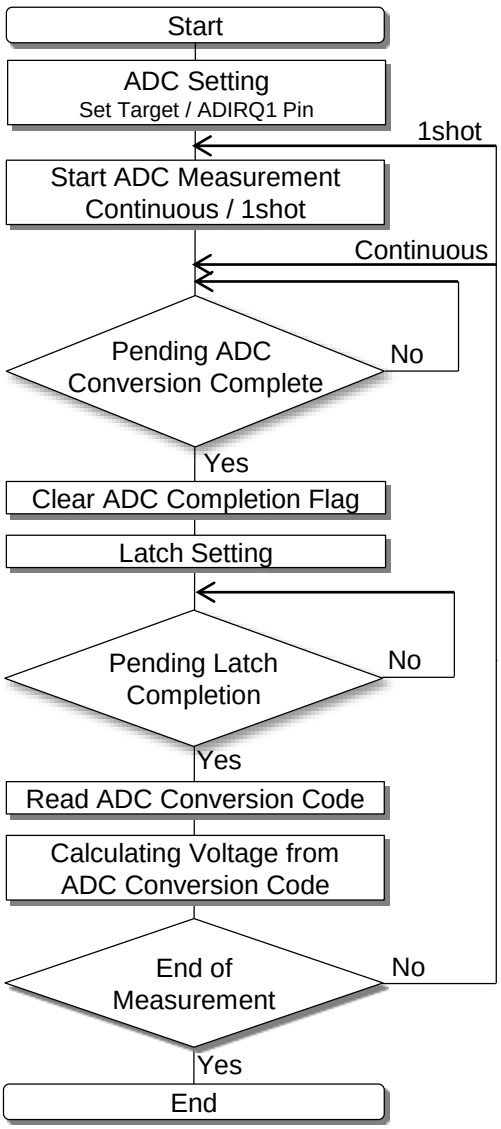
Description of Functions

10. Current Measurement of SRP / SRN

10.3 SRP / SRN Current Measurement Setting Procedure (High Speed / Low Speed)

10.3.1 SRP/SRN Current (High Speed) Measurement Setting Procedure

HS Current measurement uses the following setting.



■ADC Setting
Set the GPIO1SEL flag (address 0D[11:8]) to “0011” to output ADIRQ1. Set the GPIO1_NOE flag (address 0D[1]) to “0” to set GPIO1 as output.

■Start ADC Measurement
ADIH_ON Setting : Set ADSWHY_EN flag (address 0x18[13]) and ADIH_ON flag (address 0x18[0]) to “1”, start measurement in synchronize with the voltage measurement.

Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin : ADIRQ1 → “H” when measurement complete.
Using flag polling : Read IADH_DONE flag (address 0x1C[6]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write IADH_DONE flag (address 0x1C[6]) to “1” to clear this flag.

■Latch Setting
When write ADIH_LATCH flag (address 0x0C[1]) to “1”, latch Voltage measurement result for HS current register.
※ If it is cleared ADIRQ1 pin, write ADV_LATCH flag (address 0x0C[0]) to "1". It uses an interrupt of voltage ADC.

■Pending Latch Completion
Polling until ADIH_LATCH flag (address 0x0C[1]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read CVIH_AD register (0x47[15:0])

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from SRP/SRN current conversion table.10.3.1.

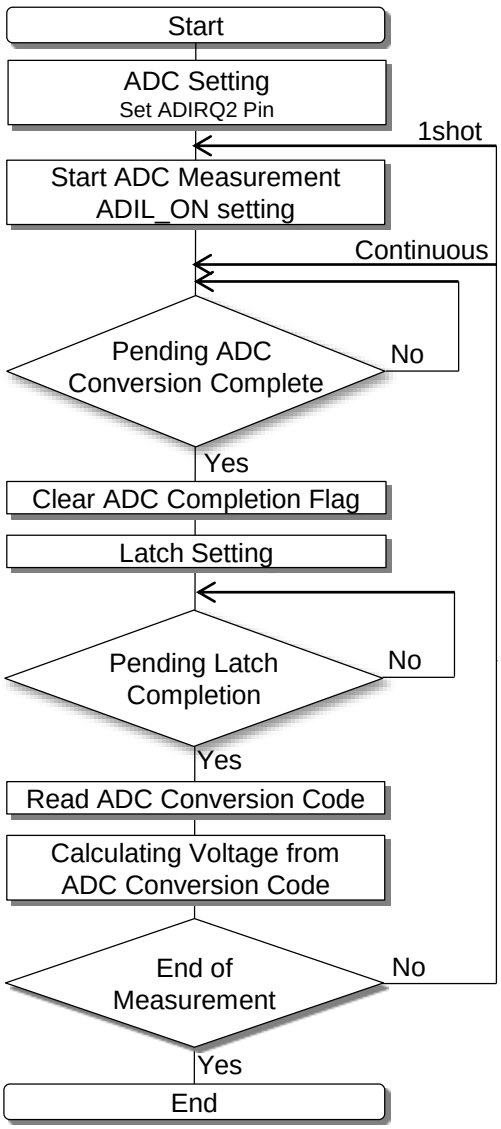
Description of Functions

10. Current Measurement of SRP / SRN

10.3 SRP / SRN Current Measurement Setting Procedure (High Speed / Low Speed)

10.3.2 SRP/SRN Current (Low Speed) Measurement Setting Procedure

LS Current measurement uses the following setting.



■ADC Setting
Set the GPIO2SEL flag (address 0x0E[11:8]) to “0100” to output ADIRQ2. Set the GPIO2_NOE flag (address 0x0E[1]) to “0” to set GPIO2 as output.

■Start ADC Measurement
ADIL_ON Setting : Set ADSWSD_EN flag (address 0x18[12]) and ADIL_ON flag (address 0x18[1]) to “1”, start measurement

■Pending ADC Conversion Completion
When using interrupt ADIRQ2 signal at GPIO2 pin : ADIRQ2 → “H” when measurement complete.
Using flag polling : Read IADS_DONE flag (address 0x1C[7]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write IADS_DONE flag (address 0x1C[7]) to “1” to clear this flag.

■Latch Setting
When write ADIL_LATCH flag (address 0x0C[2]) to “1”, latch Voltage measurement result for LS current register.

■Pending Latch Completion
Polling until ADIL_LATCH flag (address 0x0C[2]) become “0” or ADIRQ2 pin become “L”. Or wait for 48us.

■Reading ADC Conversion Code
Read CVIL_AD register (0x48[15:0])

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from SRP/SRN current conversion table.10.3.1.

Description of Functions

10. Current Measurement of SRP / SRN

10.3 SRP / SRN Current Measurement Setting Procedure (High Speed / Low Speed)

10.3.3 SRP/SRN Current Measurement Conversion Table

The full range and resolution of current measurement (High Speed / Low Speed) is shown below and listed in table below.

- Maximum input voltage : +179.994507 mV = 360 mV X (2^{15} – 1) / 2^{16}
- Minimum input voltage : -180 mV
- Resolution : 0.005493 mV = 360 mV / 2^{16}

Table.10.3.1 SRP/SRN Current Measurement Conversion Table

Analog level [mV] (typ)	Code	Digital output (CVIL_AD[15:0] / CVIH_AD[15:0])															
		MSB															LSB
		b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
179.994507	0x7FFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
0.005493	0x0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0.000000	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.005493	0xFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
-179.994507	0x8001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
-180.000000	0x8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

From the voltage between the SRP-SRN pins which has been calculated in the above,
The current flowing between the SRP-SRN pins can then be calculated.
The voltage between the SRP-SRN pins is V_{SRPN}.
Current = V_{SRPN} ÷ shunt resistor

Description of Functions

10. Current Measurement of SRP / SRN

10.1 V-I synchronized measurement function (VI sync)

In VI-Sync mode, this IC can measure current synchronously with individual cell voltage measurement. This synchronization allows user to better analyze individual cell impedance.
VI-Sync mode can be enabled by ADIH_CSYNC flag (address 0x18[5]) to “1”. User can select which cell to measure current synchronously to, by setting ADIH_CSYNC_SEL flag (address 0x1B[15:11]) 0x01 to 0x11 respectively. Fast speed current ADC will always measure at the selected cell slot and output synchronized voltage and current data into the output register in this mode.

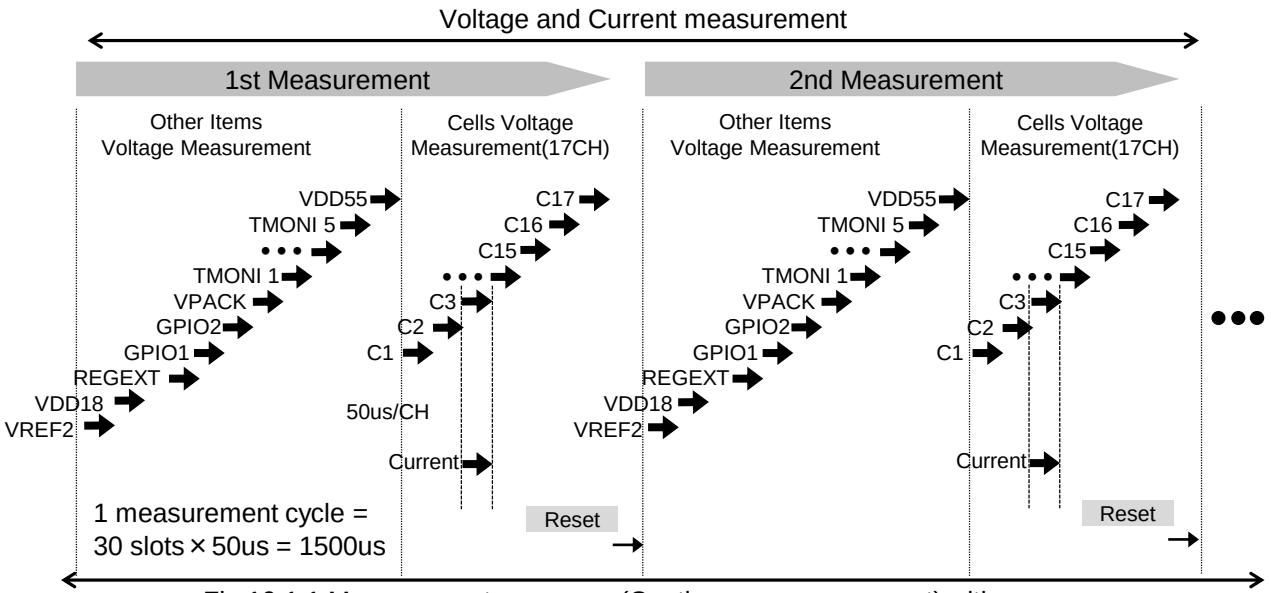


Fig.10.1.1 Measurement sequence (Continuous measurement) with VI-Sync measurement sequence (ADIH_CSYNC_SEL = 0x03)

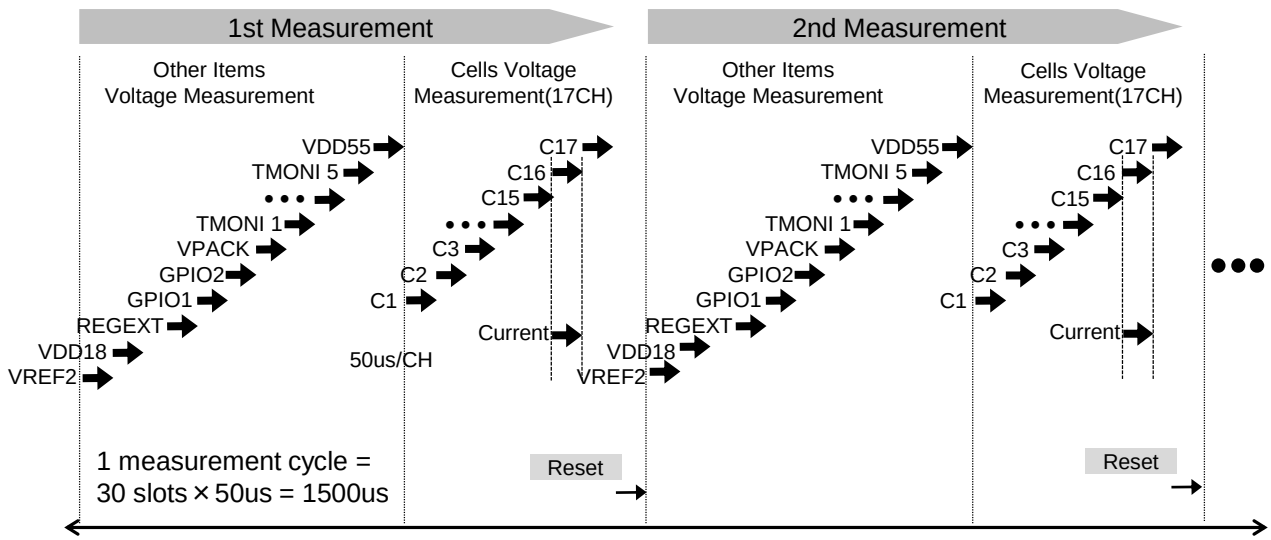


Fig.10.1.2 Measurement sequence (Continuous measurement) with VI-Sync measurement sequence (ADIH_CSYNC_SEL = 0x11)

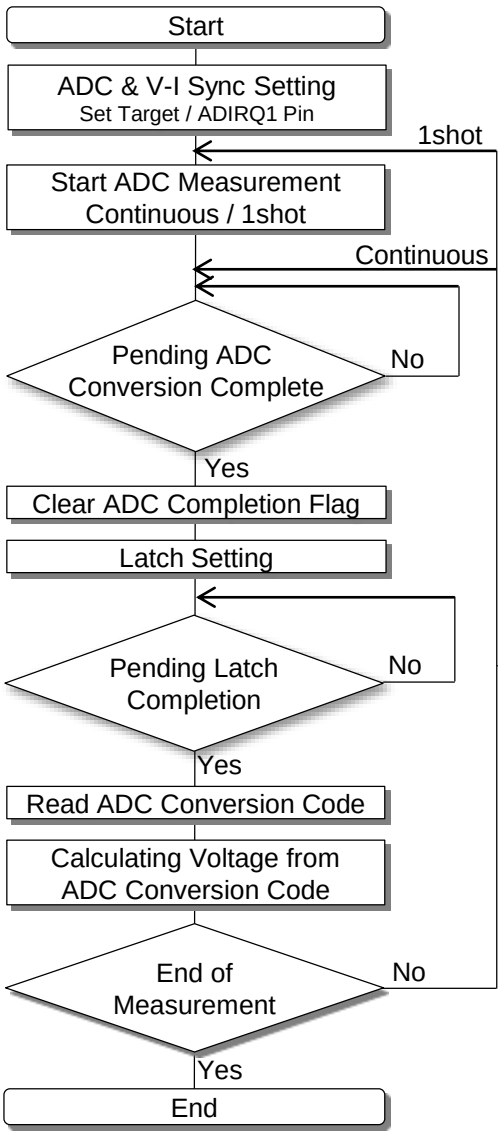
Description of Functions

10. Current Measurement of SRP / SRN

10.2 V-I synchronized measurement function (VI sync) Setting Procedure

Voltage across each cell (C1, C2 … C17) will be measured during voltage measurement cycle.
Fast speed current ADC will be measured at the selected voltage cell during the measurement cycle.

Cell Voltage use the following settings
- Set Measurement Target: Cell 1~17
- ADIQR1 Pin Setting
- Set the target VI sync channel



■ADC Setting
Set the CV[n]SEL flag (address 0x05[15:0] and address 0x06[0] to 0xFFFF, 0x0001 respectively to set measurement target.
Set the GPIO1SEL flag (address 0x0D[11:8]) to “0011” to output ADIRQ1.
Set the GPIO1_NOE flag (address 0x0D[1]) to “0” to set GPIO1 as output.
Set ADSWHY_EN flag (address 0x18[13]) and ADIH_ON flag (address 0x18[0]) to “1”

■VI-Sync Setting
Set ADIH_CSYNC flag (address 0x18[5]) to enable VI-Sync mode.
Set ADIH_CSYNC_SEL flag (address 0x1B[15:11]) to the cell number to synchronize current measurement to.

■Start ADC Measurement
Continuous Measurement : Set the ADC_CONT flag (address 0x01[15]) to “1” to start ADC measurement.
1shot Measurement : Set the ADC_TRG flag (address 0x0C[4]) to “1” to start ADC Measurement, this flag is auto cleared to “0” after measurement completed.

■Pending ADC Conversion Completion
When using interrupt ADIRQ1 signal at GPIO1 pin : ADIRQ1 → “H” when measurement complete.
Using flag polling : Read VAD_DONE flag (address 0x1C[5]), it become “1” when measurement complete.

■Clear of ADC Conversion Completion Flag
Write VAD_DONE flag (address 0x1C[5]) to “1” to clear this flag.

■Latch Setting
When write ADV_LATCH flag (address 0x0C[0]) to “1”, latch Voltage measurement result for CVn_AD register.
When write ADIH_LATCH flag (address 0x0C[1]) to “1”, latch Current measurement result for CVIH_AD register.

■Pending Latch Completion
Polling until ADV_LATCH flag (address 0x0C[0]) become “0” or ADIRQ1 pin become “L”. Or wait for 315ns.

■Reading ADC Conversion Code
Read CVn_AD register (address: 0x28-0x38)
Read CVIH_AD register (address: 0x47)

■Calculating Voltage from ADC Conversion Code
Calculate the voltage from Cell voltage conversion table.9.3.1.
Calculate the current from SRP/SRN current conversion table.10.3.1.

Description of Functions

11. Monitoring and Protection

11.1 Function Description of Monitoring and Protection

KA49517A is able to detect the abnormal cell voltage (Over Voltage / Under voltage) and abnormal current. The external NMOS FET can be turned OFF automatically according to abnormal status and register setting, which will be explained in this chapter.

Over Voltage / Under Voltage can only be detected in Active Mode. In Standby Mode, it operates differently. Refer to 11.3.1 for more details on cell voltage abnormality.

Over Current in Charge (OCC), Over Current in Discharge(OCD), Short Circuit in Discharge(SCD) can be detected in Active Mode and Standby Mode and is explained in 11.3.2.

Table.11.1.1 Abnormality status list

Abnormality status	Abnormality source	Active mode	Low Power or Standby mode
OV : Over Voltage	Cell voltage	YES	NA
UV : Under Voltage	Cell voltage	YES	NA
OCC : Over Current in Charge	SRP/SRN differential voltage	YES	YES
OCD : Over Current in Discharge	SRP/SRN differential voltage	YES	YES
SCD : Short Circuit in Discharge	SRP/SRN differential voltage	YES	YES

Description of Functions

11. Monitoring and Protection

11.1 Function Description of Monitoring and Protection

Alarm condition will be triggered when the detected abnormal condition remains longer than delay time and will be released when the release condition is met as shown in Table 11.1.2.
Current alarm should be released by external control (register access from MCU). Voltage alarm can be released automatically when the release condition met, i.e When voltage goes lower than the hysteresis setting. The setting for alarm detection consist of threshold value, delay time and hysteresis value.

Table.11.1.2 Abnormality detection setting list

Abnormality status		MIN	MAX	STEP	BITS	Release method
Over Voltage (OV)	Threshold	2.0V	4.5V	50mV	6	Automatically or External Control
	Delay time1	200ms	800ms	200ms	3	
	Delay time2	1.5s	6s	1.5s		
	Hysteresis Value	25mV	200mV	25mV	3	
Under Voltage (UV)	Threshold	0.5V	3.0V	50mV	6	
	Delay time1	200ms	800ms	200ms	3	
	Delay time2	1.5s	6s	1.5s		
	Hysteresis Value	25mV	200mV	25mV	3	
Over Current in Charge (OCC)	Threshold	5mV	120mV	5 mV	5	External Control
	Delay time	10ms	320ms	10ms	5	
Over Current in Discharge (OCD)	Threshold	10mV	320mV	10mV	5	
	Delay time	10ms	320ms	10ms	5	
Short Circuit in Discharge (SCD)	Threshold	20 mV	640 mV	20mV	5	
	Delay time	0 us	946 us	30.5 us	5	

When Alarm is triggered, the ALARM1/2 pin will be set to inform the abnormal status, two kinds of high-side FET control and digital output, which is used for such as Low side N-ch MOSFET or Relay etc, are provided. The operation is explained in detail from 11.4 onward.

Table.11.1.3 Protection control list

Control Pin	Usage
ALARM1	To inform MCU (ALARM1 for all alarm status is available)
ALARM2	
CHG	High Side N-ch MOSFET
DIS	
GPOH1	High Side P-ch MOSFET
GPOH2	
GPIO1	Digital Output Note: High voltage is CVDD Level.
GPIO2	
GPIO3	

Description of Functions

11. Monitoring and Protection

11.1 Function Description of Monitoring and Protection

Fig.11.1.1 describes a flow chart for Protection setting and control

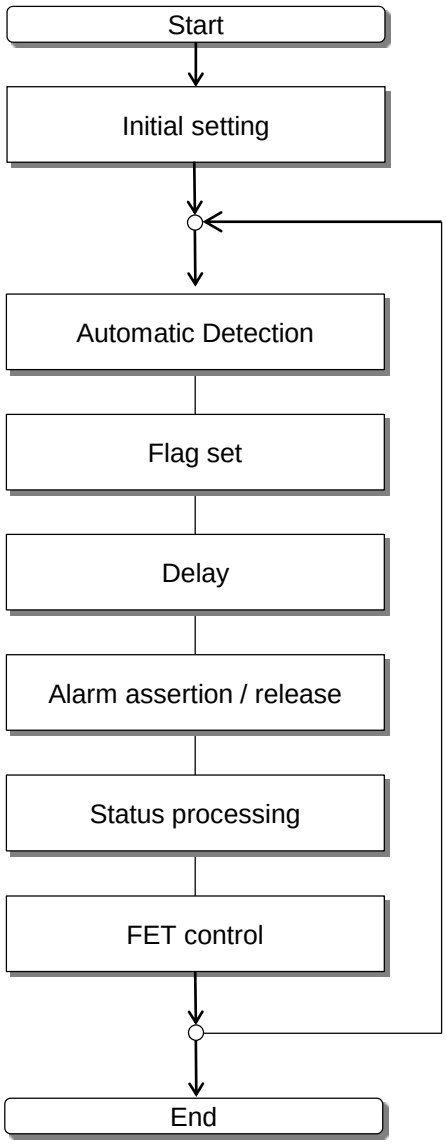


Fig.11.1.1 Protection setting Flow

■Initial setting
Enable or disable
Threshold value, delay time, hysteresis value
Protection methods for detected alarm

■Automatic Detection
Detect voltage abnormal by using measured voltage from ADC
Detect current abnormal by using analog comparator

■Flag set
Voltage Flag
OVn_F flag (address 0x22[15:0]; address 0x23[0])
UVn_F flag address 0x24[15:0]; address 0x25[0])
OVn_LF flag (address 0x4D[15:0]; address 0x4E[0])
UVn_LF flag (address 0x4F[15:0]; address 0x50[0])
Current Flag
SCD_F flag (address 0x21[7])
OCD_F flag (address 0x21[6])
OCC_F flag (address 0x21[5])
Status Flag
ST_OV flag (address 0x27 [1])
ST_UV flag (address 0x27 [0])

■Delay
if there is an abnormality or back to normal

■Alarm occurrence / release
Output ALARM1/2
“L”: Alarm asserted
“H”: Alarm released
Status
ST_SCD(address 0x21[15])
ST_OCD(address 0x21[14])
ST_OCC(address 0x21[13])

■Status Processing
Decide if change FET Control according to Alarm status and setting.

■FET control
Output FET control

Description of Functions

11. Monitoring and Protection

11.2 Protection Control Register

Protection control register is listed as Table.11.2.1.

Table.11.2.1 Protection control register list

Address	Description
0x01	Mode of Operation control related registers
0x04	FET Driver Operation Control registers
0x0A	OV/UV setting register
0x0B	OV/UV setting register2
0x0C	UV detection setting register
0x0C	OV detection register
0x12	Alarm control register1
0x13	Alarm control register2
0x14	Alarm control register3
0x0D 0x0E 0x0F	GPIO output selection GPIO Output control register
0x10	General purpose high-voltage output pin setting
0x21	Mode and status register
0x21	ALARM status register
0x22 0x23	OV status register
0x24 0x25	UV status register
0x4D 0x4E	OV detection flag register
0x4F 0x50	UV detection flag register
0x1C	FET driver status register

Description of Functions

11. Monitoring and Protection

11.3 Abnormality Detection

11.3.1 Cell Voltage Abnormality

Cell voltage abnormality consists of over charge (OV: Over Voltage) and over discharge (UV: Under Voltage)and is detected by using measured value from ADC.

The cell OV and UV detection can be enabled by setting OVMSKn flag (address 0x0C[6]) and UVMSKn flag (address 0x0C[7]) to “0” and disabled by setting these flag to “1”.

The setting for OV/UV abnormality detection consist of threshold limit, delay time and hysteresis value. The delay timer will start once the voltage is beyond the set threshold, and release threshold will be set by hysteresis value. The delay timer will be reset when the voltage meets the release condition. The registers to set threshold value, delay time and hysteresis value is summarized on Table 11.3.3.

If abnormality is detected, respective flag (OVn_F flag (address 0x22[15:0] and address 0x23[0]), OVn_LF flag (address 0x4D[15:0] and address 0x4E[0]), UVn_F flag (address 0x24[15:0] and address 0x24[0]), UVn_LF flag (address 0x4F[15:0] and address 0x50[0]) and ST_OV flag (address 0x27[1]) will be set to “1” immediately. OVn_F, UVn_F and ST_OV flag will be automatically cleared when released condition met. OVn_LF and UVn_LF flag are used for history check and is cleared only by writing “0000” to the register.

The reaction of Alarm pin and control output to cell voltage abnormality is explained from 11.4 onward. During Standby/Low Power Mode, as voltage ADC is not operating by default, OV/UV detection is not performed.
During intermittent Standby or Intermittent Low Power mode, ADC is operating at certain interval, so OV/UV detection is performed differently. Only when IC return to Active mode during intermittent operation, the voltage measurement will be carried out once and OV/UV detection can be carried out.

No OV Alarm assertion :
OV condition is less than delay time set

OV Alarm assertion & Release :
OV condition is more than delay time set

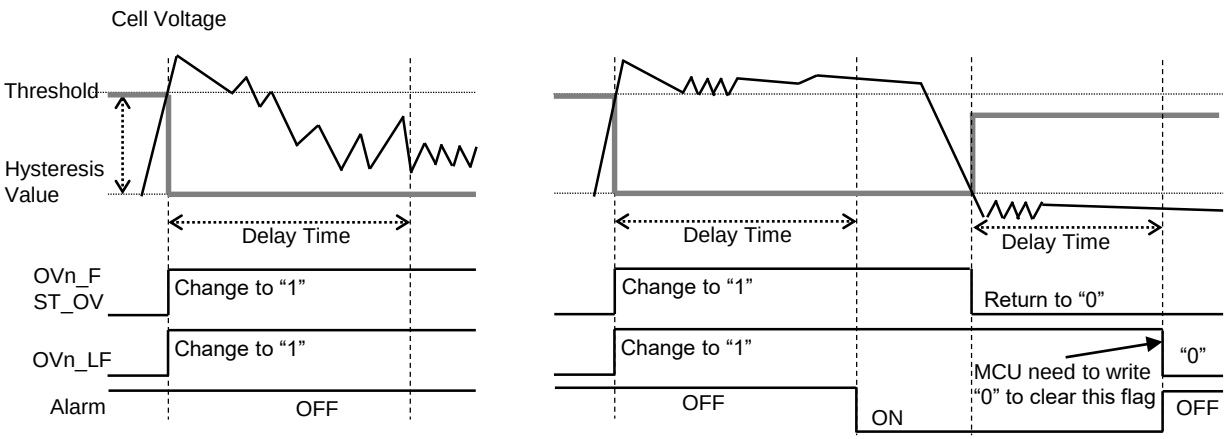


Fig.11.3.1 Block diagram of Cell voltage abnormality detection

Description of Functions

11. Monitoring and Protection

11.3 Abnormality Detection

11.3.1 Cell Voltage Abnormality

Table.11.3.1 Register for intermittent measurement in Standby/Low Power mode

Item	Register	flag	00	01; 10; 11
Automatic measurement in Intermittent Standby/ Low power mode	0x01 Bit 14~13	INTMSEL[1:0]	No measurement	Do interval measurement (interval timing depends on setting of INTMSEL
	0x01 Bit 15	ADC_CONT	No measurement	Continuous measurement mode

Note: Please set ADC_CONT to “1” when setting INTMSEL to “01/10/11”.

Table.11.3.2 OV/UV enable register

Item	register	flag	0	1
OV/UV Mask	OVMSK	OVMSKn	Detection Enable	Detection Disable
	UVMSK	UVMSKn	Detection Enable	Detection Disable

Table.11.3.3 OV/UV setting register 1

Item		Register	Address [bit]	0	1
Over Voltage (OV)	Detection Mask	OVMSK	0x0C [6]	Detection Enable	Detection Disable
	Abnormality happening	OVn_F	0x22 [15:0]; 0x23 [0]	Normal	Happening
	Abnormality history	OVn_LF	0x4D [15:0]; 0x4E [0]	Normal	Abnormality happened
	Status	ST_OV	0x27 [1]	Normal	Happening
Under Voltage (UV)	Detection Mask	UVMSK	0x0C [7]	Detection Enable	Detection Disable
	Abnormality happening	UVn_F	0x24 [15:0]; 0x25 [0]	Normal	Happening
	Abnormality history	UVn_LF	0x4F [15:0]; 0x50 [0]	Normal	Abnormality happened
	Status	ST_UV	0x27 [0]	Normal	Happening

Description of Functions

11. Monitoring and Protection

11.3 Abnormality Detection

11.3.1 Cell Voltage Abnormality

Table.11.3.4 OV/UV setting register 2

Item		register	flag	MIN	MAX	STEP	BITS
Over Voltage (OV)	Threshold	OUVCTL1	OVTH	2.0V	4.5V	50mV	6
	Delay time1	OUVCTL2	OV_DLY	200ms	800ms	200ms	3
	Delay time2	OUVCTL2	OV_DLY	1.5s	6s	1.5s	
	Hysteresis	OUVCTL2	OV_HYS	25mV	200mV	25mV	3
Under Voltage (UV)	Threshold	OUVCTL1	UVTH	0.5V	3.0V	50mV	6
	Delay time	OUVCTL2	UV_DLY	200ms	800ms	200ms	3
	Delay time2	OUVCTL2	OV_DLY	1.5s	6s	1.5s	
	Hysteresis	OUVCTL2	UV_HYS	25mV	200mV	25mV	3

Table.11.3.5 OV Threshold Setting value

Threshold [V] (typ)	Code	Setting value (OVTH[5:0])					
		MSB					LSB
		b5	b4	b3	b2	b1	b0
4.500	0x34	1	1	0	1	0	0
4.450	0x33	1	1	0	0	1	1
.	.		.	.	.	.	.
3.550	0x21	1	0	0	0	0	1
3.500	0x20	1	0	0	0	0	0
3.450	0x1F	0	1	1	1	1	1
.	.		.	.	.	.	.
2.050	0x03	0	0	0	0	1	1
2.000	0x02	0	0	0	0	1	0

Table.11.3.6 UV Threshold Setting value

Threshold [V] (typ)	Code	Setting value (UVTH[5:0])					
		MSB					LSB
		b5	b4	b3	b2	b1	b0
3.000	0x32	1	1	0	0	1	0
2.950	0x31	1	1	0	0	0	1
.	.		.	.	.	.	.
0.550	0x01	0	0	0	0	0	1
0.500	0x00	0	0	0	0	0	0

Description of Functions

11. Monitoring and Protection

11.3 Abnormality Detection

11.3.2 Current Abnormality

Current abnormality detection consists of Over Current in charge detection (OCC), Over Current in Discharge (OCD) and Short Current in Discharge(SCD). Current abnormality is detected by monitoring the differential voltage between SRP and SRN with analog comparator. Analog comparator will work in all modes except for Sleep and Shutdown mode.

Set the following register to "1" for enable and “0” for disable detection:

EN_CP flag (address 0x12[0]) EN_OCC flag (address 0x12[1])
EN_OCD flag (address 0x12[2]) EN_SCD flag(address 0x12[3])

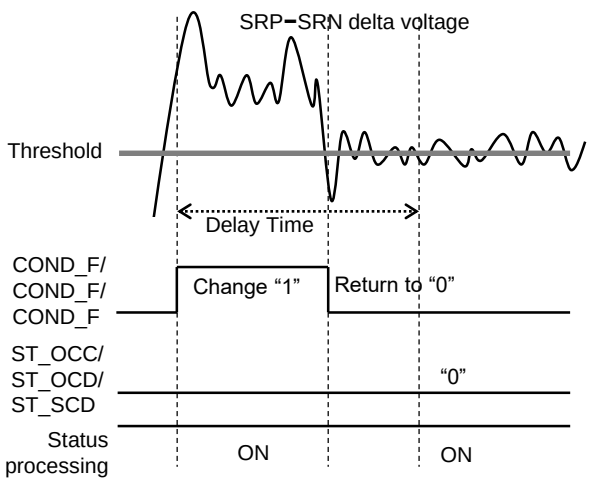
The setting for OCC/OCD/SCD abnormality detection consist of threshold value and delay time and is summarized on Table 11.3.8. There is no hysteresis value for current abnormality detection.
Delay timer will start to count once the current is beyond the threshold and will be cleared once the current goes under the threshold value.

When current abnormality is detected, these flags will be set to “1” :
OCC_F flag (address 0x21[5]), OCD_F flag (address 0x21[6]), SCD_F flag (address 0x21[7])
And when alarm is asserted after delay time, these flags will be set to “1” :
ST_OCC flag (address 0x21[13]), ST_OCD flag (address 0x21[14]), ST_SCD flag (address 0x21[15])

The reaction of Alarm pin and control output to current abnormality is explained from 11.4 onward.
The flag (OCC_F/OCD_F/SCD_F) will be clear automatically when current goes to normal.
The status (ST_OCC/ST_OCD/ST_SCD) will not be clear automatically, and writing "1" to the corresponding register to clear if it is needed.

No current abnormality Alarm :

Current abnormality is less than delay time set



Current abnormality alarm assertion :

Current abnormality is more than delay time set

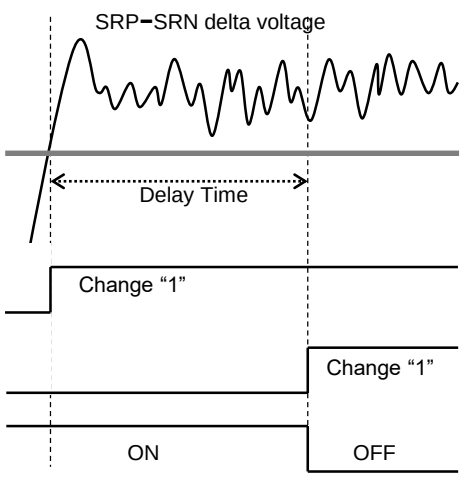


Fig.11.3.2 Example Current Alarm assertion & Control timing

Description of Functions

11. Monitoring and Protection

11.3 Abnormality Detection

11.3.2 Current Abnormality

Table.11.3.7 OCC/OCD/SCD enable register

Item	Address	flag	0	1
CP enable	0x12	EN_CP	Disable	Enable
OCC enable		EN_OCC	Disable	Enable *1
OCD enable		EN_OCD	Disable	Enable *1
SCD enable		EN_SCD	Disable	Enable *1

Note *1 : Only effective when *EN_CP* flag = “1”

Table.11.3.8 OCC/OCD/SCD setting register 1

Item		Address	flag	MIN	MAX	STEP	BITS
OCC	Threshold	0x13	OCC_D	5mV	120mV	5mV	5
	Delay time	0x14	OCC_DLY	10ms	320ms	10ms	5
OCD	Threshold	0x13	OCD_D	10mV	320mV	10mV	5
	Delay time	0x14	OCD_DLY	10ms	320ms	10ms	5
SCD	Threshold	0x13	SCD_D	20mV	640mV	20mV	5
	Delay time	0x14	SCD_DLY	0us	968.75us	31.25us	5

Table.11.3.9 OCC/OCD/SCD setting register 2

Item		Register	Address [bit]	0	1
OCC	Abnormality happening	OCC_F	0x21[5]	Normal	Happening
	Alarm happening	ST_OCC	0x21[13]	Normal	Alarm happened
OCD	Abnormality happening	OCD_F	0x21[6]	Normal	Happening
	Alarm happening	ST_OCD	0x21[14]	Normal	Alarm happened
SCD	Abnormality happening	SCD_F	0x21[7]	Normal	Happening
	Alarm happening	ST_SCD	0x21[15]	normal	Alarm happened

Description of Functions

11. Monitoring and Protection

11.3 Abnormality Detection

11.3.2 Current Abnormality

Table.11.3.10 OCC detection threshold

Threshold [mV] (typ)	Setting value (OCC_D[4:0])					
	Code	MSB				LSB
		b4	b3	b2	b1	b0
120	0x13	1	0	0	1	1
115	0x12	1	0	0	1	0
.	.	.	.	.	.	.
10	0x01	0	0	0	0	1
5	0x00	0	0	0	0	0

Table.11.3.11 OCD Threshold Setting value

Threshold [mV] (typ)	Setting value (OCD_D[4:0])					
	Code	MSB				LSB
		b4	b3	b2	b1	b0
320	0x1F	1	1	1	1	1
310	0x1E	1	1	1	1	0
.	.	.	.	.	.	.
20	0x01	0	0	0	0	1
10	0x00	0	0	0	0	0

Table.11.3.12 SCD Threshold Setting value

Threshold [mV] (typ)	Setting value (SCD_D[4:0])					
	Code	MSB				LSB
		b4	b3	b2	b1	b0
640	0x0F	1	1	1	1	1
620	0x0E	1	1	1	1	0
.	.	.	.	.	.	.
40	0x01	0	0	0	0	1
20	0x00	0	0	0	0	0

Description of Functions

11. Monitoring and Protection

11.4 Alarm 1 and Alarm 2 pin

These pins are used to inform the alarm assertion.
One-pin mode (ALARM1) and two-pin mode through selected GPIO pin (pin ALARM1 and pin ALARM2) are available.

ALARMSEL flag (Address 0x12[15]) is used to select pin mode.
ALARM pin goes “L” when the alarm is asserted.
ALARM1/2 will return to “H” when Alarm is released.

Voltage Measurement alarm can be released automatically.
Current Measurement alarm is released by writing “1” to ST_OCC/ST_OCD/ST_SCD flag register.

Table.11.4.1 Alarm assertion vs. ALARM1/2 output

	Alarm	ALARMSEL = 0	ALARMSEL = 1	
		ALARM1	ALARM1	ALARM2
Abnormal	OV/UV OCC/OCD	"L"	"H"	"L"
	SCD	"L"	"L"	"H"
Normal	-	"H"	"H"	"H"

Description of Functions

11. Monitoring and Protection

11.5 Alarm Status Processing for CHG, DIS and GPHO

11.5.1 Registers of Alarm Status Processing

In case of Alarm is asserted, the desired reaction of output control for NMOS FET (CHG and DIS) and GPOH is set/selected by the Status Processing Flags.
The desired reaction are : Enable or Disable the protection output, and Release mode.

For Current Measurement abnormality, the release method is only by external control.
It is cleared, when set FDRV_ALM_CLR flag (address 0x04[13]) to "1".

Table.11.5.1 Alarm Status Processing flag

Register	Address [bit]	Function
FDRV_ALM_SD	0x04 [15]	CHG/DIS FET and GPOH pins response to ALARM condition 1: CHG/DIS FET auto OFF and GPOH become value set, refer to specification section 11 CHG FET OFF : OV/UV/OCC DIS FET OFF : OV/UV/OCD/SCD 0: CHG/DIS FET and GPOH not response to ALARM condition (Default)
FDRV_ALM_RCV	0x04 [14]	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV) condition removed (when FDRV_ALM_SD = 1) with the following setting. 1: Depend on FDRV_ALM_CLR 0: Recover when ALARM(OV/UV) condition is removed (Default)
FDRV_ALM_CLR	0x04 [13]	CHG/DIS FET and GPOH pins recover when ALARM (OV/UV/OCD/OCC/SCD) condition removed (when FDRV_ALM_SD = 1 & FDRV_ALM_RCV=1) 1: CHG/DIS FET and GPOH pins recover 0: No change (Default) * This bit is not cleared automatically. * If ALARM condition continue and this bit is set, CHS/DIS FET remains OFF.

Description of Functions

11. Monitoring and Protection

11.5 Alarm Status Processing for CHG, DIS and GPHO

11.5.2 Alarm Status Timing

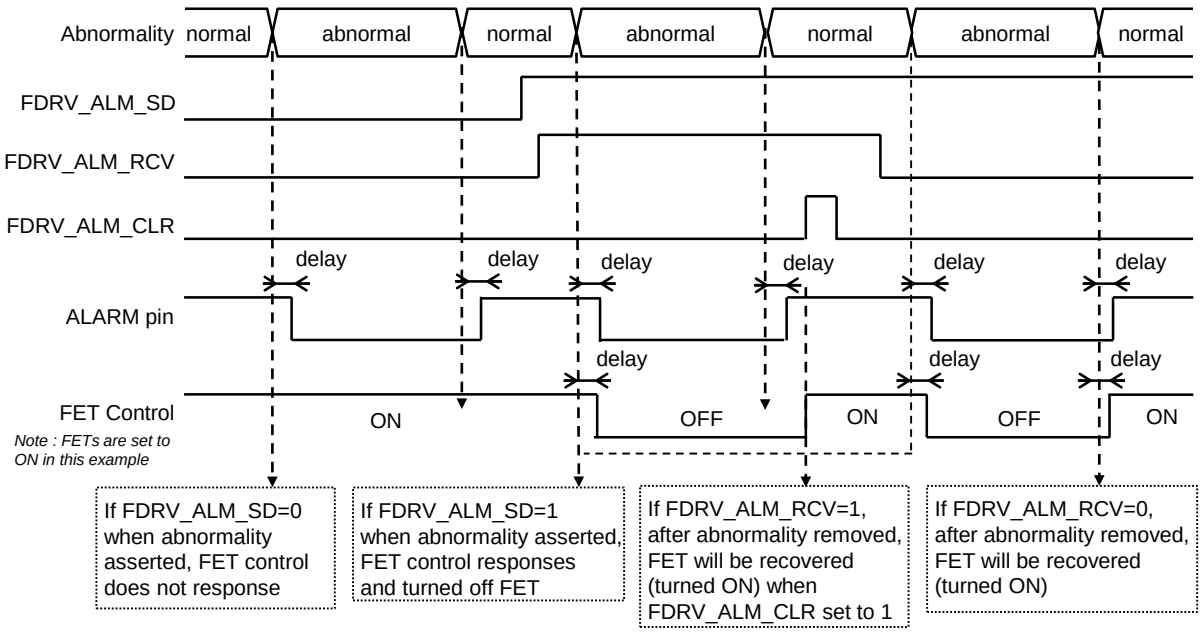


Fig.11.5.1 Status Processing timing for OV/UV

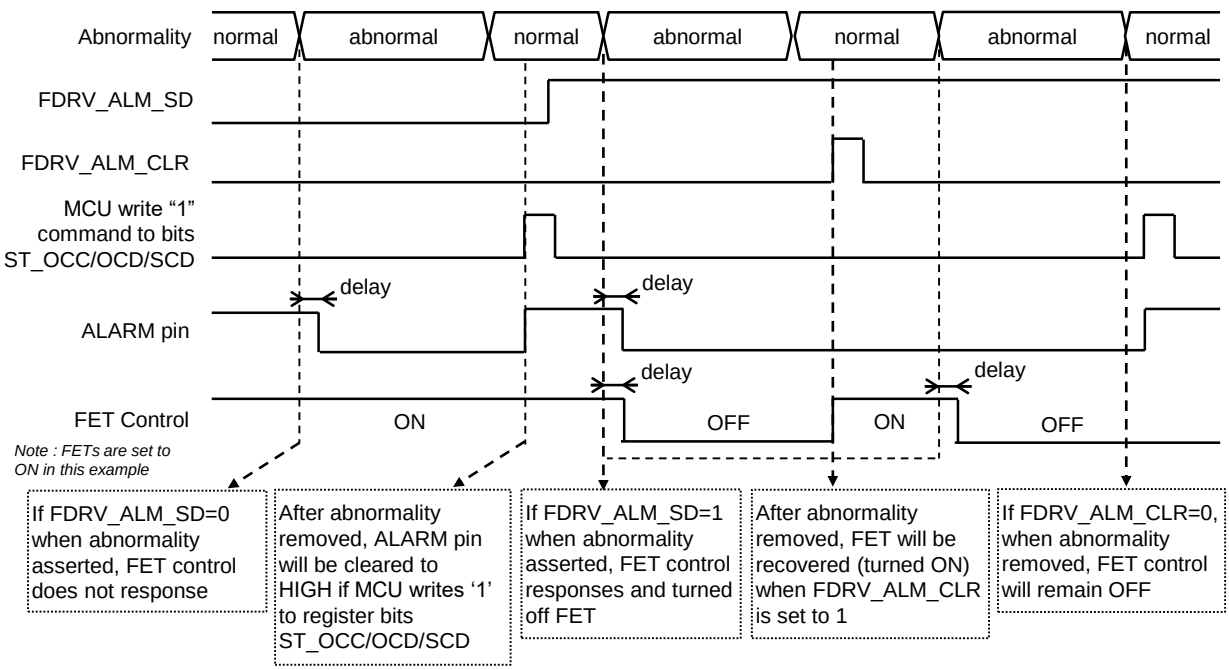


Fig.11.5.2 Status processing timing for OCC/OCD/SCD

Description of Functions

11. Monitoring and Protection

11.6 Control of Output Pin

11.6.1 CHG/DIS pin output

This protection function is for usage of High side N-ch MOSFET.
CHG/DIS pin is controlled according to FDRV_CHG_FET flag (address 0x04[10]) and FDRV_DIS_FET flag (address 0x04[9]) in normal condition, and when alarm is asserted it will be switched to the value described as the following list.
FDRV_OUVCTL flag (address 0x04[1]) is used to select CHG/DIS pin output when alarm is asserted.

If FET driver is in power reduction mode, Changes of CHG/DIS (On to OFF or OFF to On) will need very long time, so please shift to normal mode if you want change the CHG/DIS. But, when the protection control, it automatically return from the intermittent operation to the normal mode.

Table.11.6.1 Alarm assertion vs. CHG/DIS pin

	Alarm type	FDRV_OUVCTL=0 (default)		FDRV_OUVCTL=1	
		CHG	DIS	CHG	DIS
Abnormal	UV	-	OFF	OFF	OFF
	OV	OFF	-	OFF	OFF
	OCC	OFF	-	OFF	-
	OCD/SCD	-	OFF	-	OFF

11.6.2 GPOH1/2 pin output

This protection function is for usage of High side P-ch MOSFET.
GPOH1/2 pin is controlled according to *GPOH1_EN* flag (address 0x10[0]), *GPOH2_EN* flag (address 0x10[1]) in normal condition, and when alarm is asserted it will be switched to the value set by *GPOH1_ALM_ST* flag (address 0x10[4]), *GPOH2_ALM_ST* flag (address 0x10[5]) described as the following list.
GPOH_FET flag (address 0x10[2]) should be set to “1” to enable protection output for GPOH1/2.

Table.11.6.2 Alarm assertion vs. GPOH1/2

	Alarm type	GPOH1	GPOH2
Abnormal	OV/UV OCC/OCD/SCD	According to GPOH1_ALM_ST	According to GPOH2_ALM_ST
Normal	-	According to GPOH1_EN	According to GPOH2_EN

Description of Functions

11. Monitoring and Protection

11.6 Control of Output Pin

11.6.3 GPIO1/2 pin output

Setting Register for GPIO1/2 is the same with GPOH1/2.
GPIO output is enabled by Setting GPIO1SEL flag (address 0x0D[11:8]) to “0001” and GPIO2SEL flag (address 0x0E[11:8]) to “0010”
When alarm is triggered it will be switched to the value described as the following list.

Table.11.6.3 Alarm assertion vs. GPIO1/2 pin

	Alarm type	GPIO1	GPIO2
Abnormal	OV/UV OCC/OCD/SCD	According to GPOH1_ALM_ST flag	According to GPOH2_ALM_ST flag
Normal	-	According to GPOH1_EN flag	According to GPOH2_EN flag

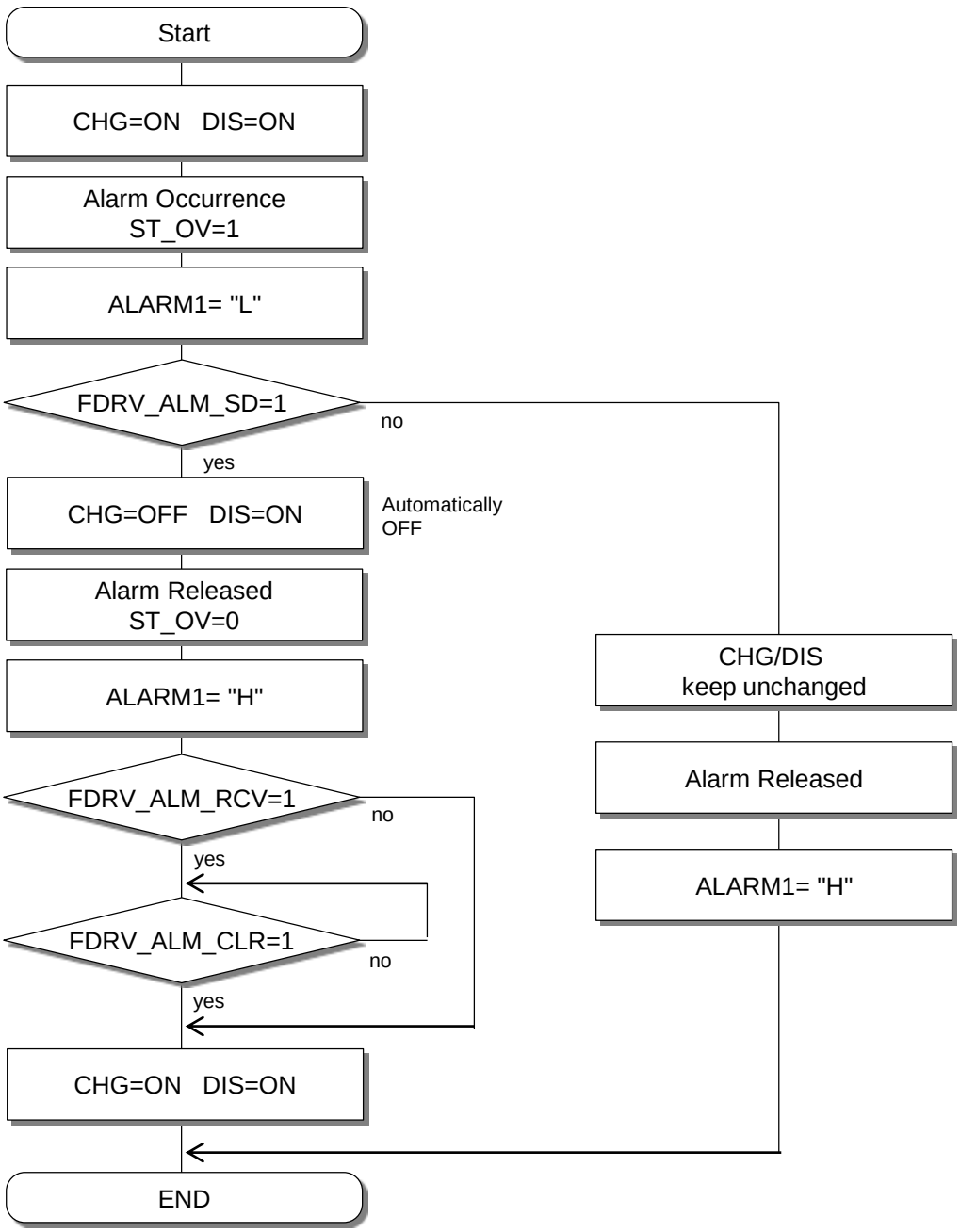
Description of Functions

11. Monitoring and Protection

11.7 Example for Control Output when Alarm Occurred

11.7.1 CHG/DIS Control Flow when OV Alarm Occurred

Case: ALARM1 only



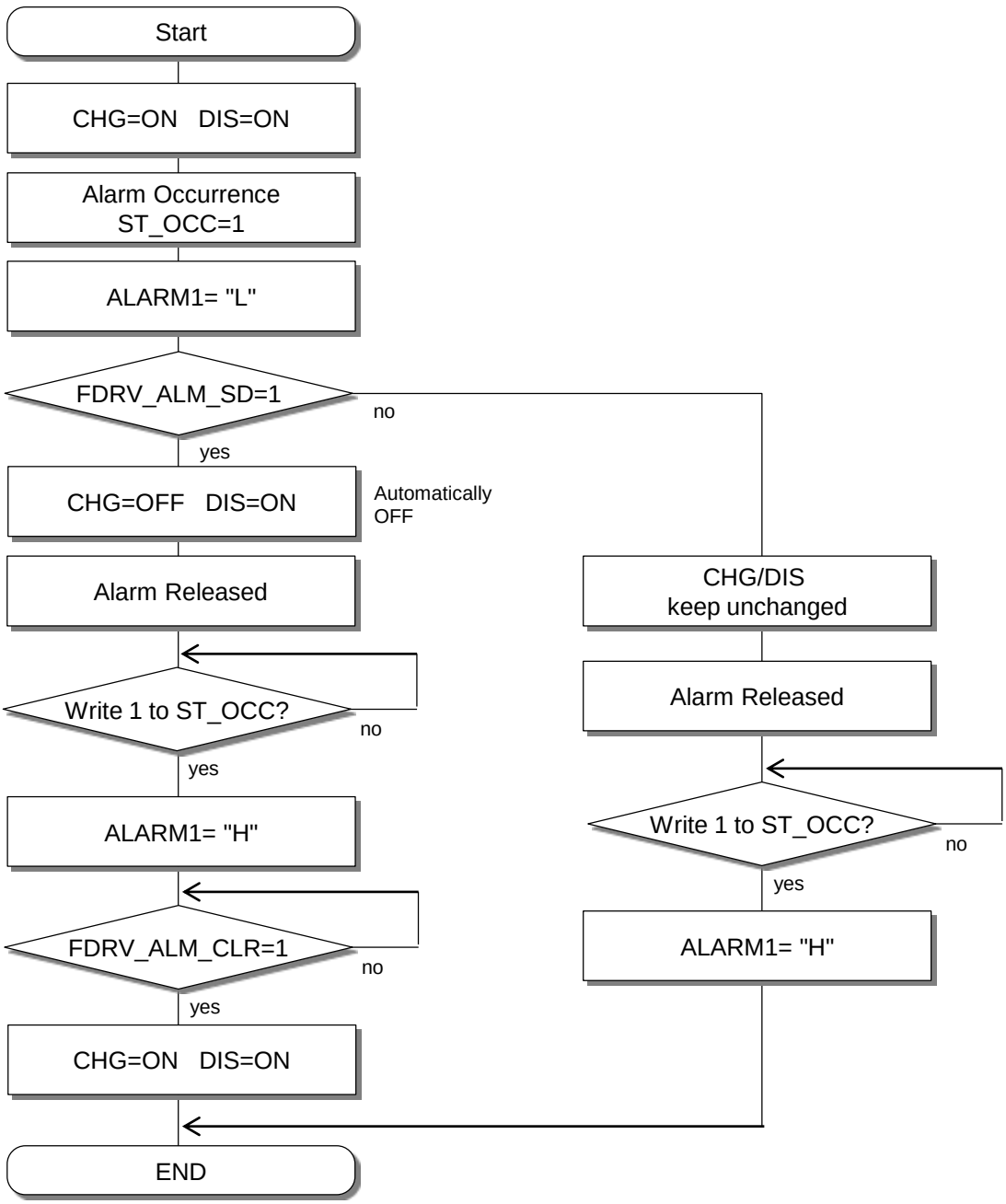
Description of Functions

11. Monitoring and Protection

11.7 Example for Control Output when Alarm Occurred

11.7.2 CHG/DIS Control Flow when OCC Alarm Occurred

Case: ALARM1 only



Description of Functions

12. Safety Diagnostic Features

12.1 CHG DIS NMOS FET Diagnostic Check

KA49517A has built-in with Charge FET(CHG FET) and Discharge FET (DIS FET) driver diagnostic function. This function allows user to check if FET driver, the charge pump output is operating correctly or not as a form of safety coverage. This function can be turned on via FET_DIAG_EN bit (address 0x1B[10]). CHG FET and DIS FET driver output can be checked in either ON mode or OFF mode. This is decided by FET_DIAG_SEL bit(address 0x1B[9:8]. MCU will need to ensure FET is ON/OFF mode via FDRV_CHG_FET bit (address 0x04[10]) and FDRV_DIS_FET bit (address 0x04[9]) before enabling the correct checking mode. Result of the check is stored in internal registers at address 0x21h[3:0] for MCU to read back. Please do note that FET detector check is only available when KA49517A is in Active mode of operation.

It is recommended for MCU to have sufficient wait time as indicated in the next 2 pages flow chart after FET_DIAG_EN has been turned ON before reading back the output flag to check the result. Refer to below register summary table for the details of this setting.

Table 12.1.1 FET Diagnostic registers settings

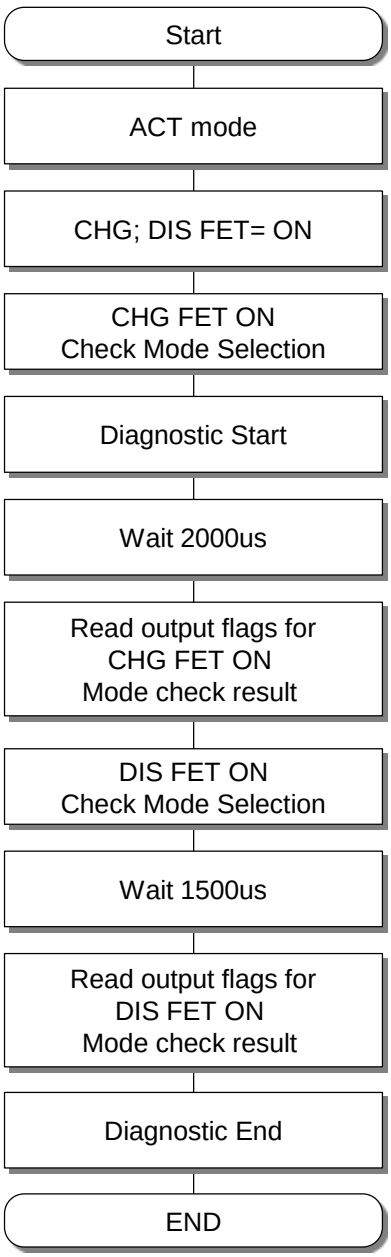
Register	Address [bit]	Function
FDRV_CHG_FET	0x04 [10]	External CHG FET (CFET)control 1: CFET ON 0: CFET OFF (Default)
FDRV_DIS_FET	0x04 [9]	External DISFET (DFET) control 1: DFET ON 0: DFET OFF (Default)
FET_DIAG_EN	0x1B [10]	Enable Diagnostic check for CFET and DFET 1: Enable 0: Disable (Default)
FET_DIAG_SEL	0x1B [9:8]	Diagnostic check for CFET and DFET 00 : CFET ON check (Default) 01 : DFET ON check 10 : CFET OFF check 11 : DFET OFF check
CFETON_F	0x21 [3]	Output bit to indicate CFET ON diagnostic check result 1: OK 0: NG (Default 0 if function is off)
CFETOFF_F	0x21 [2]	Output bit to indicate CFET OFF diagnostic check result 1: OK 0: NG (Default 0 if function is off)
DFETON_F	0x21 [1]	Output bit to indicate DFET ON diagnostic check result 1: OK 0: NG (Default 0 if function is off)
DFETOFF_F	0x21 [0]	Output bit to indicate DFET OFF diagnostic check result 1: OK 0: NG (Default 0 if function is off)

Description of Functions

12. Safety Diagnostic Features

12.1 CHG DIS NMOS FET Diagnostic Check

12.1.1 NMOS FET ON Diagnostic Check Control Flow



■Initial setting
KA49517A must be operating in Active mode of operation and CHG FET and DIS FET in ON mode
ST_ACT (address 0x1C[0]) = “1”
FDRV_DIS_FET;
FDRV_CHG_FET (address 0x04 [10:9]) =“11”

■CHG FET ON Mode check selection
To perform CHG FET ON mode check
FET_DIAG_SEL (address 0x1B[9:8]) =“00”

■Start Diagnostic Mode
Enable Diagnostic mode check
FET_DIAG_EN (address 0x1B[10])=“1”

■Delay
Ensure wait time of 2000us upon FET_DIAG_EN command sending before the completion of CHG FET ON diagnostic.

■Status Processing
Read back CFETON_F for the output of this check.
CFETON_F(address 0x21[3])
CFETON_F=“1” → OK; CFETON_F=“0” → NG

■DIS FET ON Mode check selection
To perform DIS FET ON mode check
FET_DIAG_SEL (address 0x1B[9:8]) =“01”

■Delay
Ensure wait time of 1500us upon FET_DIAG_SEL command sending before the completion of DIS FET ON diagnostic.

■Status Processing
Read back DFETON_F for the output of this check.
DFETON_F(address 0x21[1])
DFETON_F=“1” → OK; DFETON_F=“0” → NG

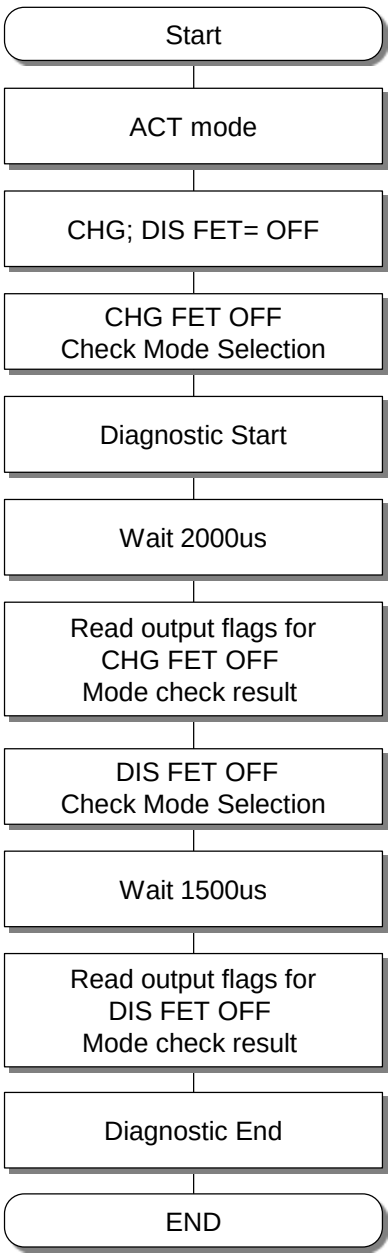
■Diagnostic End
Turn off diagnostic enable
FET_DIAG_EN (address 0x1B[10])=“0”

Description of Functions

12. Safety Diagnostic Features

12.1 CHG DIS NMOS FET Diagnostic Check

12.1.2 NMOS FET OFF Diagnostic Check Control Flow



■Initial setting
KA49517A must be operating in Active mode of operation and CHG FET and DIS FET in ON mode
ST_ACT (address 0x1C[0]) = “1”
FDRV_DIS_FET;
FDRV_CHG_FET (address 0x04 [10:9]) =“00”

■CHG FET OFF Mode check selection
To perform CHG FET OFF mode check
FET_DIAG_SEL (address 0x1B[9:8]) =“10”

■Start Diagnostic Mode
Enable Diagnostic mode check
FET_DIAG_EN (address 0x1B[10])=“1”

■Delay
Ensure wait time of 2000us upon FET_DIAG_EN command sending before the completion of CHG FET OFF diagnostic.

■Status Processing
Read back CFETOFF_F for the output of this check.
CFETOFF_F(address 0x21[2])
CFETOFF_F=“1” → OK; CFETON_F=“0” → NG

■DIS FET ON Mode check selection
To perform DIS FET OFF mode check
FET_DIAG_SEL (address 0x1B[9:8]) =“11”

■Delay
Ensure wait time of 1500us upon FET_DIAG_SEL command sending before the completion of DIS FET ON diagnostic.

■Status Processing
Read back DFETOFF_F for the output of this check.
DFETOFF_F(address 0x21[20)
DFETOFF_F=“1” → OK; DFETOFF_F=“0” → NG

■Diagnostic End
Turn off diagnostic enable
FET_DIAG_EN (address 0x1B[10])=“0”

Description of Functions

12. Safety Diagnostic Features

12.2 Current ADC Diagnostic Check

Both the high speed (HS) and low speed (LS) current ADC can undergo self diagnostic check when its diagnostic function check is turned ON. In diagnostic mode, current ADC sensing will be connected to a fix 100mV internal reference voltage instead of to SRP and SRN pins.

When DIAG_IHY_EN=1 (address 0x1B[6]); fast speed current ADC will finish its existing measurement slot before enabling and entering diagnostic mode. Likewise for slow speed current ADC, When DIAG_ISD_EN="1"(address 0x1B[5]); Slow speed current ADC will finish its existing measurement slot before enabling and entering diagnostic mode.

It is recommended to wait for 2 ADIRQ1/ADIRQ2 measurement completion interrupt signal after issuing DIA_IHY_EN or DIAG_ISD_EN signal before reading out the diagnostic measurement output at the respective output registers. Refer to chapter 10 for current ADC measurement procedure.

When fast speed current ADC measurement is completed, IADH_DONE flag (address 0x1C[6]) will be set to "1", and the measured data is latched to CVIH_AD flag (address 0x47[15:0]) when ADIH_LATCH flag (address 0x0C[1]) is set to "1", this ADIH_LATCH flag is cleared to "0" after completion. IADH_DONE flag (address 0x1C[6]) is cleared by write "1" to it.

When slow speed current ADC measurement is completed, IADS_DONE flag (address 0x1C[7]) will be set to "1". The measured data will be updated to CVIL_AD flag (address 0x48[15:0]) when ADIL_LATCH flag (address 0x0A[2]) is set to "1". ADIRQ2 pin is cleared when ADIL_LATCH flag (address 0x0A[2]) is set to "1". This flag is cleared to "0" after completion. IADS_DONE flag (address 0x1C[7]) is cleared by write "1" to it.

By reading back the ADC result at CVIH_AD (address 0x47[15:0]) and CVIL_AD(address 0x48[15:0]) after diagnostic measurement, user can check if the internal current ADC is functioning correctly or not as a form of diagnostic check. The value decoded should be around +100mV for both high speed and slow speed current ADC to ensure proper operation. Current diagnostic check value will be able to be measured by internal current ADC to be within ±10mV from 100mV during normal operation.

Refer to table 12.2.1 for registers setting summary table for this mode.

Description of Functions

12. Safety Diagnostic Features

12.2 Current ADC Diagnostic Check

12.2.1 Registers Setting of Current ADC Diagnostic Check

Table 12.2.1 HS / LS Current ADC Diagnostic registers settings

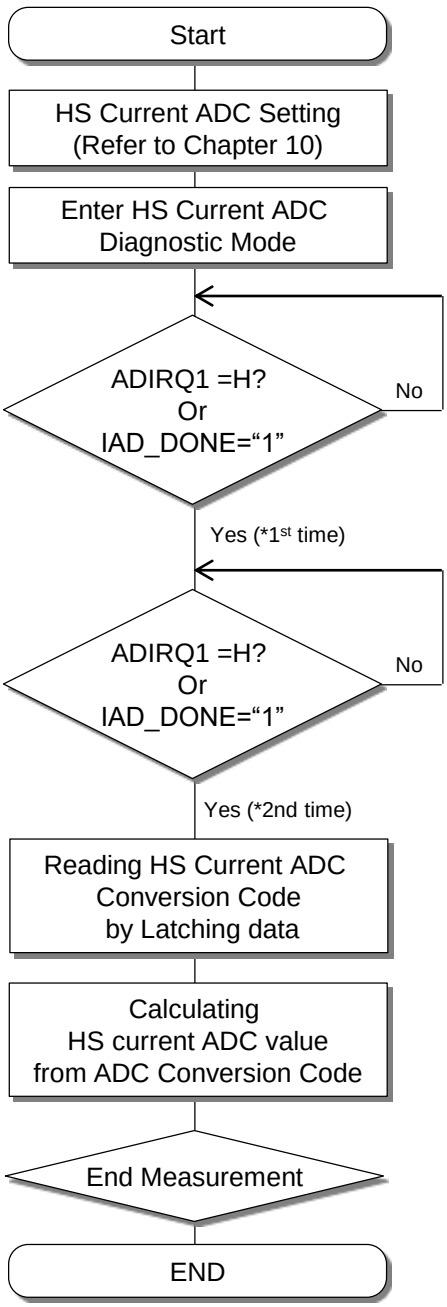
Register	Address [bit]	Function
ADIH_ON	0x18 [0]	Enable High-speed current ADC operation 1: Enable 0: Disable (Default)
ADIL_ON	0x18 [1]	Enable Low-speed current ADC operation 1: Enable 0: Disable (Default)
DIAG_IHY_EN	0x1B [6]	Diagnosis for High Speed Current ADC 1: Enable 0: Disable (Default)
DIAG_ISD_EN	0x1B [5]	Diagnosis for Low Speed Current ADC 1: Enable 0: Disable (Default)
CVIH_AD[15:0]	0x47 [15:0]	High-speed (HS) current ADC Measurement output value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V 0xFFFF: -0.005493mV ～ 0x8001: -179.994507mV Measured voltage = 2's complement data * 360mV/2^16 0x8000: -180mV Voltage/step = 0.005493mV
CVIL_AD[15:0]	0x48 [15:0]	Low-speed current ADC measurement output value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V 0xFFFF: -0.005493mV ～ 0x8001: -179.994507mV Measured voltage = 2's complement data * 360mV/2^16 0x8000: -180mV Voltage/step = 0.005493mV

Description of Functions

12. Safety Diagnostic Features

12.2 Current ADC Diagnostic Check

12.2.2 High Speed (HS) Current ADC Diagnostic Check Flow Chart



■ADC Setting for normal High Speed (HS) current measurement. Refer to chapter 10 for this settings.

When using interrupt ADIRQ1 signal at GPIOx pin : ADIRQ1 → "H" when measurement complete. ADIRQ1 signal will be cleared to "L" once the data has been latched for reading by the MCU by writing ADIH_LATCH bit (address 0x0C[1])="1"

When using flag polling : Read IADH_DONE flag (address 0x1C[6]), it become "1" when measurement complete. Write IADH_DONE flag (address 0x1C[6]) to "1" to clear this flag after the required data has been acquired.

■Entering Diagnostic check for HS current ADC

Write DIA_IHY_EN (address 0x1B[6])="1" to enter diagnostic mode for HS current ADC. After sending DIA_IHY_EN="1", it will take the second completion cycle indication at ADIRQ1 or IAD_DONE flags before diagnostic result is completed.

Subsequently the next Completion cycle indication will be diagnostic check result as well until diagnostic mode is exited.

■ Recording the data of diagnostic check result for HS current.

Result of diagnostic check for HS current ADC can be read back at the same HS current ADC output registers, CVIH_AD[15:0] (address 0x47[15:0])

Since 100mV is fix for this measurement, user should expect an equivalent current measurement value conversion of 100A to know that the diagnostic result is a pass.

■Exiting Diagnostic check for HS current ADC

To exit diagnostic mode for HS current ADC, user will need to write into DIA_IHY_EN bit (address 0x1B[6])="0"

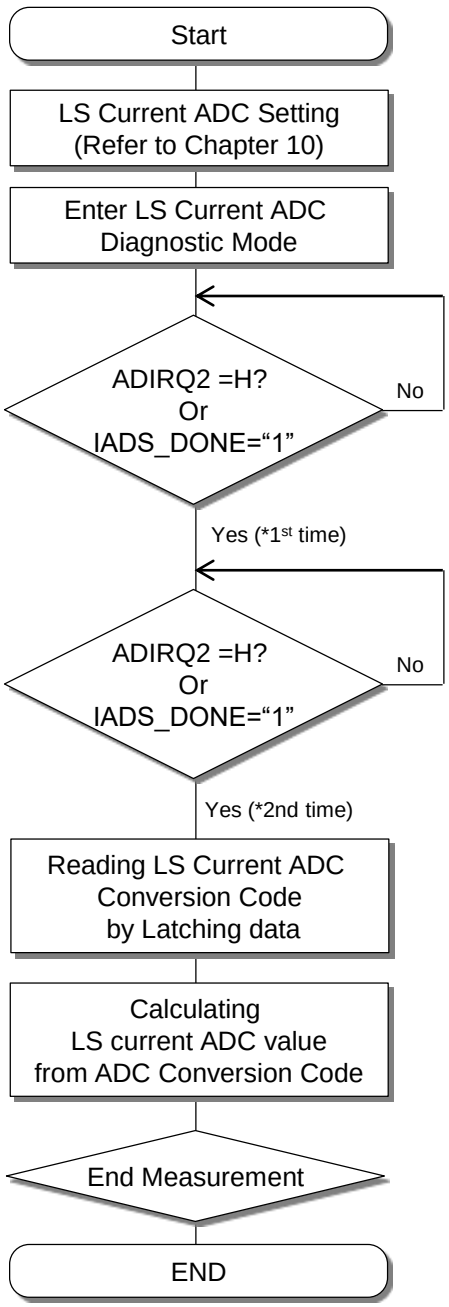
Similar to entering, only data after the second completion cycle indication at ADIRQ1 or IADH_DONE flag after sending DIA_IHY_EN="0" reflects the actual cell current measurement output.

Description of Functions

12. Safety Diagnostic Features

12.2 Current ADC Diagnostic Check

12.2.3 Low Speed (LS) Current ADC Diagnostic Check Flow Chart



■ADC Setting for normal Low Speed (LS) current measurement. Refer to chapter 10 for this settings.
When using interrupt ADIRQ2 signal at GPIOx pin : ADIRQ2 → "H" when measurement complete. ADIRQ2 signal will be cleared to "L" once the data has been latched for reading by the MCU by writing ADIL_LATCH bit (address 0x0C[2])="1"

When using flag polling : Read IADHS_DONE flag (address 0x1C[7]), it become "1" when measurement complete. Write IADHS_DONE flag (address 0x1C[7]) to "1" to clear this flag after the required data has been acquired.

■Entering Diagnostic check for LS current ADC
Write DIA_ISD_EN (address 0x1B[5])="1" to enter diagnostic mode for LS current ADC. After sending DIA_ISD_EN="1", it will take the second completion cycle indication at ADIRQ2 or IADS_DONE flags before diagnostic result is completed.

Subsequently the next Completion cycle indication will be diagnostic check result as well until diagnostic mode is exited.

■ Recording the data of diagnostic check result for LS current.
Result of diagnostic check for LS current ADC can be read back at the same LS current ADC output registers, CVIL_AD[15:0] (address 0x48[15:0])

Since 100mV is fix to this measurement. User should expect an equivalent current measurement value conversion of 100A to know that the diagnostic result is a pass.

■Exiting Diagnostic check for LS current ADC
To exit diagnostic mode for LS current ADC, user will need to write into DIA_ISD_EN bit (address 0x1B[5])="0"

Similar to entering, only data after the second completion cycle indication at ADIRQ2 or IADHS_DONE flag after sending DIA_ISD_EN="0" reflects the actual cell current measurement output.

Description of Functions
12. Safety Diagnostic Features

12.3 Regulator Diagnostic Check

Internal regulators inside KA49517A are measured by digital voltage ADC as well as analog comparator in the IC. This data are measured and monitored against possible over or under voltage. In the event over or under voltage is determined, respectively output registers will be updated accordingly for users to know any possibilities of abnormal voltages. This also serves as a form of diagnostic check for all internal regulator in the IC. In the event that OVP_F_SET bit (address 0x11[14]) is set to 0, IC will also enter shutdown mode when analog OV flag is registered at VDD55 or VDD18 regulator. Refer to below table

Table 12.3.1 Regulators ADC Diagnostic registers settings

Register	Address [bit]	Function
HBIAS1A	0x26 [8]	VDD18 Analog OV Flag 1: OV detected (>2.25V) 0: OV not detected
HBIAS1D	0x26 [7]	VDD18 Digital OV Flag 1: OV detected (>1.93V) 0: OV not detected
LBIAS1D	0x26 [6]	VDD18 Digital UV Flag 1: UV detected (<1.77V) 0: UV not detected
HBIAS2A	0x26 [5]	REG_EXT Analog OV Flag 1: OV detected (>6V/4V/3V) 0: OV not detected
HBIAS2D	0x26 [4]	REG_EXT Digital OV Flag 1: OV detected (>5.3V/3.6V/2.8V) 0: OV not detected
LBIAS2D	0x26 [3]	REG_EXT Digital UV Flag 1: UV detected (<4.7V/3V/2.2V) 0: UV not detected
HBIAS3A	0x26 [2]	VDD55 Analog OV Flag 1: OV detected (>6V) 0: OV not detected
HBIAS3D	0x26 [1]	VDD55 Digital OV Flag 1: OV detected (>5.8V) 0: OV not detected
LBIAS3D	0x26 [0]	VDD55 Digital UV Flag 1: UV detected (<5.2V) 0: UV not detected
OVP_F_SET	0x11 [14]	Transition to shutdown when abnormal high voltage is detected at VDD55/VDD18 1: No change (Default) 0: Shutdown immediately
OVP_F_SET_ REGEXT	0x20 [2]	Transition to shutdown when abnormal high voltage is detected at REGEXT 1: No change (Default) 0: Shutdown immediately
UVP_F_SET_ REGEXT	0x20 [1]	Transition to shutdown when abnormal low voltage is detected at REGEXT 1: No change (Default) 0: Shutdown immediately

Description of Functions

12. Safety Diagnostic Features

12.4 VREF Diagnostic Check

Internal reference voltage, VREF2 is measured by the voltage ADC and compare by digital comparator in the IC. VREF2 used as reference voltages for slow speed current ADC in the IC.

By measuring VREF2 using voltage ADC which has reference using VREF1, user will be able to know if this 2 references voltage ratio remain constant or not. In normal circumstance, the ratio should stay the same. In the event either VREF1 or VREF2 has changed, it can be detected by the measurement of VREF2 voltage as well as the OV and UV flag of VREF2. This can serve as diagnostic check in case either reference voltage has changed. Each reference voltages are 0.9V. VREF2 should be able to be measured by internal voltage ADC to be within ±50mV from 0.9V during normal operation.

In the event these voltages has been detected as over voltage (OV) or under voltage (UV), internal register flags will be updated accordingly to serve as a diagnostic check against abnormalities.

Refer to below table 12.4.1 for the register setting of this function.

Table 12.4.1 VREF ADC Diagnostic registers settings

Register	Address [bit]	Function
HVREF2	0x26 [10]	VREF2 OV Flag 1: OV detected (>1.2V) 0: OV not detected
LVREF2	0x26 [9]	VREF2 UV Flag 1: UV detected (<0.6V) 0: UV not detected

Description of Functions

12. Safety Diagnostic Features

12.5 Measurement Sequence Diagnostic Check

Voltage ADC follows a certain sequence during measurement by using multiplexing technique. In the event the sequence is not following the designed sequence, MUX1A_F flag will output a “1” to signify abnormities. Table 12.5.1 below shows the status register for anomaly detection of the voltage measurement sequence. For the details of sequence function, see chapter 9, Voltage Measurement functions.

Table 12.5.1 ADC Sequence Diagnostic registers settings

Register	Address [bit]	Function
MUX1A_F	0x21 [10]	Data acquisition system, process anomaly detection • Compare the selected measurement target between the data acquisition system to detect any abnormality in the voltage measurement sequence Error for sequence control counter measurement system diagnostic check 1: Abnormal 0: Normal

Description of Functions

12. Safety Diagnostic Features

12.6 Internal Clocks Diagnostic Check

KA49517A has 2 internal clocks to be used for internal signal generation. Both clock signals can be output through the required GPIO pins. The clocks can be divided down to lower frequency before being output to the selected GPIO pins. MCU will then be able to check IC internal clock against a known system clock. In the event there is abnormalities to IC clock, it can be easily checked by MCU.

Table 12.6.1 below shows the status register to output the clock for diagnostic check. For the details of output signal through GPIO pins, see chapter 6, on GPIO settings.

Table 12.6.1 Internal Clocks Diagnostic registers settings

Register	Address [bit]	Function
OSCH_DIV	0x11 [9]	Setting of GPIOx output dividing frequency of OSCH 1: 1/512 = 40kHz (Default) 0: 1/128 = 160kHz
OSCL_DIV	0x11 [8]	Setting of GPIOx output dividing frequency of OSCL 1: 1/64 = 4.096kHz (Default) 0: 1/1 = 262.144kHz

Description of Functions

12. Safety Diagnostic Features

12.7 Description of Open Connection Detection

KA49517A has built-in with open connection detection function.
This function can be turned ON during Active Mode, and Standby and Low power Mode .

Each pins has the current source shown in Fig.12.7.1 .
C0, C1 pins have the current source (Typ.40μA) pushing to the outside of the IC from the pin.
C2 ~ C17 pins have the current sink (Typ.37μA) pulling into the IC from the pin.
By using these current sources when the open detect function is ON, user can judge whether the wires are
open or not by comparing the cell voltages before and after this function.
User can select the pin for detecting by the flag and select multiple detection at the same time.

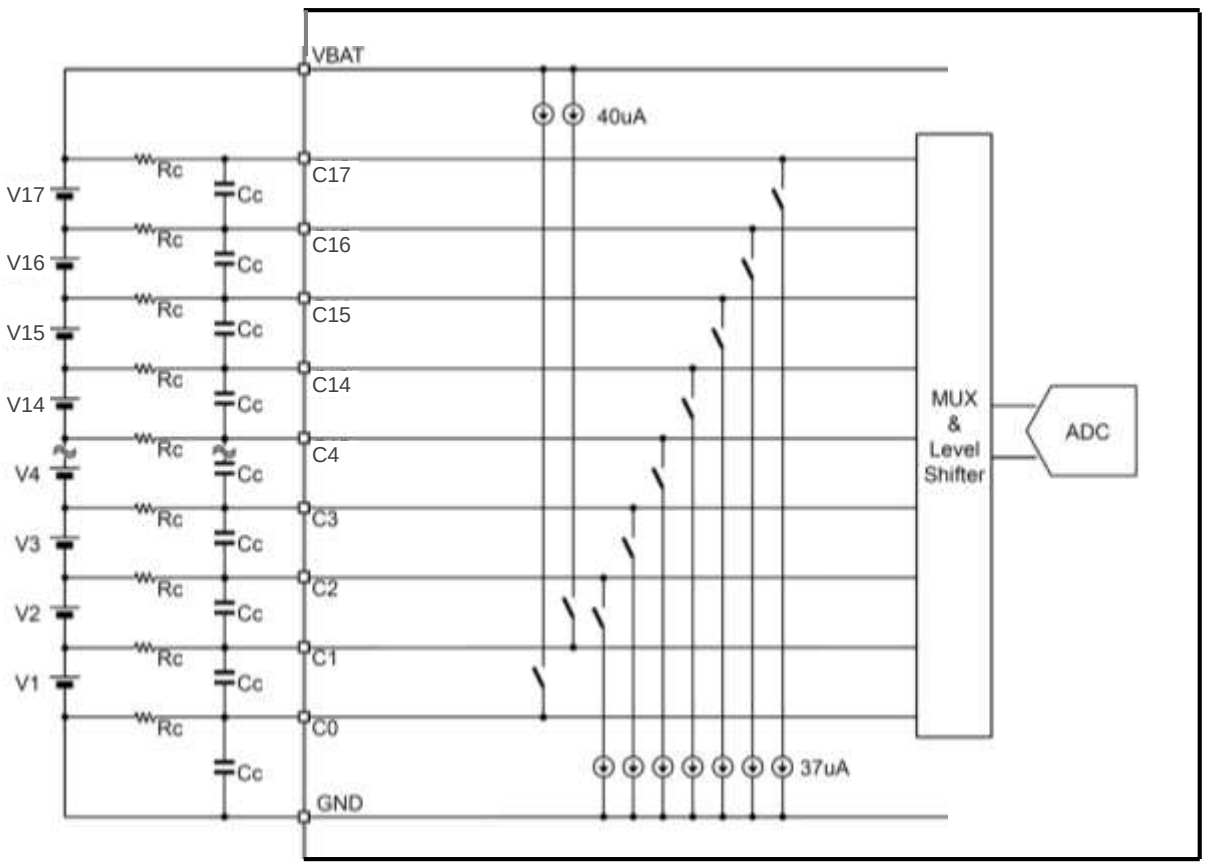


Fig.12.7.1 Open Connection Detection circuit

Description of Functions

12.7 Description of Open Connection Detection

Open Detection at C0,C1 pins

First, you shall obtain the cell voltage immediately before the open detection function.

If open detection function is done when wire is normal, the voltage of C2 pin decreases and the voltage of C0 , C1 pins shown in Fig.12.7.2(a) increase.

The decrease of voltage at C2 pin is obtained from the multiplication the sink current and the resistance (Rc) at C2 pin.

The increase voltage of C1 and C0 pins are obtained from the multiplication the source current and the resistance (Rc) at C1 and C0 pins.

If C1 pin is open shown in Fig.12.12(b), the voltage of C1 pin increases rather than normal condition by the pushing current and then V1 increase.

If C0 pin is open shown in Fig.12.12(c), the voltage of C0 pin increases rather than normal condition by the pushing current and then V1 decrease.

Then, you shall obtain the cell voltage again after the response time (latency) obtained from the following equation 12-1. If the difference between the two measured cell voltage before and after open detection ON is more than 100mV, it considered that the wire is open.

$$\text{The response time[ms]} = 100 \times Cc\ [\mu F] \quad (12\text{-}1)$$

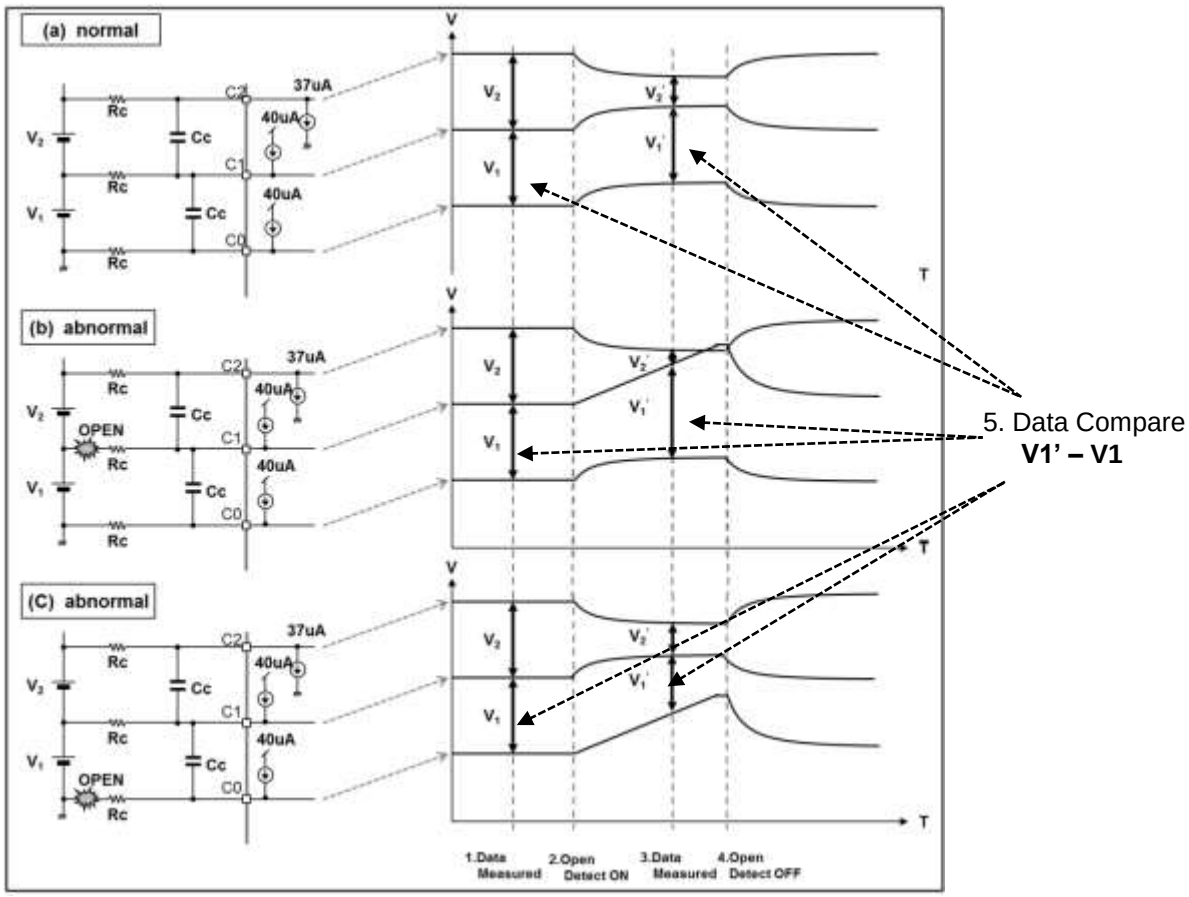


Fig.12.7.2 C0, C1 and C2 pin Voltage on Open Connection Detection
(a: Normal b & c: Abnormal)

Description of Functions

12. Safety Diagnostic Features

12.7 Description of Open Connection Detection

Open Detection at C2 pin

Although it is similar to the C1and C0 pins, please note that when comparing the cell voltage.
If open detection with the C1 and C2 pins are done at the same time ,on the polarity of the current source , the decrease voltage of V2 will be Rc x I (Typ.77μA) despite normal condition.

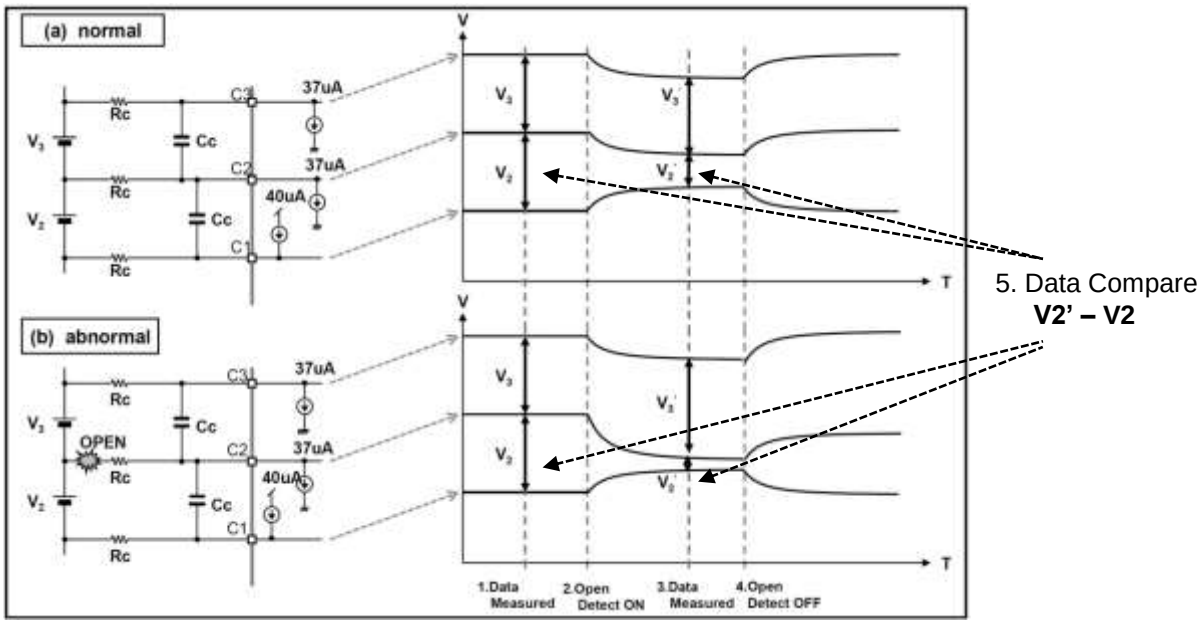


Fig.12.7.3 C2, C3 and C4 pin Voltage on Open Connection Detection
(a: Normal b: Abnormal)

Description of Functions

12. Safety Diagnostic Features

12.7 Description of Open Connection Detection

Open Detection at C3 ~ C16 pins
It is similar to the C1and C0 pins, first you shall obtain the cell voltage immediately before the open detection.
If open detection is done when wire is normal, the voltage of Cn-1 , Cn , and Cn+1 pins decreases and this decrease voltage is obtained from the multiplication the sink current and the resistance (Rc).
If Cn pin is open shown in Fig.12.7.4(b), the voltage of Cn pin decreases rather than normal condition by the sink current and then VN decrease.

Then, you shall obtain the cell voltage again after the response time (latency) obtained from the following equation 12-2. If the difference between the cell voltage of open detection ON just before and the current result changes more than 100mV , it considered that the wire is open.

The response time[ms] = 100 × Cc [μF] (12-2)

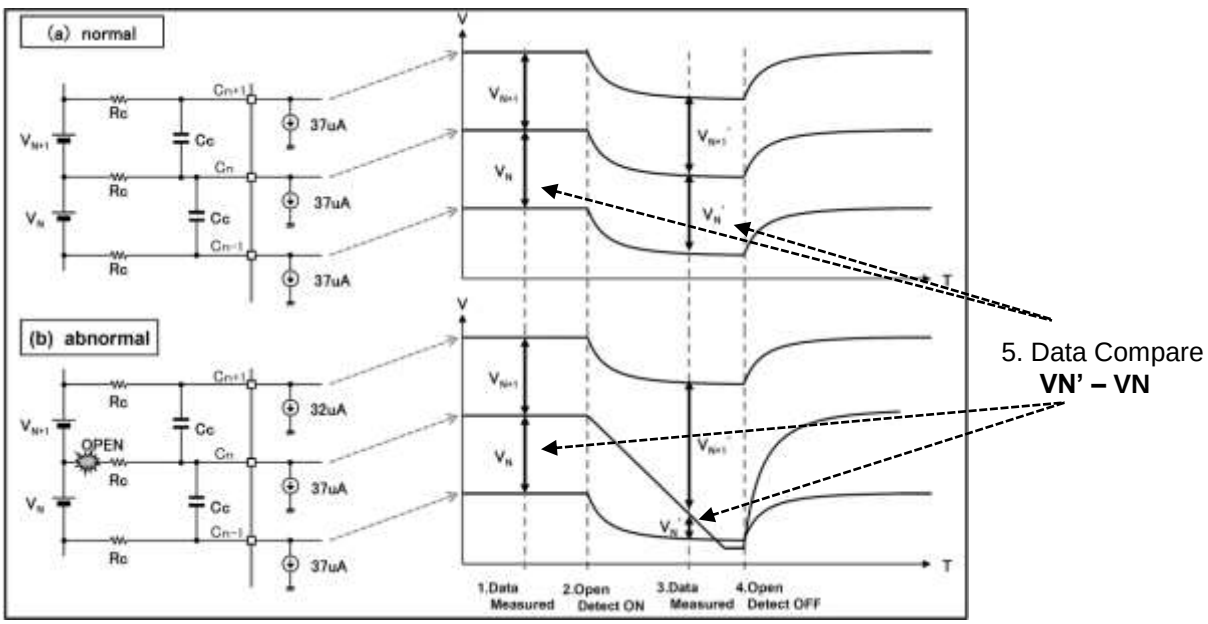


Fig.12.7.4 C3~C16 Pins Voltage on Open Detection
(a: Normal b: Abnormal)

Description of Functions

12. Safety Diagnostic Features

12.7 Description of Open Connection Detection

Table.12.7.1 Example of Open Detection judgment

Open	Judgment
C0	$(CV01\_AD)_{before}$ – $(CV01\_AD)_{after}$ > 100mV
C1	$(CV01\_AD)_{after}$ – $(CV01\_AD)_{before}$ > 100mV
C2	$(CV2\_AD)_{before}$ – $(CV2\_AD)_{after}$ > 200mV ※ external resistor (Rc) =1kΩ
C3	$(CV3\_AD)_{before}$ – $(CV3\_AD)_{after}$ > 100mV
C4	$(CV4\_AD)_{before}$ – $(CV4\_AD)_{after}$ > 100mV
C5	$(CV5\_AD)_{before}$ – $(CV5\_AD)_{after}$ > 100mV
C6	$(CV6\_AD)_{before}$ – $(CV6\_AD)_{after}$ > 100mV
C7	$(CV7\_AD)_{before}$ – $(CV7\_AD)_{after}$ > 100mV
C8	$(CV8\_AD)_{before}$ – $(CV8\_AD)_{after}$ > 100mV
C9	$(CV9\_AD)_{before}$ – $(CV9\_AD)_{after}$ > 100mV
C10	$(CV10\_AD)_{before}$ – $(CV10\_AD)_{after}$ > 100mV
C11	$(CV11\_AD)_{before}$ – $(CV11\_AD)_{after}$ > 100mV
C12	$(CV12\_AD)_{before}$ – $(CV12\_AD)_{after}$ > 100mV
C13	$(CV13\_AD)_{before}$ – $(CV13\_AD)_{after}$ > 100mV
C14	$(CV14\_AD)_{before}$ – $(CV14\_AD)_{after}$ > 100mV
C15	$(CV15\_AD)_{before}$ – $(CV15\_AD)_{after}$ > 100mV
C16	$(CV16\_AD)_{before}$ – $(CV16\_AD)_{after}$ > 100mV
C16M	$(CV16M\_AD)_{before}$ – $(CV16M\_AD)_{after}$ > 100mV
C17	$(CV17\_AD)_{before}$ – $(CV17\_AD)_{after}$ > 100mV

Note: This table is an example of detection judgment for 1-line open

12.7.1 Open Detection Control Registers

Table.12.7.2 shows the registers that control Open Detection.

Table.12.7.2 Open Connection Detection control registers

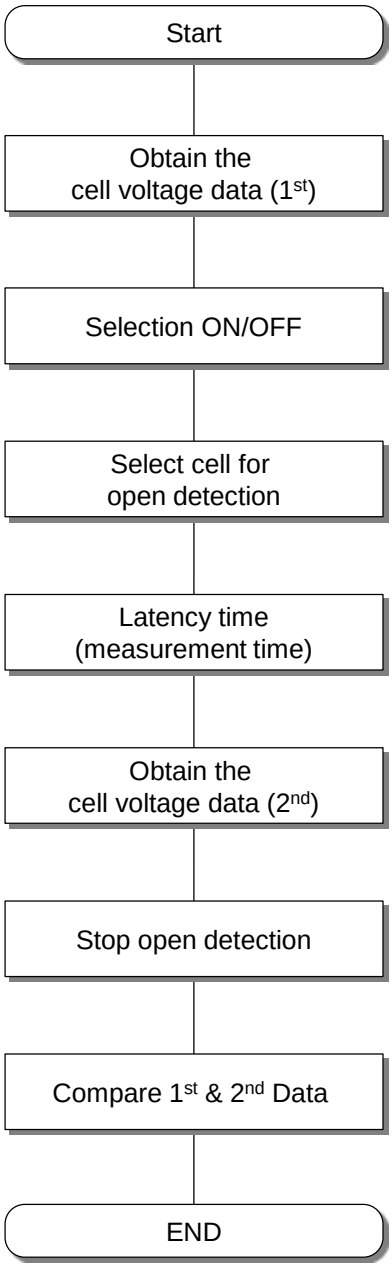
Register	Address [bit]	Function
NPD_INR	0x1B [0]	Open Detection ON/OFF control register
INRCV1	0x19 [15:0]	Selection of Open Detection Pin (C0 ~ C15)
INRCV2	0x1A [1:0]	Selection of Open Detection Pin (C16 ~ C17)

Description of Functions

12. Safety Diagnostic Features

12.7 Description of Open Connection Detection

12.7.2 Open Connection Detection Flow



■Obtain the cell voltage data (1st)
Obtain the cell voltage immediately before the open detection.
(See Chapter 9 voltage measurement)

■Selection ON/OFF
Set NPD_INR control (address: 0x1B[0]) to “1”, for detection ON

■Selection of cell for open detection
Pin to be performed open detection is set to “1”.
C0～C16 pin : Set INR_CV_n flag (address 0x19[15:0]) and (address 0x1A[1:0]) to “1”.
INR_CV_n is corresponding to Cn pin.
(e.g. In the case of INR_CV_0, open detection is done at C0 pin.)

C17 pin : Set INR_CV_17 flag(address 0x1A[2]) to “1”.

■Latency time(measurement time)
After previous step (Selection of cell for open detection) starts , latency time is necessary. Latency time is decided by following formula and external Cc shown in Fig.12.1.2.

Latency time [ms] = 100 X Cc [μF]
(e.g. Cc=1uF, Latency time is 100ms)

■Obtain the cell voltage data (2nd)
Obtain the cell voltage data again.

■Stop open detection
Set INR_CV_n (address 0x19[15:0]) and (address 0x1A[2:0]) to “0”.
Set NPD_INR (address: 0x1B[0]) to “0”.

■Compare Data
Compare the obtained cell voltage 1st & 2nd data.
If 100mV or more of the difference was found,
it will be considered as open.
※If open detection with the C1 and C2 pin is done at the same time, on the polarity of the current source, the decrease voltage of V2 will be Rc x I (Typ.77μA) in spite of normal condition.

Fig.12.7.5 Open Detection Flow

Description of Functions

13. SPI Communication Interface

13.1 Description of SPI Communication Interface

KA49517A communicates with MCU using four lines SPI communication interface, with SDI, SDO, SCL and SEN pins.
Refer to table below for SPI function.

Table.13.1.1 SPI communication function

Use Pin	SDO (Data output : Pin61) SDI (Data input : Pin62) SCL (Clock input : Pin63) SEN (Enable input : Pin64)	
Communication mode	Data Writing (2 byte) Data writing to the set address	
	Data Reading (2 byte) Data readout to the set address	
	Continuous Reading (2 byte * M) Data reading of n consecutive addresses from set address	
Communication Time	Data Writing	$(1/f_{SCK} * 40) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
	Data Reading	$(1/f_{SCK} * 48) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
	Continuous Reading	$(1/f_{SCK} * (40+(16 * M))) + t_{SEN\_LD} + t_{SEN\_LG} + t_{SEN\_LO}$
Polynomial for CRC	$X^8+X^7+X^6+X^4+X^2+1$ Initial value: 0xD5 (Refer to page 137 and 138 for the computation)	
Communication Error detection	Output SDO Pin(When the error "L" output) Output STATUS Flag(SPI_F(SPI_STAT:bp14))	
SPI Watchdog Timer	Configurable Time : 1 ~ 4096s (Default:60s)	

M : continuous read data number
t_{SEN_xx} : delay time for communication (refer to electrical characteristic)

Description of Functions

13. SPI Communication Interface

13.2 Control Registers of SPI

13.2.1 Registers

Table.13.2.1 shows the Registers that control SPI.

Table.13.2.1 SPI Control Registers

Register	Address	Function
SPI_WDTCOUNT	0x03; Bit 0 ~ 11	SPI watchdog timer control register
SDI_PLDW SCL_PLDW SEN_PLDW	0x17; Bit 8,9,10	Communication Control register
SPI_F	0x21; Bit 12	SPI Status register

Description of Functions

13. SPI Communication Interface

13.3 SPI Communication Mode

KA49517A has built-in with the following communication mode.
- Data Writing(2bytes)
- Data Reading(2bytes)
- Continuous Reading(2bytes * M)

It is able to communicate by the following behavior.

When wake up to Active Mode from Shutdown Mode, SDO will change from “L” to “H”, indicating KA49517A is ready for communication, communication can be started after 500ns.

SDO pin is used to indicate the correctness of communication, when there is error with the communication, SDO pin will become “L”.
To find out the reason of the error, read the SPI_F flag(address 0x21[12]).
Please always set "1110000" the beginning 7bit of transmitted data.

13.3.1 Data Writing (2bytes)

The figure below is the timing chart of Data Writing(2 Bytes).

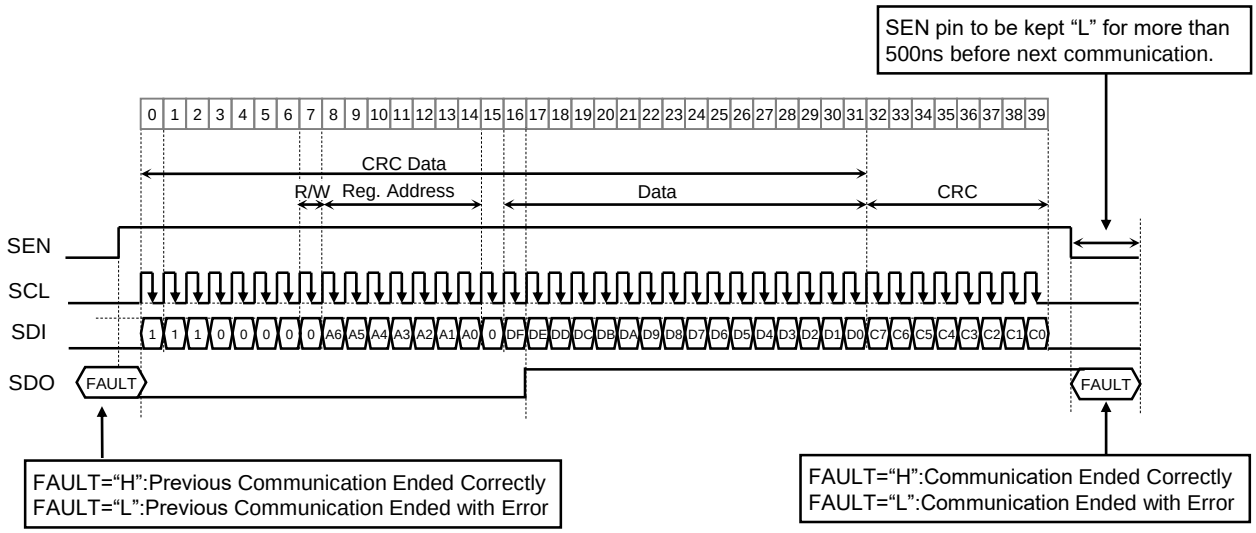


Fig.13.3.1 Data Communication Control Timing <Data Writing(2 Bytes)>

Description of Functions

13. SPI Communication Interface

13.3 SPI Communication Mode

13.3.2 Data Reading (2bytes)

The figure below is the timing chart of Data Reading (2 Bytes).

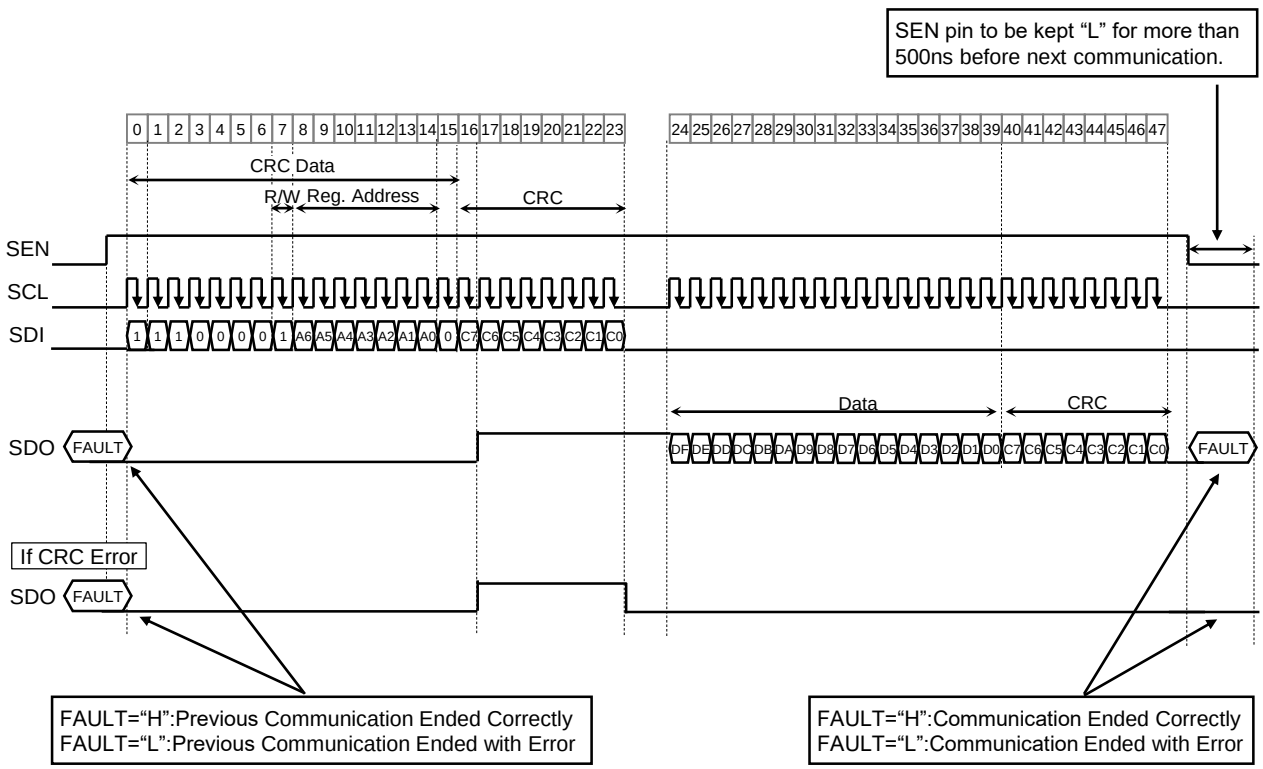


Fig.13.3.2 Data Communication Control Timing <Data Reading(2 Bytes)>

Description of Functions

13. SPI Communication Interface

13.3 SPI Communication Mode

13.3.3 Continuous Reading (2bytes * M)

The figure below is the timing chart of Continuous Reading (2bytes * M).

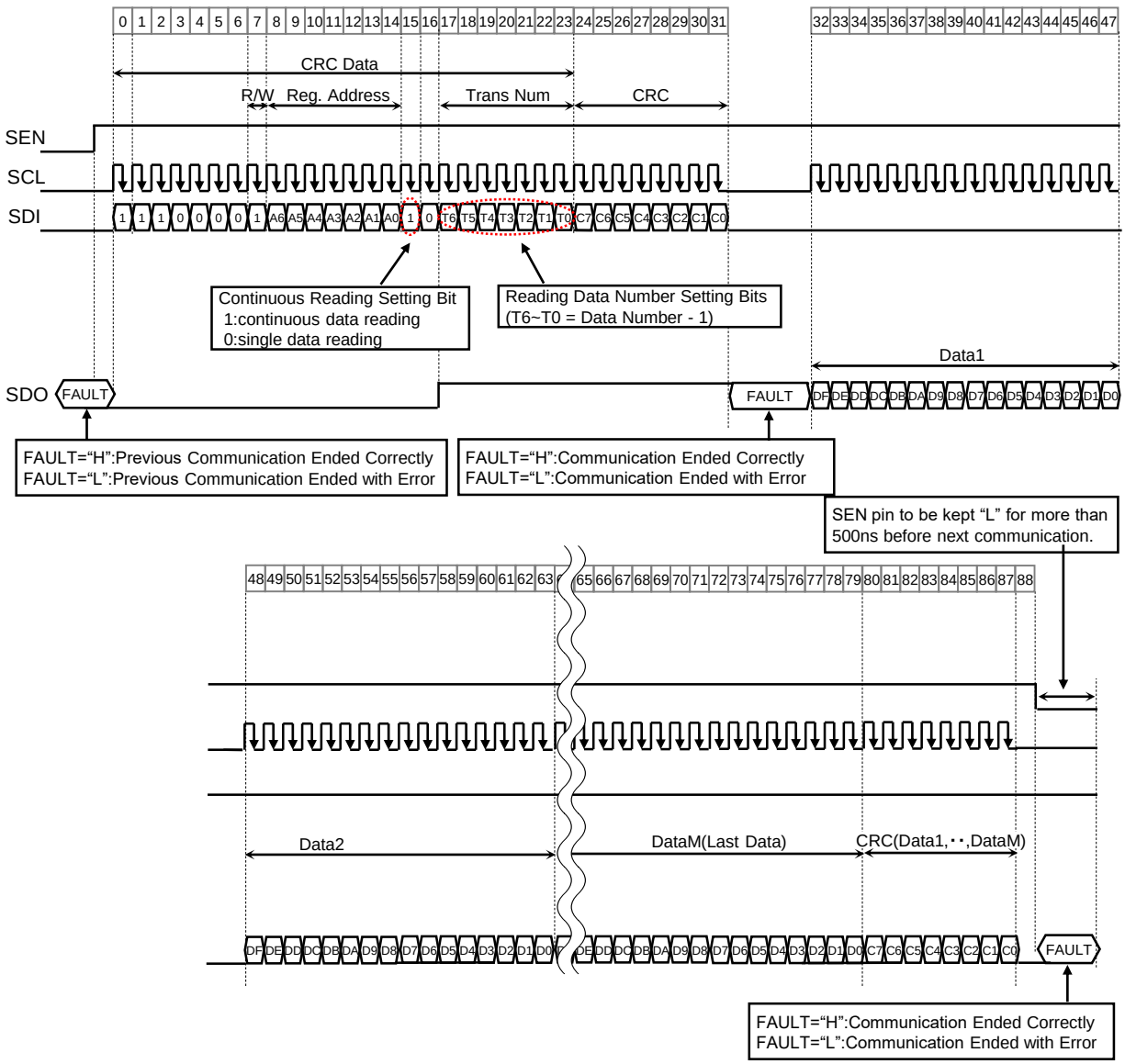


Fig.13.3.3 Data Communication Control Timing <Continuous Reading (2byte × M) >

Description of Functions

13. SPI Communication Interface

13.4 SPI Communication Time

Table below listed required time for communication at different operation.

Table.13.4.1 Time for communication at different operation

Communication	MCU - KA49517A Communication Time
Data Writing	$(1/f_{SCK}$ X 40) + t_{SEN_LD} + t_{SEN_LG} + t_{SEN_LO}
Data Reading	$(1/f_{SCK}$ X 48) + t_{SEN_LD} + t_{SEN_LG} + t_{SEN_LO}
Continuous Reading	$(1/f_{SCK}$ X (40+(16 X M))) + t_{SEN_LD} + t_{SEN_LG} + t_{SEN_LO}

M : continuous read data number
t_{SEN_xx} : delay time for communication (refer to electrical characteristic)

13.5 Communication Error

During communication, SDO pin become “L” when communication error occur.
To find out the reason of the error, read *SPI_F* flag (address 0x21[12]).

13.6 CRC

Command CRC calculation:

KA49517A validates the command frame of SPI communication based on CRC judgment. Command CRC is calculated employing the polynomial below, using the target bits of the command frame except for the command CRC itself. The number of target bits is 32 bits for a write command, 16 bits for a read command and 24 bits for a continuous read command.

- Polynomial (8-bit CRC) : $X^8+X^7+X^6+X^4+X^2+1$
  Initial value : 0xD5, Calculation direction: MSB first
  Calculation result : Non-inverted output

Table 13.6.1 shows an example of the command CRC calculation method.

Data CRC calculation:

In order for the MCU to validate the read-out data, data CRC is attached to the read-out data frame.

The Data CRC is calculated using the polynomial below with an 8-bit CRC for a read command and a 16-bit CRC for a continuous read command.

- Polynomial (8-bit CRC) : $X^8+X^7+X^6+X^4+X^2+1$
  Initial value : 0xD5, Calculation direction: MSB first
  Calculation result : Non-inverted output

Table 13.6.2 shows an example of data CRC judgment.

Description of Functions

13. SPI Communication Interface

13.6 CRC

Table 13.6.1 Example of command CRC calculation (Target data: read command register 0x28)

Calculation direction: MSB first

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
Target Data (0xE150)	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Initial value	1	1	0	1	0	1	0	1																
XOR	0	0	1	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Polynomial	0	0	1	1	1	0	1	0	1	0	1													
XOR	0	0	0	0	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Polynomial	0	0	0	0	1	1	1	0	1	0	1	0	1											
XOR	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
Polynomial	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1						
XOR	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0	0	0	0	0	0
Polynomial	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1					
XOR	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0
Polynomial	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1				
XOR	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	0
Polynomial	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1			
XOR	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0
Polynomial	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1		
XOR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1	0	0
Polynomial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1	
XOR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0

Calculation result: CRC = 0xE6

Table 13.6.2 Example of data CRC judgment (Target data: 0x1234 + CRC 0x2D)

Calculation direction: MSB first

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Target Data(0x1234) +CRC(0x2D)	0	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	0	1	0	1	1	0	1
Initial value	1	1	0	1	0	1	0	1																
XOR	1	1	0	0	0	1	1	1	0															
Polynomial	1	1	1	0	1	0	1	0	1															
XOR			1	0	1	1	0	1	1	0	1													
Polynomial			1	1	1	0	1	0	1	0	1													
XOR				1	0	1	1	1	0	0	0	1												
Polynomial				1	1	1	0	1	0	1	0	1												
XOR					1	0	1	0	0	1	0	0	0											
Polynomial					1	1	1	0	1	0	1	0	1											
XOR						1	0	0	1	1	1	0	1	1										
Polynomial						1	1	1	0	1	0	1	0	1										
XOR							1	1	1	0	1	1	1	0	0									
Polynomial							1	1	1	0	1	0	1	0	1									
XOR												1	0	0	1	0	0	0	1	0				
Polynomial												1	1	1	0	1	0	1	0	1				
XOR													1	1	1	1	0	1	1	1	1			
Polynomial													1	1	1	0	1	0	1	0	1			
XOR																1	1	1	0	1	0	1	0	1
Polynomial																1	1	1	0	1	0	1	0	1
XOR																	0	0	0	0	0	0	0	0

Calculation result: normal = 0, abnormal = not 0

Description of Functions

13. SPI Communication Interface

13.7 Watchdog Timer of Communication

As part of the communication safety features, KA49517A has a Watchdog Timer (WDT) that will countdown to the set time when there is no communication between the MCU and the IC. This feature can be used as a safety mechanism to shutdown the system in case there is a problem with the MCU.

Upon expiry of the KA49517A WDT, it is possible to shutdown the MCU immediately through shutting down the REGEXT power supply, assuming the MCU is powered by this Regulator. An interrupt will be sent to the MCU about 100ms prior to the expiry of the WDT countdown via GPIO pin interrupt.
This serves as a form of interrupt to the MCU prior to actual WDT expiry. In case the MCU is able to resume communication with the KA49517A before expiry of the WDT countdown, the WDT counter will be reset and normal operation will be resumed. Refer to chapter 7 for GPIO interrupt settings details.

REGEXT shutdown behavior can be set by WDT_REGEXT_OFF bit register (address 0x03[13]). When this bit is set to “1”, KA49517A will shut down the REGEXT (MCU supply) upon expiry of the WDT for the first time and then restart the REGEXT output after a predetermined delay time. In the event that WDT expires again for the second time, the REGEXT output as well as KA49517A will be shutdown permanently until a wakeup signal is issued by the MCU again. This feature allows for the MCU to reboot once in case of a nonpermanent fault. The IC internal register settings will also be reset after the first WDT expiry so as to synchronize with the repowering up of the MCU.

When WDT_REGEXT_OFF bit (address 0x03[13]) is set to “0”, REGEXT output as well as KA49517A will shut down upon WDT expiry, permanently until a wakeup signal is issued by the MCU again. Refer to Fig 13.7.1 for the different cases upon WDT expiry.

The WDT can be programed from 1s ~ 4096s at SPI_WDTCOUNT[11:0] register (address 0x03[11:0]).
This function also be turned off by setting COMTIMON register (address 0x03[12]) to be “0”.
WDT function is available in both Active and Low power mode of operation. During Standby mode when communication is turned OFF, WDT can still be turned ON by setting WDT_STB_EN register (address 0x03[14]) to be “1”. Do not change WDT Timing Setting when Watchdog Timer is already in operation.

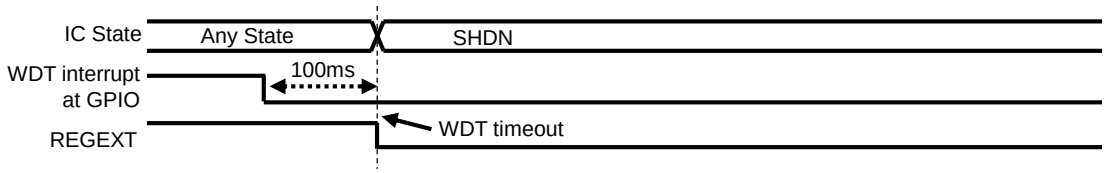
Description of Functions

13. SPI Communication Interface

13.7 Watchdog Timer of Communication

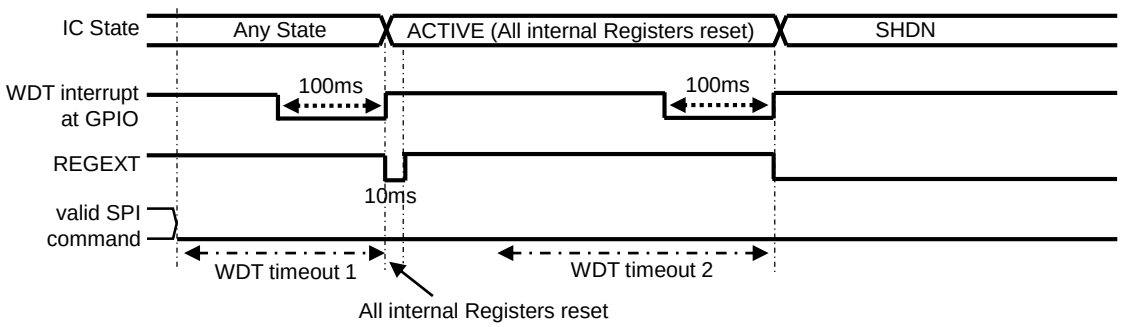
The diagrams below show the timing of the Watchdog Timer upon expiry for the different detections.

(1) WDT_REGEXT_OFF (address 0x03[13]) = “0” case



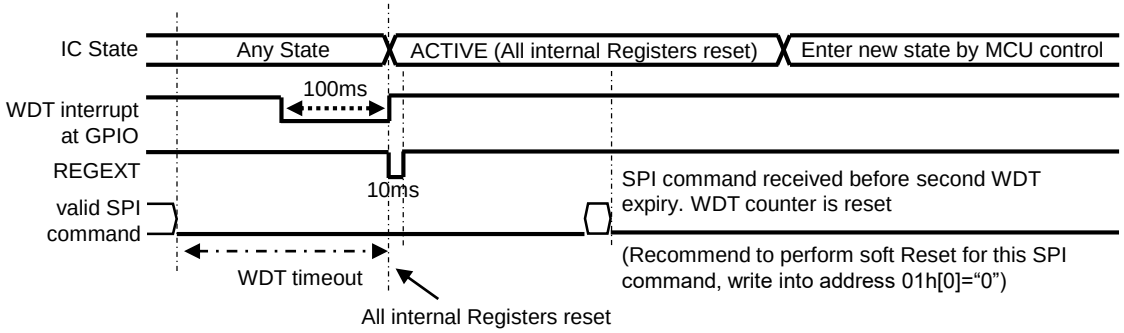
*REGEXT and IC enter shut down state when WDT expiry.

(2) WDT_REGEXT_OFF bit (address 0x03[13]) = “1” case (SPI is still not received after reset MCU)



*WDT expires twice when there is no MCU SPI communication.
*REGEXT power OFF in two attempts; at the second attempt, IC also enter Shutdown state

(3) WDT_REGEXT_OFF (address 0x03[13]) = “1” case (SPI is received after reset MCU)



*WDT expire one time and SPI command is received next.
*REGEXT power OFF in 1 attempt. IC did not enter shutdown mode

Fig.13.7.1 Timing diagrams of the Watchdog Timer upon expiry for different scenario

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.1 Description of Self-Control Fuse SCF (Chemical Fuse) Control Function

KA49517A includes a SCF Fuse Blow function which is able to provide a secondary protection in addition to the CHG/DIS FET control. This function serves as a protection of last resort by blowing the fuse to protect the battery in the event of battery cell fault and in addition to failure of the FETs to protect the cells.

This function operate in a certain algorithm by checking Cell voltage or cell current fault. This function can be turned ON/OFF by MCU control by setting register FUSE_ENV (address 0x08[8]) and FUSE_ENC (address 0x08[0]) respectively. Both the voltage and current abnormality are used as criteria to arrive at the Fuse blow decision.

Refer to flow chart shown in figure 14.1.2 and 14.1.3 for the flow used to judge if SCF fuse blow circuit is to be activated or not.

14.1.1 Self-Control Fuse SCF (Chemical Fuse) Gate driver circuit

The SCF Fuse Gate driver can be programmed to be output from any GPIO pin.
Refer to chapter 7 on how to output the Fuse gate driver to the selected GPIO pin.

An external NMOS accompany by suitable Gate RC filter are recommended to be connected to the chemical fuse for this function (as shown in the Fig 14.1.1 below). External NMOS FET with suitable power dissipation should be chosen such that it is able to handle the current when blowing the selected chemical fuse.

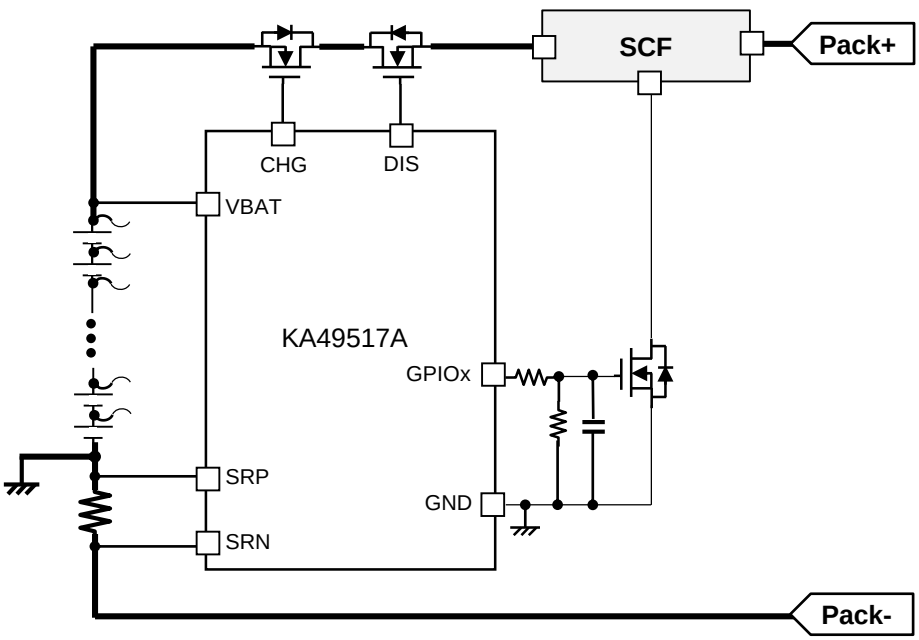


Fig.14.1.1 Example of SCF Fuse Gate Driver Circuit

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.2 Flowchart of Self-Control Fuse SCF (Chemical Fuse) Decision (Over Voltage)

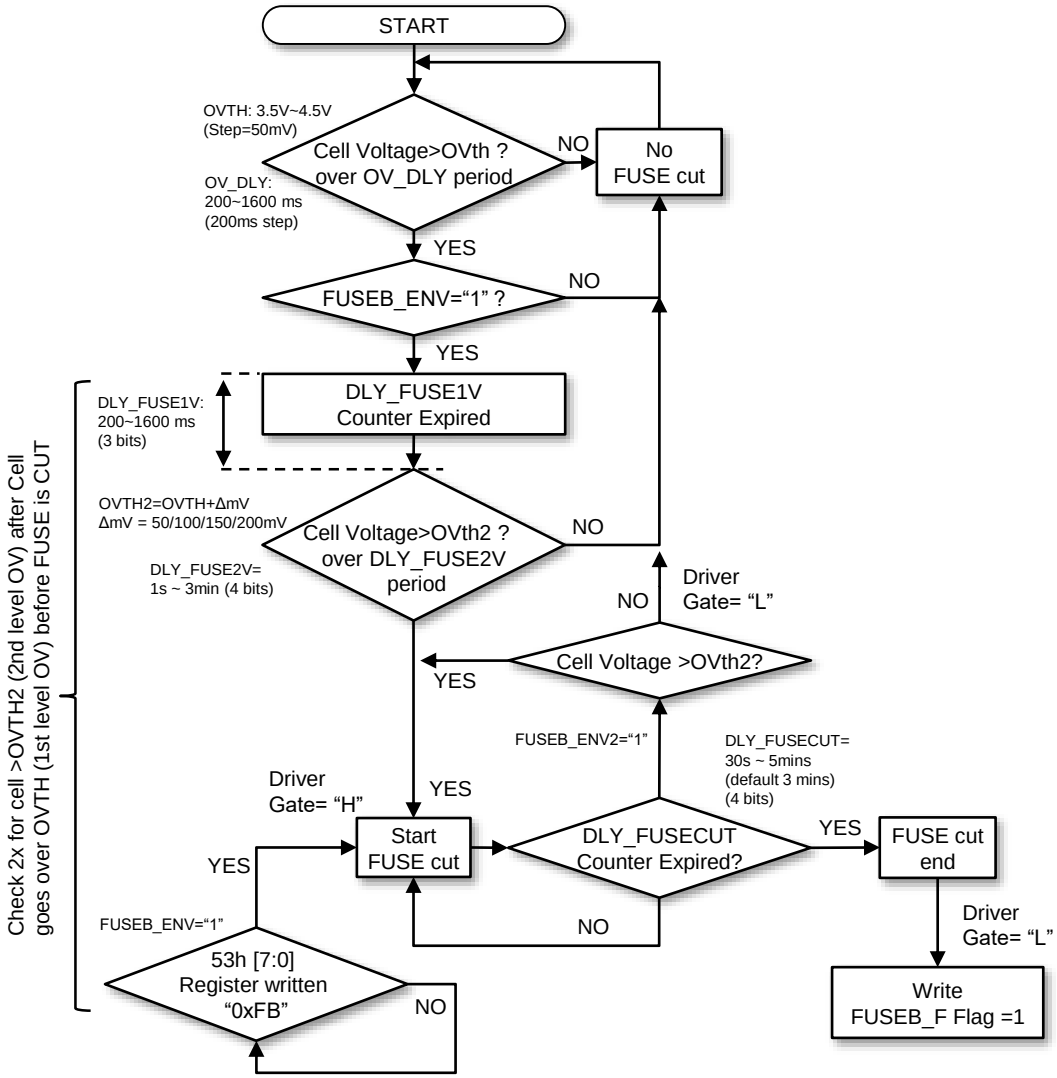


Fig.14.2.1 Chemical Fuse Blow Function Decision by Over Voltage Detection

Upon detection of continuous over voltage over OV_{th} setting (address 0x0A[11:6] over the entire duration of the OV_DLY (address 0x0B[6:4] counter(i.e Alarm condition triggered), KA49517A will enter FUSE monitoring check if FUSEB_ENV register(address 0x08[8]) is set to "1". KA49517A will then start the count down a counter that is preset in DLY_FUSE1V (address 0x08[11:9]). In a typical system, the CHG and DIS FET should be turned OFF in the event of an Over voltage. Upon expiry of DLY_FUSE1V counter, the cell voltage will be continuously checked if it exceeds a higher threshold of OV_{th2} (address 0x09[7:6]) with countdown of another timer, DLY_FUSE2V (address 0x08[15:12]).

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.2 Flowchart of Self-Control Fuse SCF (Chemical Fuse) Decision (Over Voltage)

If cell voltage goes below OV_{th2} before expiry of the DLY_FUSE2V counter, the counter will reset and operation will return to monitor if Alarm condition happen or not again. On the other hand if cell voltage goes above OV_{th2} upon the expiry of the DLY_FUSE2V counter, Fuse Blow operation will begin.

When fuse cutting process is activated, another counter, DLY_FUSECUT(address 0x09[3:0]) will start counting down during the Fuse Blow operation. Fuse blow function will continue by turning on Driver Gate="H" until DLY_FUSECUT counter has expired. Upon expiry of the DLY_FUSECUT counter, Fuse Blow operation will be turned off (Driver Gate="L") and Flag FUSEB_F (address 0x27[4]) will be written with "1".

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.2.1 Registers setting of SCF Control (Over Voltage)

In the event Fuse cutting process is on-going, MCU can decide to abort the Fuse Blow operation by setting another register, FUSEB_ENV2 (address 0x9[5])="1", Fuse Blow operation will be aborted once the cell voltage goes below OV_{th2} and DLY_FUSECUT counter will be reset.

MCU can also decide to start the Fuse Blow operation (bypassing all detection path) by directly writing FUSEB_ENV="1" and writing special code "0xFB" into FUSE_BLOW (address0x53h [7:0]) register (see Fig.14.2.1). In this case Fuse Blow operation will be executed to completion until the DLY_FUSECUT timer expiry. Before DLY_FUSECUT timer expiry, this operation can be terminated by writting any other code other than "0xFB" into FUSE_BLOW register.

Below table 14.2.1 shows the required register settings to progam the fuse cut setting for voltage abnormalities condition.

Table.14.2.1 Timing and Voltage Threshold Settings for Fuse Blow Function (Over Voltage)

Register	Address [bit]	Function
OVTH	0x0A [11:6]	Over voltage threshold setting for alarm triggering
OV_DLY	0x0B [7:4]	Over voltage delay after over voltage is triggered and before alarm output
FUSEB_ENV	0x08 [8]	Over Voltage Fuse blow algorithm function enable
DLY_FUSE_1V	0x08 [11:9]	Over voltage fuse blow delay after alarm is triggered by OVTH
DLY_FUSE_2V	0x08 [15:12]	Over voltage fuse blow delay after OVTH2 is triggered
OVTH2_SEL	0x09 [7:6]	Selection for OVTH2 threshold . Decide the additional voltage in additional to OVTH before deciding to cut fuse
FUSEB_ENV2	0x09 [5]	To enable OVTH2 to continue to be monitored when fuse cutting is in progress
DLY_FUSECUT	0x09 [3:0]	Counter to hold Gate High after fuse is decided to be cut
FUSE_BLOW	0x53 [7:0]	Fuse blow function direct activation Fuse blow function by MCU control will be activated when "0xFB" is written to this register. Not dependent on Cell and current fault algorithm.
FUSEB_F	0x27 [4]	Fuse blow status 1: Fuse blow is completed 0: Fuse blow not completed (Default)

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.3 Flowchart of Self-Control Fuse SCF (Chemical Fuse) Decision (Over Current)

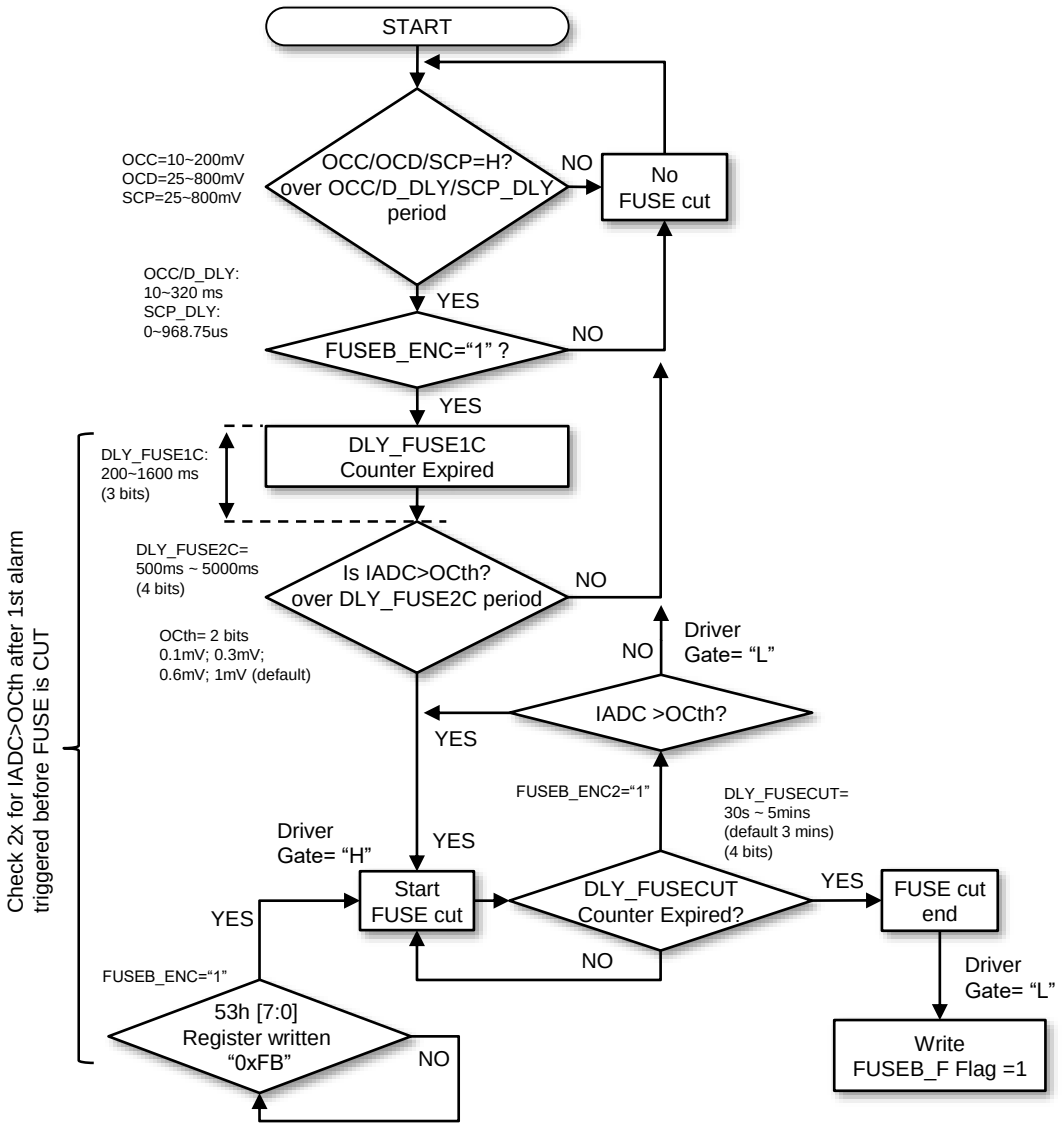


Fig.14.3.1 Chemical Fuse Blow Function Decision by Over Current Detection

In the event of continuous triggering of OCC/OCD/SCP condition over the threshold setting at address 0x13[15:0] over the entire duration of the OCD_DLY/OCC_DLY/SCP_DLY (address 0x14[14:0]) counter period.(i.e Alarm condition triggered) and if FUSEB_ENC="1" (address 0x08[0]), KA49517A will start the count down of the DLY_FUSE1C (address 0x8[3:1])counter. Upon expiry of this counter, the current through the shunt resistor will be continuously checked if it exceed OCth (address 0x0A[11:6]) over the DLY_FUSE2C (address 0x8[7:4]) counter period, as shown in Fig.14.3.1.

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.3 Flowchart of Self-Control Fuse SCF (Chemical Fuse) Decision (Over Current)

If IADC goes below OCth before expiry of the DLY_FUSE2C counter, the counter will reset and operation will return to monitor if Alarm condition happen or not again. On the other hand, if IADC maintain above OCth threshold, Fuse Blow operation will begin.

Another counter, DLY_FUSECUT (address 0x9[3:0]) will start counting down during the Fuse Blow operation. Fuse blow function will continue by turning on Driver Gate="H" until DLY_FUSECUT counter has expired. Upon expiry of the DLY_FUSECUT counter, Fuse Blow operation will be turned off (Driver Gate="L") and Flag FUSEB_F (address 0x27[4]) will be written with "1".

Description of Functions

14. Self-Control Fuse SCF (Chemical Fuse) Control Function

14.3.1 Registers setting of SCF Control (Over Current)

In the event Fuse cutting process is on-going, MCU can decided to abort the Fuse Blow operation by setting another register, FUSEB_ENVC="1", Fuse Blow operation will be aborted if IADC is checked to be below OCth and DLY_FUSECUT can be reset.

MCU can also decide to start the Fuse Blow operation (bypassing all detection path) by writing FUSEB_ENV="1" and writing special code "0xFB" into FUSE_BLOW (address 0x53h [7:0]) registe(see Fig.14.3.1). In this case Fuse Blow operation will be executed to completion until the DLY_FUSECUT timer expiry. Before DLY_FUSECUT timer expiry, this operation can be terminated by writting any other code other than "0xFB" into FUSE_BLOW register

Below table shows the required register settings to progam the fuse cut setting for current abnormalities condition.

Table.14.3.1 Timing and Voltage Threshold Settings for Fuse Blow Function (Over Current)

Register	Address [bit]	Function
SCD_D OCD_D OCC_D	0x13 [14:0]	Setting of Over Charge; Over discharge and Short circuit detection current for alarm output
SCD_DLY OCD_DLY OCC_DLY	0x14 [14:0]	Setting of Over Charge; Over discharge and Short circuit detection delay after detection for alarm output
FUSEB_ENC	0x08 [0]	Over current fuse blow algorithm function enable
DLY_FUSE_1C	0x08 [3:1]	Over current fuse blow delay after alarm is triggered by SCD/OCC/OCD fault
DLY_FUSE_2C	0x08 [7:4]	Over current detection (IADC>OCTH) delay period before fuse blow is decided
OCTH_SEL	0x0A [13:12]	Current threshold settings to check for current abnormality before Fuse cut after DLY_FUSE_1C delay has passed
FUSEB_ENC2	0x09 [4]	To enable IADC>OCTH check to continue to be monitored when fuse cutting is in progress
DLY_FUSECUT	0x09 [3:0]	Counter to hold Gate High after fuse is decided to be cut
FUSE_BLOW	0x53 [7:0]	Fuse blow function direct activation Fuse blow function by MCU control will be activated when "0xFB" is written to this register. Not dependent on Cell and current fault algorithm.
FUSEB_F	0x27 [4]	Fuse blow status 1: Fuse blow is completed 0: Fuse blow not completed (Default)

Explanation of Registers

A.1 Overview of registers

This IC is equipped with registers for control, status and data. Each register consists of 16 bits flag.
The accessibility of each flag is defined as:

- R : Readable - R/W : Readable and writable always

bit/ Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x01	ADC_ CONT	INTM_TIM[1:0]		INTMSEL[1:0]		LDM_SLP _EN	VPC_SLP _EN	LDM_ST B_EN	VPC_STB _EN	AUTO_TIM[1:0]		MSET_ STB	MSET_LP	MSET_ SLP	MSET_ SHDN	NPD_RS T
0x02	INT5_EN	INT4_EN	INT3_EN	INT2_EN	INT1_EN	CHG_DIS _CLR	-	REGEXT _EN	-	STB_RE GEXT_ LPEN	SLP_RE GEXT_ LPEN	INTM_RE GEXT_ LPEN	STB_VD D55_LPE N	SLP_VDD 55_LPEN	INTM_VD D55_ LPEN	Reserve d
0x03	-	WDT_ST B_EN	WDT_RE GEXT_ OFF	COMTI MON	SPI_WDTCOUNT[11:0]											
0x04	FDRV_ ALM_SD	FDRV_ ALM_RC V	FDRV_ ALM_CL R	NPD_ FDRV	FDRV_S EL_CLK	FDRV_ CHG_FE T	FDRV_ DIS_FET	FDRV_ STBY	Reserved			FDRV_LEVEL[2:0]			FDRV_ OUVCTL	Reserve d
0x05	CV16SEL	CV15SEL	CV14SEL	CV13SEL	CV12SEL	CV11SEL	CV10SEL	CV9SEL	CV8SEL	CV7SEL	CV6SEL	CV5SEL	CV4SEL	CV3SEL	CV2SEL	CV1SEL
0x06	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	CV17SE L
0x07	Reserved	VREF2 SEL	REGEXT SEL	VDD18 SEL	-	-	-	GPAD2 SEL	GPAD1 SEL	VDD55 SEL	TMONI5 SEL	TMONI4 SEL	TMONI3 SEL	TMONI2 SEL	TMONI1 SEL	VPACK SEL
0x08	DLY_FUSE_2V[3:0]				DLY_FUSE_1V[2:0]			FUSEB_ ENV	DLY_FUSE_2C[3:0]				DLY_FUSE_1C[2:0]			FUSEB_ ENC
0x09	-	-	-	-	-	-	-	-	OVTH2_SEL[1:0]		FUSEB_ ENV2	FUSEB_ ENC2	DLY_FUSECUT[3:0]			
0x0A	-	-	OCTH_SEL[1:0]		OVTH[5:0]						UVTH[5:0]					
0x0B	-	OV_HYS[2:0]			-	UV_HYS[2:0]			-	OV_DLY[2:0]			-	UV_DLY[2:0]		
0x0C	-	-	-	-	-	-	-	CB_SET	UVMSK	OVMSK	-	ADC_TR G	-	ADIL_ LATCH	ADIH_ LATCH	ADV_ LATCH
0x0D	-	-	-	-	GPIO1SEL[3:0]				-	-	GPIO1_ CHDRV	GPIO1_ OUT	GPIO1_ OD	GPIO1_ PD	GPIO1_ NOE	GPIO1_I E
0x0E	-	-	-	-	GPIO2SEL[3:0]				-	-	GPIO2_ CHDRV	GPIO2_ OUT	GPIO2_ OD	GPIO2_ PD	GPIO2_ NOE	GPIO2_I E
0x0F	-	-	-	-	GPIO3SEL[3:0]				-	-	GPIO3_ CHDRV	GPIO3_ OUT	GPIO3_ OD	GPIO3_ PD	GPIO3_ NOE	GPIO3_I E
0x10	-	-	-	-	-	-	-	-	-	-	GPOH2_ ALM_ST	GPOH1_ ALM_ST	-	GPOH_ FET	GPOH2_ EN	GPOH1_ EN
0x11	-	OVP_F_ SET	TSD_F_ SET	-	-	-	OSCH_ DIV	OSCL_DI V	PULLUP_SEL[5:1]					-	ACTV_DLY[1:0]	
0x12	ALARM SEL	-	-	-	-	-	-	-	-	-	-	-	EN_SCD	EN_OCD	EN_OCC	EN_CP
0x13	-	SCD_D[4:0]					OCD_D[4:0]					OCC_D[4:0]				
0x14	-	SCD_DLY[4:0]					OCD_DLY[4:0]					OCC_DLY[4:0]				
0x15	DI_CBSEL[16:1]															
0x16	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	DI_CBS EL[17]
0x17	Reserved	DIS_OSC _OFF	Reserved	Reserved	-	SDI_ PLDW	SCL_ PLDW	SEN_ PLDW	-	PD_ REG55	Reserved	Reserved	Reserved	-	Reserved	NPD_CB
0x18	-	-	ADSWHY _EN	ADSWSD _EN	Reserved	-	Reserved	Reserved	Reserved		ADIH_ CSYNC	ISD_ STOPEN	ADI_ LATCH_ SET	ADV_ LATCH_ SET	ADIL_ON	ADIH_O N
0x19	INR_CV[15:0]															

Explanation of Registers

A.1 Overview of registers

This IC is equipped with registers for control, status and data. Each register consists of 16 bits flag.
The accessibility of each flag is defined as:

- R : Readable - R/W : Readable and writable always

bit/ Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x1A	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved INR_CV[17:16M]		
0x1B	ADIH_CSYNC_SEL[4:0]					FET_DIAG_EN	FET_DIAG_SEL[1:0]		-	DIAG_IHY_EN	DIAG_ISD_EN	-	-	-	-	NPD_INR
0x1C	ST_GPIO3	ST_GPIO2	ST_GPIO1	Reserved	FDRV_DIS_ST	FDRV_CHG_ST	GPOH2_ST	GPOH1_ST	IADS_DONE	IADH_DONE	VAD_DONE	ST_INTM	ST_LP	ST_SDWN	ST_STBY	ST_ACT
0x1D	ST_CV16SEL	ST_CV15SEL	ST_CV14SEL	ST_CV13SEL	ST_CV12SEL	ST_CV11SEL	ST_CV10SEL	ST_CV9SEL	ST_CV8SEL	ST_CV7SEL	ST_CV6SEL	ST_CV5SEL	ST_CV4SEL	ST_CV3SEL	ST_CV2SEL	ST_CV1SEL
0x1E	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	ST_CV17SEL
0x1F	-	-	-	ST_TMONI5SEL	ST_TMONI4SEL	ST_TMONI3SEL	ST_TMONI2SEL	ST_TMONI1SEL	ST_GPAD2SEL	ST_GPAD1SEL	ST_VPACKSEL	ST_VDD18SEL	ST_REGEXTSEL	ST_VDD55SEL	Reserved	ST_VREF2SEL
0x20	Reserved	Customer Reserved								Reserved			NPD_LDM	OVP_F_SET_REGEXT	UVP_F_SET	LDM_SHRT
0x21	ST_SCD	ST_OCD	ST_OCC	SPI_F	Reserved	MUX1A_F	-	-	SCD_F	OCD_F	OCC_F	TSD_F	CFETON_F	CFETOFF_F	DFETON_F	DFETOFF_F
0x22	OV16_F	OV15_F	OV14_F	OV13_F	OV12_F	OV11_F	OV10_F	OV9_F	OV8_F	OV7_F	OV6_F	OV5_F	OV4_F	OV3_F	OV2_F	OV1_F
0x23	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	OV17_F
0x24	UV16_F	UV15_F	UV14_F	UV13_F	UV12_F	UV11_F	UV10_F	UV9_F	UV8_F	UV7_F	UV6_F	UV5_F	UV4_F	UV3_F	UV2_F	UV1_F
0x25	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	UV17_F
0x26	-	-	-	-	-	HVREF2	LVREF2	HBIAS1A	HBIAS1D	LBIAS1D	HBIAS2A	HBIAS2D	LBIAS2D	HBIAS3A	HBIAS3D	LBIAS3D
0x27	LDM_DET_F	VPC_DET_F	WDT_F	CUR_H_F	LDM_H_F	LDM_L_F	VPC_H_F	VPC_L_F	-	-	-	FUSEB_F	ST_OTH	ST_BIAS	ST_OV	ST_UV
0x28	CV01_AD[15:0]															
0x29	CV02_AD[15:0]															
0x2A	CV03_AD[15:0]															
0x2B	CV04_AD[15:0]															
0x2C	CV05_AD[15:0]															
0x2D	CV06_AD[15:0]															
0x2E	CV07_AD[15:0]															
0x2F	CV08_AD[15:0]															
0x30	CV09_AD[15:0]															
0x31	CV10_AD[15:0]															
0x32	CV11_AD[15:0]															
0x33	CV12_AD[15:0]															
0x34	CV13_AD[15:0]															
0x35	CV14_AD[15:0]															
0x36	CV15_AD[15:0]															
0x37	CV16_AD[15:0]															
0x38	CV17_AD[15:0]															
0x39	Reserved															

Explanation of Registers

A.1 Overview of registers

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- R : Readable
- R/W : Readable and writable always

bit/ Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x3A	Reserved															
0x3B	Reserved															
0x3C	Reserved															
0x3D	Reserved															
0x3E	VPACK_AD[15:0]															
0x3F	TMONI1_AD[15:0]															
0x40	TMONI2_AD[15:0]															
0x41	TMONI3_AD[15:0]															
0x42	TMONI4_AD[15:0]															
0x43	TMONI5_AD[15:0]															
0x44	VDD55_AD[15:0]															
0x45	GPIO1_AD[15:0]															
0x46	GPIO2_AD[15:0]															
0x47	CVIH_AD[15:0]															
0x48	CVIL_AD[15:0]															
0x49	VDD18_AD[15:0]															
0x4A	REGEXT_AD[15:0]															
0x4B	VREF2_AD[15:0]															
0x4C	Reserved															
0x4D	OV16_LF	OV15_LF	OV14_LF	OV13_LF	OV12_LF	OV11_LF	OV10_LF	OV9_LF	OV8_LF	OV7_LF	OV6_LF	OV5_LF	OV4_LF	OV3_LF	OV2_LF	OV1_LF
0x4E	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	OV17_LF
0x4F	UV16_LF	UV15_LF	UV14_LF	UV13_LF	UV12_LF	UV11_LF	UV10_LF	UV9_LF	UV8_LF	UV7_LF	UV6_LF	UV5_LF	UV4_LF	UV3_LF	UV2_LF	UV1_LF
0x50	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	UV17_LF
0x51	CB_ST[16:1]															
0x52	-	-	-	-	-	-	-	-	-	-	Reserved					CB_ST [17]
0x53	-	-	-	-	-	-	-	-	FUSE_BLOW[7:0]							
0x54	Reserved	Reserved														
0x55	-	AUTO_ITHL[14:0]														
0x56	-	-	-	-	-	Reserved	R55GAIN[2:0]			R55TC[2:0]			R55VC[2:0]			Reserved
0x57	-	-	-	-	-	-	PULLUP_TMONI1[9:0]									
0x58	PULLUP_TMONI3[7:0]								PULLUP_TMONI2[7:0]							
0x59	PULLUP_TMONI5[7:0]								PULLUP_TMONI4[7:0]							

Explanation of Registers

A.2 Detailed explanation

Address: 0x01 PWR_CTRL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADC_CONT	INTM_TIM [1:0]		INTMSEL [1:0]		LDM_SLP_EN	VPC_SLP_EN	LDM_STB_EN	VPC_STB_EN	AUTO_TIM [1:0]		MSET_STB	MSET_LP	MSET_SLP	MSET_SHDN	NPD_RST
Initial	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	ADC_CONT	ADC Operation Setting 1: Voltage and HS current measurement is performed during Active Mode. Once this bit is set, measurement will be done repeatedly 0: Voltage and HS Current Measurement are performed only when register (0x0c) ADC_TRG = 1 (Default)	
[14:13]	INTM_TIM[1:0]	2 Bits programmable Delay to return from STB/Low Power mode to ACT mode to check Cell voltage in intermittent mode 00: 20ms (Default) 01: 40ms 10: 80ms 11: 160ms	
[12:11]	INTMSEL[1:0]	Intermittent mode selection 00: No intermittent; (Stay at STB or Low Power mode) (Default) 01: Intermittent mode using no SPI>1s (intermittent mode of previous IC AN49503) 10: Intermittent mode using INTM_TIM; (Intermittent STB/Lower power mode) 11: Intermittent mode using AUTO_TIM (Sense current auto mode)	
10	LDM_SLP_EN	Enable control by LDM pin 1: Enable return to active mode from SLP mode when Load is detected(Default) 0: No control	
9	VPC_SLP_EN	Enable control by VPC pin 1: Enable return to active mode from SLP mode when VPC is high (Default) 0: No control	
8	LDM_STB_EN	Enable control by LDM pin 1: Enable return to active mode from LP/STB mode when load is detected (Default) 0: No control	
7	VPC_STB_EN	Enable control by VPC pin 1: Enable return to active mode from LP/STB mode when VPC is high (Default) 0: No control	
[6:5]	AUTO_TIM[1:0]	2 Bits programmable Delay to return to Active mode by checking sense current using Fast ADC vs ITH_L in AUTO current detection mode 00: 10ms (Default) 01: 20ms 10: 40ms 11: 80ms	
4	MSET_STB	Standby mode control 1: Standby mode 0: Normal operation (Default)	
3	MSET_LP	Low sampling speed Active mode (Low power mode) 1: Low power mode 0: Normal operation (Default)	
2	MSET_SLP	Sleep mode control 1: Sleep mode 0: Normal operation (Default)	
1	MSET_SHDN	Shutdown control 1: Shutdown Mode 0: Normal operation (Default)	
0	NPD_RST	Soft Reset 1: Normal operation (Default) 0: Reset (Soft -reset is used to reset all registers to default setting.) * It returns to "1" automatically after writing "0".	

Explanation of Registers

A.2 Detailed explanation

Address: 0x02` REG_INT_EN

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT5_EN	INT4_EN	INT3_EN	INT2_EN	INT1_EN	CHG_DIS_CLR	-	REGEXT_EN	-	STB_REGEXT_LPEN	SLP_REGEXT_LPEN	INTM_REGEXT_LPEN	STB_VDD55_LPEN	SLP_VDD55_LPEN	INTM_VDD55_LPEN	Reserved
Initial	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Explanation	Reference
15	INT5_EN	Enable control of WDT_F flag trigger (WDT pre expiry warning interrupt) 1: Enable WDT_F flag to be triggered when WDT_TRG is rising 0: No status indication (Default)	
14	INT4_EN	Enable control of CUR_H_F flag trigger (Current detection interrupt when in Auto current detection mode; current detected) 1: Enable CUR_H_F flag to be triggered when sense current is detected 0: No status indication (Default)	
13	INT3_EN	Enable current detection interrupt when in Auto current detection mode; current release 1: Enable interrupt to be triggered when sense current is released 0: No status indication (Default)	
12	INT2_EN	Enable control of LDM_L_F & LDM_H_F flag trigger (LDM , Load detection interrupt) 1: Enable LDM_L_F & LDM_H_F flag to be triggered when LDM is falling/rising 0: No status indication (Default)	
11	INT1_EN	Enable control of VPC_L_F & VPC_H_F flag trigger (VPC, charger detection interrupt) 1: Enable VPC_L_F & VPC_H_F flag to be triggered when VPC is falling/rising 0: No status indication (Default)	
10	CHG_DIS_CLR	Enable clear for FDRV_CHG_FET, FDRV_DIS_FET after enter sleep mode. 1: Enable clear (Default) 0: No change	
9	-		
8	REGEXT_EN	Enable REG_EXT by user setting 1: ON (Default) 0: OFF	
7	-		
6	STB_REGEXT_LPEN	Enable REGEXT to enter Low Power mode during Standby/Low Power mode 1: Select LP mode 0: Select HP Mode (Default)	
5	SLP_REGEXT_LPEN	Enable REGEXT to enter Low Power during Sleep mode 1: Select LP mode 0: Select HP Mode (Default)	
4	INTM_REGEXT_LPEN	Enable REGEXT to enter Low Power during Intermittent mode 1: Select LP mode 0: Select HP Mode (Default)	
3	STB_VDD55_LPEN	Enable VDD55 to enter Low Power mode during Standby/Low Power mode 1: Select LP mode 0: Select HP Mode (Default)	
2	SLP_VDD55_LPEN	Enable VDD55 to enter Low Power during Sleep mode 1: Select LP mode 0: Select HP Mode (Default)	
1	INTM_VDD55_LPEN	Enable VDD55 to enter Low Power during Intermittent mode 1: Select LP mode 0: Select HP Mode (Default)	
0	Reserved	Please always set to "0".	

Explanation of Registers

A.2 Detailed explanation

Address: 0x03 SPIWD_CTL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	WDT_STB_EN	WDT_REGEXT_OFF	COMTIMON	SPI_WDTCOUNT[11:0]											
Initial	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1
R/W	R	R/W	R/W	R/W	R/W											

bit	Name	Explanation	Reference
15	-		
14	WDT_STB_EN	Enable WDT during Standby mode 1: Enable 0: Disable (Default)	
13	WDT_REGEXT_OFF	REG_EXT status when WDT expires 1: REG_EXT will be turned OFF → ON → OFF in 2 tries upon WDT expiry 0: REG_EXT will be turned OFF upon WDT expiry (Default)	
12	COMTIMON	SPI communication watchdog timer control 1: ON 0: OFF (Default)	
[11:0]	SPI_WDTCOUNT [11:0]	Watchdog Timer Timing Setting 0xFFF: 4096s ～ 0x03B: 60s (Default) ～ 0x000: 1s * Time = (value +1) x 1 s	

Explanation of Registers

A.2 Detailed explanation

Address: 0x04 FDRV_CTRL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FDRV_ALM_SD	FDRV_ALM_RCV	FDRV_ALM_CLR	NPD_FDRV	FDRV_SEL_CLK	FDRV_CHG_FET	FDRV_DIS_FET	FDRV_STBY	Reserved			FDRV_LEVEL[2:0]			FDRV_OUVCTL	Reserved
Initial	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			R/W			R/W	R/W

bit	Name	Explanation	Reference
15	FDRV_ALM_SD	CHG/DIS FET and GPOH pins response to ALARM condition 1: CHG/DIS FET auto OFF and GPOH become value set, refer to specification section 11 CHG FET OFF: OV/UV/OCC DIS FET OFF: OV/UV/OCD/SCD 0: CHG/DIS FET and GPOH no response to ALARM condition (Default)	
14	FDRV_ALM_RCV	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV) condition removed (when FDRV_ALM_SD = 1) with the following setting. 1: Depend on FDRV_ALM_CLR 0: Recover when ALARM(OV/UV) condition is removed (Default)	
13	FDRV_ALM_CLR	CHG/DIS FET and GPOH pins recover when ALARM(OV/UV/OCD/OCC/SCD) condition removed (when FDRV_ALM_SD = 1 & FDRV_ALM_RCV=1) 1: CHG/DIS FET and GPOH pins recover 0: No change (Default) * This bit is not cleared automatically. * If ALARM condition continue and this bit is set, CHS/DIS FET remains OFF.	
12	NPD_FDRV	Power down control of FET driver 1: Normal operation (Default) 0: Power down	
11	FDRV_SEL_CLK	FDRV clock division selection 1: 128 division (0.5 kHz) 0: 32 division (2 kHz) (Default)	
10	FDRV_CHG_FET	External CHGFET control 1: FET ON 0: FET OFF (Default)	
9	FDRV_DIS_FET	External DISFET control 1: FET ON 0: FET OFF (Default)	
8	FDRV_STBY	FET driver's standby mode switch 1: power reduction mode (Standby) 0: Normal (Default)	
[7:5]	Reserved	Please always set to "000".	
[4:2]	FDRV_LEVEL[2:0]	Setting of external NMOS FET V_{GS} overdrive voltage (typical value). 111: V_{GS} overdrive = 4V 110: V_{GS} overdrive = 5V 101: V_{GS} overdrive = 6V 100: V_{GS} overdrive = 7V 011: V_{GS} overdrive = 8V 010: V_{GS} overdrive = 9V 001: V_{GS} overdrive = 10V 000: V_{GS} overdrive = 11V (Default)	
1	FDRV_OUVCTL	CHG/DIS FET OFF mode setting when alarm is asserted 1: Both of CHG/DIS FET OFF when OV or UV 0: CHG FET OFF when OV, DIS FET OFF when UV (Default)	
0	Reserved	Please always set to "0".	

Explanation of Registers

A.2 Detailed explanation

Address: 0x05 CVSEL1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV16 SEL	CV15 SEL	CV14 SEL	CV13 SEL	CV12 SEL	CV11 SEL	CV10 SEL	CV9 SEL	CV8 SEL	CV7 SEL	CV6 SEL	CV5 SEL	CV4 SEL	CV3 SEL	CV2 SEL	CV1 SEL
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	CV16SEL	ON/OFF switch for cell 16 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
14	CV15SEL	ON/OFF switch for cell 15 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
13	CV14SEL	ON/OFF switch for cell 14 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
12	CV13SEL	ON/OFF switch for cell 13 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
11	CV12SEL	ON/OFF switch for cell 12 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
10	CV11SEL	ON/OFF switch for cell 11 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
9	CV10SEL	ON/OFF switch for cell 10 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
8	CV9SEL	ON/OFF switch for cell 9 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
7	CV8SEL	ON/OFF switch for cell 8 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
6	CV7SEL	ON/OFF switch for cell 7 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
5	CV6SEL	ON/OFF switch for cell 6 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
4	CV5SEL	ON/OFF switch for cell 5 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
3	CV4SEL	ON/OFF switch for cell 4 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
2	CV3SEL	ON/OFF switch for cell 3 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
1	CV2SEL	ON/OFF switch for cell 2 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	
0	CV1SEL	ON/OFF switch for cell 1 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x06 CVSEL2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	CV17SEL
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0	CV17SEL	ON/OFF switch for cell 17 voltage measurement 1: Measurement ON (Default) 0: Measurement OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x07 GVSEL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	VREF2SEL	REGEXTSEL	VDD18SEL	-	-	-	GPAD2SEL	GPAD1SEL	VDD55SEL	TMONI5SEL	TMONI4SEL	TMONI3SEL	TMONI2SEL	TMONI1SEL	VPACKSEL
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name		Reference
15	Reserved		
14	VREF2SEL	VREF2 voltage monitor's ON/OFF switch 1: Measurement ON 0: Measurement OFF (Default)	
13	REGEXTSEL	REG_EXT voltage monitor's ON/OFF switch 1: Measurement ON 0: Measurement OFF (Default)	
12	VDD18SEL	ON/OFF switch of VDD18 voltage monitor (result of measurement by system AD measurement) 1: Measurement ON 0: Measurement OFF (Default)	
11	-		
10	-		
9	-		
8	GPAD2SEL	ON/OFF switch of analog measurement of terminal GPIO2 1: Measurement ON 0: Measurement OFF (Default) * Please set the GPIO2_NOE bit beforehand and set “1" and the GPIO2_IE bit to “1" when making it to the GPAD2SEL bit "1".	
7	GPAD1SEL	ON/OFF switch of analog measurement of terminal GPIO1 1: Measurement ON 0: Measurement OFF (Default) * Please set the GPIO1_NOE bit beforehand and set “1" and the GPIO1_IE bit to “1" when making it to the GPAD1SEL bit "1".	
6	VDD55SEL	ON/OFF switch of VDD55 voltage monitor (result of measurement by system AD watch) 1: Measurement ON 0: Measurement OFF (Default)	
5	TMONI5SEL	ON/OFF switch of TMONI5 voltage monitor 1: Measurement ON 0: Measurement OFF (Default)	
4	TMONI4SEL	ON/OFF switch of TMONI4 voltage monitor 1: Measurement ON 0: Measurement OFF (Default)	
3	TMONI3SEL	ON/OFF switch of TMONI3 voltage monitor 1: Measurement ON 0: Measurement OFF (Default)	
2	TMONI2SEL	ON/OFF switch of TMONI2 voltage monitor 1: Measurement ON 0: Measurement OFF (Default)	
1	TMONI1SEL	ON/OFF switch of TMONI1 voltage monitor 1: Measurement ON 0: Measurement OFF (Default)	
0	VPACKSEL	VPAC voltage monitor's ON/OFF switch 1: Measurement ON (Default) 0: Measurement OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x08 FUSE_CTL1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DLY_FUSE_2V[3:0]				DLY_FUSE_1V[2:0]			FUSEB_ENV	DLY_FUSE_2C[3:0]				DLY_FUSE_1C[2:0]			FUSEB_ENC
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W				R/W			R/W	R/W				R/W			R/W

bit	Name	Explanation	Reference
[15:12]	DLY_FUSE_2V[3:0]	Counter/delay2 to judge to blow chemical fuse for voltage abnormality 0000 : 1000ms (Default) 0001 : 2000ms 0010 : 3000ms 0011 : 4000ms 0100 : 5000ms 0101 : 10000ms 0110 : 20000ms 0111 : 30000ms 1000 : 40000ms 1001 : 50000ms 1010 : 75000ms 1011 : 100000ms 1100 : 120000ms 1101 : 140000ms 1110 : 160000ms 1111 : 180000ms	
[11:9]	DLY_FUSE_1V[2:0]	Counter/delay1 to judge to blow chemical fuse for voltage abnormality 000 : 200ms (Default) 001: 400ms 010 : 600ms 011 : 800ms 100 : 1000ms 101 : 1200ms 110 : 1400ms 111 : 1600ms	
8	FUSEB_ENV	Enable bit for chemical fuse monitor function (Voltage abnormalities) 1: Enable 0: Disable (Default)	
[7:4]	DLY_FUSE_2C[3:0]	Counter/delay2 to judge to blow chemical fuse for current abnormality 0000 : 500ms (Default) 0001 : 800ms 0010 : 1100ms 0011 : 1400ms 0100 : 1700ms 0101 : 2000ms 0110 : 2300ms 0111 : 2600ms 1000 : 2900ms 1001 : 3200ms 1010 : 3500ms 1011 : 3800ms 1100 : 4100ms 1101 : 4400ms 1110 : 4700ms 1111 : 5000ms	
[3:1]	DLY_FUSE_1C[2:0]	Counter/delay1 to judge to blow chemical fuse for current abnormality 000 : 200ms (Default) 001 : 400ms 010 : 600ms 011 : 800ms 100 : 1000ms 101 : 1200ms 110 : 1400ms 111 : 1600ms	
0	FUSEB_ENC	Enable bit for chemical fuse monitor function (Current abnormalities) 1: Enable 0: Disable (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x09 FUSE_CTL2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	OVTH2_SEL [1:0]		FUSE B _ENV2	FUSE B _ENC2	DLY_FUSECUT[3:0]			
Initial	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R/W	R	R	R	R	R	R	R	R	R/W		R/W	R/W	R/W			

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
[7:6]	OVTH2_SEL[1:0]	Selection for OVTH2 threshold (additional from OVTH settings from address 0x0A) 00 : +200mV (Default) 01 : +150mV 10 : +100mV 11 : + 50mV	
5	FUSEB_ENV2	Enable OVTH2 to continue to be monitored when fuse cutting in progress 1: Enable 0: Disable (Default)	
4	FUSEB_ENC2	Enable OCTH to continue to be monitored when fuse cutting in progress 1: Enable 0: Disable (Default)	
[3:0]	DLY_FUSECUT[3:0]	Counter to hold Gate High after FUSE decided to cut 0000 : 30000ms 0001 : 45000ms 0010 : 60000ms 0011 : 75000ms 0100 : 90000ms 0101 : 105000ms 0110 : 120000ms 0111 : 135000ms 1000 : 150000ms 1001 : 165000ms 1010 : 180000ms (Default) 1011 : 195000ms 1100 : 210000ms 1101 : 225000ms 1110 : 240000ms 1111 : 300000ms	

Explanation of Registers

A.2 Detailed explanation

Address: 0x0A OUVCTL1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	OCTH_SEL [1:0]		OVTH[5:0]						UVTH[5:0]					
Initial	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W						R/W					

bit	Name	Explanation	Reference
15	-		
14	-		
[13:12]	OCTH_SEL[1:0]	Current threshold settings to check for current abnormality before Fuse cut 11 : 0.1mV 10 : 0.3mV 01 : 0.6mV 00 : 1.0mV (Default)	
[11:6]	OVTH[5:0]	Over-Voltage Detection Threshold 110100 : 4.50V (Default) ～ 100000 : 3.50V ～ 000010 : 2.00V 111111～110101 (remains at 4.5V) 000001, 000000: Prohibited	
[5:0]	UVTH[5:0]	Under-Voltage Detection Threshold 110010 : 3.00V ～ 000000 : 0.50V (Default) 111111-110011: Prohibited	

Explanation of Registers

A.2 Detailed explanation

Address: 0x0B OUVCTL2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	OV_HYS[2:0]			-	UV_HYS[2:0]			-	OV_DLY[2:0]			-	UV_DLY[2:0]		
Initial	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
R/W	R	R/W			R	R/W			R	R/W			R	R/W		

bit	Name	Explanation	Reference
15	-		
[14:12]	OV_HYS[2:0]	OV Detection Hysteresis level 000 : 25mV 001 : 50mV 010 : 75mV 011 : 100mV (Default) 100 : 125mV 101 : 150mV 110 : 175mV 111 : 200mV	
11	-		
[10:8]	UV_HYS[2:0]	UV Detection Hysteresis level 000 : 25mV 001 : 50mV 010 : 75mV 011 : 100mV (Default) 100 : 125mV 101 : 150mV 110 : 175mV 111 : 200mV	
7	-		
[6:4]	OV_DLY[2:0]	OV ALARM Delay Time 000 : 200ms 001 : 400ms 010 : 600ms 011 : 800ms (Default) 100 : 1500ms 101 : 3000ms 110 : 4500ms 111 : 6000ms	
3	-		
[2:0]	UV_DLY[2:0]	UV ALARM Delay Time 000 : 200ms 001 : 400ms 010 : 600ms 011 : 800ms (Default) 100 : 1500ms 101 : 3000ms 110 : 4500ms 111 : 6000ms	

Explanation of Registers

A.2 Detailed explanation

Address: 0x0C OP_MODE

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	CB_ SET	UV MSK	OV MSK	-	ADC_ TRG	-	ADIL_ LATCH	ADIH_ LATCH	ADV_ LATCH
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	CB_SET	Cell balance operation control 1: Cell balance operation ON 0: Cell balance operation OFF (Default)	
7	UVMSK	Cell Voltage Under-Voltage Detection ON/OFF 1: UV OFF 0: UV ON (Default)	
6	OVMSK	Cell Voltage Overvoltage Detection ON/OFF 1: OV OFF 0: OV ON (Default)	
5	-		
4	ADC_TRG	Manual ADC Measurement Trigger 1: Voltage ADC Measurement Start, when ADC_CONT = 0 (Auto returns to 0 after completion) 0: When ADC_CONT = 1, always set this bit = 0 (Default)	
3	-		
2	ADIL_LATCH	Low Speed Current ADC Measurement Result Latch 1: Measured result latched to register 0x48 (Auto returns to 0 after data latch completed) 0: No effect (Default)	
1	ADIH_LATCH	High Speed Current ADC Measurement Result Latch 1: Measured result latched to register 0x47 (auto return to 0 after data latch completed) 0: No effect (Default)	
0	ADV_LATCH	Voltage ADC Measurement Result Latch 1: Measured result latched to register 0x28~0x46 (auto return to 0 after data latch completed) 0: No effect (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x0D GPIO_CTL1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	GPIO1SEL[3:0]				-	-	GPIO1_CHDRV	GPIO1_OUT	GPIO1_OD	GPIO1_PD	GPIO1_NOE	GPIO1_IE
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W				R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
[11:8]	GPIO1SEL[3:0]	GPIO1 output selection 0000 : GPIO (General) (Default) 0001 : GPOH1 Data output 0010 : GPOH2 Data output 0011 : ADIRQ1 output 0100 : ADIRQ2 output 0101 : High speed OSC divided output 0110 : Low speed OSC divided output 0111 : Active mode state output 1000 : Standby mode state output 1001 : Low Power mode state output 1010 : FUSE FET output 1011 : Alarm2 output 1101 : MCU INT OR output 1100, 1110 ~ 1111 : Prohibited	
7	-		
6	-		
5	GPIO1_CHDRV	GPIO1 Pin Output Drivability 1: 4mA 0: 2mA (Default)	
4	GPIO1_OUT	GPIO1 pin digital output data GPIO1_OD = 0 (push pull) 1: Output “H” 0: Output “L” (Default) GPIO1_OD = 1 (open drain) 1: Output “Hi-Z” 0: Output “L” (Default)	
3	GPIO1_OD	GPIO1 Pin Output Configuration 1: Nch Open Drain 0: Push Pull (Default)	
2	GPIO1_PD	GPIO1 Pin Pull-Down Resistor 1: Pull-down resistor ON 0: Pull-down resistor OFF (Default)	
1	GPIO1_NOE	GPIO1 Pin Output Enable 1: Disabled (Default) 0: Enabled	
0	GPIO1_IE	GPIO1 Pin Input Enable 1: Enabled 0: Disable (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x0E GPIO_CTL2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	GPIO2SEL[3:0]				-	-	GPIO2_CHDRV	GPIO2_OUT	GPIO2_OD	GPIO2_PD	GPIO2_NOE	GPIO2_IE
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W				R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
[11:8]	GPIO2SEL[3:0]	GPIO2 output selection 0000 : GPIO (General) (Default) 0001 : GPOH1 Data output 0010 : GPOH2 Data output 0011 : ADIRQ1 output 0100 : ADIRQ2 output 0101 : High speed OSC divided output 0110 : Low speed OSC divided output 0111 : Active mode state output 1000 : Standby mode state output 1001 : Low Power mode state output 1010 : FUSE FET output 1011 : Alarm2 output 1101 : MCU INT OR output 1100, 1110 ～ 1111 : Prohibited	
7	-		
6	-		
5	GPIO2_CHDRV	GPIO2 Pin Output Drivability 1: 4mA 0: 2mA (Default)	
4	GPIO2_OUT	GPIO2 pin digital output data GPIO2_OD = 0 (push pull) 1: Output “H” 0: Output “L” (Default) GPIO2_OD = 1 (open drain) 1: Output “Hi-Z” 0: Output “L” (Default)	
3	GPIO2_OD	GPIO2 Pin Output Configuration 1: Nch Open Drain 0: Push Pull (Default)	
2	GPIO2_PD	GPIO2 Pin Pull-Down Resistor 1: Pull-down resistor ON 0: Pull-down resistor OFF (Default)	
1	GPIO2_NOE	GPIO2 Pin Output Enable 1: Disabled (Default) 0: Enabled	
0	GPIO2_IE	GPIO2 Pin Input Enable 1: Enabled 0: Disable (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x0F GPIO_CTL3

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	GPIO3SEL[3:0]				-	-	GPIO3_CHDRV	GPIO3_OUT	GPIO3_OD	GPIO3_PD	GPIO3_NOE	GPIO3_IE
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R/W				R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
[11:8]	GPIO3SEL[3:0]	GPIO3 output selection 0000 : GPIO (General) (Default) 0001 : GPOH1 Data output 0010 : GPOH2 Data output 0011 : ADIRQ1 output 0100 : ADIRQ2 output 0101 : High speed OSC divided output 0110 : Low speed OSC divided output 0111 : Active mode state output 1000 : Standby mode state output 1001 : Low Power mode state output 1010 : FUSE FET output 1011 : Alarm2 output 1101 : MCU INT OR output 1100, 1110 ～ 1111 : Prohibited	
7	-		
6	-		
5	GPIO3_CHDRV	GPIO3 Pin Output Drivability 1: 4mA 0: 2mA (Default)	
4	GPIO3_OUT	GPIO3 pin digital output data GPIO3_OD = 0 (push pull) 1: Output “H” 0: Output “L” (Default) GPIO3_OD = 1 (open drain) 1: Output “Hi-Z” 0: Output “L” (Default)	
3	GPIO3_OD	GPIO3 Pin Output Configuration 1: Nch Open Drain 0: Push Pull (Default)	
2	GPIO3_PD	GPIO3 Pin Pull-Down Resistor 1: Pull-down resistor ON 0: Pull-down resistor OFF (Default)	
1	GPIO3_NOE	GPIO3 Pin Output Enable 1: Disabled (Default) 0: Enabled	
0	GPIO3_IE	GPIO3 Pin Input Enable 1: Enabled 0: Disable (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x10 GPOH_CTL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	GPOH2_ALM_ST	GPOH1_ALM_ST	-	GPOH_FET	GPOH2_EN	GPOH1_EN
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	GPOH2_ALM_ST	If using FET at GPOH2 pin, to set GPOH2 pin data to output during ALARM. Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 . 1: Low output 0: Hi-Z (Default)	
4	GPOH1_ALM_ST	If using FET at GPOH1 pin, set GPOH1 pin data to output during ALARM. Effective only when FDRV_ALM_SD=1 & GPOH_FET=1 . 1: Low output 0: Hi-Z (Default)	
3	-		
2	GPOH_FET	FET control settings of GPOH Pin 1: FET control used Control of FET driver ON/OFF is possible in GPOH pin by FDRV_CTL(0x04). 0: FET control not in use (Default)	
1	GPOH2_EN	GPOH2 output data 1: Low output 0: Hi-Z (Default)	
0	GPOH1_EN	GPOH1 output data 1: Low output 0: Hi-Z (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x11 GPIO_CTL4

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	OVP_F_SET	TSD_F_SET	-	-	-	OSCH_DIV	OSCL_DIV	PULLUP_SEL[5:1]					-	ACTV_DLY[1:0]	
Initial	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1
R/W	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	

bit	Name	Explanation	Reference
15	-		
14	OVP_F_SET	Transition to shutdown when abnormal high voltage is detected at VDD55/VDD18 1: No change (Default) 0: Shutdown immediately	
13	TSD_F_SET	Transition to shutdown when abnormal high temperature is detected 1: No change (Default) 0: Shutdown immediately	
12	-		
11	-		
10	-		
9	OSCH_DIV	Setting of GPIO output dividing frequency of OSCH 1: 1/512 = 40kHz (Default) 0: 1/128 = 160kHz	
8	OSCL_DIV	Setting of GPIO output dividing frequency of OSCL 1: 1/64 = 4.096kHz (Default) 0: 1/1 = 262.144kHz	
[7:3]	PULLUP_SEL[5:1]	Pull up setting for TMONI1 to TMONI5 pin 1: Pull-up resistor ON 0: Pull-up resistor OFF (Default)	
2	-		
[1:0]	ACTV_DLY[1:0]	Number of ADC scan cycles after returning back to Active when INTSEL==2'b11 (intermittent auto current detection mode) 00: 1 cycle 01: 2 cycles (Default) 10: 3 cycles 11: 4 cycles	

Explanation of Registers

A.2 Detailed explanation

Address: 0x12 ALARM_CTL1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ALARM SEL	-	-	-	-	-	-	-	-	-	-	-	EN_ SCD	EN_ OCD	EN_ OCC	EN_ CP
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	ALARMSEL	ALARM1 pin setting 1: ALARM for SCD (ALARM2 can be used for OV/UV/OCD/OCC ALARM when at any of the 3 GPIO pins based on GPIOnSEL bits.) 0: ALARM for OV/UV/OCD/OCC/SCD (Default)	
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	-		
4	-		
3	EN_SCD	Short circuit detection at discharge 1: Enable 0: Disable (Default)	
2	EN_OCD	Overcurrent detection at discharge 1: Enable 0: Disable (Default)	
1	EN_OCC	Overcurrent detection at charge 1: Enable 0: Disable (Default)	
0	EN_CP	Current Protection 1: Enable 0: Disable (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x13 ALARM_CTL2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	SCD_D[4:0]					OCD_D[4:0]					OCC_D[4:0]				
Initial	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
R/W	R	R/W					R/W					R/W				

bit	Name	Explanation	Reference
15	-		
[14:10]	SCD_D[4:0]	Short circuit detection at discharge threshold 0x1F: 640mV ～ 0x01: 40mV (Default) 0x00: 20mV * Threshold = (SCD_D[4:0]+1) x 20mV	
[9:5]	OCD_D[4:0]	Overcurrent detection at discharge threshold 0x1F: 320mV ～ 0x01: 20mV (Default) 0x00: 10mV * Threshold = (OCD_D[4:0]+1) x 10mV	
[4:0]	OCC_D[4:0]	Overcurrent detection at charge threshold 0x17~0x1F: 120mV ～ 0x01: 10mV (Default) 0x00: 5mV * Threshold = (OCC_D[4:0]+1) x 5mV	

Explanation of Registers

A.2 Detailed explanation

Address: 0x14 ALARM_CTL3

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	SCD_DLY[4:0]					OCD_DLY[4:0]					OCC_DLY[4:0]				
Initial	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W					R/W					R/W				

bit	Name	Explanation	Reference
15	-		
[14:10]	SCD_DLY[4:0]	Delay time for Short circuit detection at discharge 0x1F: 968.75us ～ 0x01: 31.25us (Default) 0x00: 0us * Time = SCD_DLY[4:0] x 31.25us * If alarm condition continues after delay time, ALARM will be turned ON.	
[9:5]	OCD_DLY[4:0]	Overcurrent detection at discharge delay time 0x1F: 320ms ～ 0x00: 10ms (Default) * Time = (OCD_DLY[4:0]+1) x 10ms * If alarm condition continues after delay time, ALARM will be turned ON.	
[4:0]	OCC_DLY[4:0]	Overcurrent detection at charge delay time 0x1F: 320ms ～ 0x00: 10ms (Default) * Time = (OCC_DLY[4:0]+1) x 10ms. *If alarm condition continues after delay time, ALARM will be turned ON.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x15 CBSEL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DI_CBSEL[16:1]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W															

bit	Name	Explanation	Reference
[15:0]	DI_CBSEL[16:1]	Selection of cell for balancing 1: Cell balance selected 0: Cell balance not selected (Default)	

Address: 0x16 CBSEL_17

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved					DI_CBSEL[17]
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W					

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
[5:1]	Reserved	Please always set to "00000".	
0	DI_CBSEL[17]	Selection of cell for balancing 1: Cell balance selected 0: Cell balance not selected (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x17 OTHCTL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	DIS_OSC_OFF	Reserved	Reserved	-	SDI_PLDW	SCL_PLDW	SEN_PLDW	-	PD_REG55	Reserved	Reserved	Reserved	-	Reserved	NPD_CB
Initial	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W

bit	Name	Explanation	Reference
15	Reserved	Please always set to "0".	
14	DIS_OSC_OFF	OSCL ON/OFF control during Sleep mode 1: OSCL ON in Logic clocking during Sleep mode 0: OSCL OFF in Logic clocking during Sleep mode (Default)	
13	Reserved	Please always set to "0".	
12	Reserved	Please always set to "0".	
11	-		
10	SDI_PLDW	SDI pin pull-down control signal 1: Pull-down ON (Default) 0: Pull-down OFF	
9	SCL_PLDW	SCL pin pull-down control signal 1: Pull-down ON (Default) 0: Pull-down OFF	
8	SEN_PLDW	SEN pin pull-down control signal 1: Pull-down ON (Default) 0: Pull-down OFF	
7	-		
6	PD_REG55	VDD55 regulator power down 1: Power down 0: Normal (Default).	
5	Reserved	Please always set to "0".	
4	Reserved	Please always set to "0".	
3	Reserved	Please always set to "0".	
2	-		
1	Reserved	Please always set to "0".	
0	NPD_CB	Cell balance control power down 1: Normal. 0: Power down (Default).	

Explanation of Registers

A.2 Detailed explanation

Address: 0x18 ADCTL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	AD SWHY _EN	AD SWSD _EN	Reserv ed	-	Reserv ed	Reserv ed	Reserved		ADIH_ CSYNC	ISD_ STOP EN	ADI_ LATCH _SET	ADV_ LATCH _SET	ADIL_ ON	ADIH_ ON
Initial	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Explanation	Reference
15	-		
14	-		
13	ADSWHY_EN	High-speed current ADC input switch enable 1: ON 0: OFF (Default)	
12	ADSWSD_EN	Low-speed current ADC input switch enable 1: ON 0: OFF (Default)	
11	Reserved	Please always set to "0".	
10	-		
9	Reserved	Please always set to "1".	
8	Reserved	Please always set to "0".	
[7:6]	Reserved	Please always set to "00".	
5	ADIH_CSYNC	Enable V-I sync function 1: Enable 0: Disable (Default)	
4	ISD_STOPEN	Low Speed Current ADC Stop Control 1: Disable Low Speed Current ADC for high speed current ADC operation. (Default) 0: Enable simultaneous operation high speed and low speed current ADC	
3	ADI_LATCH_SET	High-speed current ADC measurement data Latch timing switch 1: After issuing ADIH_LATCH, on-going 1 ADC cycle is completed and subsequently latched 0: After issuing ADIH_LATCH, recent available data is latched immediately (Default)	
2	ADV_LATCH_SET	Voltage measurement ADC measurement data Latch timing switch 1: After issuing ADV_LATCH, on-going 1 ADC cycle is completed and subsequently latched 0: After issuing ADV_LATCH, recent available data is latched immediately (Default)	
1	ADIL_ON	Enable Low-speed current ADC operation 1: Enable 0: Disable (Default)	
0	ADIH_ON	Enable High-speed current ADC operation 1: Enable 0: Disable (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x19 INRCV1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INR_CV[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W															

bit	Name	Explanation	Reference
[15:0]	INR_CV[15:0]	Selection of cell for open detection 1: Open Detection selected 0: Open Detection not selected (Default)	

Address: 0x1A INRCV2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	Reserved				INR_CV[17:16]		
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
[6:3]	Reserved	Please always set to "00000".	
2	INR_CV[17]	Selection of cell for open detection 1: Open Detection selected 0: Open Detection not selected (Default)	
1	INR_CV[16]	Selection of cell for open detection 1: Open Detection selected 0: Open Detection not selected (Default)	
0	INR_CV[16M]	Selection of cell for open detection 1: Open Detection selected 0: Open Detection not selected (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x1B INR_CTL_DIAG_EN

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ADIH_CSYNC_SEL[4:0]					FET_DIAG_EN	FET_DIAG_SEL[1:0]		-	DIAG_IHY_EN	DIAG_ISD_EN	-	-	-	-	NPD_INR
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W					R/W	R/W		R	R/W	R/W	R	R	R	R	R/W

bit	Name	Explanation	Reference
[15:11]	ADIH_CSYNC_SEL [4:0]	Cell selection for V-I sync function 0x11: Fast speed current measurement sync with Cell 17 voltage measurement ～ 0x01: Fast speed current measurement sync with Cell 1 voltage measurement 0x00, 0x17～0x1F : Prohibited	
10	FET_DIAG_EN	Enable Diagnostic check for CFET and DFET 1: Enable 0: Disable (Default)	
[9:8]	FET_DIAG_SEL[1:0]	Diagnostic check for CFET and DFET 00 : CFET ON check (Default) 01 : DFET ON check 10 : CFET OFF check 11 : DFET OFF check	
7	-		
6	DIAG_IHY_EN	Diagnosis for High Speed Current ADC 1: Enable 0: Disable (Default)	
5	DIAG_ISD_EN	Diagnosis for Low Speed Current ADC 1: Enable 0: Disable (Default)	
4	-		
3	-		
2	-		
1	-		
0	NPD_INR	Selection of open detection at Cell pins 1: Open Detection ON 0: Open Detection OFF(Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x1C STAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_GPIO3	ST_GPIO2	ST_GPIO1	Reserved	FDRV_DIS_ST	FDRV_CHG_ST	GPOH2_ST	GPOH1_ST	IADS_DONE	IADH_DONE	VAD_DONE	ST_INTM	ST_LP	ST_SDWN	ST_STBY	ST_ACT
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R

bit	Name	Explanation	Reference
15	ST_GPIO3	State of GPIO3 pin input (It is effective only at GPIO3_IE=1). 1: Input level “H” 0: Input level “L”	
14	ST_GPIO2	State of GPIO2 pin input (It is effective only at GPIO2_IE=1). 1: Input level “H” 0: Input level “L”	
13	ST_GPIO1	State of GPIO1 pin input (It is effective only at GPIO1_IE=1). 1: Input level “H” 0: Input level “L”	
12	Reserved	Please always set to "0".	
11	FDRV_DIS_ST	Discharge FET status 1: Discharge FET is ON 0: Discharge FET is OFF	
10	FDRV_CHG_ST	Charge FET status 1: Charge FET is ON 0: Charge FET is OFF	
9	GPOH2_ST	GPOH2 state 1: Output “L” 0: Hi-Z	
8	GPOH1_ST	GPOH1 state 1: Output “L” 0: Hi-Z	
7	IADS_DONE	Low-speed current ADC completion flag 1: Measurement completed 0: Measurement incomplete It is cleared to “0” by writing "1“.	
6	IADH_DONE	High-speed current ADC completion flag 1: Measurement completed 0: Measurement incomplete It is cleared to “0” by writing "1“.	
5	VAD_DONE	Voltage measurement ADC completion flag 1: Measurement completed 0: Measurement incomplete It is cleared to “0” by writing "1“.	
4	ST_INTM	Intermittent mode (Operation Mode) Flag 1: Intermittent Mode 0: Not in Intermittent Mode	
3	ST_LP	Low Power mode (Operation Mode) Flag 1: Low Power Mode 0: Not in Low Power Mode	
2	ST_SDWN	Shutdown mode(Operation Mode) Flag 1: Shutdown Mode 0: Not in Shutdown Mode.	
1	ST_STBY	Standby mode (Operation Mode) Flag 1: Standby Mode 0: Not in Standby Mode	
0	ST_ACT	Active mode (Operation Mode) Flag 1: Active Mode 0: Not in Active Mode	

Explanation of Registers

A.2 Detailed explanation

Address: 0x1D STAT2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_CV16SEL	ST_CV15SEL	ST_CV14SEL	ST_CV13SEL	ST_CV12SEL	ST_CV11SEL	ST_CV10SEL	ST_CV9SEL	ST_CV8SEL	ST_CV7SEL	ST_CV6SEL	ST_CV5SEL	ST_CV4SEL	ST_CV3SEL	ST_CV2SEL	ST_CV1SEL
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	ST_CV16SEL	ON / OFF setting status of cell 16 voltage measurement 1: ON 0: OFF	
14	ST_CV15SEL	ON / OFF setting status of cell 15 voltage measurement 1: ON 0: OFF	
13	ST_CV14SEL	ON / OFF setting status of cell 14 voltage measurement 1: ON 0: OFF	
12	ST_CV13SEL	ON / OFF setting status of cell 13 voltage measurement 1: ON 0: OFF	
11	ST_CV12SEL	ON / OFF setting status of cell 12 voltage measurement 1: ON 0: OFF	
10	ST_CV11SEL	ON / OFF setting status of cell 11 voltage measurement 1: ON 0: OFF	
9	ST_CV10SEL	ON / OFF setting status of cell 10 voltage measurement 1: ON 0: OFF	
8	ST_CV9SEL	ON / OFF setting status of cell 9 voltage measurement 1: ON 0: OFF	
7	ST_CV8SEL	ON / OFF setting status of cell 8 voltage measurement 1: ON 0: OFF	
6	ST_CV7SEL	ON / OFF setting status of cell 7 voltage measurement 1: ON 0: OFF	
5	ST_CV6SEL	ON / OFF setting status of cell 6 voltage measurement 1: ON 0: OFF	
4	ST_CV5SEL	ON / OFF setting status of cell 5 voltage measurement 1: ON 0: OFF	
3	ST_CV4SEL	ON / OFF setting status of cell 4 voltage measurement 1: ON 0: OFF	
2	ST_CV3SEL	ON / OFF setting status of cell 3 voltage measurement 1: ON 0: OFF	
1	ST_CV2SEL	ON / OFF setting status of cell 2 voltage measurement 1: ON 0: OFF	
0	ST_CV1SEL	ON / OFF setting status of cell 1 voltage measurement 1: ON 0: OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x1E STAT3

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	ST_CV17SEL
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0	ST_CV17SEL	ON / OFF setting status of cell 17 voltage measurement 1: ON 0: OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x1F_STAT4

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	ST_TMONI5SEL	ST_TMONI4SEL	ST_TMONI3SEL	ST_TMONI2SEL	ST_TMONI1SEL	ST_GPAD2SEL	ST_GPAD1SEL	ST_VPACKSEL	ST_VDD18SEL	ST_REGEXTSEL	ST_VDD55SEL	Reserved	ST_VREF2SEL
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	ST_TMONI5SEL	ON / OFF setting status of TMONI5 measurement 1: ON 0: OFF	
11	ST_TMONI4SEL	ON / OFF setting status of TMONI4 measurement 1: ON 0: OFF	
10	ST_TMONI3SEL	ON / OFF setting status of TMONI3 measurement 1: ON 0: OFF	
9	ST_TMONI2SEL	ON / OFF setting status of TMONI2 measurement 1: ON 0: OFF	
8	ST_TMONI1SEL	ON / OFF setting status of TMONI1 measurement 1: ON 0: OFF	
7	ST_GPAD2SEL	ON / OFF setting status of GPIO2 measurement 1: ON 0: OFF	
6	ST_GPAD1SEL	ON / OFF setting status of GPIO1 measurement 1: ON 0: OFF	
5	ST_VPACKSEL	ON / OFF setting status of VPACK measurement 1: ON 0: OFF	
4	ST_VDD18SEL	ON/OFF setting condition for internal VDD18 voltage measurement 1: ON 0: OFF	
3	ST_REGEXTSEL	ON/OFF setting condition for REG_EXT voltage measurement 1: ON 0: OFF	
2	ST_VDD55SEL	ON/OFF setting condition for VDD55 voltage measurement 1: ON 0: OFF	
1	Reserved		
0	ST_VREF2SEL	ON/OFF setting condition for VREF2 voltage measurement 1: ON 0: OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x20 ANA_CTL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	Customer Reserved								Reserved			NPD_LDM	OVP_F_SET_REGEXT	UVP_F_SET_REGEXT	LDM_SHRT
Initial	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	Reserved	Read only bit, fix to “1”	
14:7	Customer Reserved	Reserved for customer specific usage	
6:4	Reserved	Please always set to "000".	
3	NPD_LDM	LDM load or load short function enable 1: Enable 0: Disable (Default)	
2	OVP_F_SET_REGEXT	Transition to shutdown when abnormal high voltage is detected at REGEXT 1: No change (Default) 0: Shutdown immediately	
1	UVP_F_SET_REGEXT	Transition to shutdown when abnormal low voltage is detected at REGEXT 1: No change (Default) 0: Shutdown immediately	
0	LDM_SHRT	LDM current drive selection 1: 400uA output current 0: 50uA output current (Default)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x21 OTHSTAT

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ST_SCD	ST_OCD	ST_OCC	SPI_F	Reserved	MUX1A_F	-	-	SCD_F	OCD_F	OCC_F	TSD_F	CFETON_F	CFETOFF_F	DFETON_F	DFETOFF_F
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Explanation	Reference
15	ST_SCD	SCD detection with alarm assertion 1: SCD detected 0: SCD not detected If SCD is detected, ST_SCD=1 and it is cleared by writing “1”. ALARM1 pin outputs LOW when ST_SCD=1.	
14	ST_OCD	OCD detection with alarm assertion 1: OCD detected 0: OCD not detected If OCD is detected, ST_OCD=1 and it is cleared by writing “1”. Either ALARM1 pin or ALARM2 pin outputs LOW when ST_OCD=1.	
13	ST_OCC	OCC detection with alarm assertion 1: OCC detected 0: OCC not detected If OCC is detected, ST_OCC=1 and it is cleared by writing “1”. Either ALARM1 pin or ALARM2 pin outputs LOW when ST_OCC=1.	
12	SPI_F	SPI communication error flag 1: Communication Error 0: No Communication Error If communication error (CRC error) is detected, SPI_F=1. It is cleared by writing "1".	
11	Reserved	Please always set to "0".	
10	MUX1A_F	Error for sequence control counter measurement system diagnostic check 1: Abnormal 0: Normal	
9	-		
8	-		
7	SCD_F	SCD detection flag 1: SCD detected (auto cleared when short circuit condition is removed) 0: SCD not detected	
6	OCD_F	OCD detection flag 1: OCD detected (auto cleared when over current at discharge condition is removed) 0: OCD not detected	
5	OCC_F	OCC detection flag 1: OCC detected (auto cleared when over current at charge condition is removed) 0: OCC not detected	
4	TSD_F	TSD detection flag 1: TSD detected 0: TSD not detected	
3	CFETON_F	Output bit to indicate CFET ON diagnostic check result 1: OK 0: NG (Default 0 if function is off)	
2	CFETOFF_F	Output bit to indicate CFET OFF diagnostic check result 1: OK 0: NG (Default 0 if function is off)	
1	DFETON_F	Output bit to indicate DFET ON diagnostic check result 1: OK 0: NG (Default 0 if function is off)	
0	DFETOFF_F	Output bit to indicate DFET OFF diagnostic check result 1: OK 0: NG (Default 0 if function is off)	

Explanation of Registers

A.2 Detailed explanation

Address: 0x22 OVSTAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OV16_F	OV15_F	OV14_F	OV13_F	OV12_F	OV11_F	OV10_F	OV9_F	OV8_F	OV7_F	OV6_F	OV5_F	OV4_F	OV3_F	OV2_F	OV1_F
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Name	Explanation	Reference
15	OV16_F	Cell 16 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
14	OV15_F	Cell 15 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
13	OV14_F	Cell 14 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
12	OV13_F	Cell 13 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
11	OV12_F	Cell 12 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
10	OV11_F	Cell 11 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
9	OV10_F	Cell 10 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
8	OV9_F	Cell 9 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
7	OV8_F	Cell 8 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
6	OV7_F	Cell 7 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
5	OV6_F	Cell 6 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
4	OV5_F	Cell 5 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
3	OV4_F	Cell 4 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
2	OV3_F	Cell 3 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
1	OV2_F	Cell 2 OV detection output (*Automatic update) 1: Abnormal 0: Normal	
0	OV1_F	Cell 1 OV detection output (*Automatic update) 1: Abnormal 0: Normal	

Explanation of Registers

A.2 Detailed explanation

Address: 0x23 OVSTAT2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	OV17_F
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0	OV17_F	Cell 17 OV detection output (*Automatic update) 1: Abnormal 0: Normal	

Explanation of Registers

A.2 Detailed explanation

Address: 0x24 UVSTAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV16_F	UV15_F	UV14_F	UV13_F	UV12_F	UV11_F	UV10_F	UV9_F	UV8_F	UV7_F	UV6_F	UV5_F	UV4_F	UV3_F	UV2_F	UV1_F
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	UV16_F	Cell 16 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
14	UV15_F	Cell 15 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
13	UV14_F	Cell 14 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
12	UV13_F	Cell 13 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
11	UV12_F	Cell 12 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
10	UV11_F	Cell 11 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
9	UV10_F	Cell 10 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
8	UV9_F	Cell 9 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
7	UV8_F	Cell 8 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
6	UV7_F	Cell 7 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
5	UV6_F	Cell 6 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
4	UV5_F	Cell 5 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
3	UV4_F	Cell 4 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
2	UV3_F	Cell 3 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
1	UV2_F	Cell 2 UV detection output (*Automatic update) 1: Abnormal 0: Normal	
0	UV1_F	Cell 1 UV detection output (*Automatic update) 1: Abnormal 0: Normal	

Explanation of Registers

A.2 Detailed explanation

Address: 0x25 UVSTAT2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	UV17_F
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0	UV17_F	Cell 17 UV detection output 1: Abnormal 0: Normal *Automatic update	

Explanation of Registers

A.2 Detailed explanation

Address: 0x26 BIASSTAT

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	Reserved	Reserved	HVREF2	LVREF2	HBIAS1A	HBIAS1D	LBIAS1D	HBIAS2A	HBIAS2D	LBIAS2D	HBIAS3A	HBIAS3D	LBIAS3D
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	Reserved		
11	Reserved		
10	HVREF2	VREF2 OV Flag 1: OV detected 0: OV not detected	
9	LVREF2	VREF2 UV Flag 1: UV detected 0: UV not detected	
8	HBIAS1A	VDD18 Analog OV Flag 1: OV detected 0: OV not detected	
7	HBIAS1D	VDD18 Digital OV Flag 1: OV detected 0: OV not detected	
6	LBIAS1D	VDD18 Digital UV Flag 1: UV detected 0: UV not detected	
5	HBIAS2A	REG_EXT Analog OV Flag 1: OV detected 0: OV not detected	
4	HBIAS2D	REG_EXT Digital OV Flag 1: OV detected 0: OV not detected	
3	LBIAS2D	REG_EXT Digital UV Flag 1: UV detected 0: UV not detected	
2	HBIAS3A	VDD55 Analog OV Flag 1: OV detected 0: OV not detected	
1	HBIAS3D	VDD55 Digital OV Flag 1: OV detected 0: OV not detected	
0	LBIAS3D	VDD55 Digital UV Flag 1: UV detected 0: UV not detected	

Explanation of Registers

A.2 Detailed explanation

Address: 0x27 STAT5

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDM_DET_F	VPC_DET_F	WDT_F	CUR_H_F	LDM_H_F	LDM_L_F	VPC_H_F	VPC_L_F	-	-	-	FUSEB_F	ST_OTH	ST_BIAS	ST_OV	ST_UV
Initial	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	LDM_DET_F	Status of Load 1: Load is detected 0: No load	
14	VPC_DET_F	Status of VPC 1: VPC pin is "H" 0: VPC pin is "L"	
13	WDT_F	Flag for watchdog timer 1: WDT will be timeout in 100ms 0: WDT timeout is not detected (Default) It is cleared by writing "1".	
12	CUR_H_F	Flag for event of Current from "L" → "H" 1: Event is detected 0: Event is not detected (Default) It is cleared by writing "1".	
11	LDM_H_F	Flag for event of Load from no load → load detected 1: Event is detected (AFE return to Active mode) 0: Event is not detected (Default) It is cleared by writing “1”.	
10	LDM_L_F	Flag for event of Load from load detected → load released 1: Event is detected 0: Event is not detected (Default) It is cleared by writing “1”.	
9	VPC_H_F	Flag for event of VPC pin from "L" → "H" 1: Event is detected 0: Event is not detected (Default) It is cleared by writing "1".	
8	VPC_L_F	Flag for event of VPC pin from "H" → "L" 1: Event is detected 0: Event is not detected (Default) It is cleared by writing "1".	
7	-		
6	-		
5	-		
4	FUSEB_F	Fuse blow status 1: Fuse blow is completed 0: Fuse blow not completed (Default)	
3	ST_OTH	Others fault status display 1: Other fault detected. 0: No Other fault If any of the bit in OTHSTAT register is "1", ST_OTH=1.	
2	ST_BIAS	BIAS fault status display 1: BIAS fault detected. 0: No BIAS fault If any of the bit in BIASSTAT register is "1", ST_BIAS=1.	
1	ST_OV	OV detection status display 1: OV detected 0: OV not detected If OV is detected in any cell, ST_OV=1.	
0	ST_UV	UV detection status display 1: UV detected 0: UV not detected If UV is detected in any cell, ST_UV=1.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x28_CV01_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV01_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV01_AD[15:0]	Cell 1 Voltage Measurement output Value: 0x3FFF: 4.999695V ～ 0x2000: 2.5V ～ 0x0001: 0.000305V 0x0000: 0V Measured Voltage = Value x 0.000305V * Bit15 and 14 are always "0"	

Address: 0x29_CV02_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV02_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV02_AD[15:0]	Cell 2 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x2A_CV03_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV03_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV03_AD[15:0]	Cell 3 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x2B_CV04_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV04_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV04_AD[15:0]	Cell 4 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x2C CV05_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV05_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV05_AD[15:0]	Cell 5 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x2D CV06_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV06_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV06_AD[15:0]	Cell 6 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x2E CV07_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV07_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV07_AD[15:0]	Cell 7 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x2F CV08_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV08_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV08_AD[15:0]	Cell 8 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x30_CV09_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV09_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV09_AD[15:0]	Cell 9 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x31_CV10_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV10_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV10_AD[15:0]	Cell 10 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x32_CV11_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV11_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV11_AD[15:0]	Cell 11 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x33_CV12_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV12_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV12_AD[15:0]	Cell 12 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x34_CV13_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV13_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV13_AD[15:0]	Cell 13 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x35_CV14_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV14_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV14_AD[15:0]	Cell 14 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x36_CV15_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV15_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV15_AD[15:0]	Cell 15 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x37_CV16_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV16_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV16_AD[15:0]	Cell 16 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x38_CV17_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CV17_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CV17_AD[15:0]	Cell 17 Voltage Measurement output * Refer to CV01_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x3E VPACK_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VPACK_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	VPACK_AD[15:0]	VPACK Voltage Measurement output Value: 0x3FFF: 109.9933V ～ 0x2000: 55.001088V ～ 0x0001: 0.006714V 0x0000: 0V Measured Voltage = Value x 0.006714V * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x3F TMONI1_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMONI1_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	TMONI1_AD[15:0]	TMONI1 Voltage Measurement output Value: 0x3FFF: 4.999695V ～ 0x2000: 2.5V ～ 0x0001: 0.000305V 0x0000: 0V Measured Voltage = Value x 0.000305V * Bit15 and 14 are always "0"	

Address: 0x40 TMONI2_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMONI2_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	TMONI2_AD[15:0]	TMONI2 Voltage Measurement output * Refer to TMONI1_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x41 TMONI3_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMONI3_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	TMONI3_AD[15:0]	TMONI3 Voltage Measurement output * Refer to TMONI1_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x42 TMONI4_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMONI4_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	TMONI4_AD[15:0]	TMONI4 Voltage Measurement output * Refer to TMONI1_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Address: 0x43 TMONI5_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TMONI5_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	TMONI5_AD[15:0]	TMONI5 Voltage Measurement output * Refer to TMONI1_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x44 VDD55_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDD55_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	VDD55_AD[15:0]	VDD55 Voltage Measurement output Value: 0x3FFF: 7.499542V ～ 0x2000: 3.75V ～ 0x0001: 0.000458V 0x0000: 0V Measured Voltage = Value x 0.000458V * Bit15 and 14 are always "0"	

Address: 0x45 GPIO1_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO1_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	GPIO1_AD[15:0]	GPIO1 Voltage Measurement output Value: 0x3FFF: 4.999695V ～ 0x2000: 2.5V ～ 0x0001: 0.000305V 0x0000: 0V Measured Voltage = Value x 0.000305V * Bit15 and 14 are always "0"	

Address: 0x46 GPIO2_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO2_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	GPIO2_AD[15:0]	GPIO2 Voltage Measurement output * Refer to GPIO1_AD[15:0] explanation for values * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x47 CVIH_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CVIH_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CVIH_AD[15:0]	High-speed current ADC Measurement output Value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V 0xFFFF: -0.005493mV ～ 0x8001: -179.994507mV data * 360mV/2^16 0x8000: -180mV Voltage/step = 0.005493mV Measured voltage = 2's complement	

Address: 0x48 CVIL_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CVIL_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CVIL_AD[15:0]	Low-speed current ADC measurement output Value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V 0xFFFF: -0.005493mV ～ 0x8001: -179.994507mV data * 360mV/2^16 0x8000: -180mV Voltage/step = 0.005493mV Measured voltage = 2's complement	

Explanation of Registers

A.2 Detailed explanation

Address: 0x49 VDD18_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VDD18_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	VDD18_AD[15:0]	VDD18 Voltage Measurement output Value: 0x3FFF: 4.999695V ～ 0x2000: 2.5V ～ 0x0001: 0.000305V 0x0000: 0V Measured Voltage = Value x 0.000305V * Bit15 and 14 are always "0"	

Address: 0x4A REGEXT_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REGEXT_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	REGEXT_AD[15:0]	REGEXT Voltage Measurement output Value: 0x3FFF: 7.499542V ～ 0x2000: 3.75V ～ 0x0001: 0.000458V 0x0000: 0V Measured Voltage = Value x 0.000458V * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x4B VREF2_AD

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VREF2_AD[15:0]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	VREF2_AD[15:0]	VREF2 Voltage Measurement output Value: 0x3FFF: 4.999695V ～ 0x2000: 2.5V ～ 0x0001: 0.000305V 0x0000: 0V Measured Voltage = Value x 0.000305V * Bit15 and 14 are always "0"	

Explanation of Registers

A.2 Detailed explanation

Address: 0x4D OVL_STAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OV16_LF	OV15_LF	OV14_LF	OV13_LF	OV12_LF	OV11_LF	OV10_LF	OV9_LF	OV8_LF	OV7_LF	OV6_LF	OV5_LF	OV4_LF	OV3_LF	OV2_LF	OV1_LF
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	OV16_LF	Cell 16 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
14	OV15_LF	Cell 15 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
13	OV14_LF	Cell 14 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
12	OV13_LF	Cell 13 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
11	OV12_LF	Cell 12 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
10	OV11_LF	Cell 11 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
9	OV10_LF	Cell 10 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
8	OV9_LF	Cell 9 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
7	OV8_LF	Cell 8 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x4D OVL_STAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OV16_LF	OV15_LF	OV14_LF	OV13_LF	OV12_LF	OV11_LF	OV10_LF	OV9_LF	OV8_LF	OV7_LF	OV6_LF	OV5_LF	OV4_LF	OV3_LF	OV2_LF	OV1_LF
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
6	OV7_LF	Cell 7 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
5	OV6_LF	Cell 6 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
4	OV5_LF	Cell 5 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
3	OV4_LF	Cell 4 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
2	OV3_LF	Cell 3 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
1	OV2_LF	Cell 2 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	
0	OV1_LF	Cell 1 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x4E OVL_STAT2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	OV17_LF
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	Reserved	Please always set to "0".	
4	Reserved	Please always set to "0".	
3	Reserved	Please always set to "0".	
2	Reserved	Please always set to "0".	
1	Reserved	Please always set to "0".	
0	OV17_LF	Cell 17 OV detection flag 1: OV detected 0: OV not detected (Default) * If OV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4D or 0x4E.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x4F_UVL_STAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV16_LF	UV15_LF	UV14_LF	UV13_LF	UV12_LF	UV11_LF	UV10_LF	UV9_LF	UV8_LF	UV7_LF	UV6_LF	UV5_LF	UV4_LF	UV3_LF	UV2_LF	UV1_LF
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	UV16_LF	Cell 16 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
14	UV15_LF	Cell 15 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
13	UV14_LF	Cell 14 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
12	UV13_LF	Cell 13 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
11	UV12_LF	Cell 12 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
10	UV11_LF	Cell 11 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
9	UV10_LF	Cell 10 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
8	UV9_LF	Cell 9 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
7	UV8_LF	Cell 8 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x4F UVL_STAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UV16_LF	UV15_LF	UV14_LF	UV13_LF	UV12_LF	UV11_LF	UV10_LF	UV9_LF	UV8_LF	UV7_LF	UV6_LF	UV5_LF	UV4_LF	UV3_LF	UV2_LF	UV1_LF
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Explanation	Reference
6	UV7_LF	Cell 7 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
5	UV6_LF	Cell 6 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
4	UV5_LF	Cell 5 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
3	UV4_LF	Cell 4 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
2	UV3_LF	Cell 3 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
1	UV2_LF	Cell 2 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	
0	UV1_LF	Cell 1 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x50 UVL_STAT2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	UV17_LF
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
5	Reserved	Please always set to "0".	
4	Reserved	Please always set to "0".	
3	Reserved	Please always set to "0".	
2	Reserved	Please always set to "0".	
1	Reserved	Please always set to "0".	
0	UV17_LF	Cell 17 UV detection flag 1: UV detected 0: UV not detected (Default) * If UV is detected, the related flag will become “1”. To clear any flag in this register, write “0x0000” to register 0x4F or 0x50.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x51 CBSTAT1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CB_ST[16:1]															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R															

bit	Name	Explanation	Reference
[15:0]	CB_ST[16:1]	Individual cell balance control status display 1: Cell balance ON 0: Cell balance OFF	

Address: 0x52 CBSTAT2

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	-	-	Reserved					CB_ST[17]
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R					

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
7	-		
6	-		
[5:1]	Reserved	Please always set to "00000".	
0	CB_ST[17]	Individual cell balance control status display 1: Cell balance ON 0: Cell balance OFF	

Explanation of Registers

A.2 Detailed explanation

Address: 0x53 FUSE_BLOW

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-	FUSE_BLOW[7:0]							
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R/W							

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
9	-		
8	-		
[7:0]	FUSE_BLOW[7:0]	Fuse blow function activation * Fuse blow function by MCU control will be activated when "0xFB" is written to this register. Not dependent on Cell and current fault algorithm.	

Explanation of Registers

A.2 Detailed explanation

Address: 0x54 Reserved

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	Reserved														
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R/W	R/W														

bit	Name	Explanation	Reference
15	Reserved	Please always set to "0".	
[14:0]	Reserved	Please always set to "000000000000000".	

Address: 0x55 AUTO_ITHL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	AUTO_ITHL[14:0]														
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R/W														

bit	Name	Explanation	Reference
15	-		
[14:0]	AUTO_ITHL[14:0]	15 bit to set detection current level to enter Low power auto mode (compare by IADC_fast) Value: 0x7FFF: 179.994507mV ～ 0x0001: 0.005493mV 0x0000: 0V Voltage/step = 0.005493mV	

Explanation of Registers

A.2 Detailed explanation

Address: 0x56 VDD55_CTL

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	Reserved	R55GAIN[2:0]			R55TC[2:0]			R55VC[2:0]			Reserved
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R/W	R/W			R/W			R/W			R/W

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	Reserved	Please always set to "0".	
[9:7]	R55GAIN[2:0]	NPN Hfe(Gain) Adjustment (Vary the output Base current to drive the external BJT based on required NPN BJT HFE specs) 000: IB = 0.89mA (Default) 001: IB = 0.79mA 010: IB = 0.7mA 011: IB = 0.64mA 100: IB = 2.2mA 101: IB = 1.65mA 110: IB = 1.32mA 111: IB = 1.09mA	
[6:4]	R55TC[2:0]	NPN Temp coefficient adjustment against external NPN beta Temp variation 000: IB% change = +33% (-25deg to 25deg) ; -40% (25deg to 125deg) (Default) 001: IB% change = +28% (-25deg to 25deg) ; -35% (25deg to 125deg) 010: IB% change = +23% (-25deg to 25deg) ; -30% (25deg to 125deg) 011: IB% change = +18% (-25deg to 25deg) ; -25% (25deg to 125deg) 100: IB% change = +50% (-25deg to 25deg) ; -57% (25deg to 125deg) 101: IB% change = +46% (-25deg to 25deg) ; -53% (25deg to 125deg) 110: IB% change = +42% (-25deg to 25deg) ; -49% (25deg to 125deg) 111: IB% change = +38% (-25deg to 25deg) ; -44% (25deg to 125deg)	
[3:1]	R55VC[2:0]	NPN VCE (Supply) coefficient adjustment against external NPN beta supply variation 000: IB% change from 30V to 62.9V = -16.5% (Default) IB% change from 62.9V to 85V = -10.4% 001: IB% change from 30V to 62.9V = -20.7% IB% change from 62.9V to 85V = -13.4% 010: IB% change from 30V to 62.9V = -25.4% IB% change from 62.9V to 85V = -16.9% 011: IB% change from 30V to 62.9V = -30.5% IB% change from 62.9V to 85V = -20.6% 100: IB% change from 30V to 62.9V = -2.7% IB% change from 62.9V to 85V = -2.3% 101: IB% change from 30V to 62.9V = -5.1% IB% change from 62.9V to 85V = -4.3% 110: IB% change from 30V to 62.9V = -10.0% IB% change from 62.9V to 85V = -6.6% 111: IB% change from 30V to 62.9V = -16.5% IB% change from 62.9V to 85V = -10.4%	
0	Reserved	Please always set to "0".	

Explanation of Registers

A.2 Detailed explanation

Address: 0x57 TMONI1

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PULLUP_TMONI1[9:0]									
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
15	-		
14	-		
13	-		
12	-		
11	-		
10	-		
[9:0]	PULLUP_TMONI1[9:0]	TMONI1 pin pull-up resistance value (absolute value) * Refer to Application Notes Chapter 9 for details.	

Address: 0x58 TMONI23

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLUP_TMONI3[7:0]								PULLUP_TMONI2[7:0]							
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
[15:8]	PULLUP_TMONI3[7:0]	TMONI3 pin pull-up resistance value (difference) * Refer to Application Notes Chapter 9 for details.	
[7:0]	PULLUP_TMONI2[7:0]	TMONI2 pin pull-up resistance value (difference) * Refer to Application Notes Chapter 9 for details.	

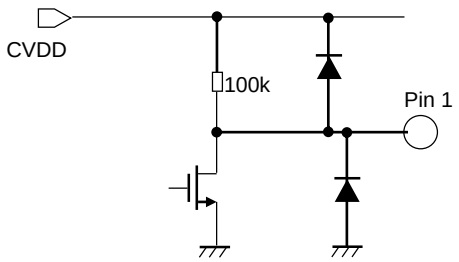
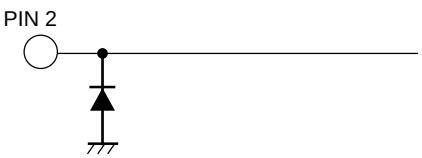
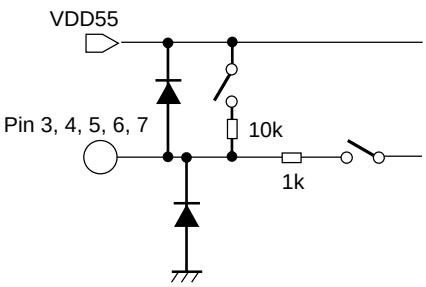
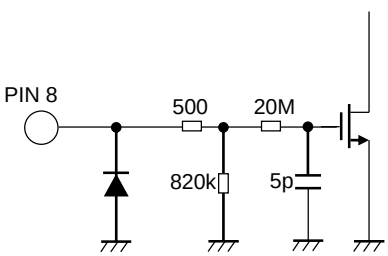
Address: 0x59 TMONI45

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PULLUP_TMONI5[7:0]								PULLUP_TMONI4[7:0]							
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

bit	Name	Explanation	Reference
[15:8]	PULLUP_TMONI5[7:0]	TMONI5 pin pull-up resistance value (difference) * Refer to Application Notes Chapter 9 for details.	
[7:0]	PULLUP_TMONI4[7:0]	TMONI4 pin pull-up resistance value (difference) * Refer to Application Notes Chapter 9 for details.	

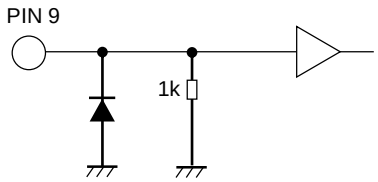
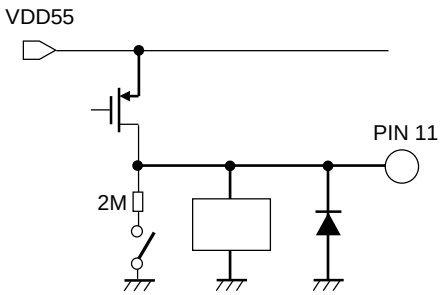
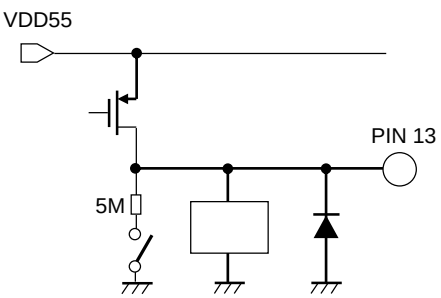
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
1	DC		Power ON Reset Output Pin (NRST)
2	DC		Digital IO Power Supply Pin (CVDD)
3 4 5 6 7	DC		Analog Voltage Input Pin (TMONI1-5)
8	DC		Shutdown Control Signal Input Pin (SHDN)

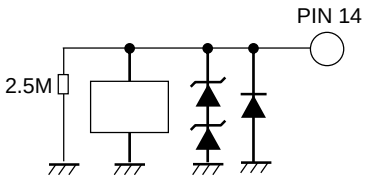
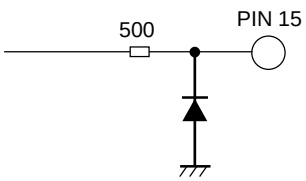
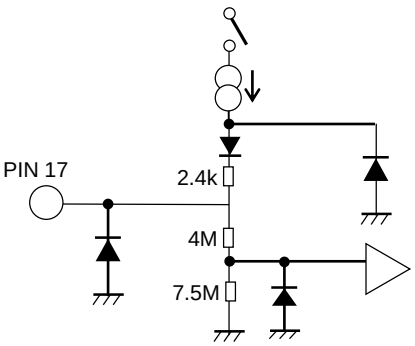
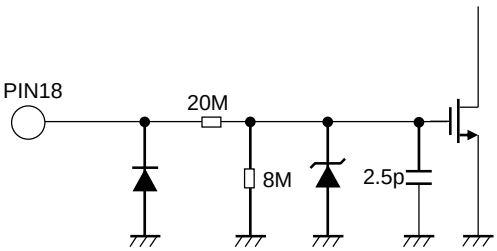
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
9	DC		Test Mode Setting Pin (MODE)
11	DC		Internal Regulator Pin (VDD18)
12	DC		REGSEL
13	DC		REGEXT

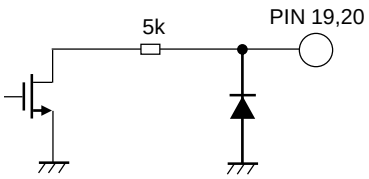
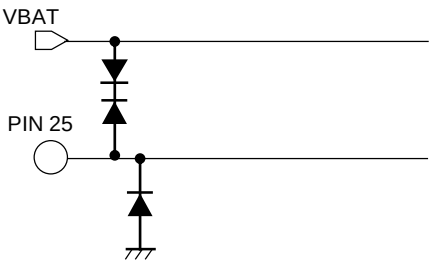
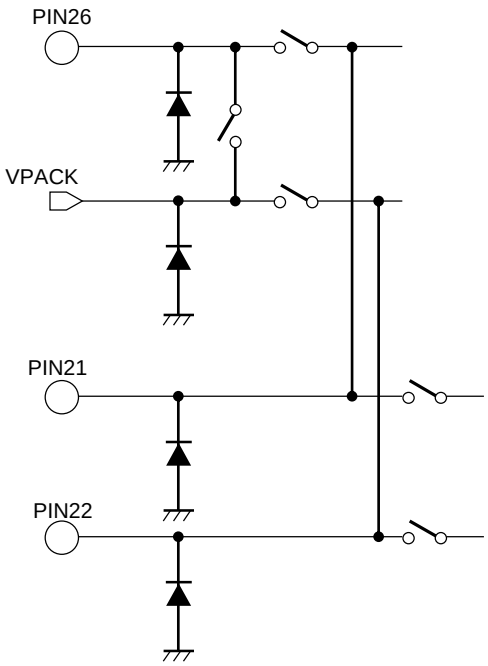
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
14	DC		5.5V Regulator Pin (VDD55)
15	DC		5.5V Regulator External NPN Base Pin (REGB)
17	DC		LDM
18	DC		Wake Up Signal Pin (VPC)

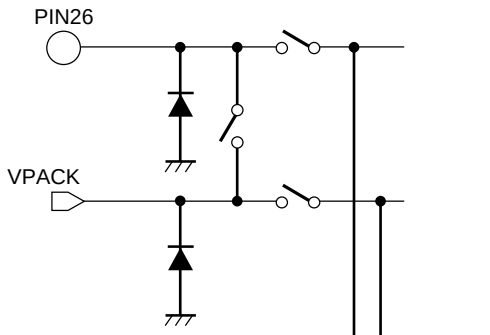
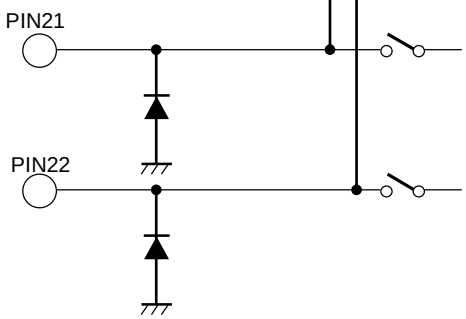
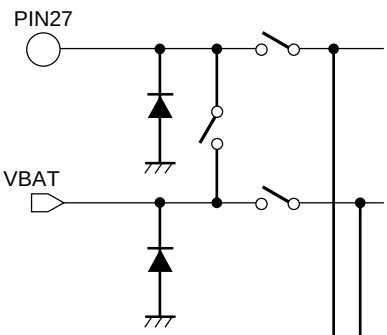
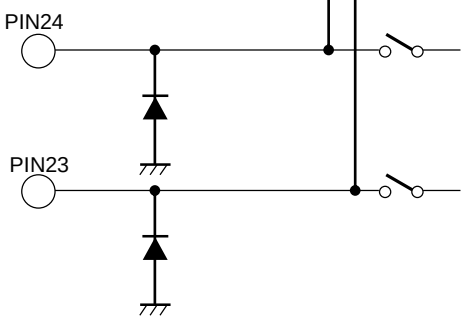
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
19 20	DC		High Breakdown Voltage GPO Pin (GPOH2/GPOH1)
25	DC		VPACK
26	AC		External DIS_FET (NMOS) Gate Driver Pin (DIS)
21	AC		Charge Pump Capacitor Pin (CP1)

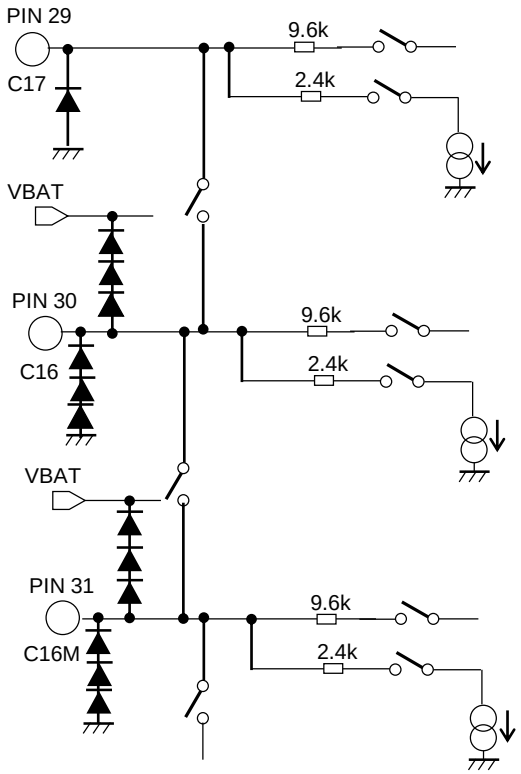
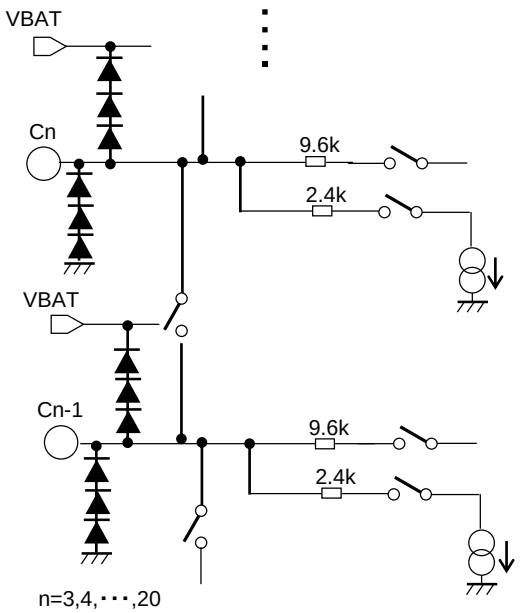
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
22	AC		Charge Pump Capacitor Pin (CN1)
23	AC		Charge Pump Capacitor Pin (CN2)
24	AC		Charge Pump Capacitor Pin (CP2)
27	AC		External CHG_FET (NMOS) Gate Driver Pin (CHG)

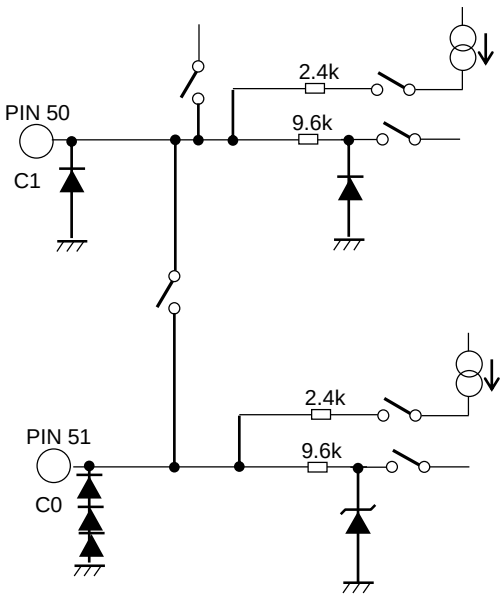
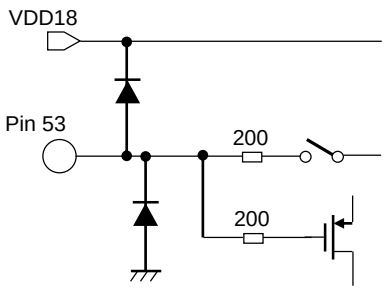
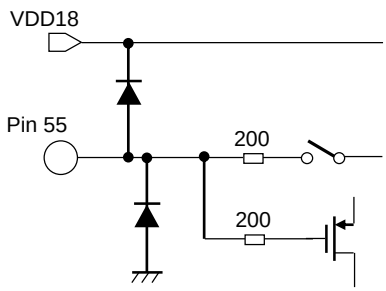
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
29	DC		Cell Voltage Input Pin (C17)
30	DC		Cell Voltage Input Pin (C16)
31 36 37 38 39 40 41 42 43 44 45 46 47 48 49	DC DC		Cell Voltage Input Pin (C16M, C15, C14…C2)

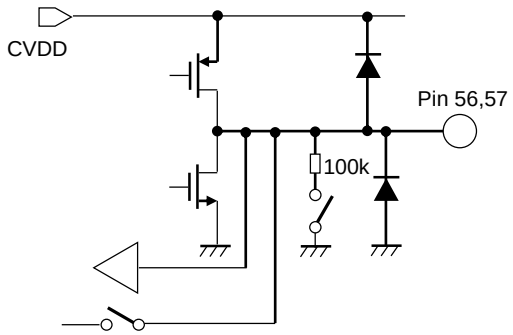
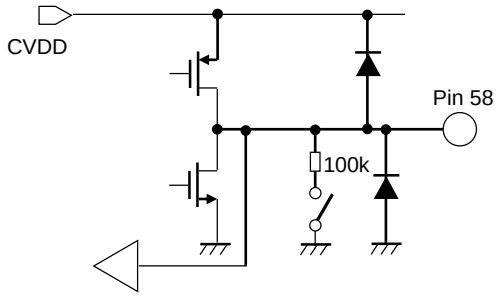
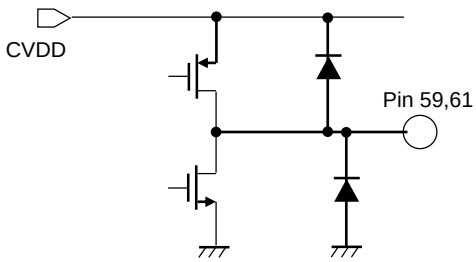
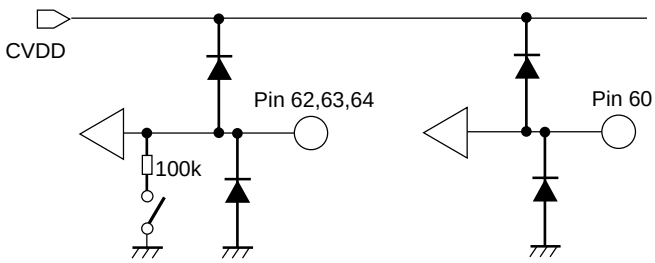
Input and Output Pin Circuit Diagram

Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

Pin No.	Waveform / voltage	Internal Circuit	Description
50	DC		Cell Voltage Input Pin (C1)
51	DC		Cell Voltage Input Pin (C0)
53	DC		Shunt Current Monitor Pin (+ve) (SRP)
55	DC		Shunt Current Monitor Pin (-ve) (SRN)

Input and Output Pin Circuit Diagram

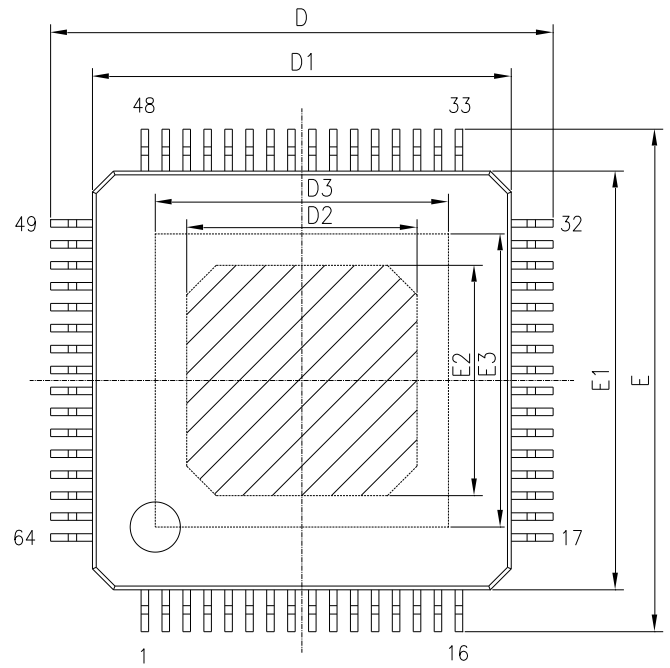
Note) The characteristics listed below are reference values based on the design: it is not a guaranteed value.

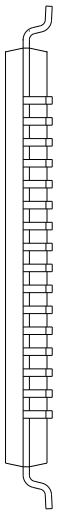
Pin No.	Waveform / voltage	Internal Circuit	Description
56 57	DC DC		GPIO1/2 Pin (GPIO1/GPIO2)
58	DC		GPIO3 Pin (GPIO3)
59 61	DC		Digital Output Pin (ALARM1,SDO)
60 62 63 64	DC		Digital Input Pin (FETOFF, SDI,SCL,SEN)

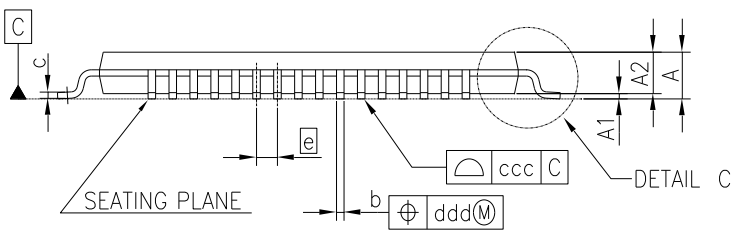
Dimensions

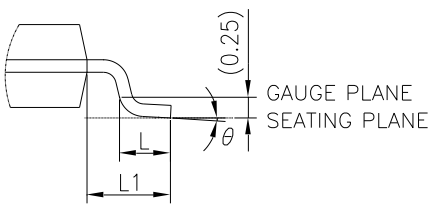
• TQFP 64L 10x10mm², Thickness 1mm, Lead Pitch 0.5mm, Lead Length 1mm, EP Size 5.5x5.5mm

Unit: mm









DETAIL C

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	0.10	0.20
A2		1.00REF	
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
D2	5.50	–	–
D3	–	–	7.00
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
E2	5.50	–	–
E3	–	–	7.00
L	0.45	0.60	0.75
L1		1.00REF	
b	0.15	0.20	0.25
c	0.10	0.15	0.20
e		0.50BSC	
ddd		0.10	
ccc		0.10	
θ	0.0°	–	8.0°

IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for measuring battery cell voltage in automotive application.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin - VBAT short, output pin – CVDD fault (Power supply fault), output pin-GND short (Ground fault), output-to-output-pin short (load short), or leakage current between pins. Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VBAT short, output pin to CVDD short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Verify the risks which might be caused by the malfunctions of external components.

Revision History

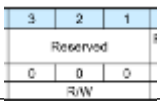
Control Number Rev 1.00

Date	Page	Item	Before	After
25 Dec 2020	—	Initial Release	—	—

Control Number rev 1.01

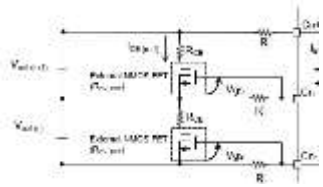
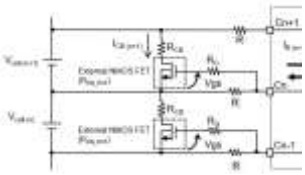
Date	Page	Item	Before	After
Jan Feb 2021	16,22	Bottom note		Added note *1
	23	Bottom note *3 updated		REGEXT can be used for as power supply for CVDD pin and external circuit. 1uF capacitor (CREGEXT) is necessary at REGEXT output. It is recommended to connect a maximum of 1uF capacitor for CVDD pin and external circuit, which is compatible with default CVDD55 and VDD55 NPN device (Diodes Inc MJD340) If it is necessary to increase these total capacitor value, the capacitor CVDD55 must be increased proportionally with about 5 times ratio to ensure stability. Please note start-up time of VDD55 and REGEXT would increase proportionally by doing this.
	121		The value decoded should be around +100mV for both high speed and slow speed current ADC to ensure proper operation.	The value decoded should be around +100mV for both high speed and slow speed current ADC to ensure proper operation. Current diagnostic check value will be able to be measured by internal current ADC to be within ±10mV from 100mV during normal operation.
	6	Specs for I_{BAT5}	Min: 0uA Typ: -- Max: 1uA	Min: -- Typ: 0uA Max: 1uA

Control Number Rev 1.02

Date	Page	Item	Before	After
Mar 2021	25	Added description of startup waveform for CVDD=REGEXT case	--	Added description at section 2.2 and added waveform for Fig 2.21.a and Fig 2.2.1b
	143	Added description on SPI command for case (3) of WDT expiry	--	Added recommendation of command type before second WDT expiry
	154	Added description for soft reset description at register table	Soft Reset 1: Normal operation (Default) 0: Reset * It returns to "1" automatically after writing "0".	Soft Reset 1: Normal operation (Default) 0: Reset (Soft -reset is used to reset all registers to default setting.) * It returns to "1" automatically after writing "0".
	103	Update SCD/OCD/OCC_F and ST_SCD/OCD/OCC address	-	SCD_F flag (address 0x21[7]) OCD_F flag (address 0x21[6]) OCC_F flag (address 0x21[5]) ST_SCD(address 0x21[15]) ST_OCD(address 0x21[14]) ST_OCC(address 0x21[13])
	32	Update ACTV_DLY default	Default is 1 cycle	Default is 2 cycle
	183	Added bit 15 description	Bit 15 description: Please always set to "0000000000000000".	Bit 15 description: Read only bit, fix to “1”
	103	■Flag set Voltage Flag	UVn_LF flag (address 0x4F[15:0]; address 0x4F[0])	UVn_LF flag (address 0x4F[15:0]; address 0x50[0])
	211			
	105	Paragraph 4	… and ST_OV flag (STAT:bp9)) …	… and ST_OV flag (address 0x27[1]) …

Revision History

Control Number Rev 1.03

Date	Page	Item	Before	After
31 May 2021	64	Added R_G resistor at MOSFET gate on Fig 8.1.2		
	161	Change register timing for DLY_FUSE_1C[2:0] & DLY_FUSE_1V[2:0] for bit 101 setting	120ms	1200ms
	114	*GPOH2_EN* flag address	0x04[1]	0x10[1]
	93;96	ADIH_LATCH flag address ADV_LATCH flag address	0x18[3] 0x18[3]	0x0C[1] 0x0C[0]
	94;97	ADIL_LATCH flag address IADL_DONE naming	0x18[3] IADL_DONE	0x0C[2] IADS_DONE
	99,100	ADIH_CSYNC_SEL flag address	0x1B[4:0]	0x1B[15:11]
	69	latched to data register "0x28~0x4C" by setting ADV_LATCH flag	0x28~0x4C	0x28~0x4B
	6 ~ 15	Added Ambient Temp Ta value in the header portion	--	T_a = 25℃±2℃
	5	Power dissipation rating	38.6 'C/W	37.7 'C/W
	30		** This function can be selectable to be ON/OFF by registers. In the event both LDM and VPC detection are set to OFF, the system will automatically select VPC as detection to return from Sleep to Active mode	** This function can be selectable to be ON/OFF by registers. # This function can be selectable to be ON/OFF by registers. In the event both LDM and VPC detection are set to OFF, the system will automatically select VPC as detection to return from Sleep to Active mode
	110	SCD threshold setting bit	SCD_D[3:0])	SCD_D[4:0])
30 June 2021	16,22		*1: There is a requirement for the usage of REGEXT and CVDD total capacitor value. Please refer to page 23 bottom note (*3) for more detail.	*1: REGEXT voltage setting can only be set to 5V or 3.3V when using as direct connection with CVDD. There is a requirement for the usage of REGEXT and CVDD total capacitor value. Please refer to page 23 bottom note (*3) for more detail.
	35	REGEXT note		Only 5V or 3.3V should be set for system using direct connection with CVDD.
	42			#1: For this case, VPC is always at "high" state when charger is connected or NMOS FET is turned On. IC cannot be moved to Shutdown mode unless charger is removed and NMOS FET is turned Off.
	113	Fig 11.5.2	ST_OCC/OCD/SCD	MCU write "1" command to bits ST_OCC/OCD/SCD
	176	ADI_LATCH_SET	High-speed current ADC measurement data Latch timing setting 1: Synchronous update 0: Instant update (Default)	High-speed current ADC measurement data Latch timing switch 1: After issuing ADIH_LATCH, on-going 1 ADC cycle is completed and subsequently latched 0: After issuing ADIH_LATCH, recent available data is latched immediately (Default)
	176	ADV_LATCH_SET	Voltage measurement ADC measurement data Latch timing setting 1: Synchronous update 0: Instant update (Default)	Voltage measurement ADC measurement data Latch timing switch 1: After issuing ADV_LATCH, on-going 1 ADC cycle is completed and subsequently latched 0: After issuing ADV_LATCH, recent available data is latched immediately (Default)
	107	Table.11.3.4 OV threshold Bits Note	2.0V/3.5V 6/5 Note: The lower limit for OVTH can be restricted to 2.0V by setting OVHLMT flag (OUVCTL2:bp15) to "0".	2.0V 6 Note deleted
	107	Table 11.3.5	Note: OVTH[5] will be fixed to "1" when OVHLMT flag (OUVCTL2:bp15) is set to "1".	Note deleted
	102	OV threshold	2.0V/3.5V 6/5bits	2.0V 6bits
	143	Words in diagram		- ACTIVE (All internal Registers reset) - valid SPI command

Revision History

Control Number Rev 1.03

Date	Page	Item	Before	After
30 June 2021				

Important Notice

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.