

Features

- $V_{DS} = -20V, I_D = -0.55A$
 $R_{DS(ON)} < 590m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} < 900m\Omega @ V_{GS} = -2.5V$
- ESD Protection

Application

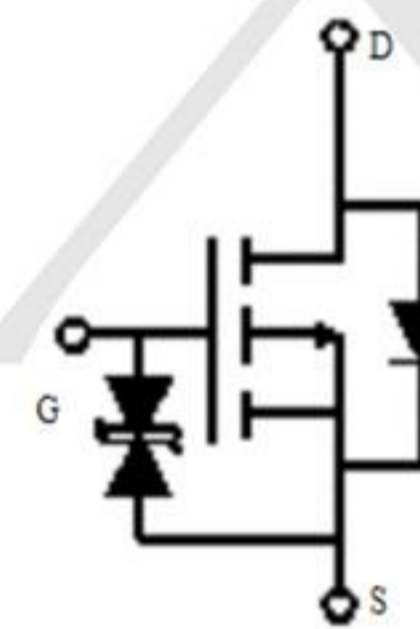
- Load/Power Switching
- Interfacing Switching
- Battery Management for Ultra Small Portable Electronics
- Logic Level Shift

Package and Pin Configuration



SOT-523

Circuit diagram



Marking: B

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	-0.8	A
Pulsed Drain Current ($t=300\mu s$) ⁽¹⁾	I_{DM}	-1.4	A
Power Dissipation ⁽²⁾	P_D	280	mW
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	452	$^\circ C/W$
Junction Temperature	T_J	150	$^\circ C$
Storage Temperature	T_{STG}	-55~ +150	$^\circ C$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 12V, V_{DS} = 0V$			± 10	μA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.5	-0.75	-1.1	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = -4.5V,$ $I_{DS} = -550mA$			590	m Ω
		$V_{GS} = -2.5V, I_{DS} = -450mA$			900	
Forward transconductance	g_{FS}	$V_{DS} = -5V, I_D = 500mA$		1		S
Dynamic characteristics⁽⁴⁾						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -10V,$ Freq. = 1MHz			60	pF
Output Capacitance	C_{oss}				6	
Reverse Transfer Capacitance	C_{rss}				5	
Switching Characteristics⁽⁴⁾						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = -4.5V, V_{DS} = -10V,$ $I_D = -1A, R_{GEN} = 3\Omega$		0.45		us
Turn-on rise time	t_r			0.04		
Turn-off delay time	$t_{d(off)}$			0.035		
Turn-off fall time	t_f			1.1		
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$I_S = 0.15A, V_{GS} = 0V$			-1.2	V



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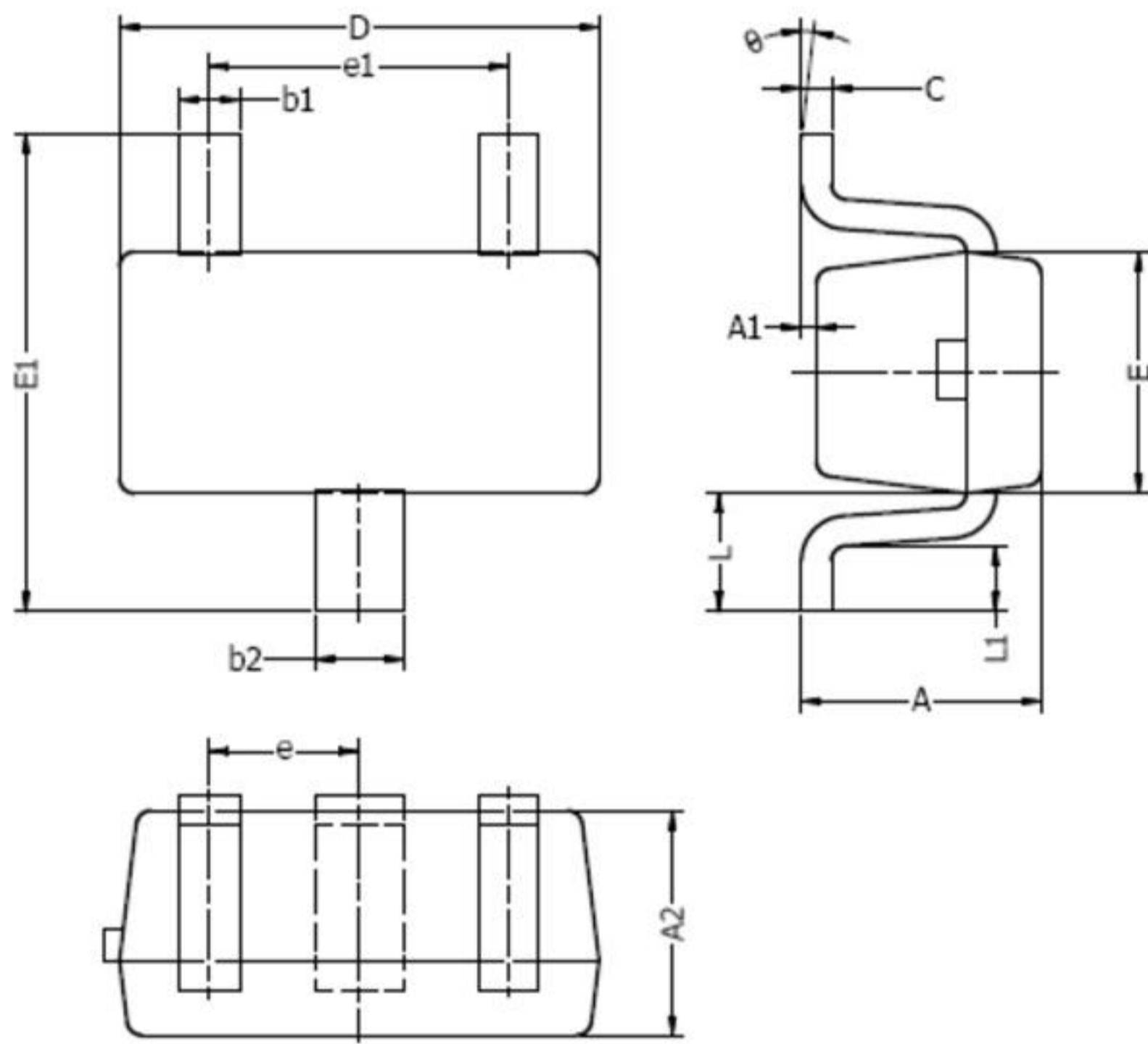
—台舟电子—

WNM4153

P-Channel Enhancement Mode MOSFET

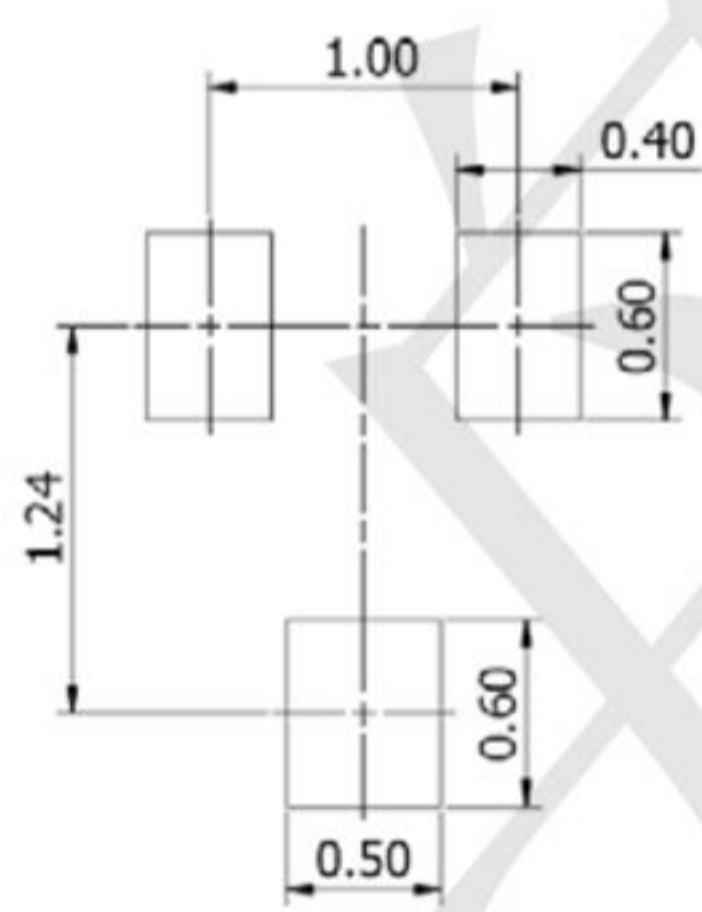
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SOT523 Package Outline Drawing



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
A1	0.00	0.10	0.000	0.004
A2	0.70	0.80	0.028	0.031
b1	0.15	0.25	0.006	0.010
b2	0.25	0.35	0.010	0.014
c	0.10	0.20	0.004	0.008
D	1.50	1.70	0.059	0.067
E	0.70	0.90	0.028	0.035
E1	1.45	1.75	0.057	0.069
e	0.50 TYP.		0.020 TYP.	
e1	0.90	1.10	0.035	0.043
L	0.40 REF.		0.016 REF.	
L1	0.10	0.30	0.004	0.012
θ	0°	8°	0°	8°

Suggested Land Pattern



NOTES:

1. Above package outline conforms to JEITA EAIJ ED-7500A SC-75A.
2. Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.