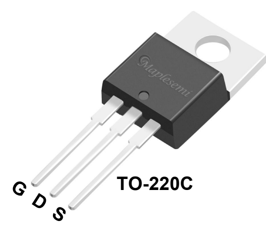
SLP12N65SV / SLF12N65SV
680V N-Channel MOSFET

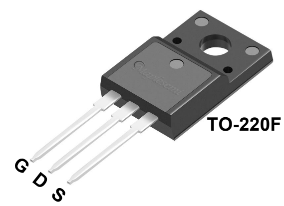
General Description

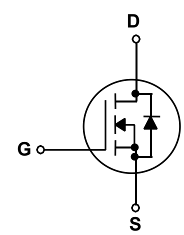
This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 12A, 680V, $R_{DS(on)Type}$=0.64Ω@V_{GS} = 10 V
- Low gate charge (typical 45nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability







Absolute Maximum Ratings T_C = 25℃ unless otherwise noted

Symbol	Parameter	SLP12N65SV	SLF12N65SV	Units
V_{DSS}	Drain-Source Voltage	680		V
I_D	Drain Current - Continuous (T_C = 25℃)	12		A
	- Continuous (T_C = 100℃)	6		A
I_{DM}	Drain Current - Pulsed (Note 1)	40		A
V_{GSS}	Gate-Source Voltage	±30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	550		mJ
I_{AR}	Avalanche Current (Note 1)	12		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	36		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	2.1		V/ns
P_D	Power Dissipation (T_C = 25℃)	-	41.7	W
	- Derate above 25℃	-	0.33	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		℃

Thermal Characteristics

Symbol	Parameter	Max		Units
		SLP12N65SV	SLF12N65SV	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	3.0	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	℃/W

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLP12N65SV	SLP12N65SV	T0-220C	Tube	1000	5000
SLF12N65SV	SLF12N65SV	T0-220F	Tube	1000	5000

Electrical Characteristics

T_C = 25℃unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	680	--	--	V
$\triangle BV_{DSS}$ / $\triangle T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	-	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	--	--	10	uA
		V_{DS} = 520 V, T_C = 125℃	--	--	100	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 6A	--	0.64	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D =6 A (Note 4)	--	11	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	2230	--	pF
C_{oss}	Output Capacitance		--	370	--	pF
C_{rss}	Reverse Transfer Capacitance		--	130	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 320 V,V_{GS} = 10V, I_D =12A, R_G = 25 Ω (Note 4, 5)	--	25	--	ns
t_r	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	45	--	ns
t_f	Turn-Off Fall Time		--	30	--	ns
Q_g	Total Gate Charge	V_{DS} = 520 V, I_D = 12A, V_{GS} = 10 V (Note 4, 5)	--	45	--	nC
Q_{gs}	Gate-Source Charge		--	8.4	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	12	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	40	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S =12A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S =12 A, dI_F / dt = 100 A/us (Note 4)	--	300	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.0	--	uC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L=11mH, I_{AS} =10A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25° C
3. I_{SD} ≤I_D, di/dt ≤ 200A/us, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25° C
4. Pulse Test : Pulse width ≤ 300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

N- Channel Typical Characteristics

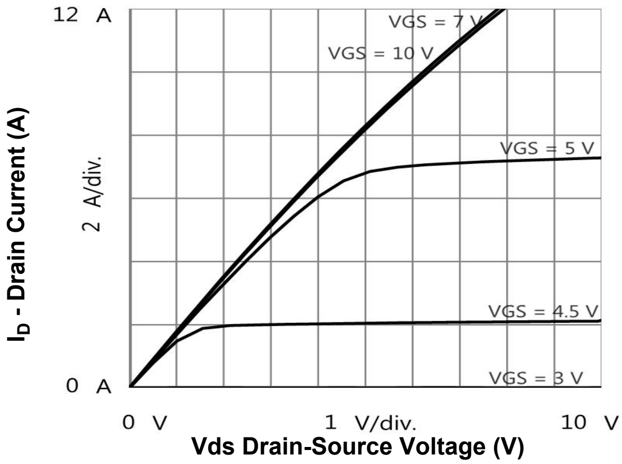


Figure 1. On-Region Characteristics

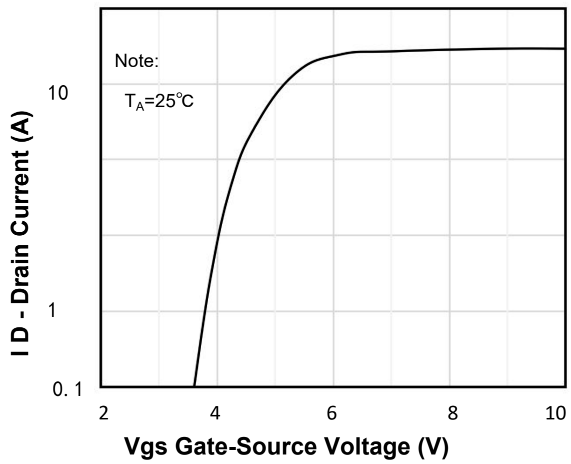


Figure 2. Transfer Characteristics

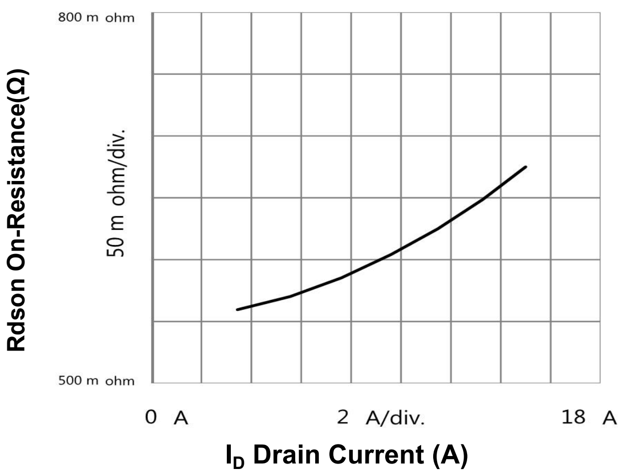


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

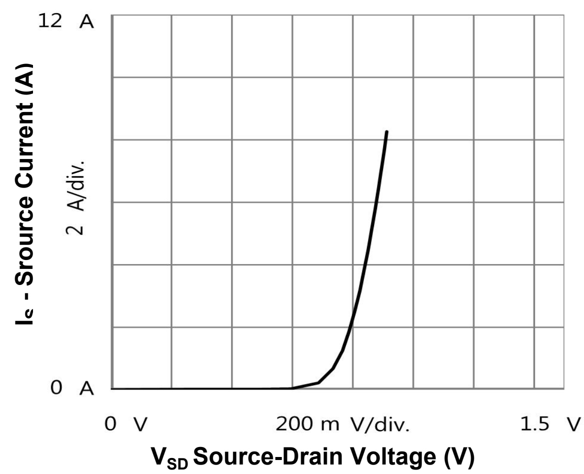


Figure 4. Source Current vs Source-Drain Voltage

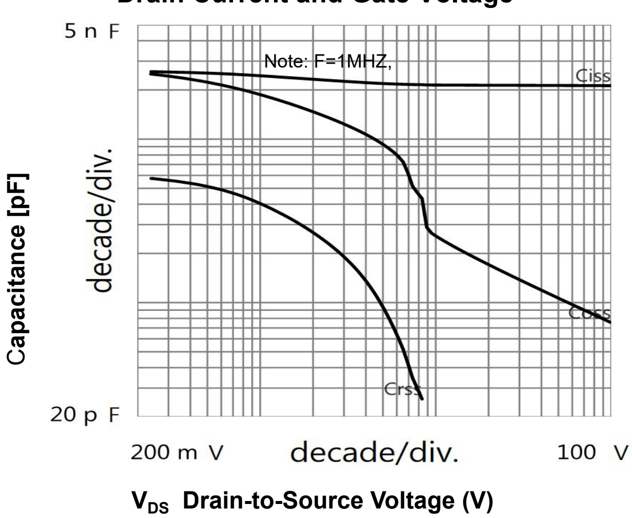


Figure 5.1 Capacitance Characteristics

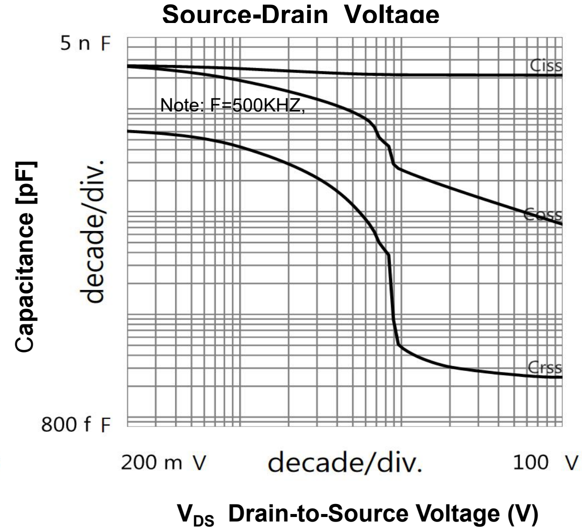


Figure 5.2 Capacitance Characteristics

N- Channel Typical Characteristics (Continued)

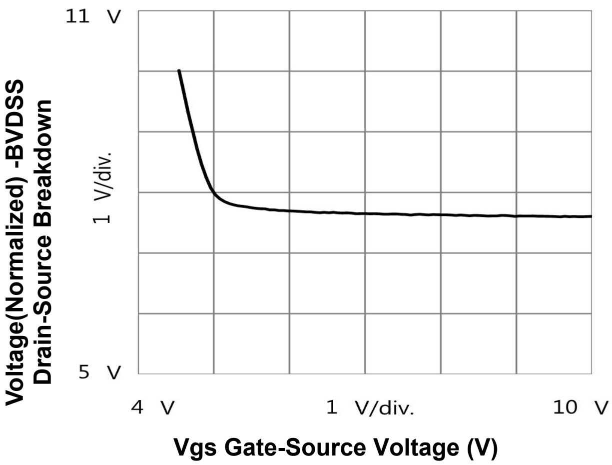


Figure 7. Breakdown Voltage Variation vs Gate-Source Voltage

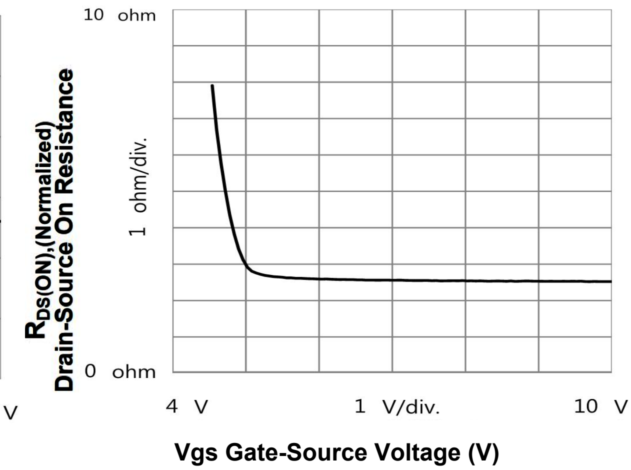


Figure 8. On-Resistance Variation vs Gate-Source Voltage

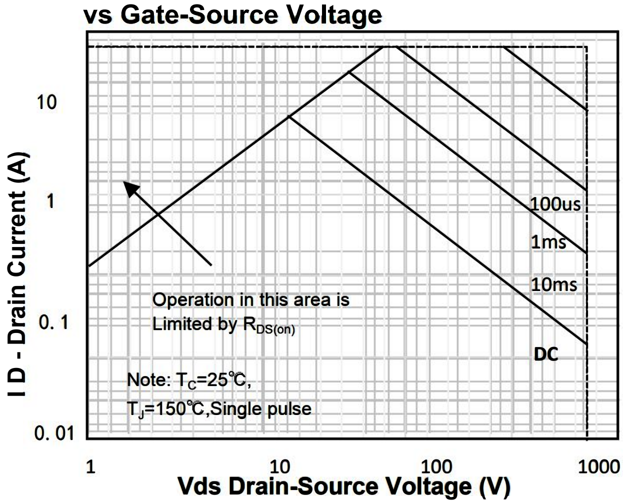


Figure 9. Maximum Safe Operating Area

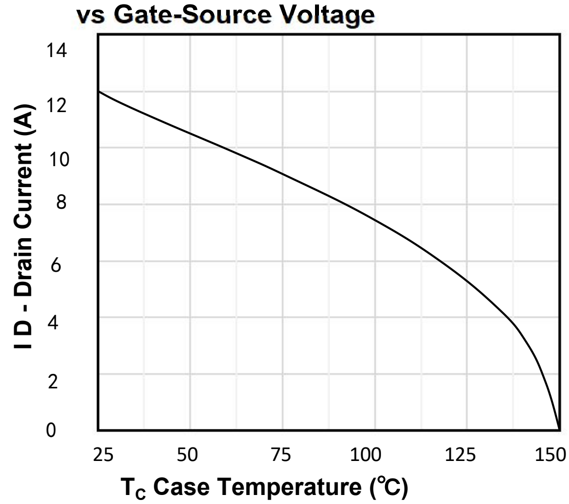
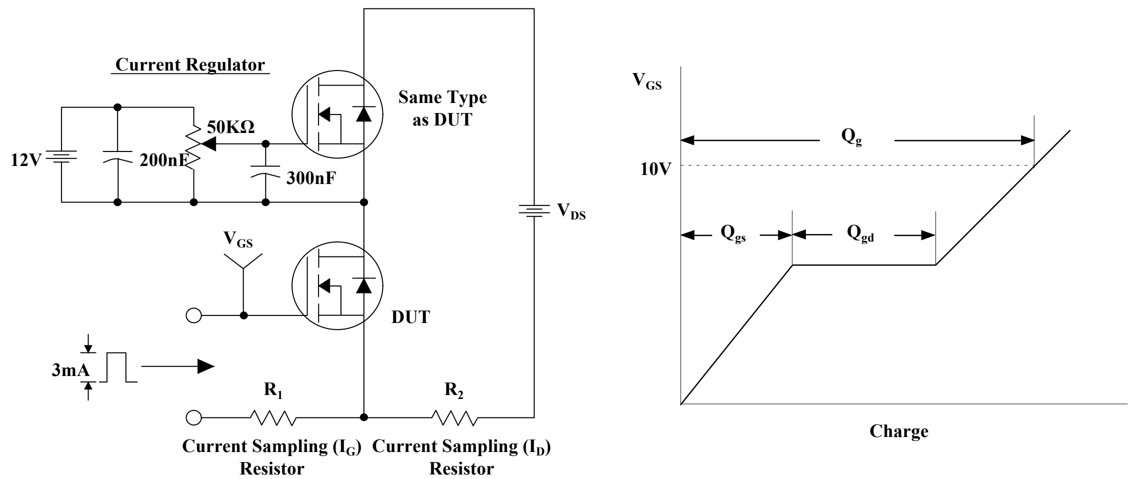
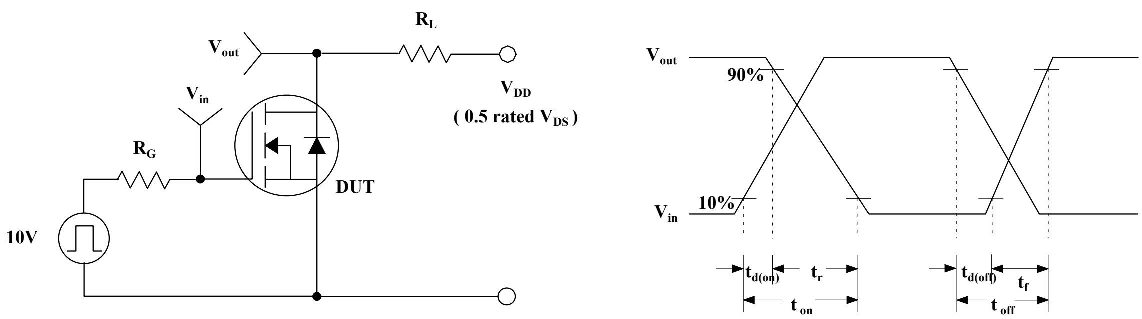


Figure 10. aximum Drain Current vs Case Temperature

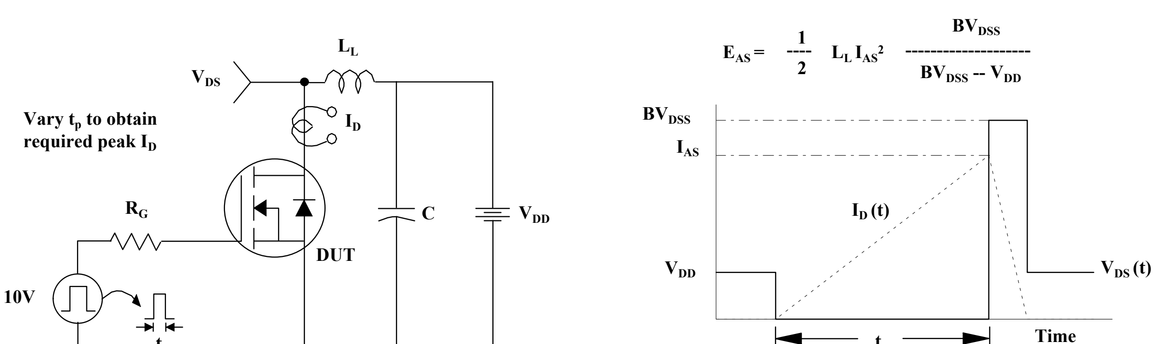
Gate Charge Test Circuit & Waveform



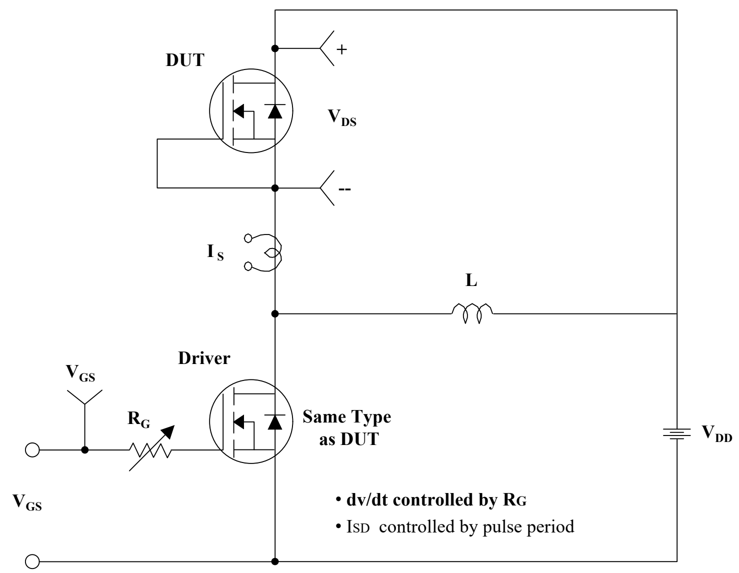
Resistive Switching Test Circuit & Waveforms

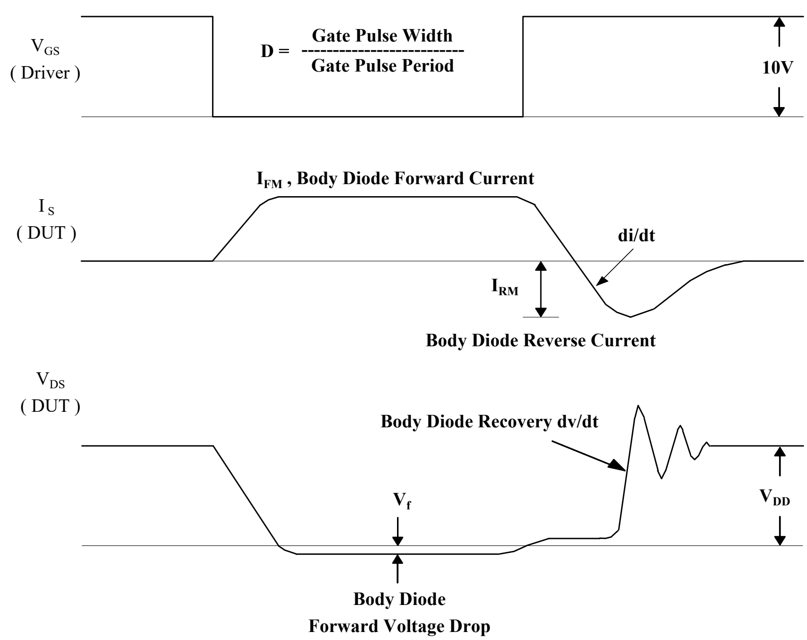


Unclamped Inductive Switching Test Circuit & Waveforms

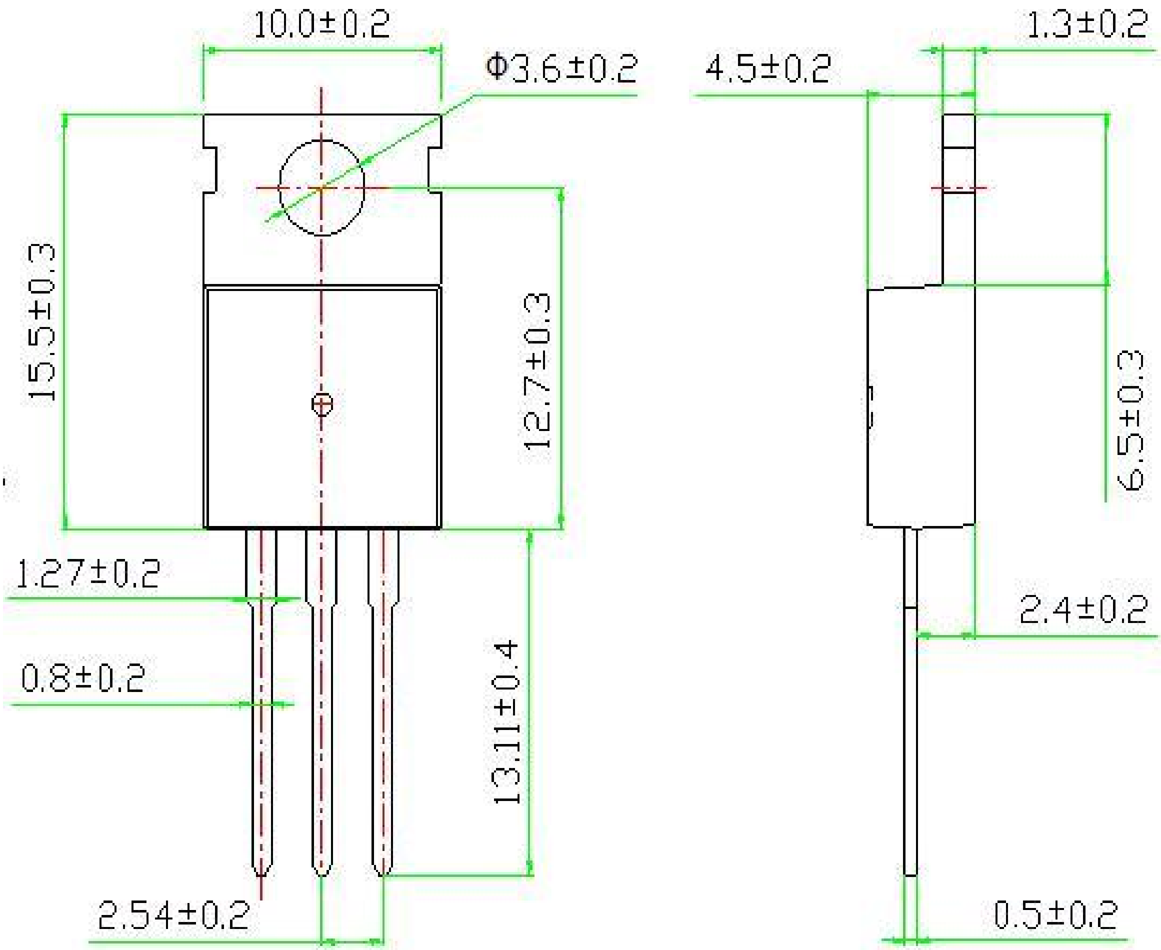


Peak Diode Recovery dv/dt Test Circuit & Waveforms



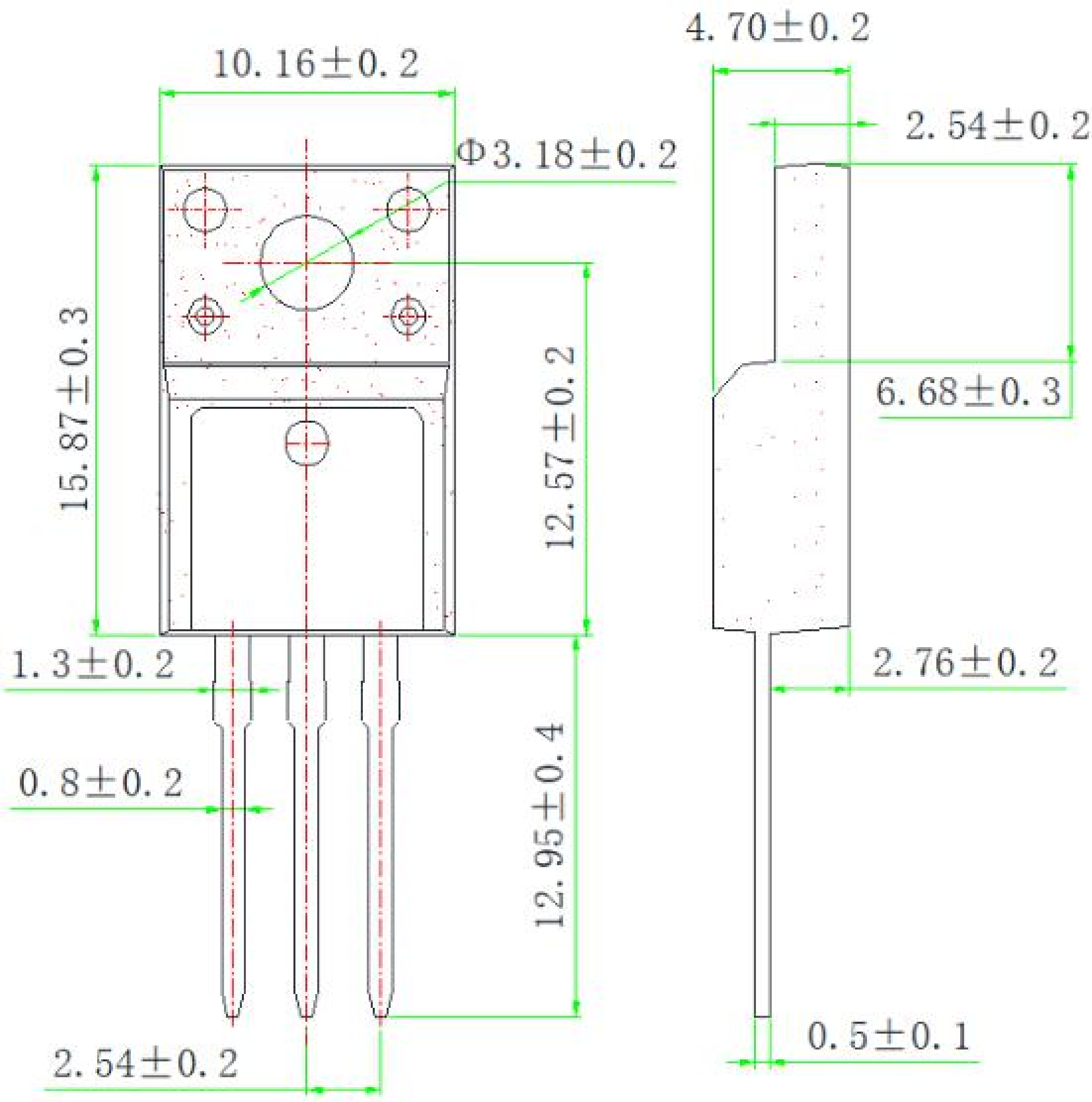


TO-220C OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

TO-220F OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subglossy surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25