

SLD7N65SV / SLF7N65SV

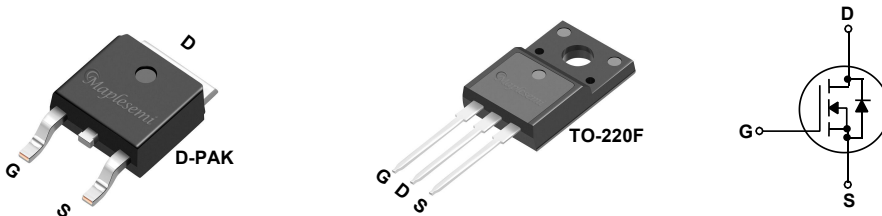
650V N-Channel MOSFET

General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 7A, 650V, $R_{DS(on)Max}=1.10\Omega@V_{GS} = 10V$
- Low gate charge (typical 26nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SLD7N65SV	SLF7N65SV	Units
V_{DSS}	Drain-Source Voltage	650		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	7		A
		-		A
I_{DM}	Drain Current - Pulsed (Note 1)	14		A
V_{GSS}	Gate-Source Voltage	± 30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	602		mJ
I_{AR}	Avalanche Current (Note 1)	7		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	141		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	2.3		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	48	35	W
		-	-	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Max		Units
		SLD7N65SV	SLF7N65SV	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	3.57	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	110	62.5	$^\circ\text{C}/\text{W}$

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD7N65SV	SLD7N65SV	T0-252	Tape & Reel	2500	25000
SLF7N65SV	SLF7N65SV	T0-220F	Tube	1000	5000

Electrical Characteristics

 $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	-	--	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$	--	1.1	1.35	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 3.5\text{ A}$ (Note 4)	--	-	--	S

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	1130	--	pF
C_{OSS}	Output Capacitance		--	86.8	--	pF
C_{RSS}	Reverse Transfer Capacitance		--	4.08	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 100\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}, R_G = 25\text{ }\Omega$ (Note 4, 5)	--	12	--	ns
t_r	Turn-On Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	74	--	ns
t_f	Turn-Off Fall Time		--	33	--	ns
Q_g	Total Gate Charge	$V_{DS} = 520\text{ V}, I_D = 8\text{ A}, V_{GS} = 10\text{ V}$ (Note 4, 5)	--	26	--	nC
Q_{GS}	Gate-Source Charge		--	4.78	--	nC
Q_{GD}	Gate-Drain Charge		--	5.82	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	7.5	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	14	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7\text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 7\text{ A},$	--	506	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	2.7	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 10\text{ mH}, I_{AS} = 7\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq I_D, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

N- Channel Typical Characteristics

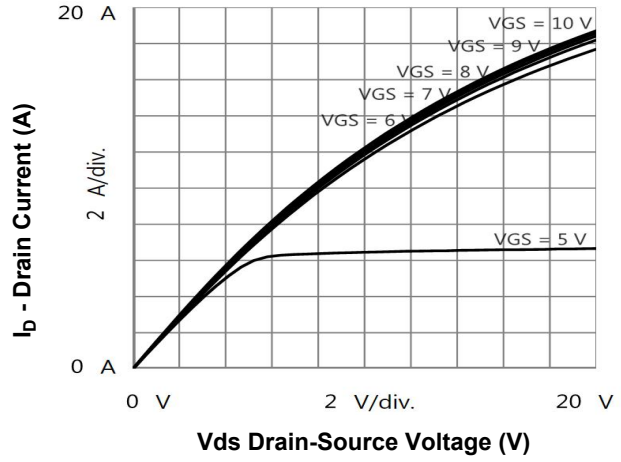


Figure 1. On-Region Characteristics

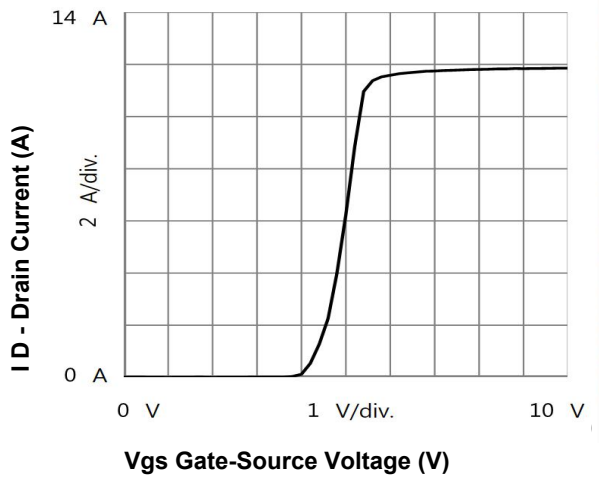


Figure 2. Transfer Characteristics

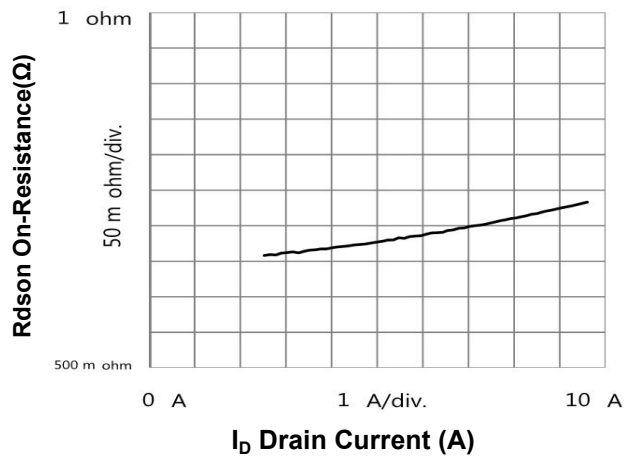


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

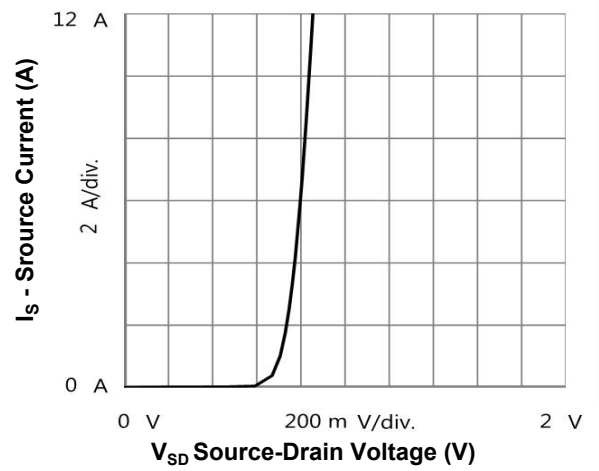


Figure 4. Source Current vs Source-Drain Voltage

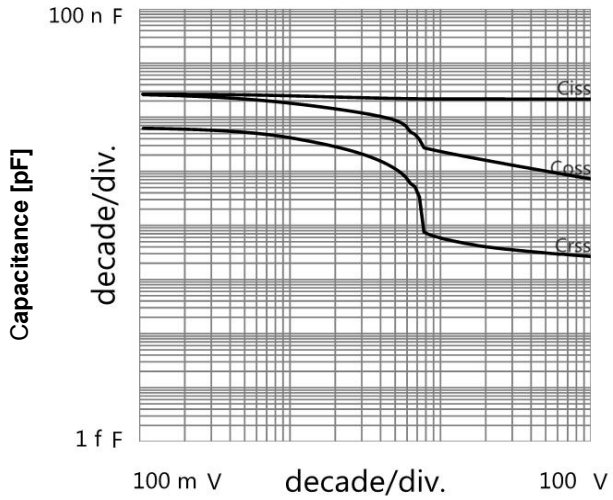


Figure 5. Capacitance Characteristics

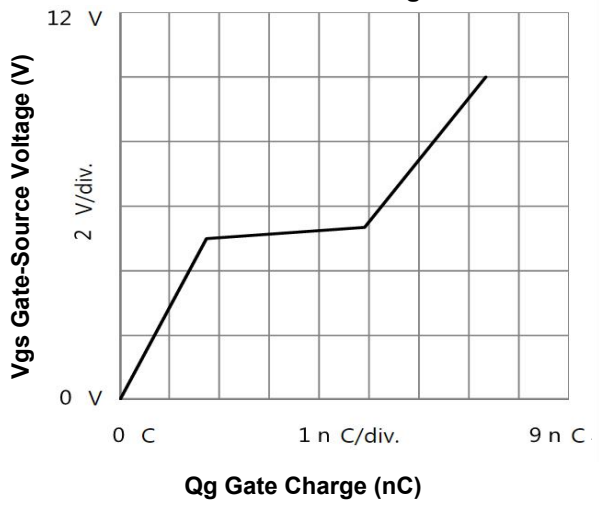


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

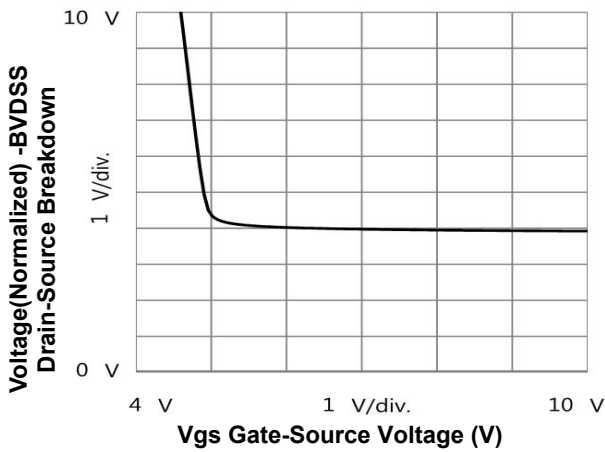


Figure 7. Breakdown Voltage Variation vs Gate-Source Voltage

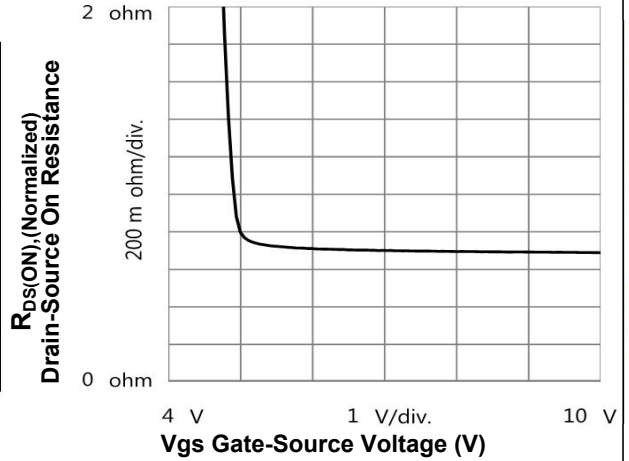


Figure 8. On-Resistance Variation vs Gate-Source Voltage

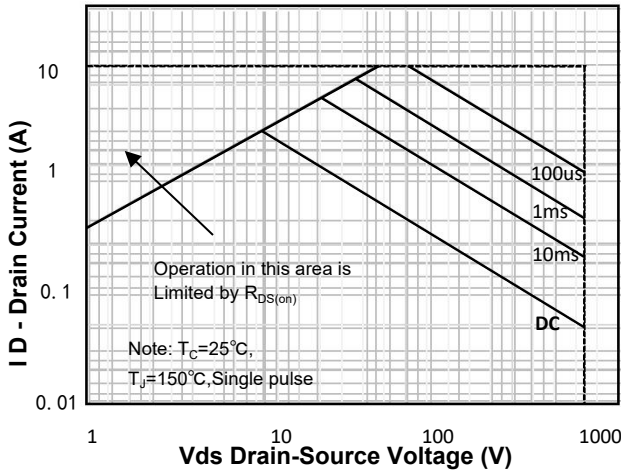
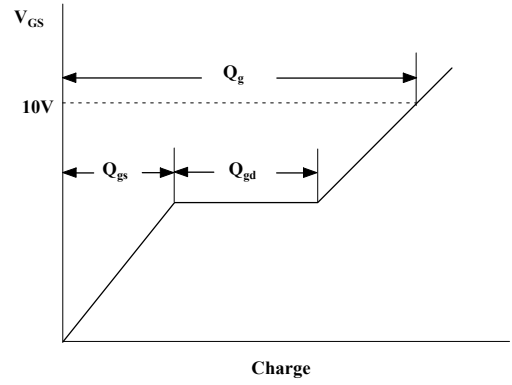
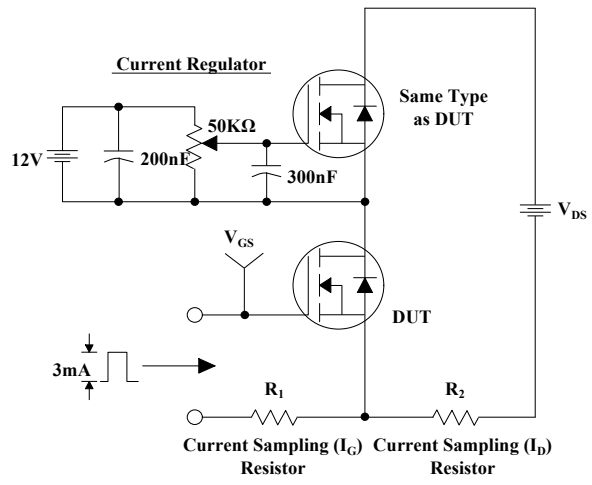
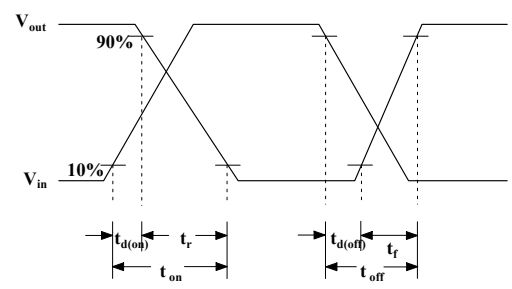
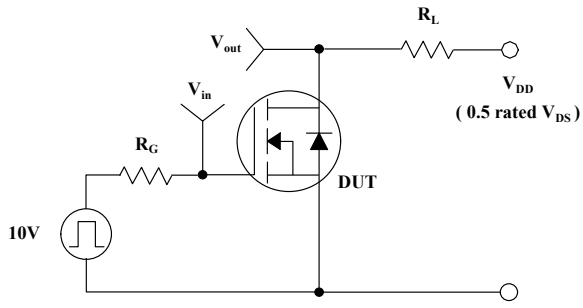


Figure 9. Maximum Safe Operating Area

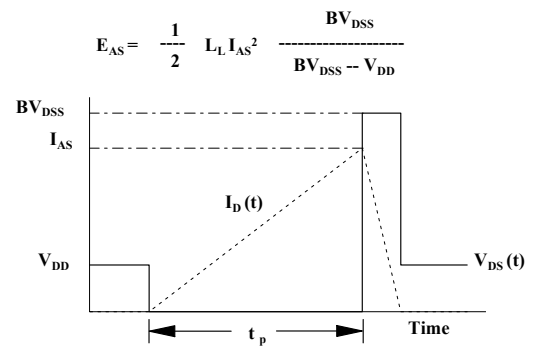
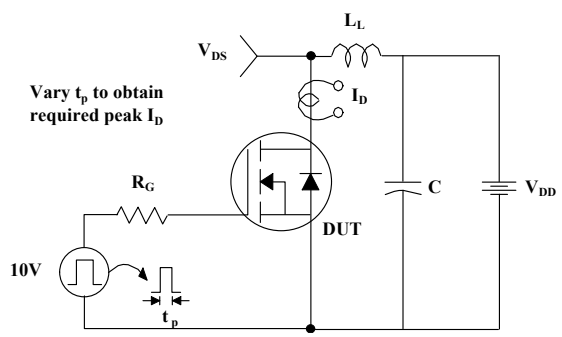
Gate Charge Test Circuit & Waveform



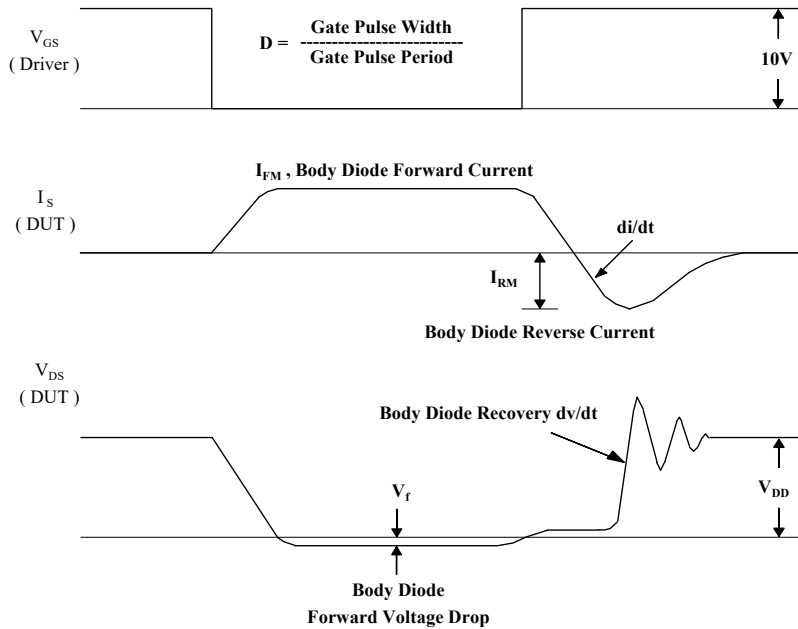
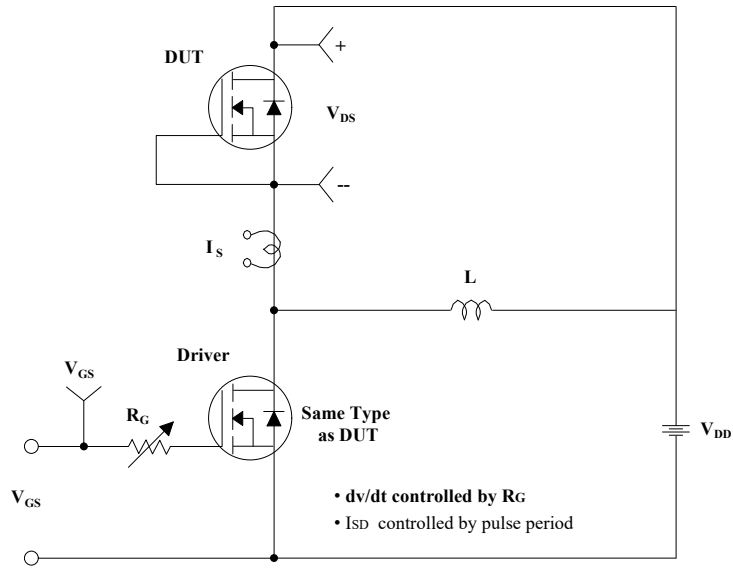
Resistive Switching Test Circuit & Waveforms



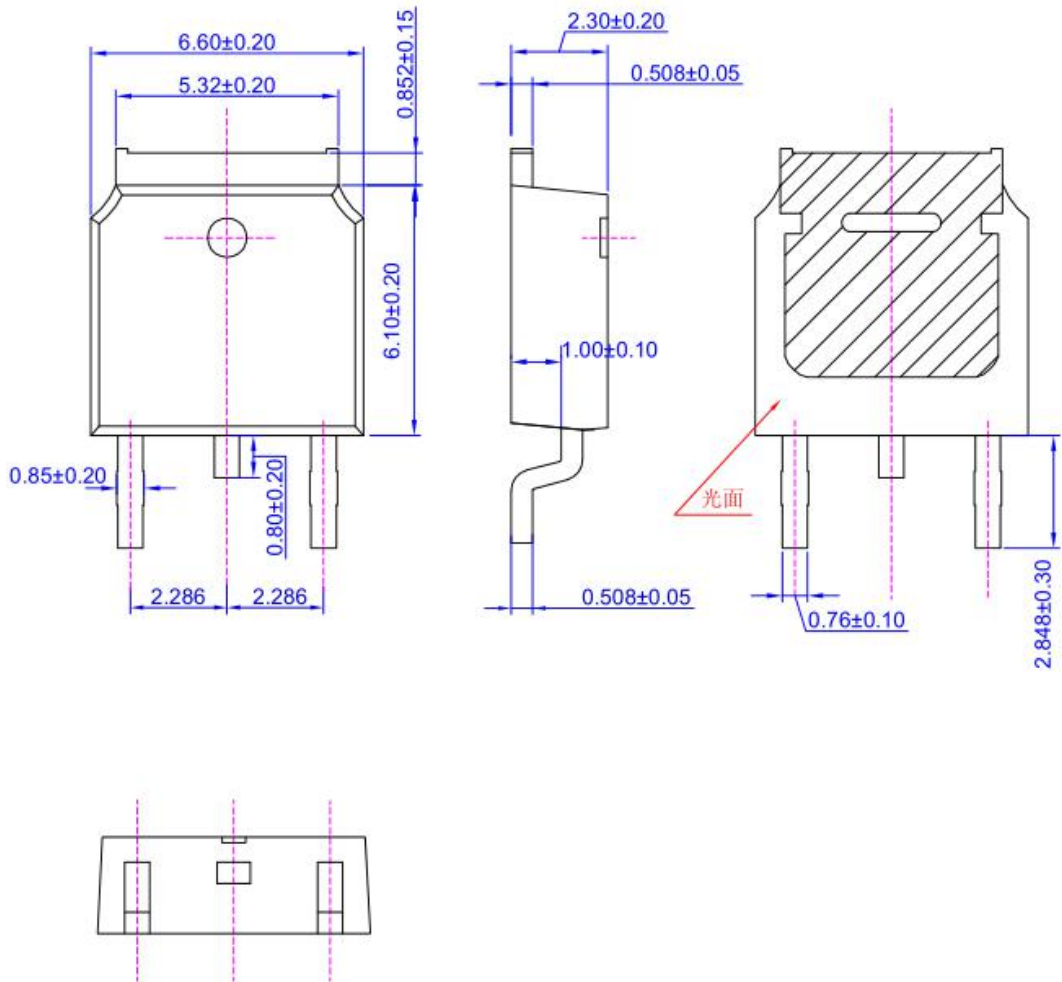
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



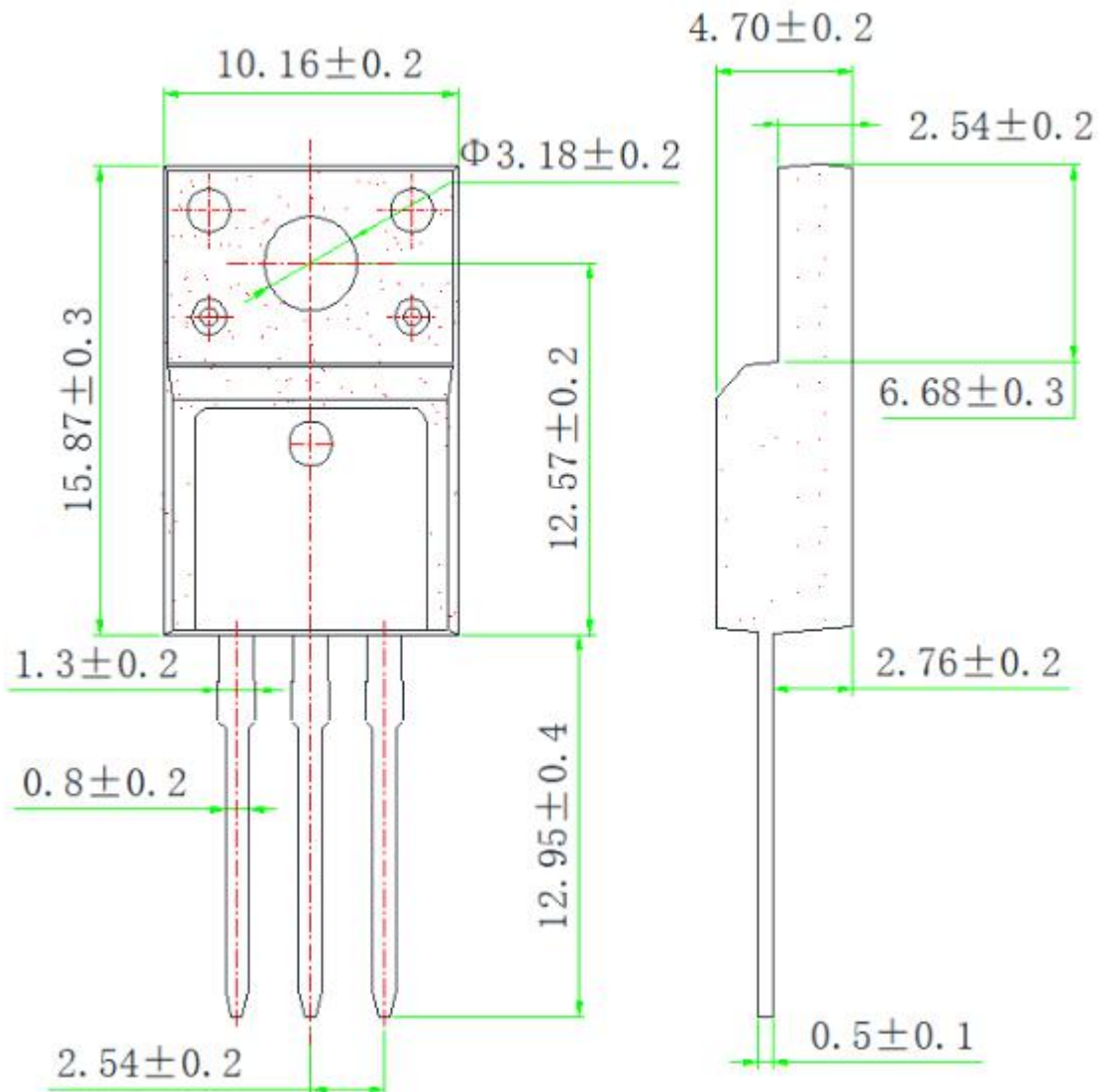
TO-252 OUTLINE



NOTE:

- 1 The plastic package is not marked as smooth surface $R_a=0.1$; Subglossy surface $R_a=0.8$
- 2 Undeclared tolerance ± 0.25 , Unmarked fillet $R_{max}=0.25$

TO-220F OUTLINE



NOTE:

1 The plastic package is not marked as smooth surface $R_a=0.1$; Subglossy surface $R_a=0.8$

2. Undeclared tolerance ± 0.25 , Unmarked fillet $R_{max}=0.25$