FOUNDER

MK NAND FLAH

MKPVXG08CX-KS Datasheet

FOUNDER

Feature Summary

■ **Single-level Cell(SLC) Technology**

■ **OPEN NAND FLASH INTERFACE(ONFI)1.0 COMPLIANT**

■ **POWER SUPPLY VOLTAGE**
- VCC/VCCQ = 2.7V ~ 3.6V

■ **MEMORY CELL ARRAY (with SPARE)**
- Page size : (4K+256 spare) bytes or
  (2K+128 spare) bytes
- Block size : (256K+16K) bytes or (128K+8K) bytes
- Plane size : 2,048blocks
- Device size :
  (4K+256) bytes x 64 pages x 2,048 blocks x 1 plane
  (2K+128) bytes x 64 pages x 2,048 blocks x 2 plane

■ **PAGE READ / PROGRAM**
- Random Read Time (tR)
  4KB Page : 55us(Typ) / 350us (Max)
  2KB Page : 45us(Typ) / 250us(Max)
  Multi-plane (2KB Page) Read Time
  : 55us(Typ) / 450us (Max)
- Sequential Access Time : 20ns(Min)
- Page Program Time : 350us(Typ) / 600us(Max)

■ **BLOCK ERASE**
- Block Erase Time: 4ms(Typ) / 10ms(Max)

■ **COMMAND SET**
- ONFI1.0 Compliant command set
- Read Unique ID

■ **SECURITY**
- Serial number (Unique ID)
- Volatile/Non-Volatile Protection
- One Time Programmable (OTP) Area

■ **PACKAGE**
- Package type : TSOP48、FBGA63
- Chip count : SDP
- Pin Count : 48
- size : 12mm x 20mm x 1.2mm
- Lead/Halogen Free

■ **ELECTRONIC SIGNATURE**
- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type
- 4th cycle : Page size, Block size, Spare size,
  Organization
- 5th cycle : Multi-plane information

■ **OPERATING TEMPERATURE**
- -25℃ to 85℃

FOUNDER

1. SUMMARY DESCRIPTION

MK NAND flash are offered in 3.3 Vcc and VccQ Power Supply, and with x8 I/O inter- face. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. In default, the device page size is (4,096 + 256 spare) bytes or (2,048 + 128 spare) bytes.

Each block can be programmed and erased up to 60,000 cycles with ECC (error correction code) on. To extend the lifetime of NAND Flash devices, the implementation of an ECC is mandatory.
The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a micro-controller, since the CE# transitions do not stop the read operation.

Program operation with multi-plane structure allows to program 2 pages at a time (one per each plane) when using of 2,048bytes of page size, or to erase 2 blocks at a time (one per each plane). As a consequence, multi-plane architecture holds reduced program/erase time compared to operation at single-plane architecture. Both single and multi-plane operations are supported both with traditional and ONFI 1.0 protocols.

Data in the page can be read out at 20ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

This device supports ONFI 1.0 specification. The Copy-back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. EDC function is not supported in this device.
A write protect pin is available to provide hardware protection against program and erase operations.
This device features an open-drain ready/busy output identifying if the program/erase/read controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pull-up resistor.

Device supports 0℃ to 70℃(Commercial), -25℃ to 85℃(Mobile), -40℃ to 85℃(Industrial, AIT AEC-Q100 grade3), -40℃ to 105℃(Automotive, AAT AEC-Q100 grade2) Operating Temperature.

The devices, available in the TSOP48 and FBGA63 48pin(12X20mm) package, support the ONFI1.0 specification and come with security features as below:
- OTP (one time programmable) area which is a restricted access area where sensitive data/code can be store permanently.
- Serial number(unique identifier) which allows the devices to be uniquely identified.
- Non-volatile protection to lock sensible data permanently.
- Volatile protection to control lock status of data according to user needs.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, no described in the datasheet. For more details about them, contact your nearest MK sales office.

1.1. Product List

Table 1 : List of supported versions / packages

Part Number	Density	Organization	Operating Temp.	# of CE RB#	Operating Range	PACKAGE
MKPV4G08CT-KS	4Gbit	x8, 2KB Page	-40℃ to 85℃	1CE & 1R/B#, single	2.7 to 3.6V	TSOP48
MKPV4G08CB-KS		x8, 4KB Page	-40℃ to 85℃			FBGA63
MKPV8G08CT-KS	8Gbit	x8, 2KB Page	-40℃ to 85℃	2CE & 2R/B#, dual		TSOP48
MKPV8G08CB-KS		x8, 4KB Page	-40℃ to 85℃			FBGA63
MKPV16G08CT-KS	16Gbit	x8, 2KB Page	-40℃ to 85℃			TSOP48
MKPV16G08CB-KS		x8, 4KB Page	-40℃ to 85℃			FBGA63

Figure 1 : Pin diagram(SDP)

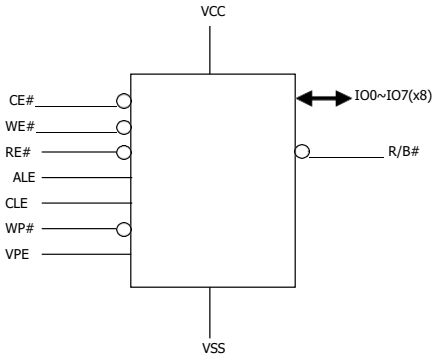
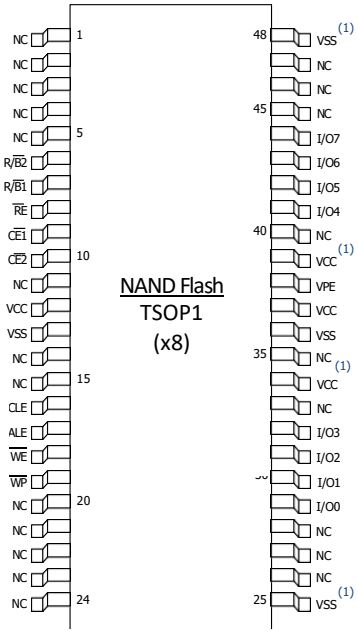
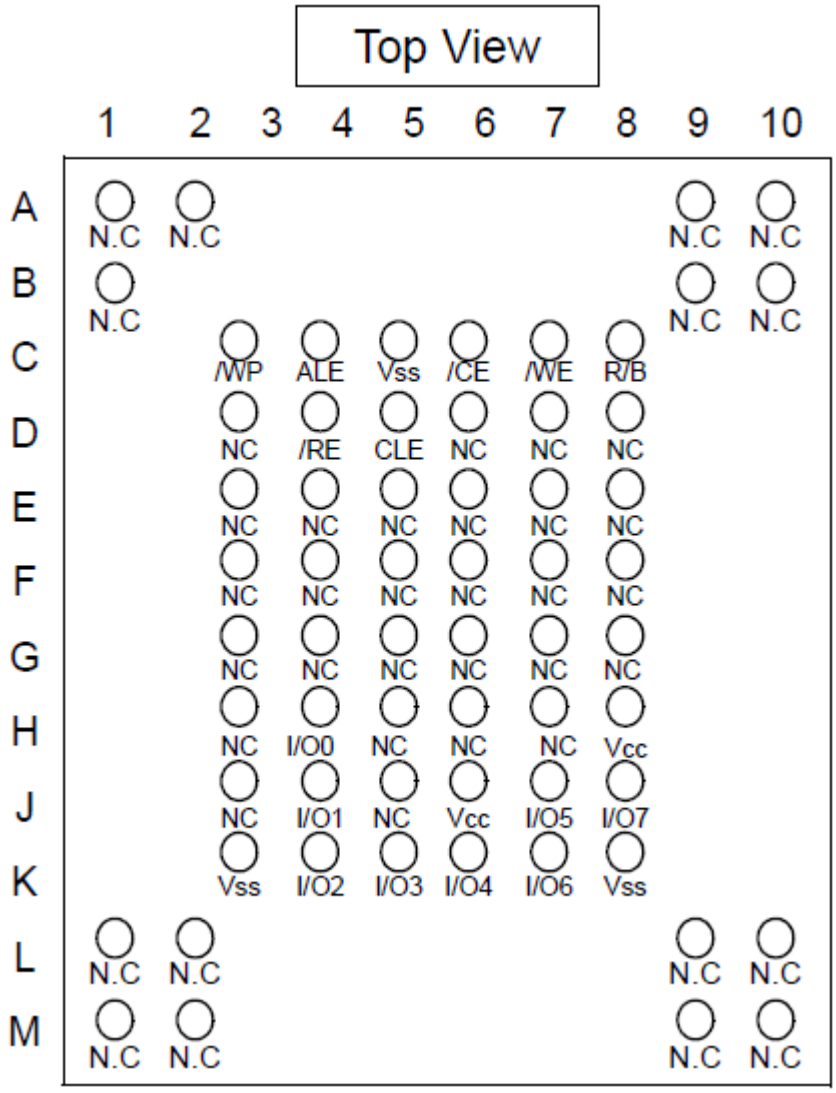


Figure 2 : 48-pin TSOP



NOTE:
These pins should be connected to power supply or ground (as designated) following the ONFI specifications, however, they might not be bonded internally.

Figure 3 : Pin Configuration (FBGA)



FOUNDER

1.2. Pin Description

Table 2 : Signal descriptions

Pin Name	Description
I/O 0 - I/O 07 (X8)	**DATA INPUTS/OUTPUTS** The I/O pins are used to COMMAND LATCH cycle, ADDRESS INPUT cycle, and DATA in-out cycles during read / write operations. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the I/O inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the I/O inputs inside the Address Register on the Rising edge of Write Enable (WE#).
CE#	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, CE# high does not deselect the memory. The device goes into Stand-by mode when CE# goes High during the device is in Ready state. The CE# signal is ignored when device is in Busy state, and will not enter Standby mode even if the CE# goes high.
WE#	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The I/O inputs are latched on the rise edge of WE#.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address by one.
WP#	**WRITE PROTECT** The WP# pin, when Low, provides a hardware protection against undesired write and erase operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition, program/erase operation cannot be started not to alter the content of the memory. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
VPE	**Volatile Protection Enable** The Volatile Protection Enable input, when high during power-on, provides block granularity hardware protection against undesired data modification (program/erase). This input has a weak internal pull-down (IPD) to disable the volatile protection features if the input is left floating.
R/B#	**READY / BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	SUPPLY VOLTAGE The VCC supplies the power for all the operations. (Read, Write, and Erase).
V_{SS}	**GROUND**
NC	**NO CONNECTED**

Note:
A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.3. Package Dimensions

Figure 4 : 48-pin TSOP

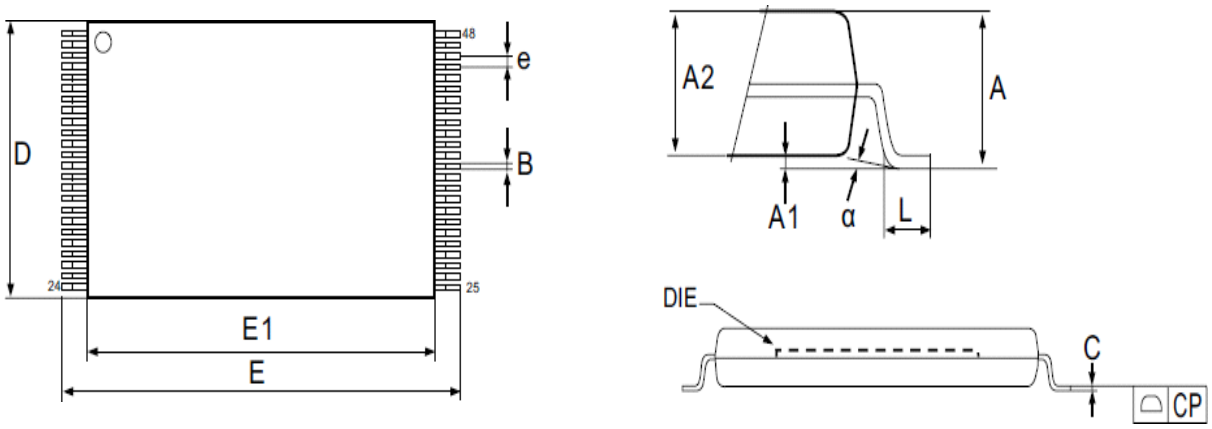
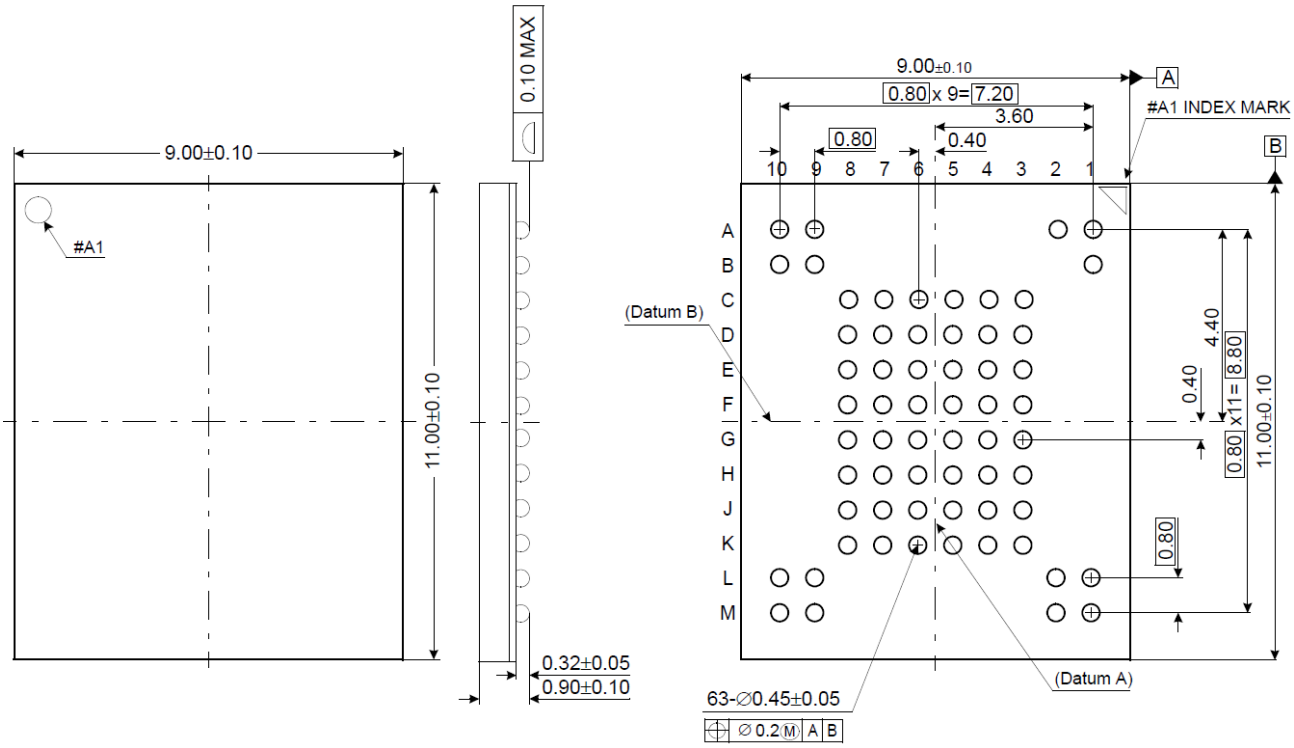


Table 3 : Package Mechanical Data

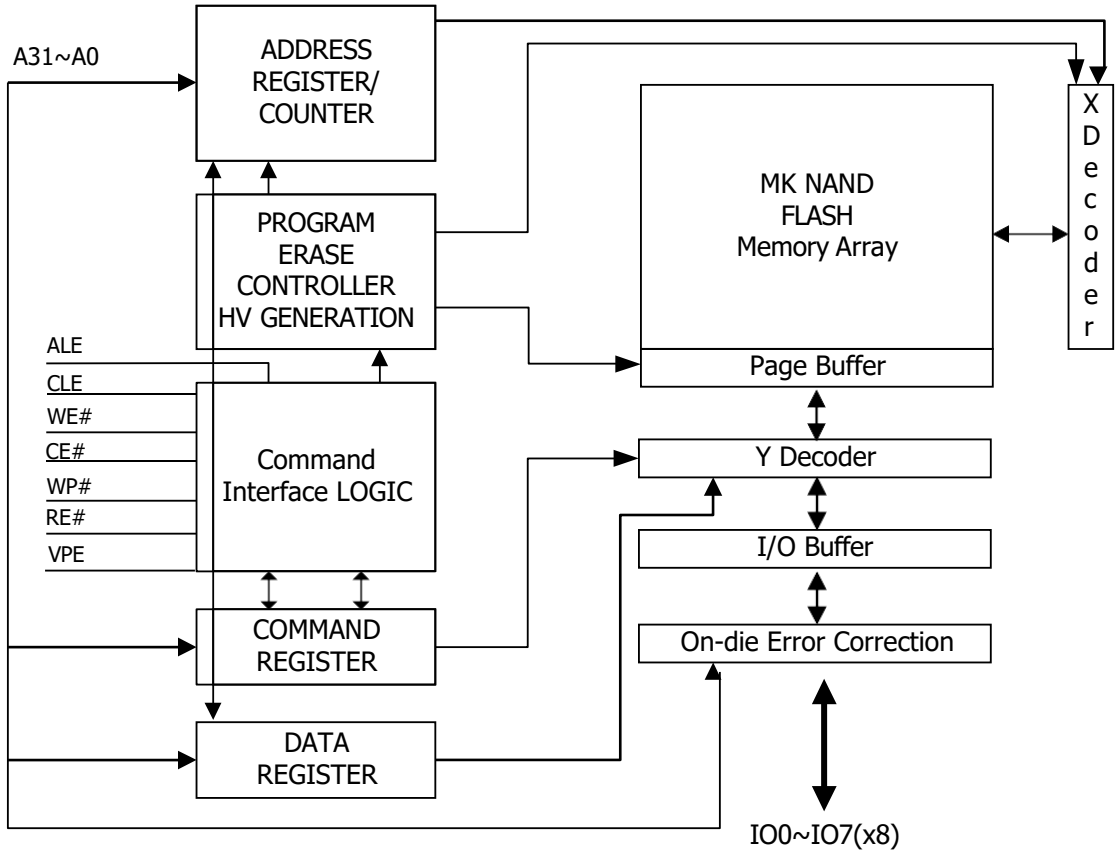
Symbol	milimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Figure 5 : 63-Ball FBGA


9.00±0.10
0.10 MAX
#A1
11.00±0.10
0.32±0.05
0.90±0.10
9.00±0.10
A
0.80 x 9= 7.20
3.60
#A1 INDEX MARK
0.80
0.40
B
10 9 8 7 6 5 4 3 2 1
A
B
C
D
E
F
G
H
J
K
L
M
(Datum B)
4.40
0.40
0.80 x11= 8.80
11.00±0.10
0.80
(Datum A)
63-∅0.45±0.05
∅0.2 M A B

1.4. Functional Block Diagram

Figure 6 : Block diagram(SDP)



1.5. Memory Organization

A device contains one or more targets. A target is controlled by one CE# signal. A target is organized into one or more logical units (LUNs).
A logical unit (LUN) is the minimum unit that can independently execute commands and report status.

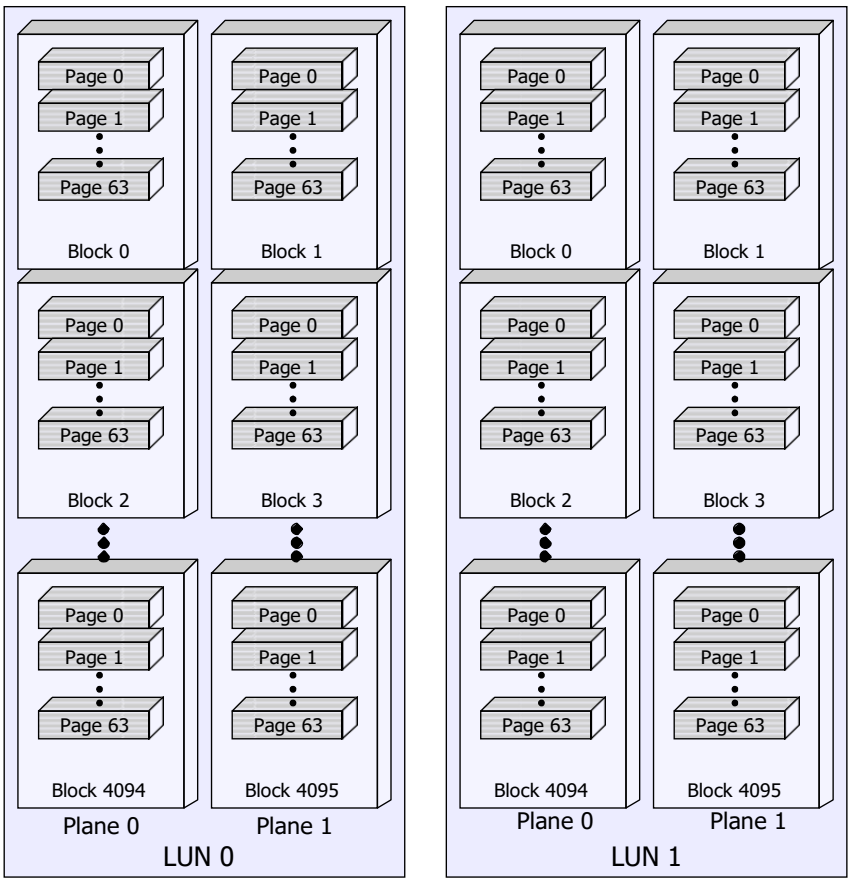
A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations. A page consists of a number of bytes.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

Figure 7 : Target Memory Organization Example (2KB Page)



1.5.1. Addressing

1.5.1.1 Column and Row Addressing

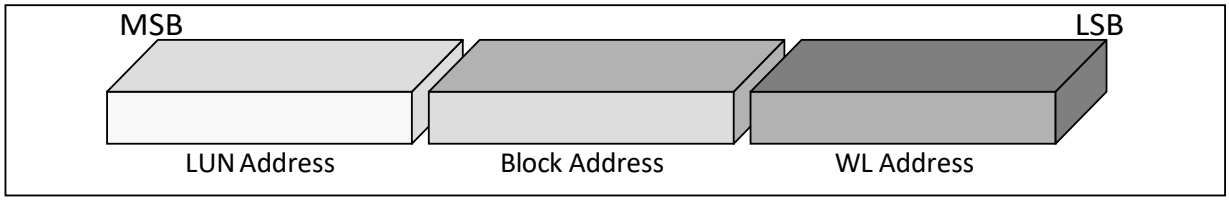
There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in ***Figure 8 "Row Addess Layout"*** with the least significant row address bit to the right and the most significant row address bit to the left.

Figure 8 : Row Address Layout



The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address.

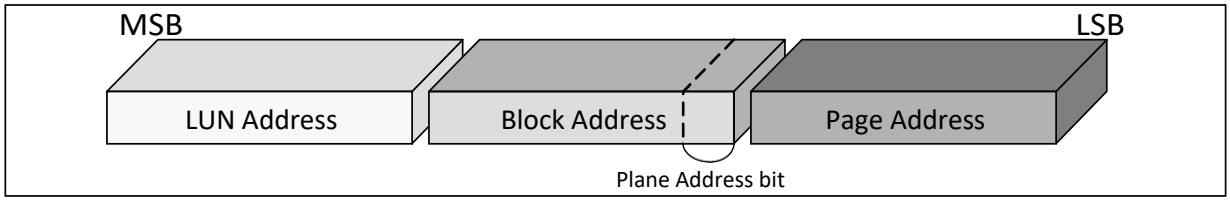
A host shall not access an address of a page or block beyond maximum Page Address or block address. The Addressing of this device is shown in Table of "*Memory addressing*".

1.5.1.2 Plane Addressing

The plane address comprises the lowest order bits of the block address as shown in ***Figure 9*** for "***Plane Address Position***". The plane address is used when performing a Two-plane command sequence on a particular LUN:

The plane address bit(s) shall be different within address setting sequences for the Two-plane-related operation, while the Page Address shall stay the same within address setting sequences for the multi-plane-related operation.

Figure 9 : Plane Address Position



1.5.2 Array Organization

Figure 10 : Array organization (4KB Page)

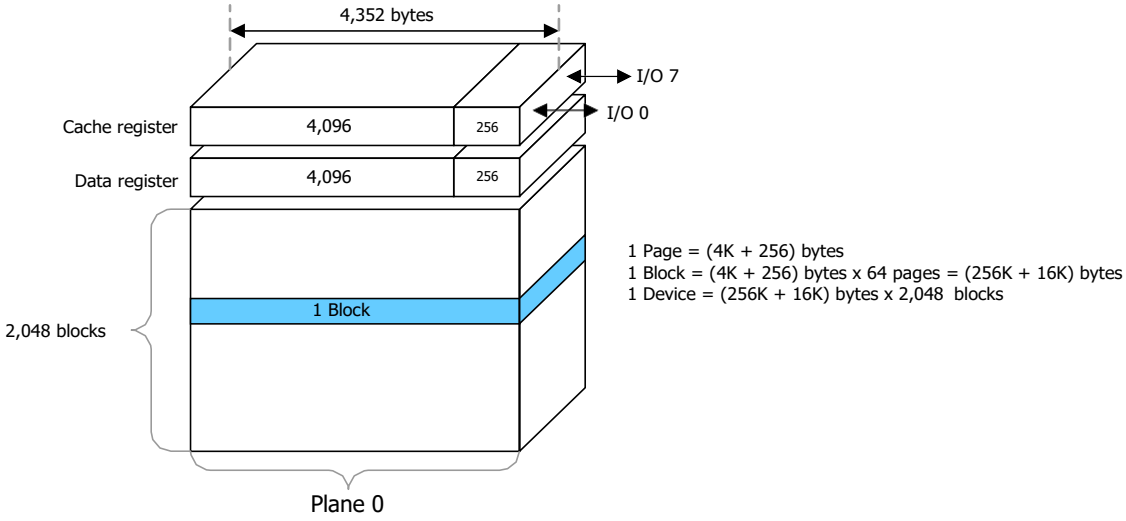


Table 4 : Address Cycle Map (4KB Page)

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	L(1)	L(1)	L(1)
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th(*) Cycle	A29	A30	A31	L(1)	L(1)	L(1)	L(1)	L(1)

(*): A30 for 8Gbit DDP(1CE). A30:A31 for 16Gbit QDP(1CE).
As far as the address bits are concerned, the following rules apply:
A0 - A12 : column address in the page
A13 - A18 : page address in the block
A19 - A31 : block address

Note:
1. L must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address

Figure 11 : Array organization (2KB Page)

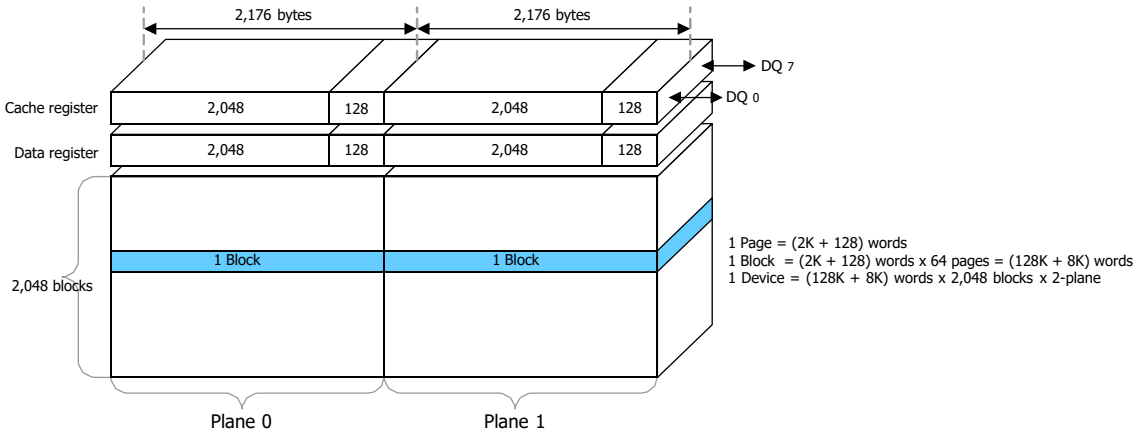


Table 5 : Address Cycle Map (2KB Page)

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th(*) Cycle	A28	A29	A30	A31	L(1)	L(1)	L(1)	L(1)

(*): A30 for 8Gbit DDP(1CE). A30:A31 for 16Gbit QDP(1CE).
As far as the address bits are concerned, the following rules apply:
A0 - A11 : column address in the page
A12 - A17 : page address in the block
A18 : plane address
A19 - A31 : block address

Note:
1. L must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address

FOUNDER

Table 6 : Block Arrangement (4KB Page)

Row Address	Block Number	
000000h ~ 00003Fh	Block 0 (Plane 0)	Main Block (2,048Blocks)
000040h ~ 00007Fh	Block 1 (Plane 0)	
000080h ~ 0000BFh	Block 2 (Plane 0)	
0000C0h ~ 0000FFh	Block 3 (Plane 0)	
000100h ~ 00013Fh	Block 4 (Plane 0)	
000140h ~ 00017Fh	Block 5 (Plane 0)	
...	...	
01FF00h ~ 01FF3Fh	Block 2044 (Plane 0)	
01FF40h ~ 01FF7Fh	Block 2045 (Plane 0)	
01FF80h ~ 01FFBFh	Block 2046 (Plane 0)	
01FFC0h ~ 01FFFFh	Block 2047 (Plane 0)	

Table 7 : Block Arrangement (2KB Page)

Row Address	Block Number	
000000h ~ 00003Fh	Block 0 (Plane 0)	Main Block (4,096Blocks)
000040h ~ 00007Fh	Block 1 (Plane 1)	
000080h ~ 0000BFh	Block 2 (Plane 0)	
0000C0h ~ 0000FFh	Block 3 (Plane 1)	
000100h ~ 00013Fh	Block 4 (Plane 0)	
000140h ~ 00017Fh	Block 5 (Plane 1)	
...	...	
03FF00h ~ 03FF3Fh	Block 4092 (Plane 0)	
03FF40h ~ 03FF7Fh	Block 4093 (Plane 1)	
03FF80h ~ 03FFBFh	Block 4094 (Plane 0)	
03FFC0h ~ 03FFFFh	Block 4095 (Plane 1)	

1.5.3. Valid Blocks

Table 8 : Valid Blocks Number

	Symbol	Page Size	Min	Max	Unit
Valid Block Number	N_{VB}	4KB	2008	2048	Blocks
		2KB	4016	4096	

Note:
1. The 1st block at plane0, 1st chip per CE is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

FOUNDER

1.6. Command Set

Table 9 : Command Set

FUNCTION	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Accept-able while accessed LUN is busy	Accept-able while other LUNs are busy
RESET	FFh	-	-	-	Yes	Yes
READ UNIQUE ID	EDh	-	-	-	-	-
READ PARAMETER PAGE	ECh	-	-	-	-	-
READ ONFI SIGNATURE	90h	20h	-	-	-	-
GET FEATURE	EEh	-	-	-	-	-
SET FEATURE	EFh	-	-	-	-	-
READ STATUS	70h	-	-	-	Yes	Yes
READ STATUS ENHANCED	78h	-	-	-	Yes	Yes
RANDOM DATA INPUT	85h	-	-	-	-	Yes
RANDOM DATA OUTPUT	05h	E0h	-	-	-	Yes
PAGE READ	00h	30h	-	-	-	Yes
MULTI-PLANE READ	00h	32h	30h	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	-	Yes
(traditional) MULTI-PLANE PROGRAM(1)	80h	11h	81h	10h	-	Yes
ONFI MULTI-PLANE PROGRAM(1)	80h	11h	80h	10h	-	Yes
PAGE RE-PROGRAM	8Bh	10h	-	-	-	Yes
MULTI-PLANE PAGE RE-PROGRAM(1)	8Bh	11h	8Bh	10h	-	Yes
BLOCK ERASE	60h	D0h	-	-	-	Yes
(traditional) MULTI-PLANE BLOCK ERASE(1)	60h	60h	D0h	-	-	Yes
ONFI MULTI-PLANE BLOCK ERASE(1)	60h	D1h	60h	D0h	-	Yes
READ FOR COPY-BACK	00h	35h	-	-	-	Yes
COPY-BACK PROGRAM	85h	10h	-	-	-	Yes
(traditional) MULTI-PLANE COPY-BACK PROGRAM(1)	85h	11h	81h	10h	-	Yes
ONFI MULTI-PLANE COPY-BACK PROGRAM(1)	85h	11h	85h	10h	-	Yes
VOLATILE LOCK ALL	2Ah	-	-	-	-	Yes
BLOCK UNLOCK LOWER	23h	-	-	-	-	Yes
BLOCK UNLOCK UPPER	24h	-	-	-	-	Yes
LOCK DOWN	2Ch	-	-	-	-	Yes
BLOCK PROTECTION STATUS	7Ah	-	-	-	-	Yes
ONE TIME PROGRAMMABLE (OTP) AREA ENTRY(2)	29h-17h-04h-19h	-	-	-	-	-
OTP PROTECTION SET UP(2)	4Ch-03h-1Dh-41h-80h	10h	-	-	-	-
PROGRAM PBP SETTINGS(2)			-	-	-	-
PROGRAM PBP LOCK DOWN(2)			-	-	-	-
Firmware SLC Mode	DAh	-	-	-	-	Yes

Note:
1. N/A for 4Gb device with 4K page featured since it supports single plane only.
2. Once, One Time Programmable (OTP) Area entry command issued, PBP Setting command is not valid. Vice versa, PBP settings command is only accepted if OTP Area entry has not been issued.

Table 10 : Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 Cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H[1)]	L	Rising	H	H		Address Input (5 Cycles)
L	L	L	Rising	H	H	Data Input	
L	L[1)]	L	H	Falling	X	Sequential Read and Data Output	
X	X	L[1)]	H	H	X	Data Output (suspended)	
L	L	L	H[3)]	H[3)]	X	During Read (Busy)	
X	X[1)]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc[2)]	Stand-By	

Note:
1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and multi-plane Read Status can be inputted to the device.

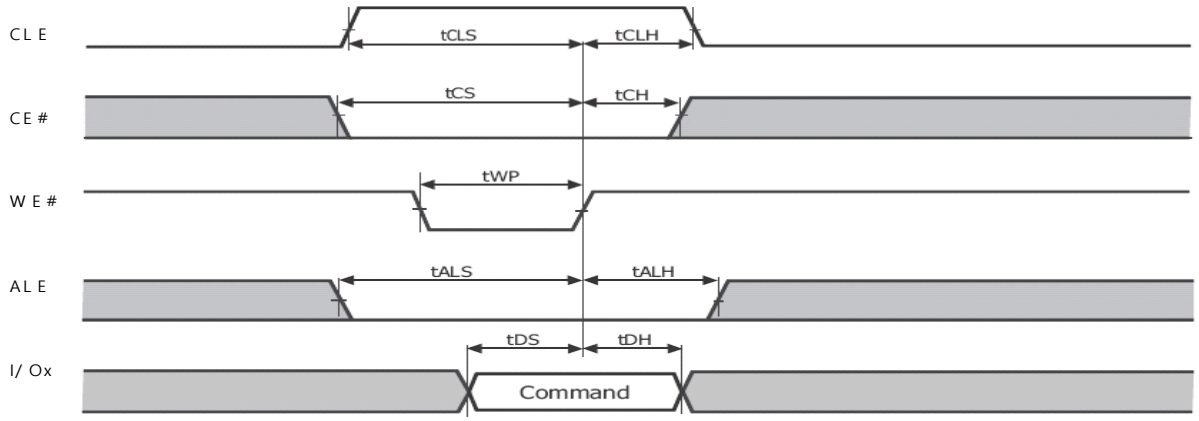
2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1. Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. During program/erase operations, the Write Protect pin must be high. See *Figure 12* and *"5.6. AC Timing Characteristics"* for details of the timings requirements.

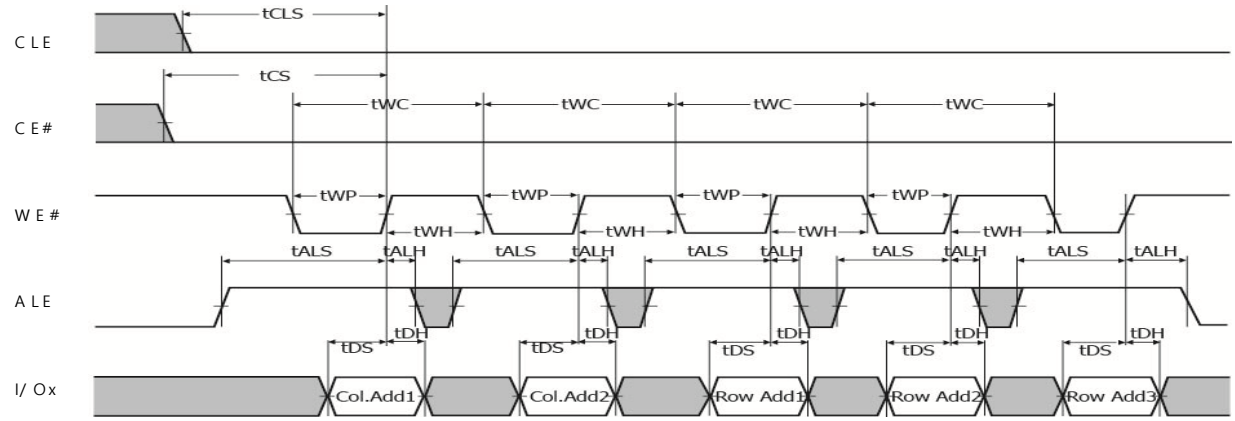
Figure 12 : Command latch timings



2.2. Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. (refer to "1.5.1 Addressing"). Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for the program/erase commands, the Write Protect pin must be high. See *Figure 13* and "*5.6. AC Timing Characteristics*" for details of the timings requirements.

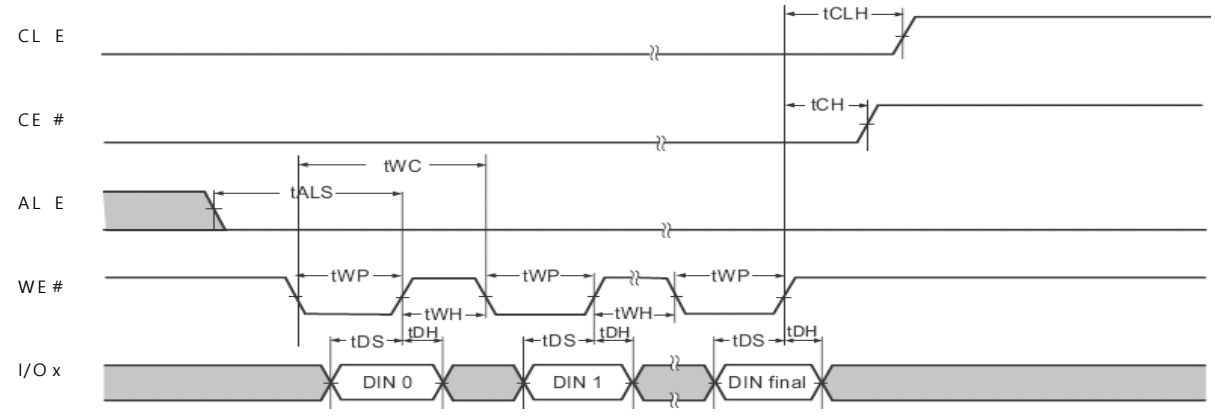
Figure 13 : Address latch timings



2.3. Data Input

Data Input bus operation allows to feed the data to be programmed. The data insertion is done in serial order by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See *Figure 14* and "*5.6. AC Timing Characteristics"* for details of the timings requirements.

Figure 14 : Data Input cycle timings

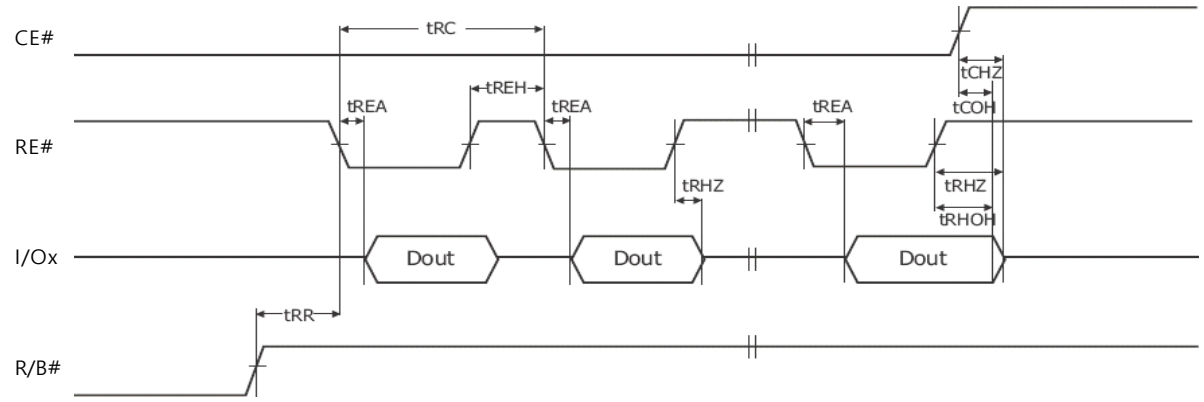


Note:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

2.4. Data Output

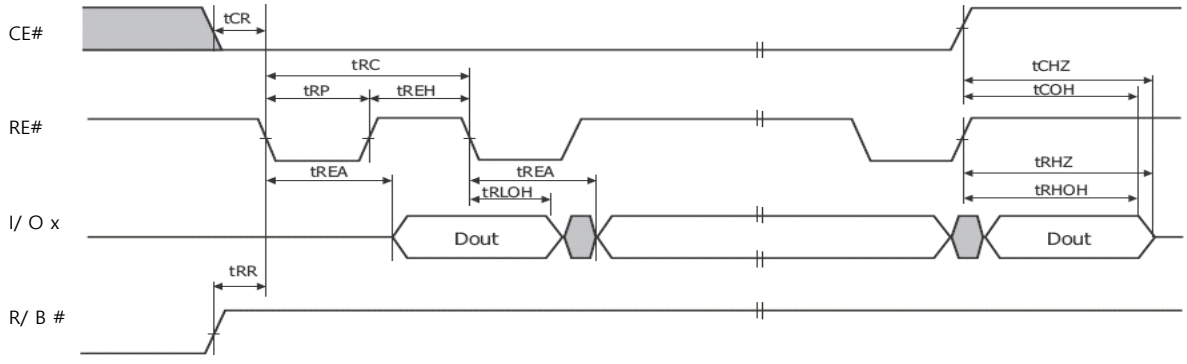
Data Output bus operation allows to read data from the memory array and to check the status register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See *Figure 13* to *Figure 15* and "*5.6. AC Timing Characteristics"* for details of the timings requirements.

Figure 15 : Data output cycle timings (CLE=L, WE#=H, ALE=L, WP#=H)



Note:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (t_{CHZ}, t_{RHZ})
2. t_{RHOH} starts to be valid when frequency is lower than 33 MHz. t_{RLOH} is valid when frequency is higher than 33 MHz

Figure 16 : Data output cycle timings (EDO type, CLE=L, WE#=H, ALE=L)



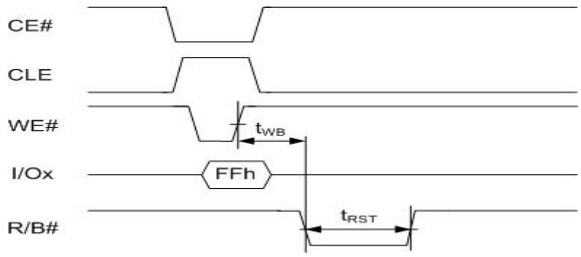
Note:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (t_{CHZ}, t_{RHZ})
2. t_{RLOH} is valid when frequency is higher than 33 MHz. t_{RHOH} starts to be valid when frequency is lower than 33 MHz.

3. Device Operation

3.1. Reset

The device offers a RESET feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the RESET operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. If the device is already in RESET state a new reset command will not be accepted by the command register. The RB# pin transitions to low for t_{RST} after the Reset command is written. Refer to *Figure 17* for further details.

Figure 17 : Reset timings



3.2. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. The 5-byte Read ID configuration are supported: The device operating mode (5-byte) is selected through cam setting.

3.2.1. Legacy Read ID

Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. *Figure 16* shows the operation sequence, while *Table 11* to *Table 15* explain the byte meaning. Complete Read ID code table is as follows.

Table 11 : "Legacy" Read ID bytes meaning

Parameter	Symbol
Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, Cell Type
4th	Page size, Block size, Spare Size, Organization
5th	Multi-plane information

FOUNDER

3.2.2. Read ID Data Table (5cycle)

Table 12 : "Legacy" Read ID for supported configurations

Density	Voltage (Vcc/VccQ)	Bus Width	Page Size	Manufacture Code	Device Code	3rd	4th	5th
4 Gbit	3.3V	X8	4KB	ADh	DCh	00h	1Ah	00h
			2KB	ADh	DCh	00h	05h	04h

Table 13 : Legacy Read ID 3rd byte description

3 rd cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2							0 0	0 1
Cell Type	2 Level Cell					0	0		
Reserved	0	0	0	0	0				

Table 14 : Legacy Read ID 4th byte description

4 th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (not including Spare Area)	2KB 4KB							0 1	1 0
Block Size (not including Spare Area)	128KB 256KB	0 0		0 0	0 1				
Spare Area Size	128B 256B					0 1	1 0		
Number of IO	X8		0						

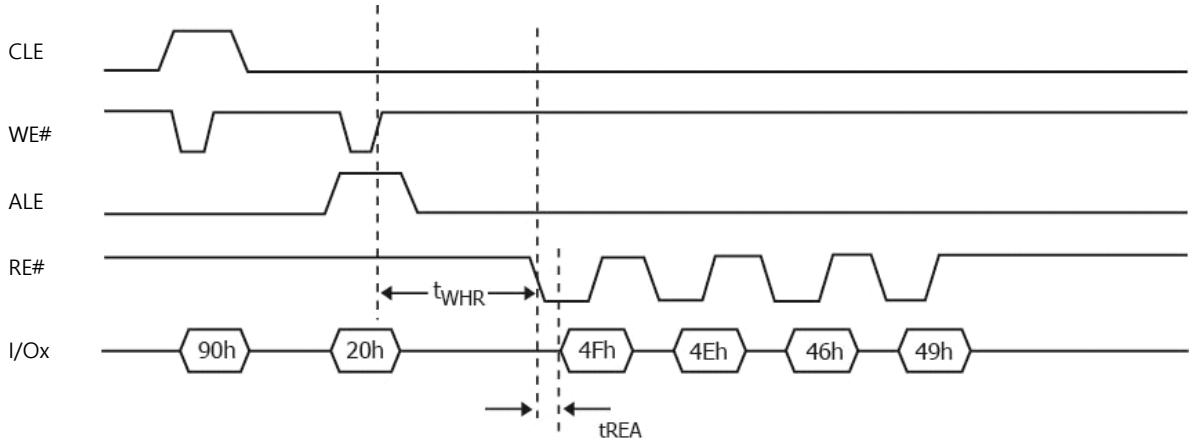
Table 15 : Legacy Read ID 5th byte description

5 th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Reserved		0	0	0	0			0	0

3.3. Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. *Figure 18* shows the operation sequence

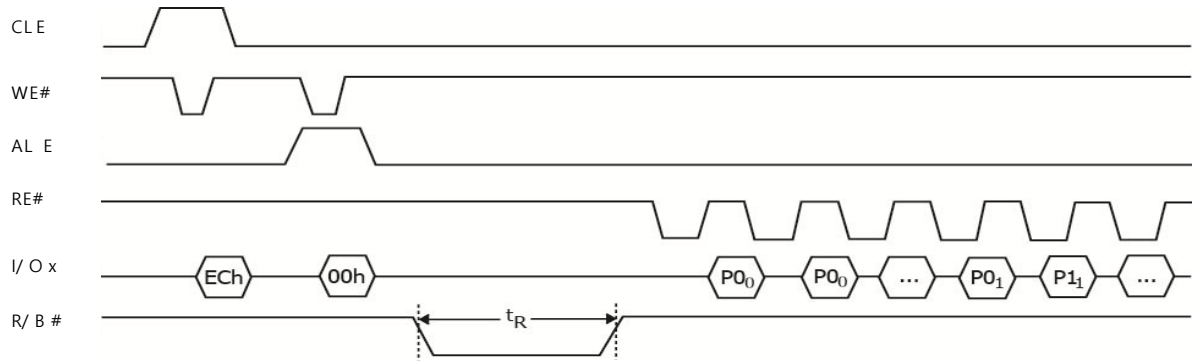
Figure 18 : ONFI Signature timing



3.4. Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. *Figure 19* defines the Read Parameter Page behavior. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at least three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.
The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

Figure 19 : Read Parameter Page timings



3.4.1. Parameter Page Data Structure Definition

For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h. For more detailed
information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Table 16 : Parameter Page Description

Byte	O/M	Description
	Revision information and features block	
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page copy-back 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports copy-back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command
10-31		Reserved (0)
	Manufacturer information block	
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-79		Reserved (0)
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
	Memory organization block	
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page

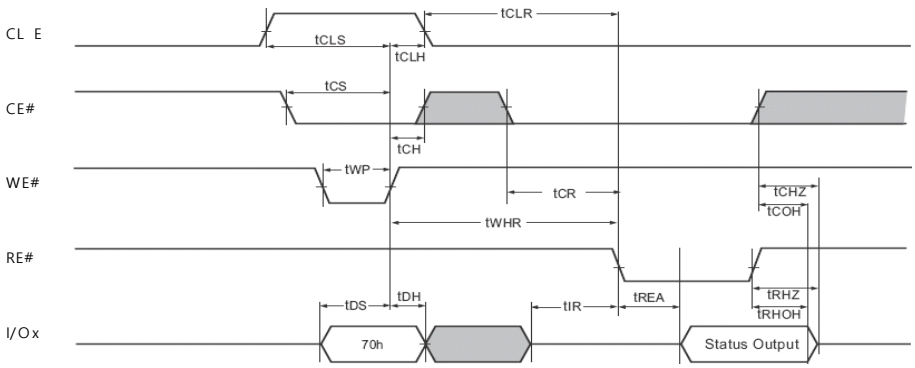
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (***μs***)
135-136	M	t_{BERS} Maximum block erase time (***μs***)
137-138	M	t_R Maximum page read time (***μs***)
139-140	M	tCCS Minimum change column setup time (ns)
141-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC
	Redundant Parameter Pages	
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Note: "O" Stands for Optional, "M" for Mandatory

3.5. Read Status

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to "*Table 17*". Status Register Coding" for specific Status Register definitions, and *Figure 20* for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Figure 20 : Read Status timings



Refer to *Table 17* for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.

Table 17 : Read Status Register Coding

	Value Definition	Block Erase	Page Program	Page Read	OTP Block Protect
DQ0	Pass : "0" Fail : "1"	Pass / Fail	Pass / Fail	Not Use	Program Pass / Fail
DQ1	Reserved	Not Use	Not Use	Not Use	Not Use
DQ2	Reserved	Not Use	Not Use	Not Use	Not Use
DQ3	OTP Not Protected : "0" OTP Protected : "1"	Not Use	Not Use	Not Use	Not Protected/ Protected
DQ4	(1) Page Recommended to Rewrite : "1" Page Normal/On-die ECC disabled : "0" (2) Page Uncorrectable : "1" Page Normal/On-die ECC disabled : "0"	Not Use	Not Use	1 (default) or 2	Not Use
DQ5	Busy : "0" Ready : "1"	Not Use	Program in progress/ Completed	Not Use	Not Use
DQ6	Busy : "0" Ready : "1"	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy
DQ7	Protected : "0" Not Protected : "1"	Write Protect	Write Protect	Write Protect	Write Protect

Note:
1. DQ0 : This bit is only valid for Program and Erase operations. If cleared to zero, then the last command was successful. If set to one, then the last command failed. For two plane operation, it indicates that one or both planes failed. The Read Status Enhanced (78h) operation can be used to determine with plane the operation failed. If a block is protected, this bit should fail
2. DQ3 : This bit indicates whether the OTP is lock down, and should be cleared to zero, when not in OTP mode, or FF command is issued, or on power up. This bit should be set to one after lock down command is issued, or when OTP operation (program/rease/erase) command is issued and OTP is lock down.
3. DQ4 : If the internal ECC is On, this bit indicates if the last pare read contained ECC errors. It is supported in two modes of 1(default) or 2, which is selectable using feature register address 90h bit [4]. These registers can be modified using the Set Feature command.
   - 1 : The 1 indicates if one page has a high ECC error count and recommending to rewrite the page. If set to one, it is recommended to rewrite the entire page. If cleared to zero, it is in normal state (internal ECC enabled, error counts are in safe level), or UECC, or internal ECC disabled.
   - 2 : The 2 indicates if the page has more ECC errors than then internal engine can correct (UECC). If set to one, it is ECC Fail and the page is uncorrectable. If cleared to zero, then it is in normal state (internal ECC enabled, safely working), or internal ECC disabled.
4. DQ5 : If set to one then there is no array operation in progress. If cleared to zero, then there is a command being progressed.
5. DQ7 : If set to one, then the device is not write protected. If cleared to zero, then the device is write protected. This bit shall always be valid regardless of state of the R/B#. For Status Enhanced command, signal follows WP pin.

3.6. Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases- on a specific die of a multi-dice stack configurations (single CE#), in case of concurrent operations When 4Gbit dies are stacked(*) to form 8Gbit DDP or 16Gbit QDP (single CE#), it is possible to run a first operation on the first 4Gbit, then activate a concurrent operation on the second (or third or fourth) device. (examples: Erase while Read, Read while Program, etc.) - on a specific plane in case of multi-plane operations in the same die.

Figure 21 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest. Read Status Enhanced command only shows block status of previously accessed block before issuing the command.

Figure 21 : Read Status Enhanced cycle

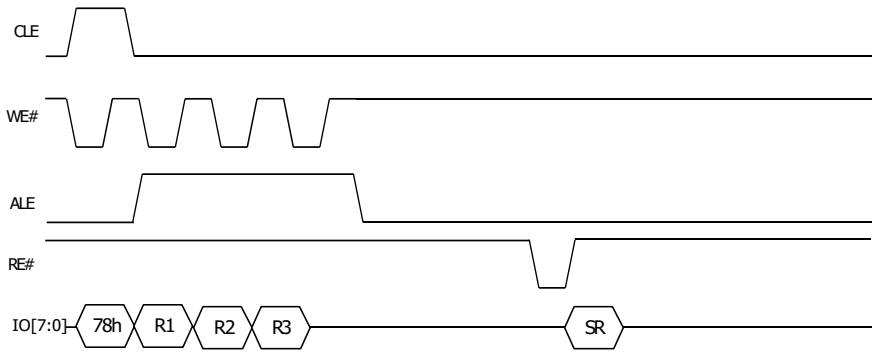


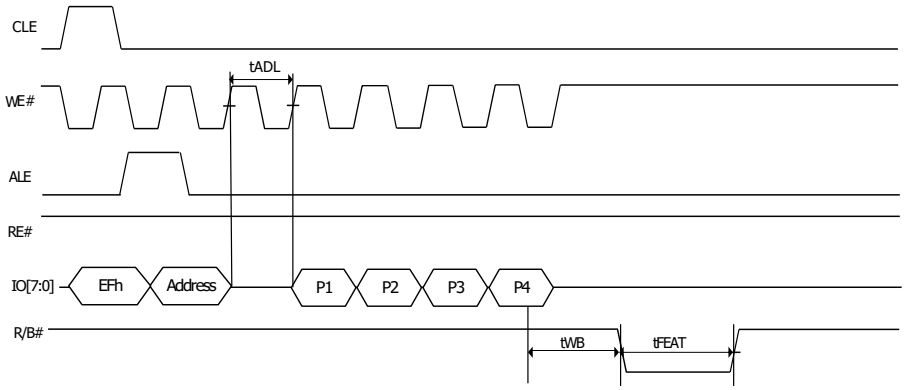
Table 18 : Read Status Enhanced Register Coding

	Value Definition	Block Erase	Page Program	Page Read	OTP Block Protect
DQ0	Pass : "0" Fail : "1"	Pass / Fail	Pass / Fail	Not Use	Not Use
DQ1	Reserved	Not Use	Not Use	Not Use	Not Use
DQ2	Reserved	Not Use	Not Use	Not Use	Not Use
DQ3	OTP Not Protected : "0" OTP Protected : "1"	Not Use	Not Use	Not Use	Not Protected/ Protected
DQ4	(1) Page Recommended to Rewrite : "1" Page Normal/On-die ECC disabled : "0" (2) Page Uncorrectable : "1" Page Normal/On-die ECC disabled : "0"	Not Use	Not Use	1 (default) or 2	Not Use
DQ5	Busy : "0" Ready : "1"	Not Use	Program in progress/ Completed	Not Use	Not Use
DQ6	Busy : "0" Ready : "1"	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy
DQ7	Protected : "0" Not Protected : "1"	Write Protect/ PBP/VBP	Write Protect/ PBP/VBP	Write Protect/ PBP/VBP	Write Protect/ PBP/VBP

Note:
DQ4, DQ5 defines ECC status.

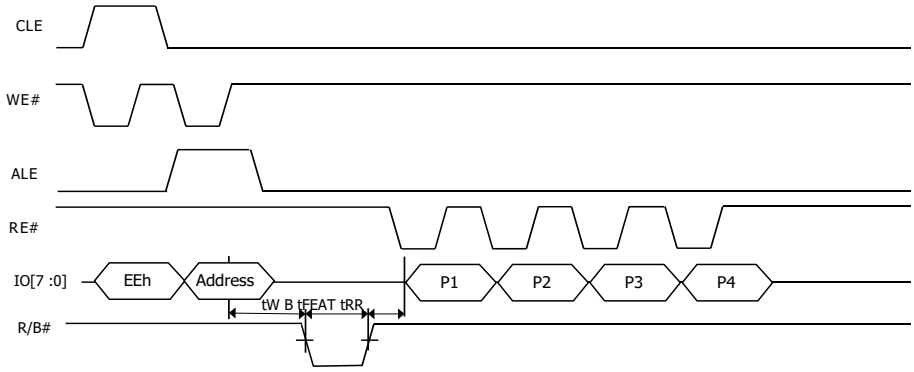
3.7. Set Feature

Figure 22 : Set Feature timing



3.8. Get Feature

Figure 23 : Get Feature timing



FOUNDER

Table 19 : Feature Address 90h - Array Operation Mode (P1 register)

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	On-die ECC Status Description Select	On-die ECC Read Status Option Select	0	0: 1 1: 2
3	ECC_EN	ECC enable	1	1 : On-die ECC enabled (Default) 0 : On-die ECC disabled
2	Reserved	Reserved	0	
1	OTP Protection	OTP Area Protect	00	00 : OTP is not selected (Default) 01 : OTP Area Entry 11 : OTP Protection (Lock)
0	Normal vs. OTP operation	Normal (Array Operation)		

Note:
1. P2/P3/P4 are 00h.
2. A software Reset command (FFh) does not alter the content of the 90h feature register.
3. Bit4 of Feature Address 90h allows user to select if Read Status DQ4 shows 1 (default) or 2.
(1) Page Recommended to Rewrite : "1", Page Normal/On-die ECC disabled : "0"
(2) Page Uncorrectable : "1", Page Normal/On-die ECC disabled : "0"

Table 20 : Feature Address 80h - Programmable I/O Strength Mode (P1 register)

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	Reserved	Reserved	0	
3 2 1 0	I/O Drive Strength	I/O Strength Selection	0000	0000: Full Strength (Default). 18Ω output impedance 0001: 75% of Full Strength, 25Ω output impedance 0010: 50% of Full Strength, 35Ω output impedance 0011: 25% of Full Strength, 50Ω output impedance

Note:
1. P2/P3/P4 are 00h.
2. A software Reset command (FFh) does not alter the content of the 80h feature register.

3.9. DQ Driver Strength

The device may be configured with multiple driver strengths with Set Features command. Device supports Underdrive, Nominal, Overdrive1, and Overdrive2 options and each settings comply with the output driver requirements followed in this section.

Table 21 : I/O Drive Strength Settings

Setting	Driver Strength	Vcc
18 Ohms	2.0x = 18 Ohms	3.3V
25 Ohms	1.4x = 25 Ohms	
35 Ohms	1.0x = 35 Ohms	
50 Ohms	0.7x = 50 Ohms	

Table 22 : Output Drive Strength Impedance Values

Output Strength	Rpd/Rpu	Vout to VSS	Minimum	Nominal	Maximum	Unit
Underdrive	Rpd	0.2 x Vcc	18.4	45.0	80.0	Ohm
		0.5 x Vcc	25.0	50.0	100.0	
		0.8 x Vcc	32.0	57.0	136.0	
	Rpu	0.2 x Vcc	32.0	57.0	136.0	
		0.5 x Vcc	25.0	50.0	100.0	
		0.8 x Vcc	18.4	45.0	80.0	
Nominal	Rpd	0.2 x Vcc	12.8	32.0	58.0	
		0.5 x Vcc	18.0	35.0	70.0	
		0.8 x Vcc	23.0	40.0	95.0	
	Rpu	0.2 x Vcc	23.0	40.0	95.0	
		0.5 x Vcc	18.0	35.0	70.0	
		0.8 x Vcc	12.8	32.0	58.0	
Overdrive1	Rpd	0.2 x Vcc	9.3	22.3	40.0	
		0.5 x Vcc	12.6	25.0	50.0	
		0.8 x Vcc	16.3	29.0	68.0	
	Rpu	0.2 x Vcc	16.3	29.0	68.0	
		0.5 x Vcc	12.6	25.0	50.0	
		0.8 x Vcc	9.3	19.0	40.0	
Overdrive2	Rpd	0.2 x Vcc	7.0	16.2	28.7	
		0.5 x Vcc	9.0	18.0	36.0	
		0.8 x Vcc	11.8	21.0	50.0	
	Rpu	0.2 x Vcc	11.8	21.0	50.0	
		0.5 x Vcc	9.0	18.0	36.0	
		0.8 x Vcc	7.0	14.0	28.7	

Test conditions for impedance value verifications are listed on *Table 23.*

Table 23 : Test Conditions for Impedance Values

Condition	Temperature	Vcc	Process
Minimum Impedance	T_{OPER}(Min)	3.6V	Fast-Fast
Nominal Impedance	+25℃	3.3V	Typical-Typical
Maximum Impedance	T_{OPER}(Max)	2.7V	Slow-Slow

The pull-up and pull-down impedance mismatch requirements are defined in *Table 24*. Impedance mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage. The testing conditions that shall be used to verify the impedance mismatch requirements are Vcc = Vcc (min), Vout = Vcc x 0.5 and T_A is across the full operating range.

Table 24 : Pull-up and Pull-down Output Impedance Mismatch

Drive Strength	Minimum	Maximum	Unit
Overdrive2	0	6.3	Ohms
Overdrive1	0	8.8	Ohms
Nominal	0	12.3	Ohms
Underdrive	0	17.5	Ohms

3.10. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 4,352 (4KB Page) or 2,176 (2KB Page) bytes of data within the selected page are transferred to the data registers in less than 400us (tR, 4KB, 2KB-multi-plane), or 200us (tR, 2KB-single plane). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B# pin. Once the data in a page is loaded into the data registers, they may be read out in 20ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address. The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page. Check *Figure 24* to *Figure 26* as references.

Figure 24 : Page Read Operation Timings (Intercepted by CE#)

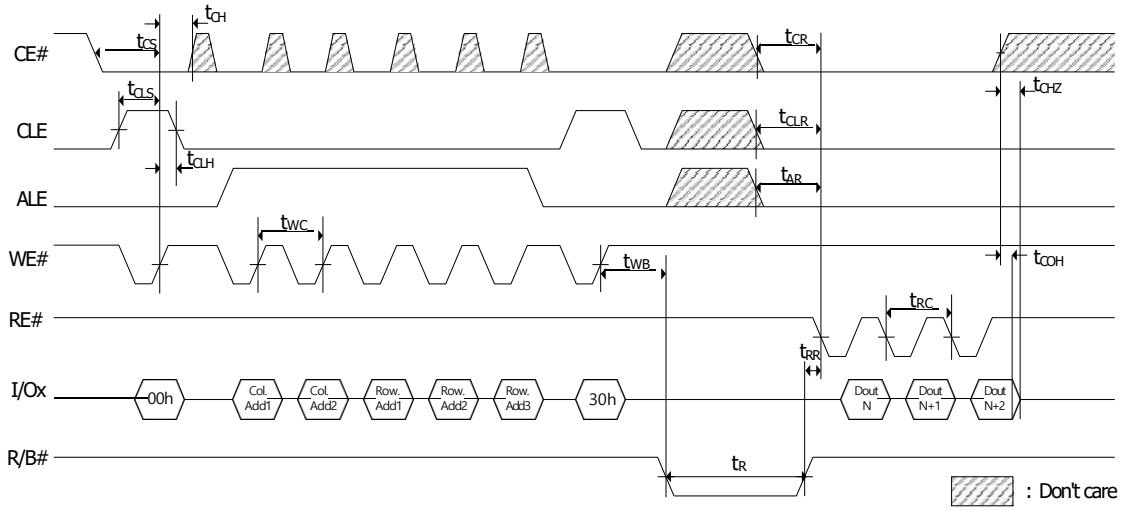


Figure 25 : Page Read Operation Timings with CE# don't care

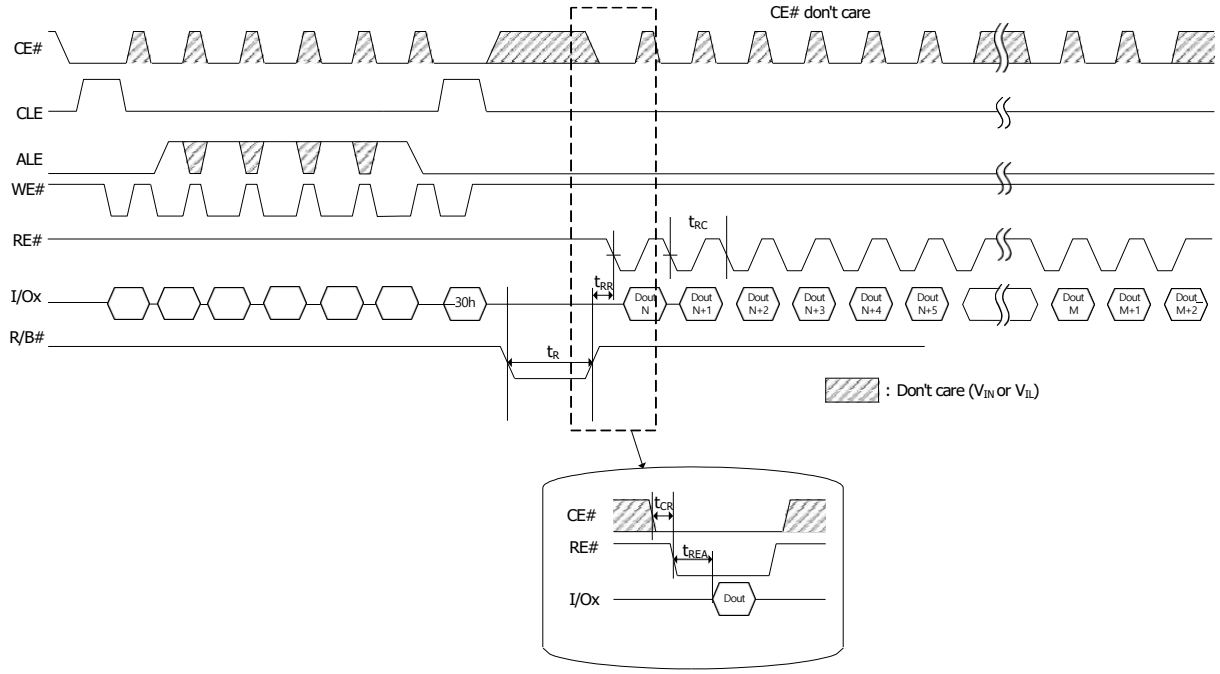
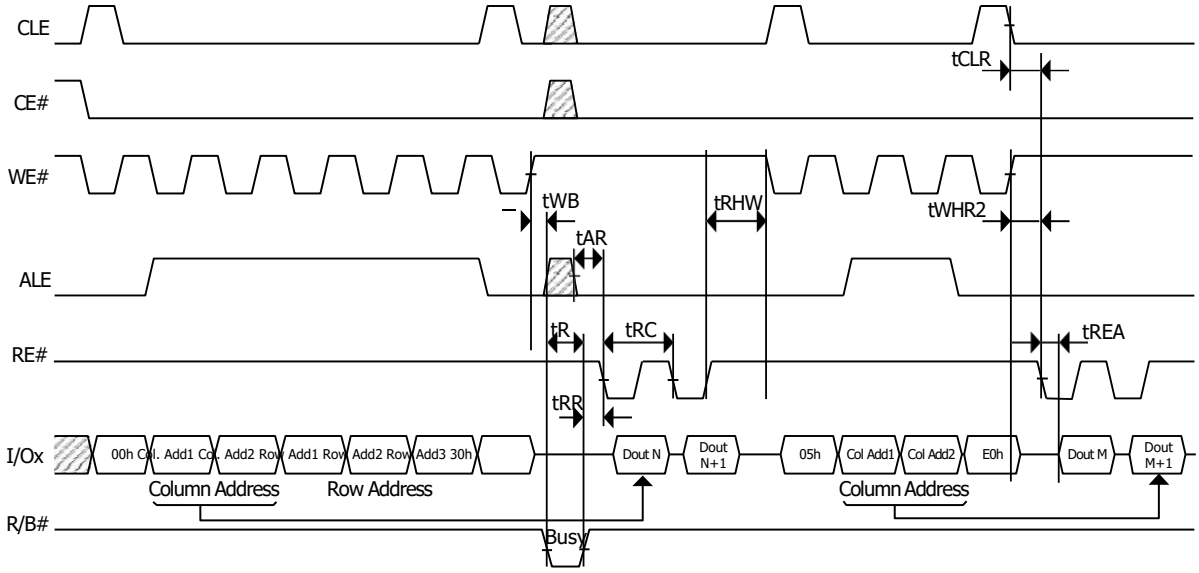


Figure 26 : Random Data Output timings



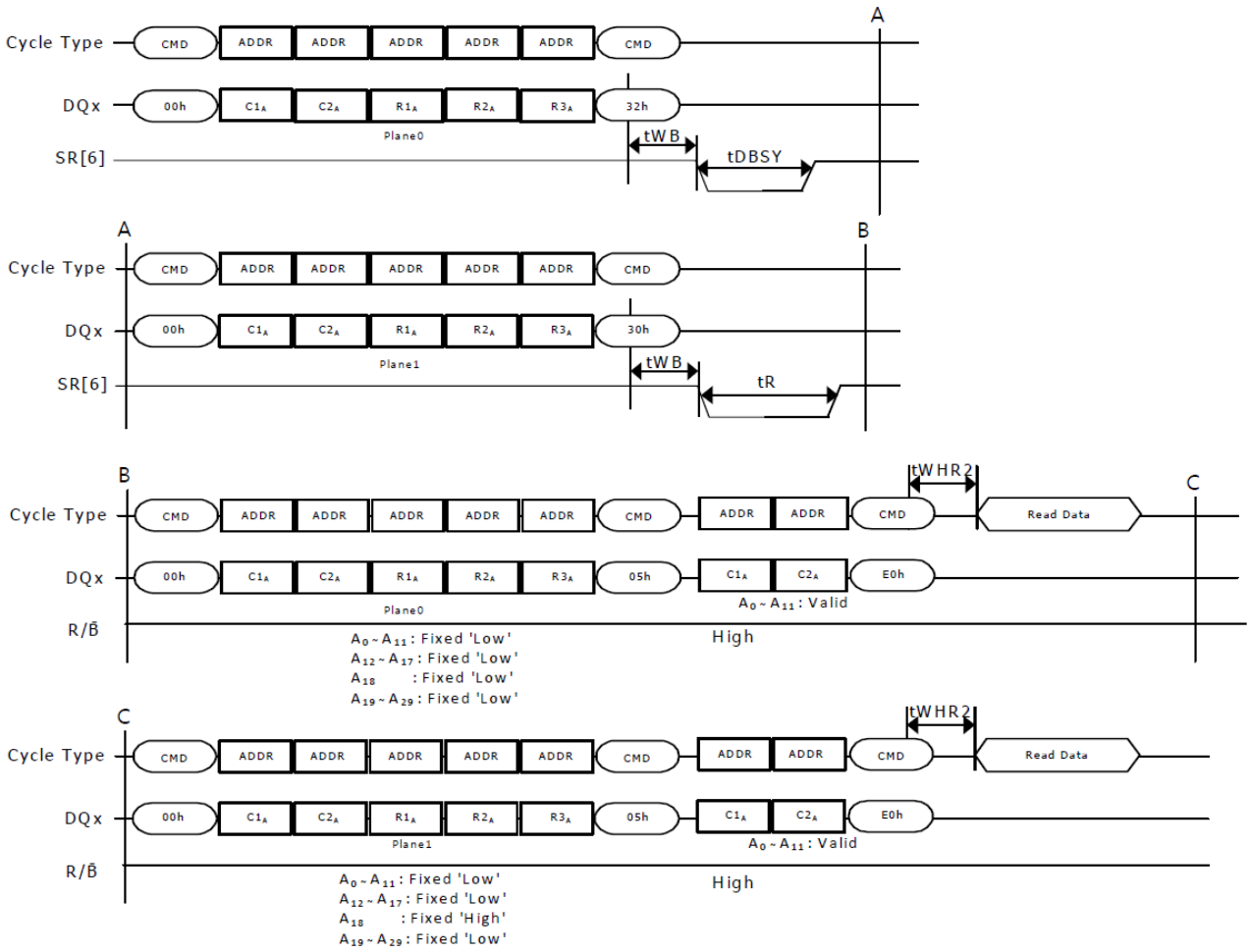
3.11. Multi-plane Page Read

Device supports multiple plane read: it is possible to read 2 pages data out in parallel, one per each plane. A multiple plane read cycle consists of a double serial data loading period in which up to 2,176 bytes (2KB page) of data may be loaded into the data register, followed by a non-volatile read period where the data gets read out.

The serial data loading period begins with inputting the Serial Data Input command (00h), followed by the five cycle address for outputting data for the 1st page. Address for this page must be in the 1st plane. The device supports random data input exactly same as in the case of page read operation. The Dummy Page Read Confirm command (32h) stops 1st page data input and devices becomes busy for a short time (tDBSY). Once it has become ready again, "00h" command must be issued once again to read serial data out from following 2nd page address (5 cycles). Read Confirm command (30h) makes sequential read out of both pages to start.

Data read out after tR will show 1st plane data, because 1st plane address was selected before going into busy state followed by instructions above. Use random data out with plane address selection (5 cycles) to read out 2nd plane data. *Figure 27* describes the Multi-plane Page Read sequence and Random data out with 5 address cycles in detail.

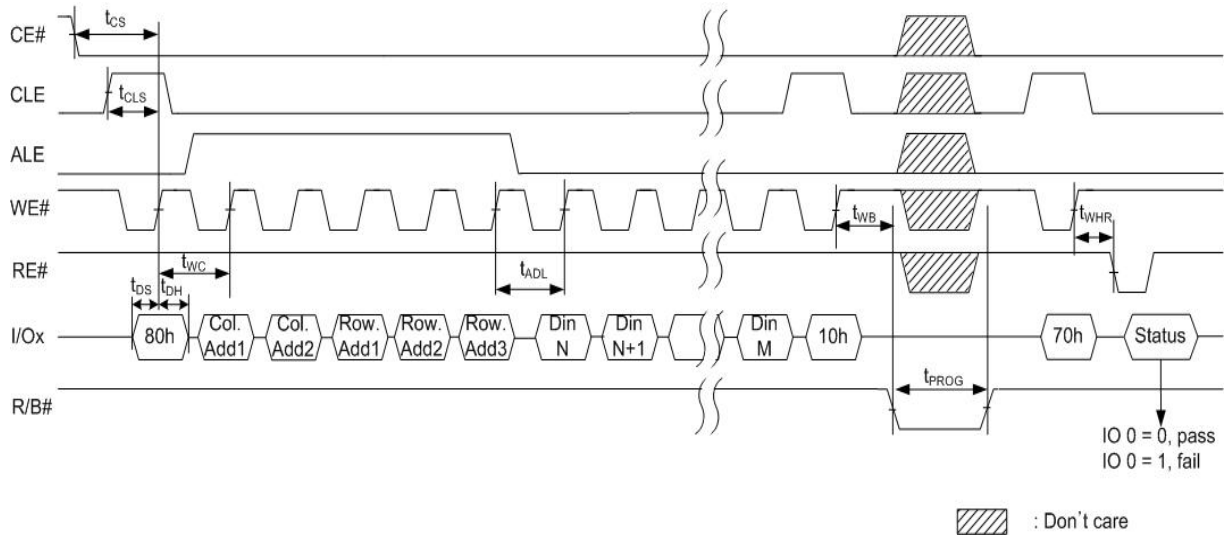
Figure 27 : Example Timing with Multi-plane Page Read Operation



3.12. Page Program

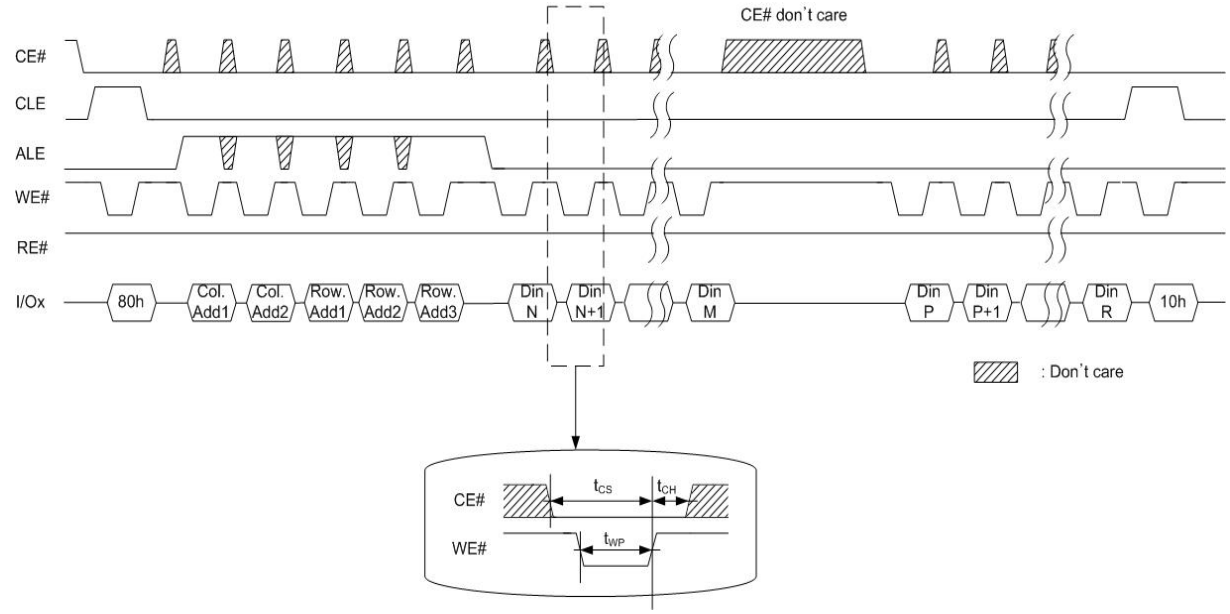
A page program cycle consists of a serial data loading period in which up to 2,176 bytes (2KB Page) or 4,352 bytes (4KB Page) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. *Figure 25* to *Figure 27* detail the sequence. The device is programmed basically by page, but it also allows multiple partial page programming of a word up to consecutive bytes up to 2,176 bytes (2KB Page) or 4,352 bytes (4KB Page) in a single page program cycle. The basic unit of Program operation is 32bytes per 1 ECC chunk and Program input shall be made if and only if 32bytes or more input data detected.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/32byte) in the case of 2KB Page. Consequent input of to be programmed main data following with ECC user spare is not allowed. Main data shall be stored in main data region, and then use Random Data Input to change column to the address of user spare for programming of corresponding user spare of input data. Both main data and user spare shall be input for NOP operation; if only user spare input without main data partially programmed (NOP) at the same time, data is no longer guaranteed.

Figure 28 : Page Program Operation Timings



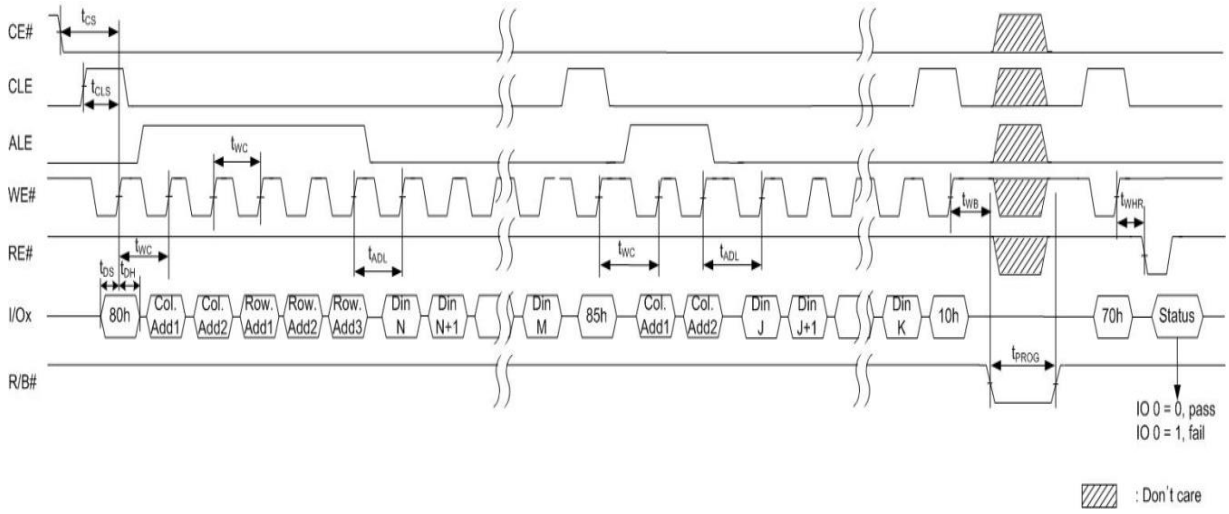
Note:
t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Figure 29 : Page Program Operation Timings with CE# don't care



Note:
t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Figure 30 : Random Data Input Timings



Note:
1. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
2. Random data input can be performed in a page.

3.12.1. Guidance to User Spare Program

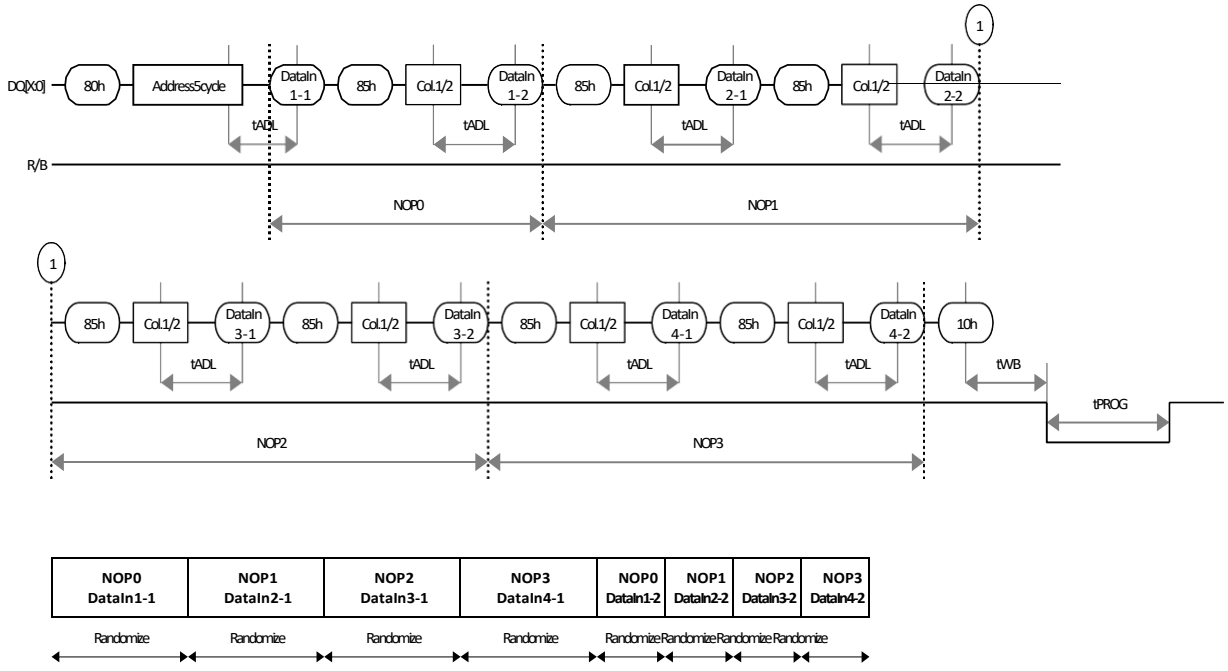
The number of consecutive partial page programming operations within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/32byte) in the case of 2KB Page. Number of Program (NOP) refers to main area that is divided and programmed in each number of partial program operation.

During NOP program, data that is designated to user spare area shall use random data input to change column address. Because NOP is allowed in maximum of 4 times, user spare area is also divided into 4 regions to match up to each NOP area. Main data is divided using NOP, and randomized while programming the data. Although user spare that is included in each NOP is also randomized, randomization done between main data and user spare are different as below ***Figure 31.*** Therefore, for each NOP, column address change shall be kept to match up correct NOP with NOP user spare.

At first, input 512 bytes of data for NOP0, then user spare data for NOP0 shall be inputted after changing of column address using Random Data Input. After programming of data, using of Random Data Input to return back to starting address of NOP1 main data shall be done. Secondly, input 512 bytes of NOP1 data, using Random Data Input to chagnge column address to user spare data for NOP1 inputting. After programming of user spare data for NOP1, return back to starting address of NOP2 main data starting address. NOP2 and NOP3 shall follow same manner as above.

If user decide to follow same order as programming order during data out, read out NOP0 area first, then using of Random Data Output to change column address to read out NOP0 user spare area shall be followed.

Figure 31 : Random Data Input Timings



FOUNDER

Table 25 : NOP Chunk Column Address (4K Page)

NOP0	Column (Hex)	NOP1	Column (Hex)	NOP2	Column (Hex)	NOP3	Column (Hex)
Chunk0	000~01F	Chunk0	400~41F	Chunk0	800~81F	Chunk0	C00~C1F
Chunk1	020~03F	Chunk1	420~43F	Chunk1	820~83F	Chunk1	C20~C3F
Chunk2	040~05F	Chunk2	440~45F	Chunk2	840~85F	Chunk2	C40~C5F
Chunk3	060~07F	Chunk3	460~47F	Chunk3	860~87F	Chunk3	C60~C7F
Chunk4	080~09F	Chunk4	480~49F	Chunk4	880~89F	Chunk4	C80~C9F
Chunk5	0A0~0BF	Chunk5	4A0~4BF	Chunk5	8A0~8BF	Chunk5	CA0~CBF
Chunk6	0C0~0DF	Chunk6	4C0~4DF	Chunk6	8C0~8DF	Chunk6	CC0~CDF
Chunk7	0E0~0FF	Chunk7	4E0~4FF	Chunk7	8E0~8FF	Chunk7	CE0~CFF
Chunk8	100~11F	Chunk8	500~51F	Chunk8	900~91F	Chunk8	D00~D1F
Chunk9	120~13F	Chunk9	520~53F	Chunk9	920~93F	Chunk9	D20~D3F
Chunk10	140~15F	Chunk10	540~55F	Chunk10	940~95F	Chunk10	D40~D5F
Chunk11	160~17F	Chunk11	560~57F	Chunk11	960~97F	Chunk11	D60~D7F
Chunk12	180~19F	Chunk12	580~59F	Chunk12	980~99F	Chunk12	D80~D9F
Chunk13	1A0~1BF	Chunk13	5A0~5BF	Chunk13	9A0~9BF	Chunk13	DA0~DBF
Chunk14	1C0~1DF	Chunk14	5C0~5DF	Chunk14	9C0~9DF	Chunk14	DC0~DDF
Chunk15	1E0~1FF	Chunk15	5E0~5FF	Chunk15	9E0~9FF	Chunk15	DE0~DFF
Chunk16	200~21F	Chunk16	600~61F	Chunk16	A00~A1F	Chunk16	E00~E1F
Chunk17	220~23F	Chunk17	620~63F	Chunk17	A20~A3F	Chunk17	E20~E3F
Chunk18	240~25F	Chunk18	640~65F	Chunk18	A40~A5F	Chunk18	E40~E5F
Chunk19	260~27F	Chunk19	660~67F	Chunk19	A60~A7F	Chunk19	E60~E7F
Chunk20	280~29F	Chunk20	680~69F	Chunk20	A80~A9F	Chunk20	E80~E9F
Chunk21	2A0~2BF	Chunk21	6A0~6BF	Chunk21	AA0~ABF	Chunk21	EA0~EBF
Chunk22	2C0~2DF	Chunk22	6C0~6DF	Chunk22	AC0~ADF	Chunk22	EC0~EDF
Chunk23	2E0~2FF	Chunk23	6E0~6FF	Chunk23	AE0~AFF	Chunk23	EE0~EFF
Chunk24	300~31F	Chunk24	700~71F	Chunk24	B00~B1F	Chunk24	F00~F1F
Chunk25	320~33F	Chunk25	720~73F	Chunk25	B20~B3F	Chunk25	F20~F3F
Chunk26	340~35F	Chunk26	740~75F	Chunk26	B40~B5F	Chunk26	F40~F5F
Chunk27	360~37F	Chunk27	760~77F	Chunk27	B60~B7F	Chunk27	F60~F7F
Chunk28	380~39F	Chunk28	780~79F	Chunk28	B80~B9F	Chunk28	F80~F9F
Chunk29	3A0~3BF	Chunk29	7A0~7BF	Chunk29	BA0~BBF	Chunk29	FA0~FBF
Chunk30	3C0~3DF	Chunk30	7C0~7DF	Chunk30	BC0~BDF	Chunk30	FC0~FDF
Chunk31	3E0~3FF	Chunk31	7E0~7FF	Chunk31	BE0~BFF	Chunk31	FE0~FFF
User Spare0 Chunk0	1000~101F	User Spare1 Chunk0	1040~105F	User Spare2 Chunk0	1080~109F	User Spare3 Chunk0	10C0~10DF
User Spare0 Chunk1	1020~103F	User Spare1 Chunk1	1060~107F	User Spare2 Chunk1	10A0~10BF	User Spare3 Chunk1	10E0~10FF

Table 26 : NOP Chunk Column Address (2K Page)

NOP0	Column (Hex)	NOP1	Column (Hex)	NOP2	Column (Hex)	NOP3	Column (Hex)
Chunk0	000~01F	Chunk0	200~21F	Chunk0	400~41F	Chunk0	600~61F
Chunk1	020~03F	Chunk1	220~23F	Chunk1	420~43F	Chunk1	620~63F
Chunk2	040~05F	Chunk2	240~25F	Chunk2	440~45F	Chunk2	640~65F
Chunk3	060~07F	Chunk3	260~27F	Chunk3	460~47F	Chunk3	660~67F
Chunk4	080~09F	Chunk4	280~29F	Chunk4	480~49F	Chunk4	680~69F
Chunk5	0A0~0BF	Chunk5	2A0~2BF	Chunk5	4A0~4BF	Chunk5	6A0~6BF
Chunk6	0C0~0DF	Chunk6	2C0~2DF	Chunk6	4C0~4DF	Chunk6	6C0~6DF
Chunk7	0E0~0FF	Chunk7	2E0~2FF	Chunk7	4E0~4FF	Chunk7	6E0~6FF
Chunk8	100~11F	Chunk8	300~31F	Chunk8	500~51F	Chunk8	700~71F
Chunk9	120~13F	Chunk9	320~33F	Chunk9	520~53F	Chunk9	720~73F
Chunk10	140~15F	Chunk10	340~35F	Chunk10	540~55F	Chunk10	740~75F
Chunk11	160~17F	Chunk11	360~37F	Chunk11	560~57F	Chunk11	760~77F
Chunk12	180~19F	Chunk12	380~39F	Chunk12	580~59F	Chunk12	780~79F
Chunk13	1A0~1BF	Chunk13	3A0~3BF	Chunk13	5A0~5BF	Chunk13	7A0~7BF
Chunk14	1C0~1DF	Chunk14	3C0~3DF	Chunk14	5C0~5DF	Chunk14	7C0~7DF
Chunk15	1E0~1FF	Chunk15	3E0~3FF	Chunk15	5E0~5FF	Chunk15	7E0~7FF
User Spare0	800~81F	User Spare1	820~83F	User Spare2	840~85F	User Spare3	860~87F

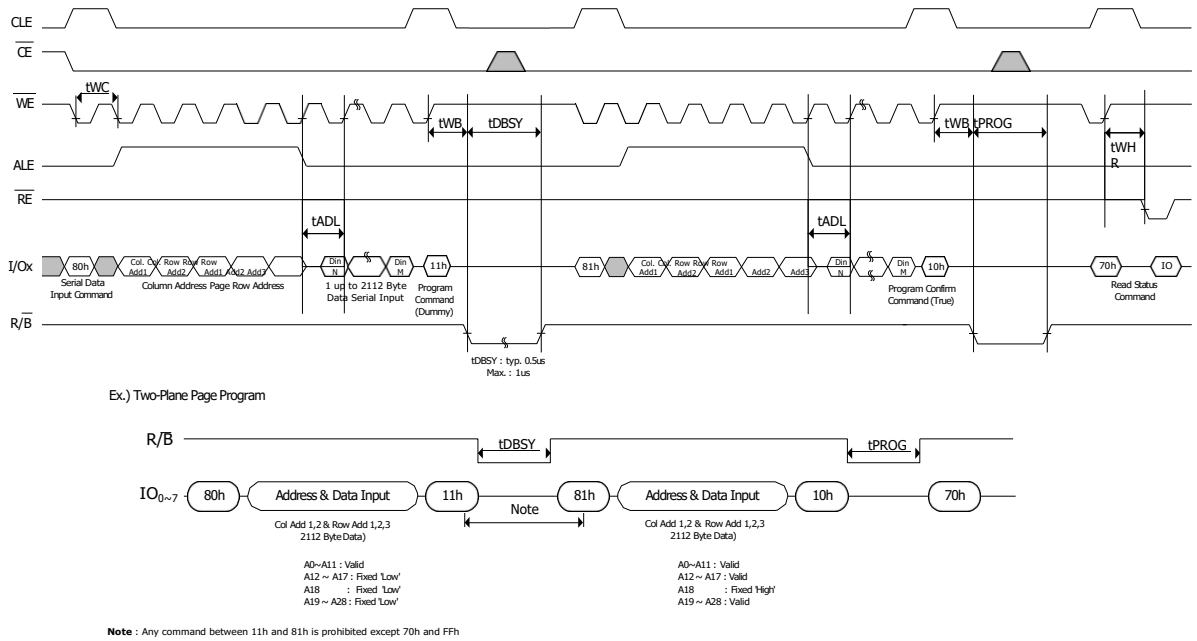
3.13. Multi-plane Page Program

Device supports multiple plane program: it is possible to program 2 pages in parallel, one per each plane. A multiple plane program cycle consists of a double serial data loading period in which up to 2,176 bytes (2KB page) or 4,352 bytes (4KB page) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane. The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (tDBSY).

Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane. Program Confirm command (10h) makes parallel programming of both pages to start. *Figure 32* and *Figure 33* describe the sequences.
User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: Read Status register command is also available during Dummy Busy time (tDBSY).

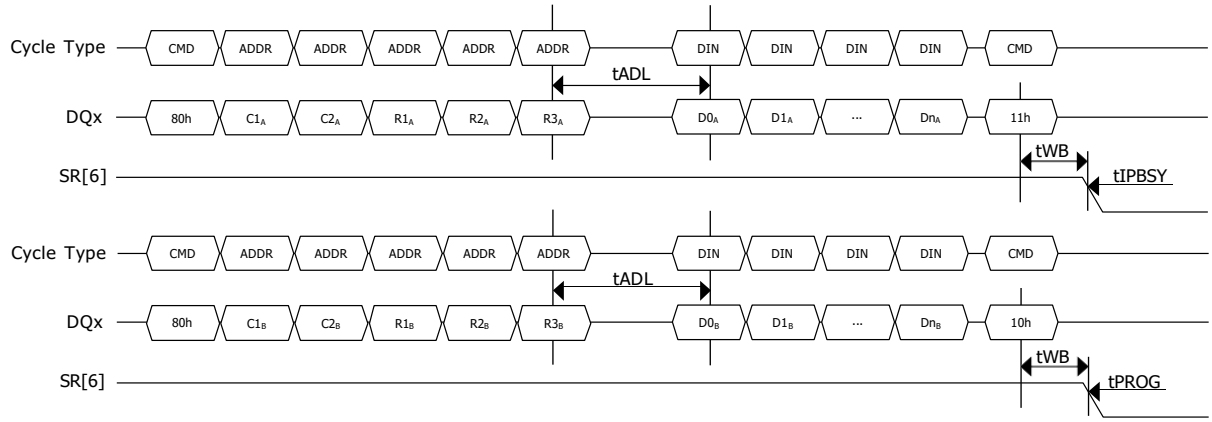
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "Read Status Enhanced" command must be issued Refer to *section 3.6* for further information.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/32byte) in the case of 2KB page.

Figure 32 : Multi-plane Page Program (Traditional Protocol)



Note:
1. Any command between 11h and 81h is prohibited except 70h, 78h and FFh

Figure 33 : Multi-plane Page Program (ONFI 1.0 Protocol)



Note:
1. C1A-C2A Column address for page A. C1A is the least significant byte.
2. R1A-R3A Row address for page A. R1A is the least significant byte.
3. D0A-DnA Data to program for page A.
4. C1B-C2B Column address for page B. C1B is the least significant byte.
5. R1B-R3B Row address for page B. R1B is the least significant byte.
6. D0B-DnB Data to program for page B.
7. Same restrictions on address of pages A and B, and allowed commands as ***Figure 33*** apply

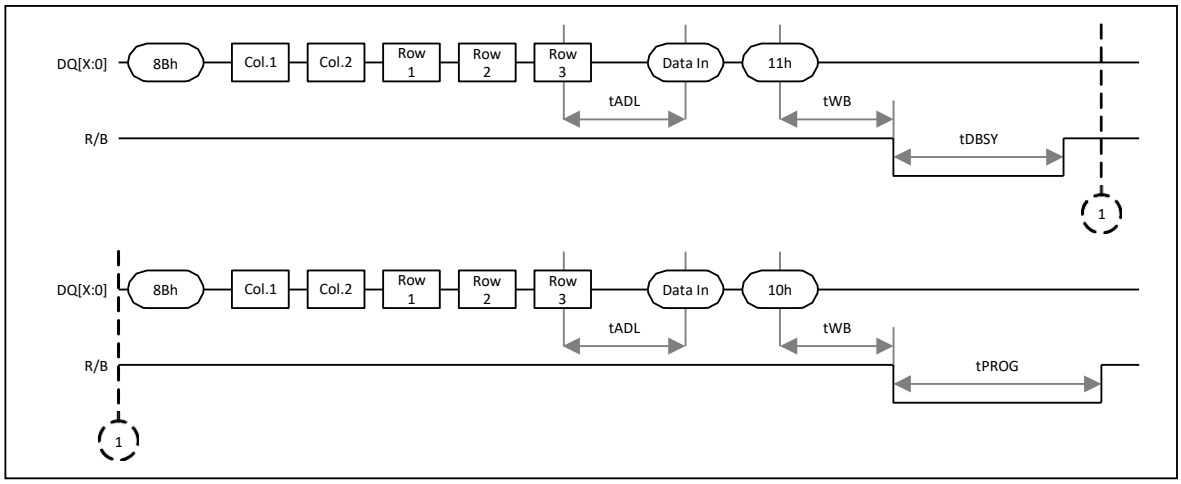
3.14. Page Re-program

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm "10h"
The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The "program confirm" command (10h) initiates the re-programming process.
The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

3.15. Multi-plane Page Re-program

Page Re-program can be worked on multi-plane, please refer to below *Figure 34* for detail description.

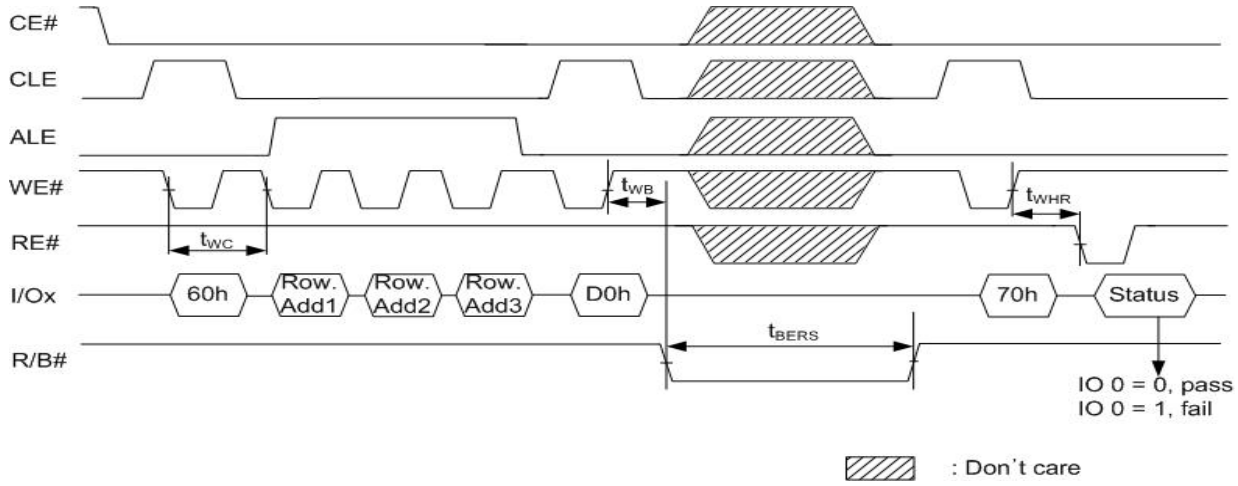
Figure 34 : Multi-plane Re-program timing



3.16. Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A31 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 35 : Block Erase Operation Timings



3.17. Multi-plane Block Erase

Multiple plane erase, allows parallel erase of two blocks in parallel, one per each memory plane.
Two different command sequences are allowed in these case, traditional and ONFI 1.0.
In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block insertion. See *Figure 35* for details.

As an alternative, the ONFI 1.0 multi-plane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multi-plane confirm). Between the two block-related sequences, a short busy time tDBSY will occur. See *Figure 36* for details.

Address limitation required for multiple plane program applies also to multiple plane erase. Also operation progress can be checked like in the multiple plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced. As for multi-plane page program, the address of the first second page must be within the first plane(A18=0 for 2KB devices) and second plane(A18=1 for 2KB devices), respectively.

Figure 36 : Multi-plane Block Erase (Traditional Protocol)

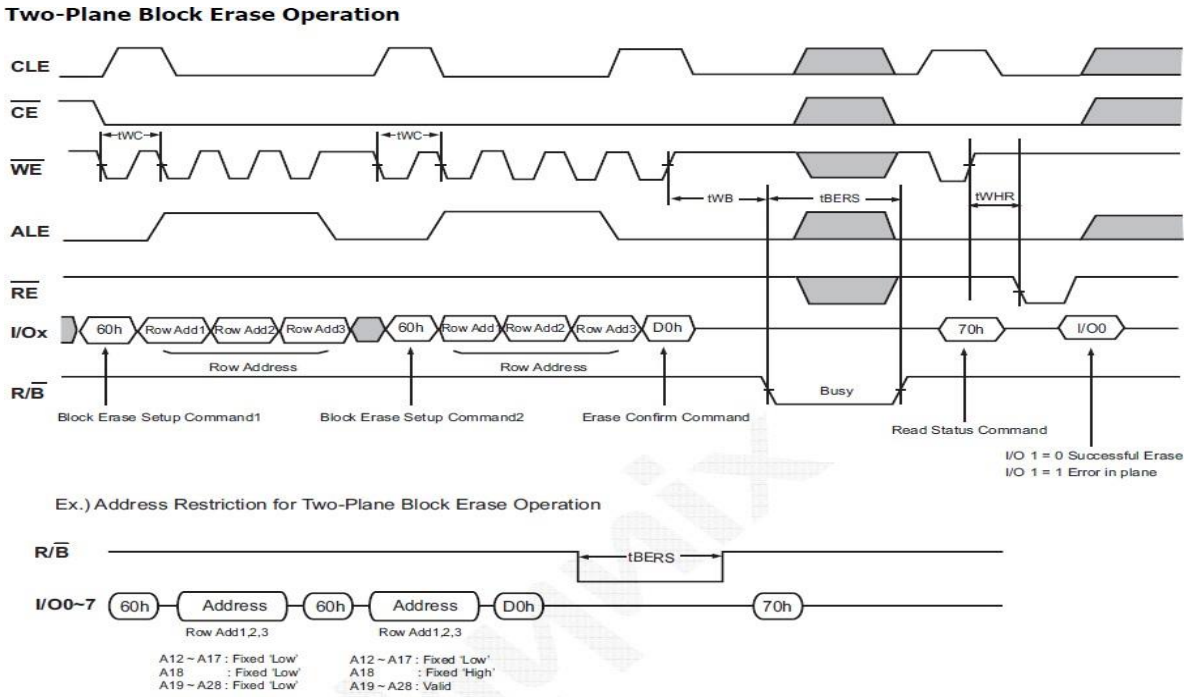
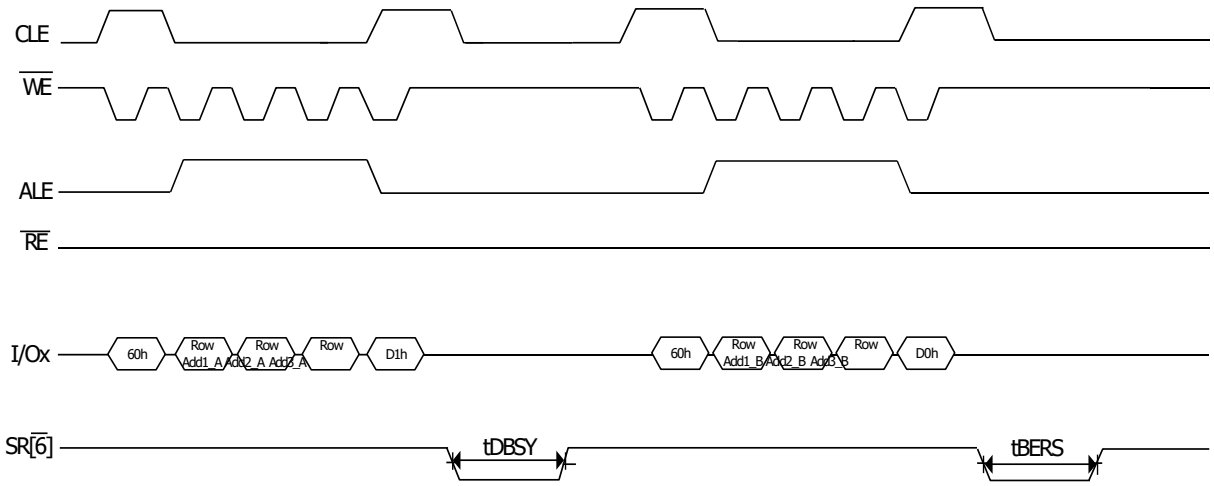


Figure 37 : Multi-plane Block Erase (ONFI 1.0 protocol)

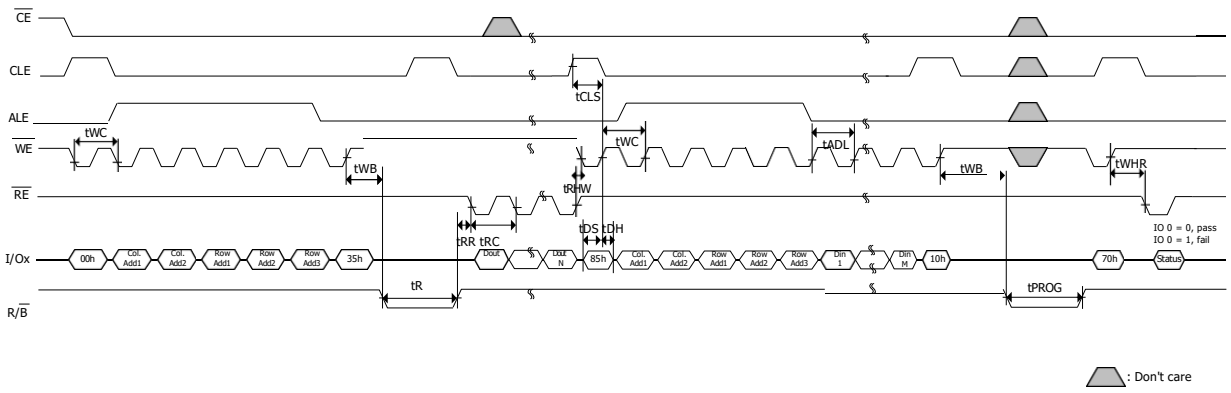


Note:
1. R1A-R3A Row address for block on plane 0. R1A is the least significant byte.
2. R1B-R3B Row address for block on plane 1. R1B is the least significant byte.
3. Same restrictions on address of blocks on plane 0(A) and 1(B) and allowed commands as ***Figure 35*** apply

3.18. Copy-back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block.
The copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2,176 bytes (2KB Page) or 4,352 bytes (4KB Page) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or copy-back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in *Figure 37* "copy-back Program with Random Data Input".
When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, one bit error correction is recommended for the use of Copy-Back operation. *Figure 37* shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy-back, while it must be set to Vcc When performing the program.

Figure 38 : Copy-back Program Operation Timing with Random Data Input



Note:
1) tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Because of sub plane structure of MKPVXG08CX-KS, copy-back read requires additional read time of 30us for 4KB Page or Multi-Plane operation and 15us for 2KB Page-single Plane. For detailed value, please refer to copy-back read timing values shown in Table 31.

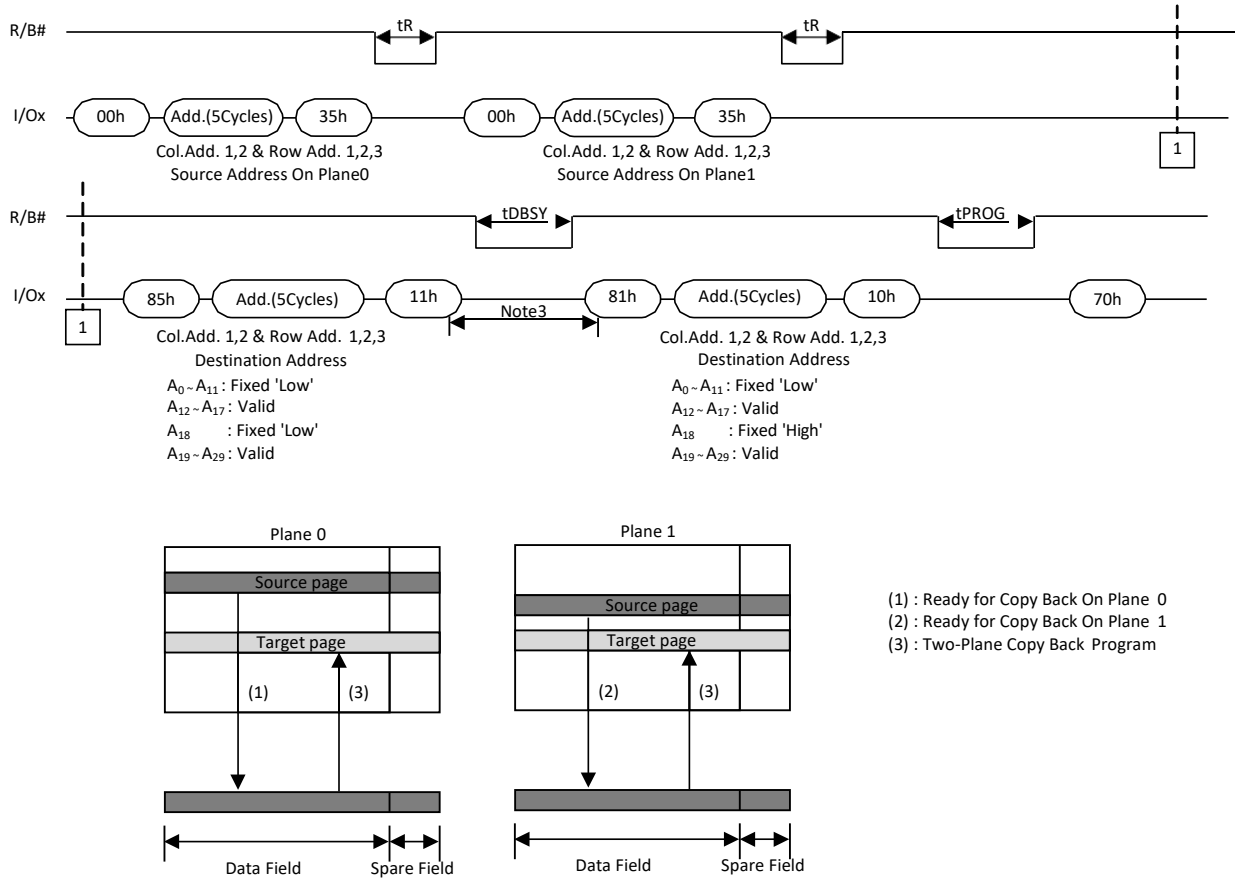
Table 31 : Copy-Back function - Read Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Single Plane Read (4KB Page)	t_R	-	70	365	us
Single Plane Read (2KB Page)		-	60	265	us
Multi-Plane Read (2KB Page)		-	85	480	us

3.19. Multi-plane Copy-back Program

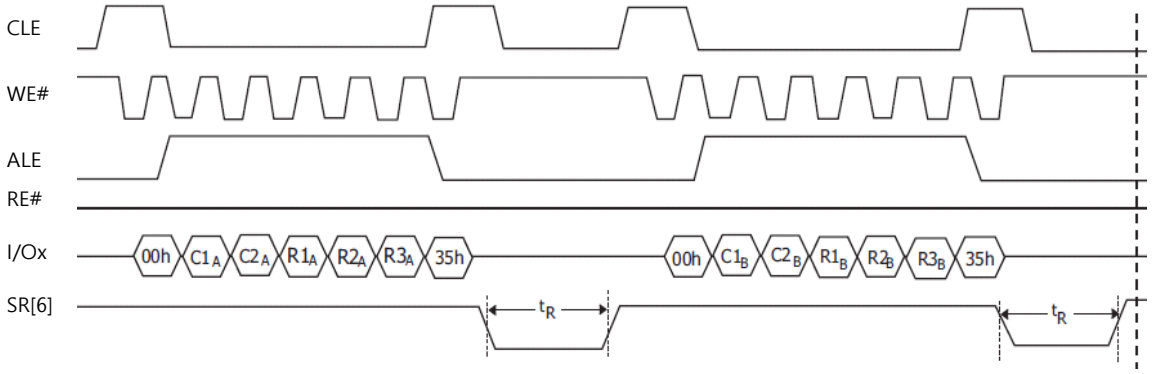
As for page program, device supports multi-plane copy-back program with exactly same sequence and limitations. Multi-plane copy-back program must be preceded by 2 single page read for copy-back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multi-plane copy-back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.
Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) represented in *Figure 39*, and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h) represented in *Figure 40* and *Figure 41.*

Figure 39 : Multi-plane Copy-back Program (Traditional Protocol)



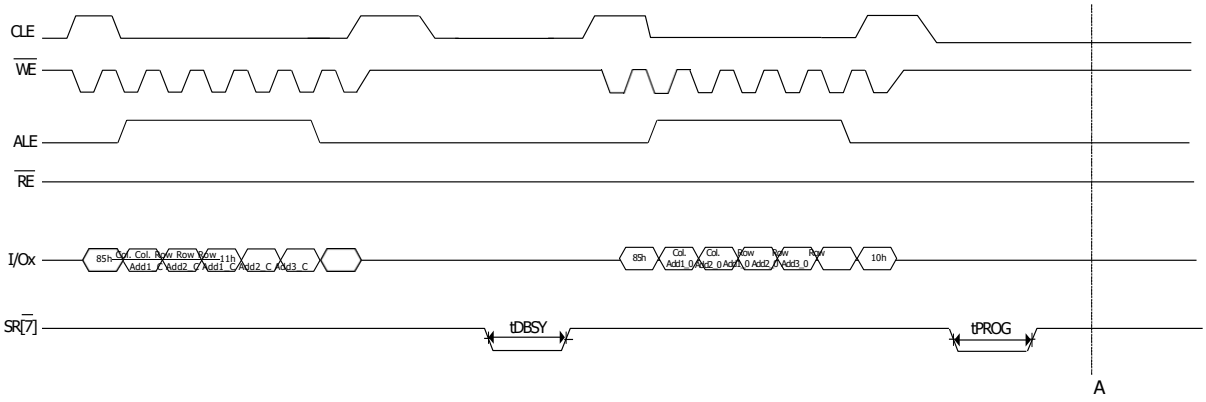
Note:
1. Copy-back program operation is allowed only within the same memory plane
2. Any command between 11h and 81 h is prohibited except 70h and FFh.
3. Plane0 A_{12}~A_{17} and Plane1 A_{12}~A_{17} are both valid and have to be the same value.

Figure 40 : Multi-plane Copy-back Read (ONFI 1.0 protocol)



Note:
1. C1A-C2A Column address for page A. C1A is the least significant byte.
2. R1A-R3A Row address for page A. R1A is the least significant byte.
3. C1B-C2B Column address for page B. C1B is the least significant byte.
4. R1B-R3B Row address for page B. R1B is the least significant byte.

Figure 41 : Multi-plane Copy-back Program (ONFI 1.0 protocol)



Note:
1. C1C-C2C Column address for page C. C1A is the least significant byte.
2. R1C-R3C Row address for page C. R1A is the least significant byte.
3. D0C-DnC Data to program for page C.
4. C1D-C2D Column address for page D. C1B is the least significant byte.
5. R1D-R3D Row address for page D. R1B is the least significant byte.
6. D0D-DnD Data to program for page D.
7. Same restrictions on address of pages C and D, and allowed commands as *Figure 36* apply

3.20. One-Time Programmable (OTP)

One-Time Programmable (OTP) entry can be done in two ways, by using vendor command sequence shown in *Table 9. Commands Set,* or issuing Set Feature (EFh) command with Feature address 90h, P1=09h, P2=00h, P3=00h, P4=00h. Please find more details on *Section 3.7 Set Features*, and *Section 3.8 Get Features*. Get Feature (EEh) to read out information prior to issue Set Feature (EFh) shall be done, and user shall not change any other I/O options from Get Feature read out data. If OTP sequence is detected, On-die ECC Correction is automatically turned on.

By issuing OTP Protection sequence shown in *Table 9. Command Set,* a page program sequence with an address of 00h-00h-00h-00h-00h and without Data Input is issued by host system to program the control bit for the OTP area. For OTP block access, block#3 should be addressed in case of 4K page size and 1 plane and block#6 should be addressed in case of 2K page and 2 plane respectively. For 4K Page-1 Plane, Row Address is 80h – 01h - 00h (Block#3), and for 2K Page-2 Plane, Row Address C0h – 00h – 00h (Block#6). The Status Read is then used to poll the status register to determine when the program operation is completed and verify that OTP area is protected. User should issue Set Feature (EFh) command with feature address 90h, P1=0Bh, P2=00h, P3=00h, P4=00h.

Copy-back and Reprogram command shown in *Table 9. Commands Set are not supported in OTP area.*

To exit the OTP area, host must issue the Reset FFh if host entered the OTP using vendor command sequence shown in ***Table 9***. If host entered the OTP using Feature address 90h, host can exit the OTP by issuing Set Feature (EFh) command with feature address 90h, P1=08h, P2=00h, P3=00h, P4=00h. A software RESET command (FFh) does not alter the content of 90h feature register, and cannot exit out of OTP mode.

If 2 dies are connected to single CE and OTP entry were made using vendor command sequence, then OTP protect will be applied and operated to 1st die only. Else if 2 dies are connected to single CE and OTP entry made by issuing Set Feature (EFh) command with Feature address 90h, then 1st and 2nd dies are OTP protected at the same time, because Set Feature is target level command.

OTP mode blocks are required to have higher retention and protection scheme, which elongates tPROG. Please refer to Table 28. PBP/OTP-Program Characteristic for detail value.

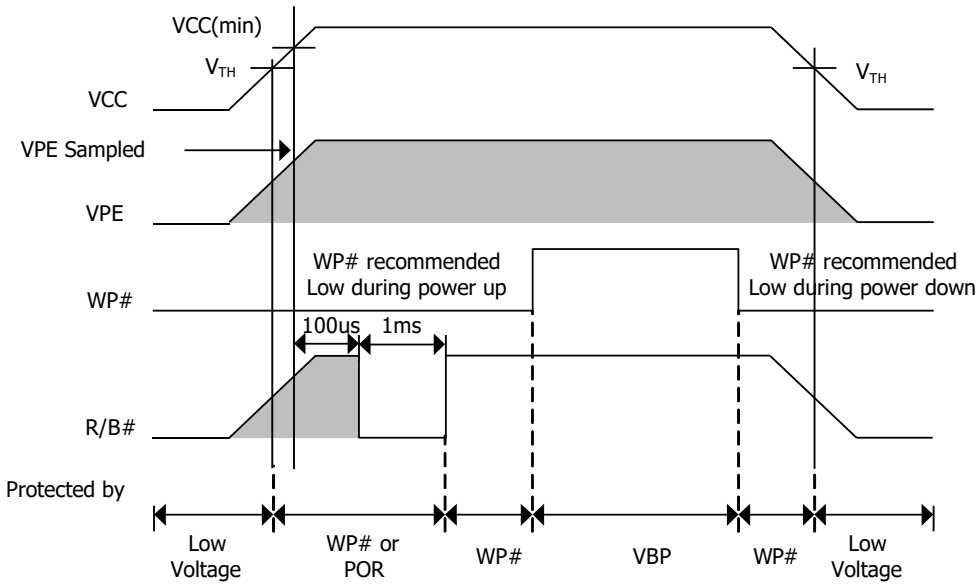
3.21. Volatile Block Protection (VBP)

The VBP security features provide block protection from program and erase operations; parameter settings are stored in a volatile memory. VBP commands are effective on the currently selected LUN(die). Power cycling will RESET the settings to the default status (all blocks protected assuming VPE pin is high). After power up, the VBP method can protect one range of contiguous blocks of 1st die, and if die selection has been changed to 2nd die using "78h"-3 address cycles, then 2nd die VBP can be activated by issuing VBP method.

This method requires use of a Volatile Protection Enable (VPE) input pin. To activate the VBP method using the VPE input, the host must power up the device with VPE input high during the Power-On Reset (POR) period and issue a set of commands to set the VBP parameter settings which consist of a Lower Boundary Address (LB_ADD) and an Upper Boundary Address (UB_ADD).

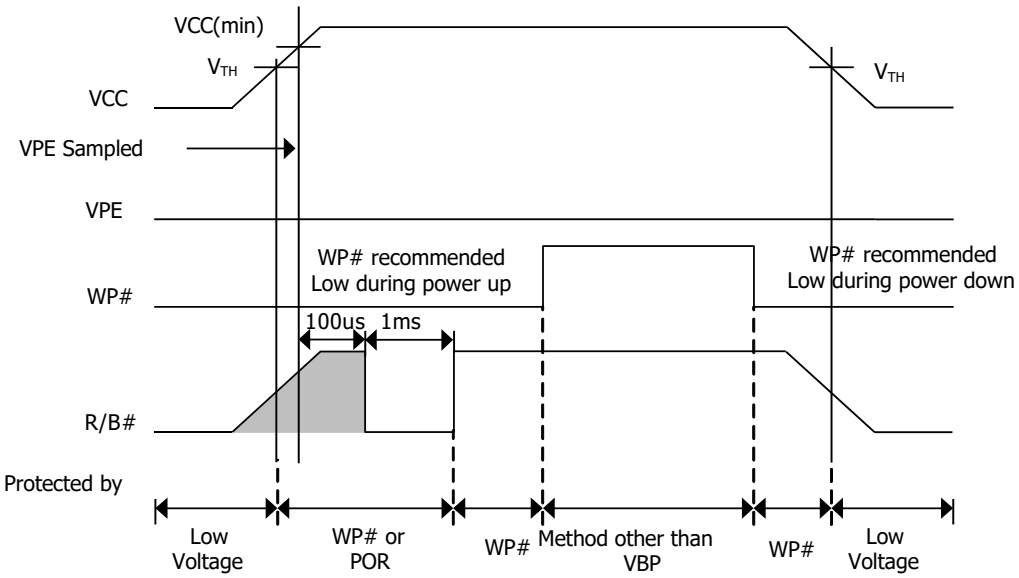
The VBP feature can protect all blocks, or one selected range of continuous blocks, excluding user One Time Programmable (OTP) area from erase and program operations. The VBP parameter settings are reset to default value after a power-cycle (all blocks protected if VPE input is high) and must be re-programmed by the host. The VPE input level, latched during Power-On Reset (POR), determines whether the VBP is enabled or disabled. If the VPE input is low at power-on, the VBP feature is disabled and the Write Protect (WP#) input controls the protection of all blocks. If the VPE input is high at power-on, all blocks are protected from programming or erasing even if the WP# input is high. Vcc and VPE rising time is same. See below ***Figures 42*** and ***Figure43***.

Figure 42 : VPE "HIGH" at Power up Timing



Note:
1. VBP enabled - default is all blocks protected until block unlock commands define unlocking VBP range.
2. Vth = 1.8V for Vcc 3.3V product.
3. The VPE pin must be sampled between Vth and Vcc (min).
4. VPE must have the same slope as Vcc.

Figure 43 : VPE "LOW" at Power up Timing

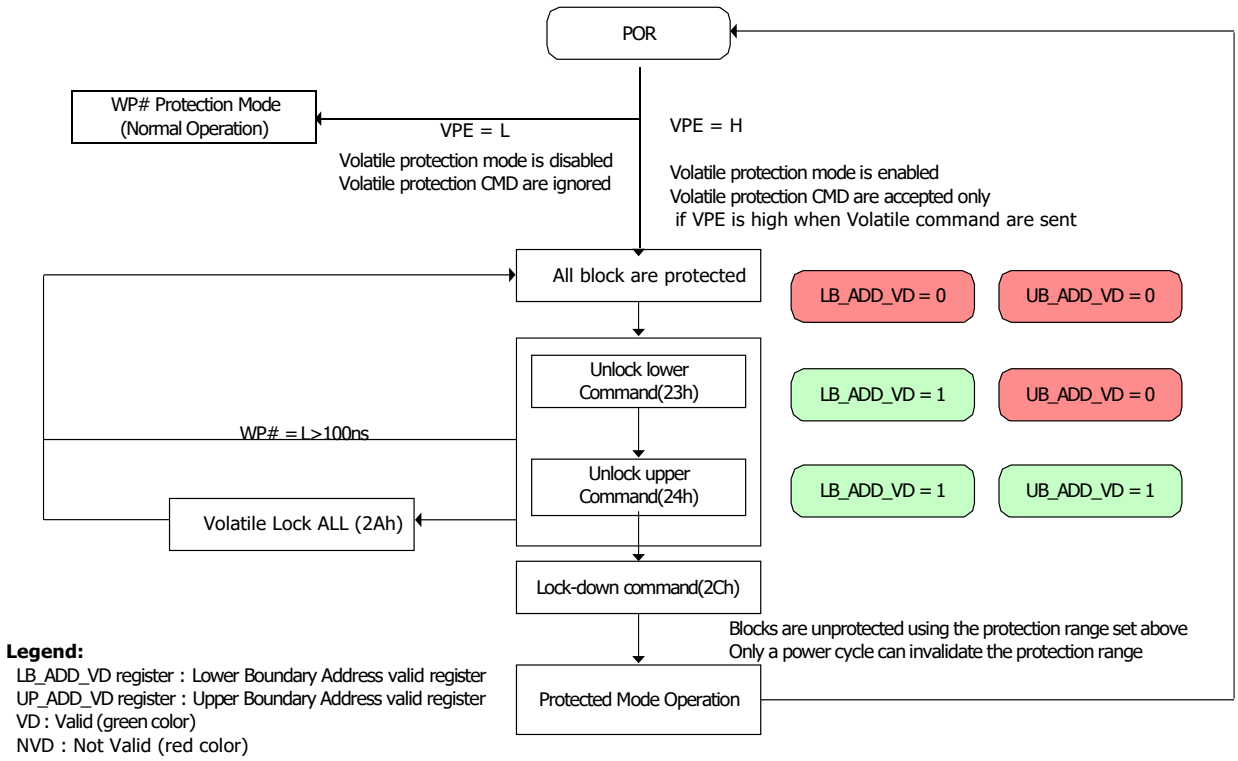


3.21.1. Volatile Unlock

The Unlock Block commands (23h & 24h) are used to un-protect a range of blocks. Volatile Unlock command is effective on the currently selected LUN(die). The Unlock Block commands set the protection registers (UB_ADD and LB_ADD).
Once the selected blocks are un-protected, those blocks can be protected again by using a Lock All Blocks (2Ah) commands or by asserting WP# low for more than 100ns.
Once the selected blocks are un-protected, the host can issue a Lock-down command (2Ch) to lock the VBP protection range configuration until the next power off to on cycle.
After, the Lock-down command is issued:
- VPE signal value and the VBP commands are ignored until the next power cycle.
- WP# can be used to protect all the blocks from program and erase, but will no longer invalidate the volatile protection parameter registers.

The Unlock Block commands define the range of blocks to be un-protected. The Unlock Lower command (23h) sets the lower block address, and must be followed by the Unlock Upper command (24h) that sets the upper block address. For example, once using 23h-24h to set LB_ADD_LD=1, UB_ADD_VD=1, then without issuing of Unlock Upper command (24h), block address boundary cannot be set using 23h-24h. Please refer to ***Figure 44*** below.

Figure 44 : VBP Flow Chart



The Unlock Block commands define the range of blocks to be un-protected. The Unlock Lower command (23h) sets the lower block address, and must be followed by the Unlock Upper command (24h) that sets the upper block address (see ***Figure 44***: ***Volatile Unlock Timing***).

To un-protect the complementary range of block, see ***Figure 45: Volatile Unlock Range option***, the host can set an invert-bit in the Unlock command address field (see ***Table 27***). If the invert-bit is set to 0, the unprotected area is within and inclusive of the upper and lower block addresses; if the bit is set to 1, the un-protected area is outside and exclusive of the upper and lower block addresses.

Figure 45 : Volatile Unlock Timing

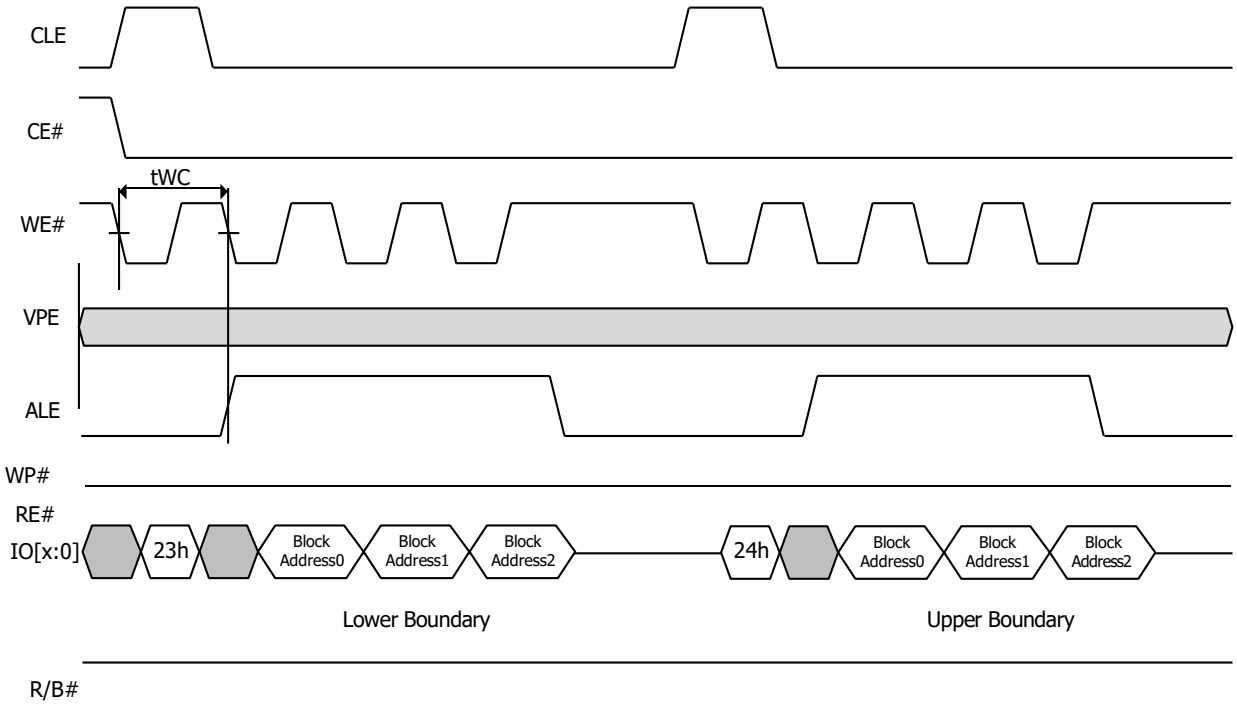
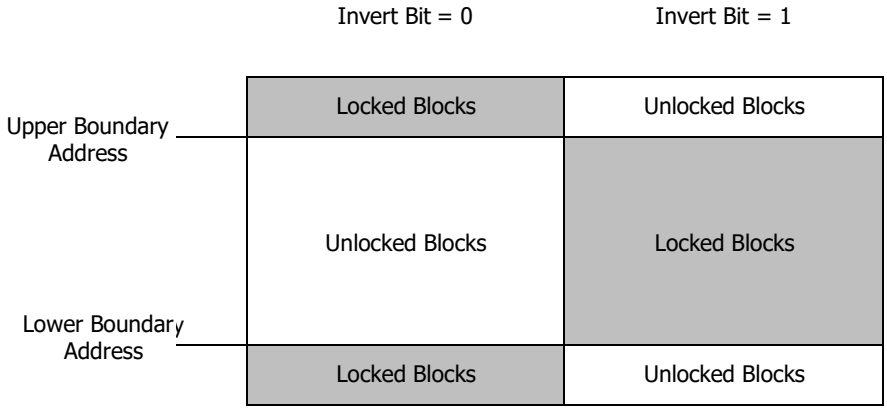


Table 27 : Volatile Unlock Address Definition (2KB Page)

	Bus Cycle	I/O[7]	I/O[6]	I/O[5]	I/O[4]	I/O[3]	I/O[2]	I/O[1]	I/O[0]
1st Block Address	1st	BA[1]	BA[0]	L(1)	L(1)	L(1)	L(1)	L(1)	Invert Bit(2)
2nd Block Address	2nd	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
3rd Block Address	3rd	L(1)	L(1)	L(1)	L(1)	BA[13]	BA[12]	BA[11]	BA[10]

Note:
1. L must set to Low.
2. The invert bit is set by 24h command to select whether the unprotected range is inside or outside of the range boundary. The bit is DON'T CARE for the 23h command.
3. BA[0] controls plane selection
4. For 4Gb device BA[13:12] must set to Low. For 8Gb device, BA[13] must set to Low.

Figure 46 : Volatile Unlock Range Option



3.21.1.1. Single and Multi-plane Volatile Block Protection

In multi-plane operation, the lower and upper address range BA[0] is internally respectively set to 0 and 1. For instance, if a block range being protected is defined to be between 1 and 4, the internal logic will actually protect block 0 to 5.

The following Figure 44 illustrates how internally the blocks are being protected for single and dual plan operation (shaded area) when the lower and upper address are respectively set to 0 and 5. It is restricted to the case using 2KB page size.

Figure 47 : Single and Multi-plane VBP example (2KB Page)

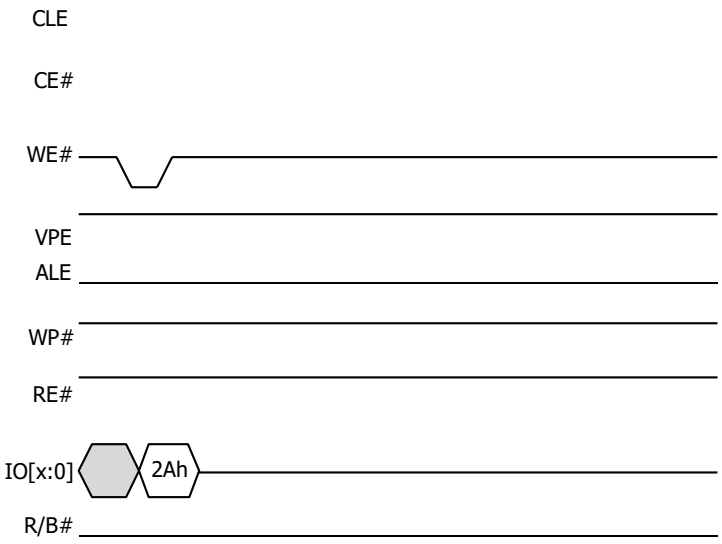
Single Plane	
Block 0	Block 1
Block 2	Block 3
Block 4	Block 5

Multi-plane	
Block 0	Block 1
Block 2	Block 3
Block 4	Block 5

3.21.2. Volatile Block Protect Lock All

The Lock All command (2Ah) can be used to protect all the blocks in the device. Volatile Block Protect Lock All command is effected on the currently selected LUN (die). This command is useful to program a new un-protected range as shown in the ***Figure 44 : VBP Flow Chart.***

Figure 48 : Volatile Block Protect - Lock All Timing

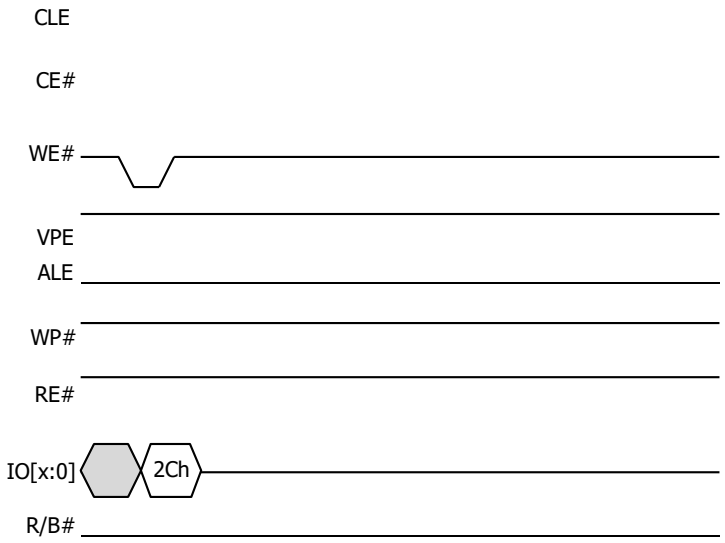


3.21.3. Volatile Block Protect Lock-down

The Lock-down Command (2Ch) maintains the block protection parameters at the time the command is issued; the protected blocks cannot be un-protected and the un-protected blocks cannot be protected by software. Volatile Block Protect Lock-down command is effective on the currently selected LUN (die). Once the Lock-down command is issued, only a power off to power on cycle will change the block protection status by returning to the default state (all blocks protected state if VPE input is high on power on). The WP# input and VPE input must be high before issuing the Lock-down command.

After, the Lock-down command is issued:
- VPE signal value and the VBP commands are ignored until the next power cycle or hardware reset.
- WP# can be used to protect all the blocks from program and erase, but will no longer invalidate the volatile protection parameter registers.

Figure 49 : Volatile Block Protect - Lock Down Timing



3.22. Permanent Block Protection (PBP)

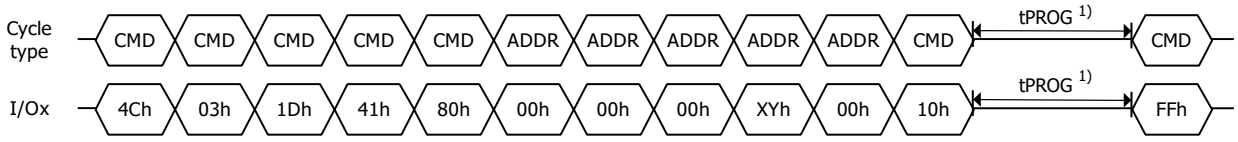
The device contains a CAM with 16 protection parameter setting entries. Each entry enables protection from program and erase of a group of 4 contiguous blocks (64 blocks total) in the main array. PBP command are only accepted if the device is not in OTP mode.
The device ships from the factory with no blocks protected by the PBP method.
Because this block protection is permanent, a power-on to power-off sequence does not affect the block protection status after the Permanent block protection command is issued.

The PBP method is used to select a group of blocks in the main array to be protected from program and erase operation. Multiple groups of blocks can be protected at the same time. Once a group of blocks is protected, the group of blocks can no longer be unprotected. During PBP program, operation commands other than Read Status (70h) and Read Status Enhanced (78h) are not supported.

Additional unprotected groups can still be protected using the PBP sequence unless the host issues a Permanent Block Protection Lock-down (PBPLD) command.
When this PBPLD command is issued, all groups of blocks protected by PBP are permanently protected from program and erase operations and a PBP operation can no longer be used to protect additional groups.
Each PBP and PBPLD sequence must be exited using the RESET command (FFh).

The PBP parameter settings are stored in CAMs. These settings will be maintained after a power cycle. The PBP method can protect up to 64 blocks (block 0 to 63) organized in groups of 4 contiguous blocks. Each group can be protected individually and are permanently protected. Once a group is protected, the group can no longer be unprotected. The PBP commands are only valid if the device is not in OTP mode. The adding of PBP is only allowed for 1st NAND device. (ex. If 1CE QDP, 2nd/3rd/4th LUN cannot add PBP)

Figure 50 : PBP Sequence Example



Note:
1) PBP blocks are required to have higher retention and protection scheme, which elongates tPROG. Please refer to Table 28. PBP/OTP-Program Characteristic for detail value.

Table 28 : PBP/OTP - Program Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	550	800	us

The group of blocks being protected is determined by the value of Y (see Table 29) on the fourth address cycle. PBP sequence can be only issued for maximum of 16 times, so if Y value or protected group is selected more than 2 times, than there will be a group that would not be able to be protected using PBP. Issuing of PBPLD sequence will both protect and lock down of the Protected Group.

Table 29 : Fourth Address Cycle (ADDR4) Protection Scheme

Y Value	Protected Group	Protected Block
0000	0	0,1,2,3
0001	1	4,5,6,7
0010	2	8,9,10,11
0011	3	12,13,14,15
0100	4	16,17,18,19
0101	5	20,21,22,23
0110	6	24,25,26,27
0111	7	28,29,30,31
1000	8	32,33,34,35
1001	9	36,37,38,39
1010	10	40,41,42,43
1011	11	44,45,46,47
1100	12	48,49,50,51
1101	13	52,53,54,55
1110	14	56,57,58,59
1111	15	60,61,62,63

Table 30 : Fourth Address Cycle (ADDR4) Protection Command Example

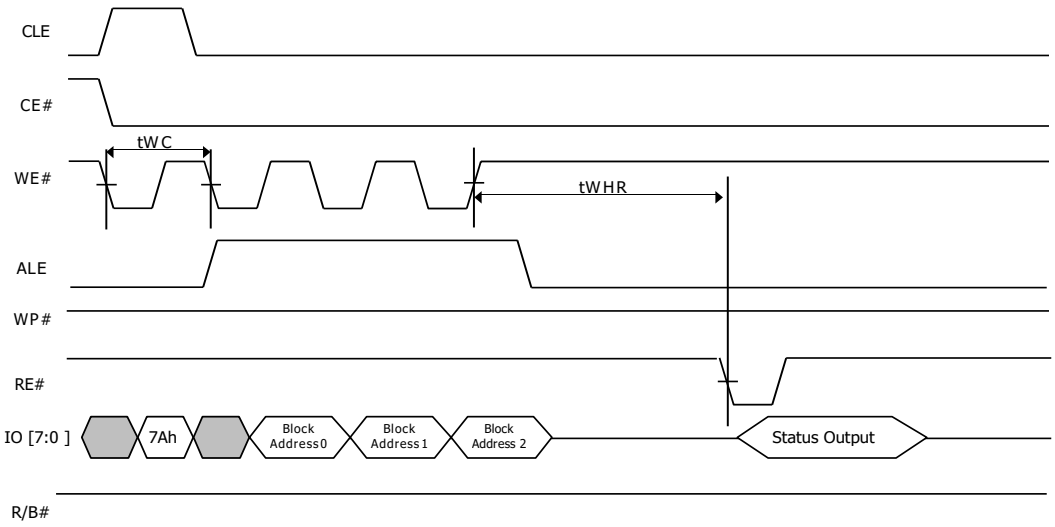
Description	Entry Sequence				CMD Cycle	Address Cycles	CMD Cycle	Read Stauts or monitor RB# output cycles	Reset (exit)
PBP Sequence	CMD1 (4Ch)	CMD2 (03h)	CMD3 (1Dh)	CMD4 (41h)	80h	00h,00h, 00h,0Yh, 00h	10h	70h or 78h (Program Operation forces RDBY Low)	FFh
PBPLD Sequence						00h,00h, 00h,1Yh, 00h			

Note:
1. When Y value or protected group address is valid, then PBPLD Sequence will protect and lockdown of the protected group at once.

3.22.1. Block Protection Status Read

Figure 51 shows the Block Protection Status Read waveform. The Block Protection Status Read command (7Ah) is followed by 3 address cycles and one data cycle.
This register indicates whether a given block (addressed in the Block protection read address command field: BA[13:0]) is locked-down, locked or unlocked using the VBP or PBP protection methods.

Figure 51 : Block Protection Status Read Operation



3.22.2. Block Lock Status Register

This register indicates whether a given block (addressed in the Block protection read address command field: BA[13:0]) is locked-down, locked or unlocked using the VBP or PBP protection methods.
Table 30 Block Lock Status register provides the BLS register definition.

Table 30 : Block Lock Status Register

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	Permanent Lockdown Status	Permanent Lockdown	0	0 : PBP NOT Lockdown 1: PBP Lockdown
3	PBP Lock/Unlock	Permanent Block Protection Lock Status	1	0: The address selected block is locked by PBP 1: The address selected block is not locked by PBP
2	VBP Block-unlock	Volatile Block Protection Block unlocked	1	001: Block is locked down by VBP 010: Block is locked by VBP 101: Block is unlocked, Device is locked-down by VBP 110 (default) : Block is unlocked, Device is not locked-down by VBP
1	VBP Not Locked-down	Volatile Block Protection Not Locked-down	1	
0	VBP Locked-down	Volatile Block Pro-tection Locked-down	0	

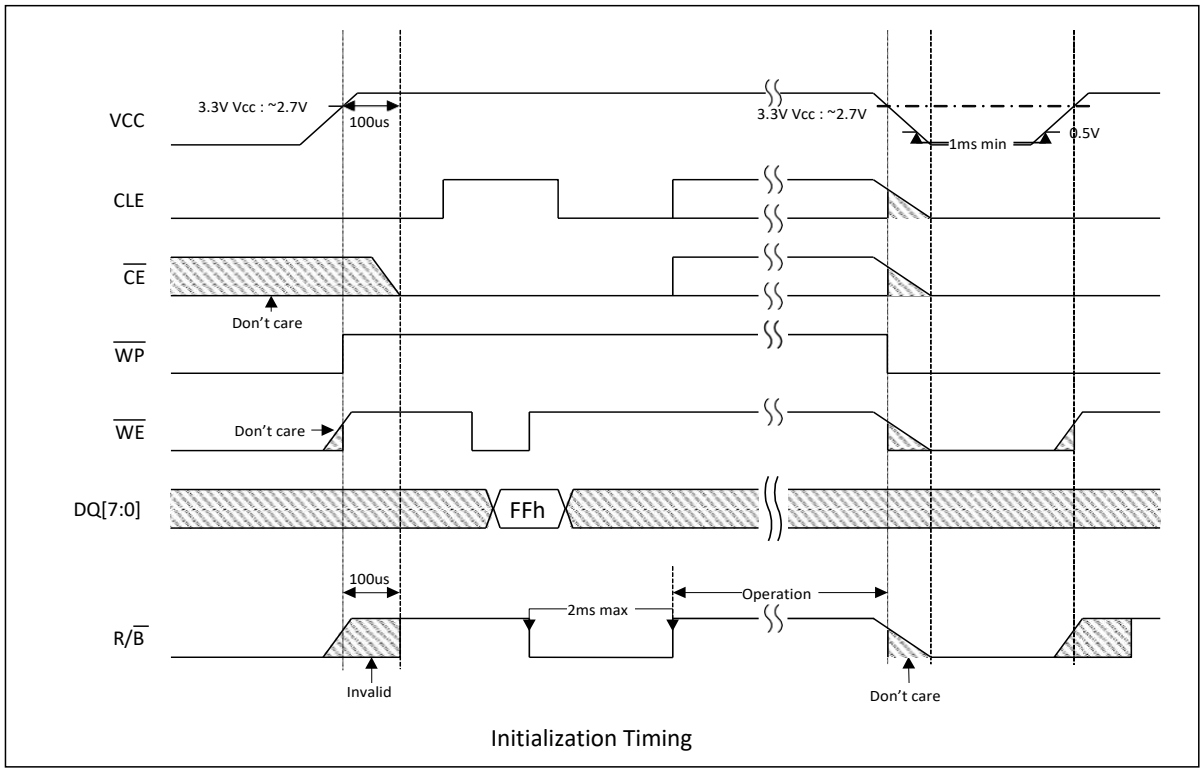
4. Other Features

4.1. Initialization (Power Up Sequence)

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 1.8 V (3.3 V Device).
WP# pin provides hardware protection and is recommended to be kept at V_{IL}
during power-up and power-down. A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences as shown in ***Figure 52***. The two-step command sequence for program/erase provides additional software protection.

Issuing of FFh command after Power Up Sequence allows Auto CAM read of the device.
The host must wait for R/B# to be valid High before issuing RESET command (FFh) to initialize any targets that share same CE#.The R/B# signal becomes valid after 100us since VCC reaches 2.7V. The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/B# becomes valid. Each target (CE) will be busy for a maximum of 2ms after the RESET command (FFh) is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command (when multi LUNs shared same CE Read Status Enhanced command should be used instead of READ STATUS). Each NAND die (LUN) may draw less than 10mA for over 1ms prior to the execution of the first RESET command (FFh) after the device is powered up. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50mA.

Figure 52 : Data Initialization

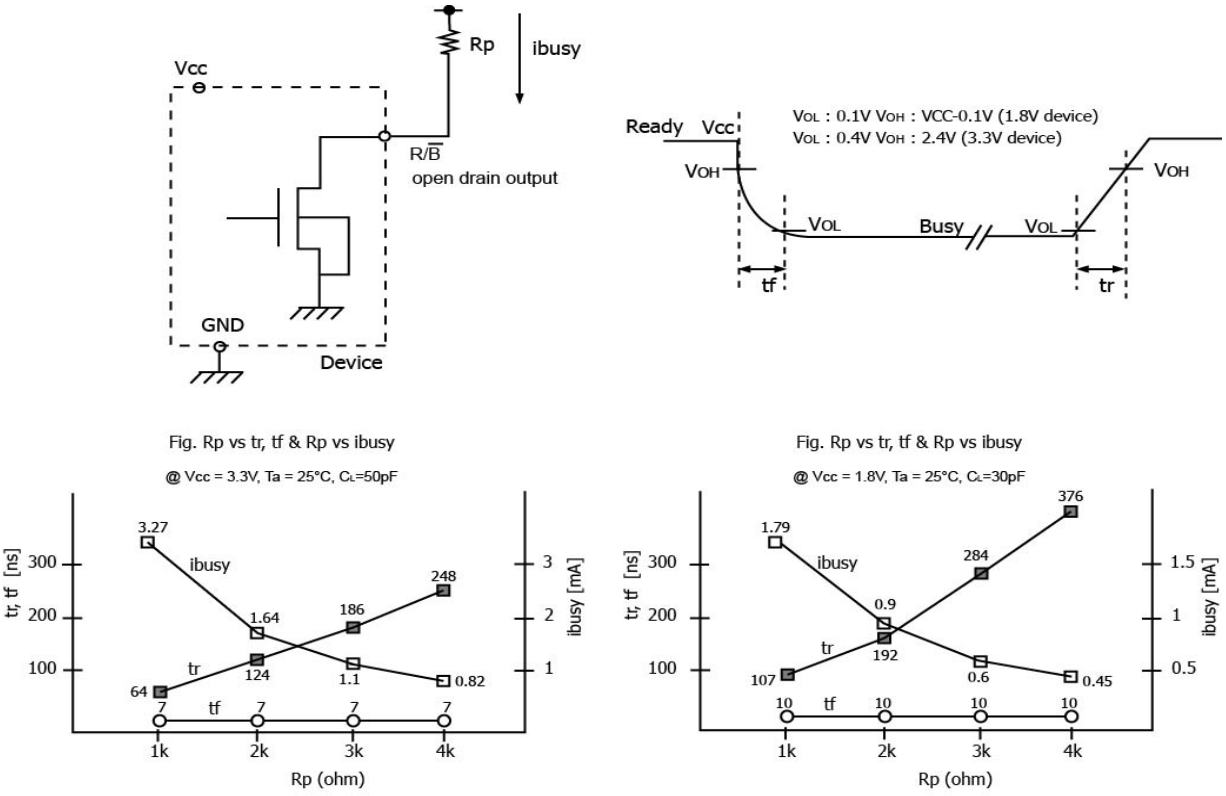


Note:
1. During the initialization, the device consumes a maximum current of ICC1.
2. Once Vcc drops under 2.5V, it is recommended to drive down Vcc to below 0.5V and stay low for at least 1ms before Vcc powered up. Floating Vcc/VccQ during power-down is prohibited.

4.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a RESET, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (I_{busy}), an appropriate value can be obtained with the following reference chart (***Figure 53***). Its value can be determined by the following guidance.

Figure 53 : Ready/Busy Pin Electrical Specifications



Rp value guidence

$$\text{Rp (min 3.3V device)} = \frac{\text{Vcc (Max.) - VOL (Max.)}}{\text{IOL + }\sum\text{IL}} = \frac{3.2\text{V}}{8\text{mA + }\sum\text{IL}}$$

$$\text{Rp (min 1.8V device)} = \frac{\text{Vcc (Max.) - VOL (Max.)}}{\text{IOL + }\sum\text{IL}} = \frac{1.85\text{V}}{3\text{mA + }\sum\text{IL}}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

4.3. Write Protect

Hardware write protection is activated, when the Write Protect pin is low. However, during program/erase operation, Write Protect pin shall stay high not to alter the content of the memory. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

4.3.1. Write Protect (WP#) handling

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100nsec. Switching WP# low during this time is equivalent to issuing a Reset command (FFh)

The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for t_{RST} (similar to ***Figure 17***). At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value. Refer to Table 17 for more information on device
status. Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the setup commands (80h or 60h).

The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command, as explained in ***Figure 54~57***. The Erase and Program Operations are automatically reset when WP# goes Low (t_{WW} = 100ns, min). The operations are enabled and disabled as follows.

Figure 54 : Enable Program

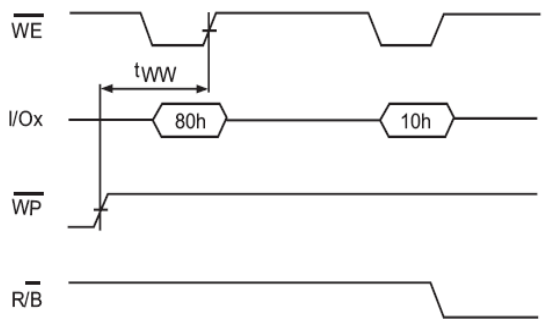


Figure 55 : Disable Program

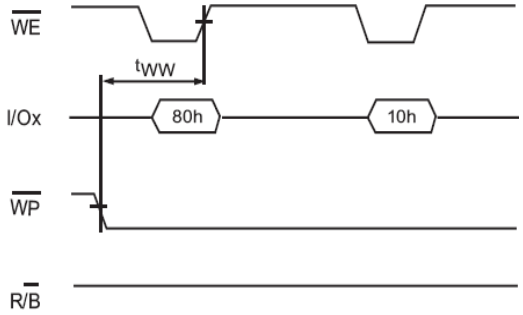


Figure 56 : Enable Erase

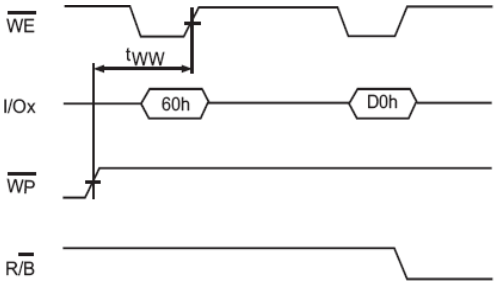
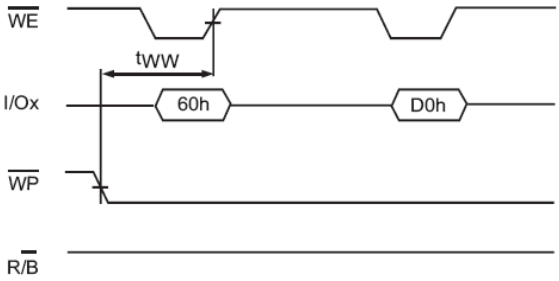


Figure 57 : Disable Erase



4.4. Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

4.5. Firmware SLC

For MKPVXG08CX-KS product, there is a unique given mode for storing Firmware codes for a controller management, called Firmware SLC mode. For Firmware SLC mode, DAh command is newly implemented to provide an user access to specific register area that is designated. To exit from Firmware SLC mode RESET FFh command can be used. If data is programmed with Page Program for Firmware SLC mode, then page read for Firmware SLC mode must be used to read out the data.

Figure 58 : Firmware SLC Mode

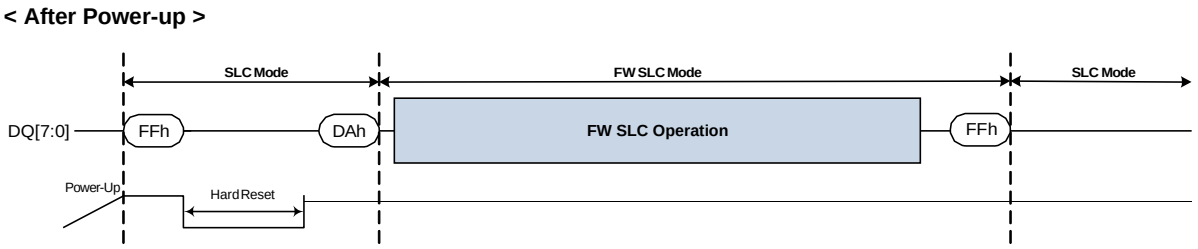


Figure 59 : Page Program for Firmware SLC Mode

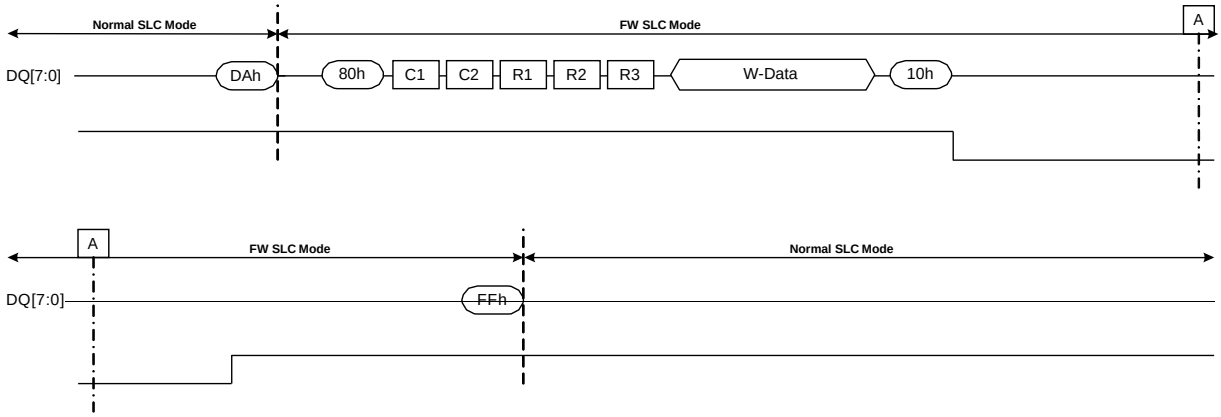
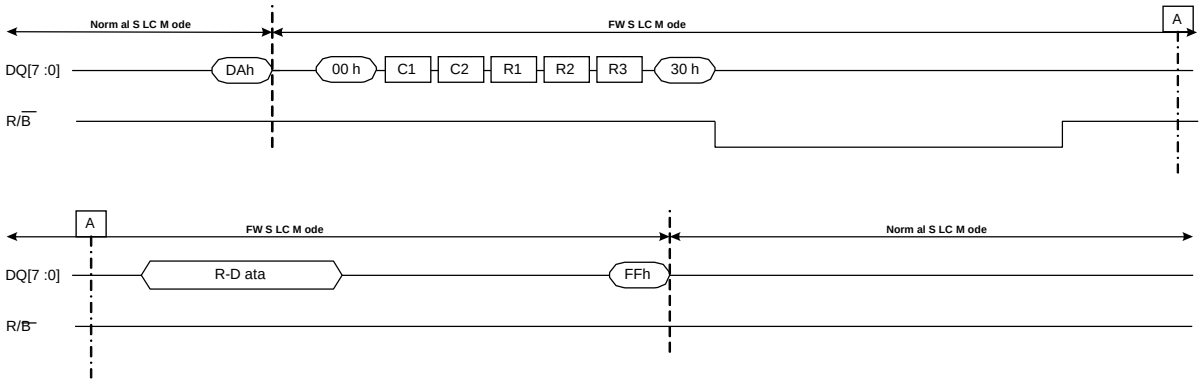


Figure 60 : Page Read for Firmware SLC Mode



For Firmware SLC mode- Program / Erase Characteristics, please refer to *Table 31 below.*

Table 31 : Firmware SLC mode - Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	550	800	us
Number of partial Program Cycles in the same page	NOP	-	-	1	cycles
Single Plane Read (4KB Page)	t_R	-	55	450	us
Single Plane Read (2KB Page)		-	45	300	us
Multi-Plane Read (2KB Page)		-	60	550	us
Block Erase Time	t_{BERS}	-	-	10	ms

4.6. Open Block Guideline

When not all the wordlines within the block is programmed, it is called Open block; if all wordlines in the blocks are fully programmed, it is called Closed block. Because remaining wordlines or region of the block is in erased status as a default, voltage difference between last programmed block and the remaining region of the block results read disturbance that causes Vt shift of programmed or erased bits in Open block case.
For MKPVXG08CX-KS product, Open block case shall not be allowed. During program, program all wordlines using dummy to make Close block to ensure NAND reliability. Otherwise, if in case of Open block, it is must to program at least one page of dummy data at the end of last programmed worldline.

Figure 61 : Closed Block Example

Wordline0	Program
Wordline01	Program
...	Program
Wordline57	Program
Wordline58	Program
Wordline59	Program
Wordline60	Program
Wordline61	Program
Wordline62	Program
Wordline63	Program

Figure 62 : Open Block Example

Wordline0	Program
Wordline01	Program
...	Program
Wordline57	Program
Wordline58	Program
Wordline59	Program
Wordline60	**Dum m y Program**
Wordline61	Erase
Wordline62	Erase
Wordline63	Erase

4.7. Small Data Input Guideline

Within NOP1, if input data size is bigger than 2 Bytes, small data input is possible by following two conditions. 1) Data size shall be 2 bytes within single NOP, and 2) 2 byte data input column address shall start from xxxx0h, xxx4h, xxx8h, and xxxCh. For 4K-single Plane, the size of data input should be more than 4 byte if random data input command is used.

5. Device Parameters

5.1. Absolute Maximum Rating

Table 32 : Absolute maximum ratings

Symbol	Parameter	Value	Unit
		Min	
T_A (Ambient Operating Temperature)	Commercial	0 to 70	℃
	Extended	-25 to 85	℃
	Industrial	-40 to 85	℃
	Automotive (AAT)	-40 to 105	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Note:
1. Please contact to MK office and confirm the availability of the product.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.
3. Except for the rating "Operating Temperature Range", stresses above those listed in the ***Table 31 "Absolute Maximum Ratings"*** may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

5.2. DC and Operating Characteristics

Table 33 : DC and Operating Characteristics

Parameter		Symbol	Test Conditions	2.7V ~ 3.6V			Units
				Min	Typ	Max	
Operating Current	Read	I_{CC1}	t_{RC}= t_{RC}(min), CE#=V_{IL}, I_{OUT}=0 mA	-	25	35	mA
	Program	I_{CC2}	Normal	-	25	35	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (CMOS)		I_{SB}	CE#=V_{CC}-0.2 , WP#=0V/V_{CC}	-	-	100	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to $V_{CC(MAX)}$	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to $V_{CC(MAX)}$	-	-	±10	uA
Input High Voltage		V_{IH}	-	V_{CC}x0.8	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xV_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-400 uA	2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}= 2.1 mA	-	-	0.4	V
Output Low Current (R/B#)		I_{OL} (R/B#)	V_{OL}= 0.4V	8	10	-	mA

5.3. AC Test Conditions

Table 34 : AC Test Conditions

Parameter	Value
	2.7V ≤ Vcc ≤ 3.6V
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (2.7V-3.6V)	1 TTL GATE and CL=50_{pF}

Note:
These parameters are verified device characterization and are not 100% tested

5.4. Pin Capacitance (T_A=25℃, F=1.0MHz)

Table 35 : Pin Capacitance Parameters

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	-	10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V	-	10	pF

5.5. Program/ Read / Erase Characteristics

Table 36 : Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	350	600	us
Number of partial Program Cycles in the same page	NOP	-	-	4	cycles
Dummy Busy Time for Multi-Plane setting	t_{DBSY}	-	TBD	1	us
Single Plane Read (4KB Page)	t_R	-	55	350	us
Single Plane Read (2KB Page)		-	45	250	us
Multi-Plane Read (2KB Page)		-	55	450	us
Block Erase Time	t_{BERS}	-	4	10	ms

Note:
1) Typical value is measured at Vcc=3.3V, T_A=25℃(3.3V Device). Not 100% tested.
2) All functions guaranteed on NOP4 cases, but reliability and data retention specification is guaranteed on NOP1 case.

5.6. AC Timing Characteristics

Table 37 : AC Timing Characteristics

Parameter	Symbol			Unit
		Min	Max	
CLE setup time	t_{CLS}	10	-	ns
CLE Hold time	t_{CLH}	5	-	ns
CE# setup time	t_{CS}	15	-	ns
CE# hold time	t_{CH}	5	-	ns
WE# pulse width	t_{WP}	10	-	ns
ALE setup time	t_{ALS}	10	-	ns
ALE hold time	t_{ALH}	5	-	ns
Data setup time	t_{DS}	7	-	ns
Data hold time	t_{DH}	5	-	ns
Write cycle time	t_{WC}	20	-	ns
WE# high hold time	t_{WH}	7	-	ns
Address to data loading time	t_{ADL}	70	-	ns
ALE to RE# delay	t_{AR}	10	-	ns
CLE to RE# delay	t_{CLR}	10	-	ns
Ready to RE# low	t_{RR}	20	-	ns
RE# pulse width	t_{RP}	10	-	ns
WE# high to busy	t_{WB}	-	100	ns
Read cycle time	t_{RC}	20	-	ns
RE# access time	t_{REA}	-	16	ns
RE# high to output high Z	t_{RHZ}	-	100	ns
CE# high to output high Z	t_{CHZ}		30	ns
CE# high to ALE or CLE Don't care	t_{CSD}	10	-	ns
RE# high to output hold	t_{RHOH}	15	-	ns
RE# low to output hold	t_{RLOH}	5	-	ns
RE# or CE# high to output hold	t_{COH}	15	-	ns
RE# high hold time	t_{REH}	7	-	ns
Output Hi-Z to RE# Low	t_{IR}	0	-	ns
RE# high to WE# low	t_{RHW}	100	-	ns
WE# high to RE# low	t_{WHR}	60	-	ns
WE# high to RE# low for Random data out	t_{WHR2}	200	-	ns
CE# low to RE# low	t_{CR}	10	-	ns
Device resetting time (Read/Program/Erase)	t_{RST}	-	5/10/500	us
Write protect time	t_{WW}	100	-	ns

Note:
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.