SGM72112B
DP12T Diversity Switch for Carrier Aggregation

GENERAL DESCRIPTION

The SGM72112B is a dual single-pole/six-throw (2xSP6T) antenna switch, which supports from 0.1GHz to 3.8GHz. The device features low insertion loss and high isolation, which make it suitable for high linearity receiving applications. It also has the advantage of High linearity performance. The SGM72112B is applied diversity receiving in carrier aggregation applications.

The SGM72112B has the ability to SP12T RF switch and MIPI controller on silicon-on-insulator (SOI) process, Internal driver and decoder for switch control signals, which makes it flexible in RF path band and routing selection.

No external DC blocking capacitors required on the RF paths as long as no external DC voltage is applied, which can save PCB area and cost.

The SGM72112B is available in a Green ULGA-2.4× 2-18L package.

APPLICATIONS

3G/4G Applications
Carrier Aggregation Diversity

FEATURES

- **Supply Voltage Range: 2.4V to 4.8V**
- **Advanced Silicon-On-Insulator (SOI) Process**
- **Frequency Range: 0.1GHz to 3.8GHz**
- **Low Insertion Loss: 0.6dB (TYP) at 3.8GHz**
- **MIPI RFFE Interface Compatible**
- **No External DC Blocking Capacitors Required**
- **Available in a Green ULGA-2.4×2-18L Package**

BLOCK DIAGRAM

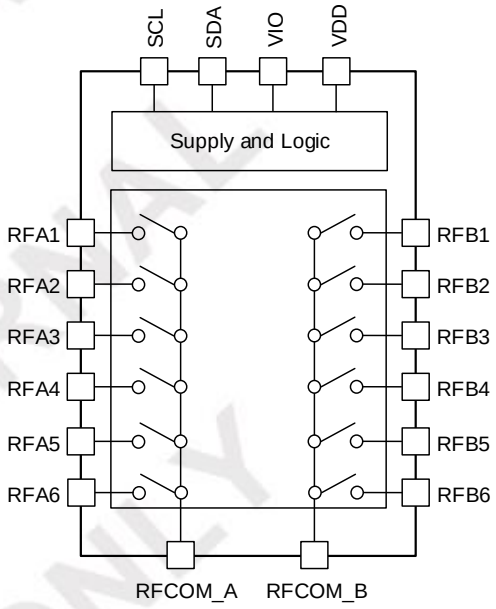


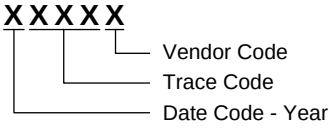
Figure 1. SGM72112B Block Diagram

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM72112B	ULGA-2.4×2-18L	-40℃ to +85℃	SGM72112BYULB18G/TR	SGMPC XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): PS Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your PSMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} 5V
Supply Voltage (MIPI), V_{IO} 2V
SDA, SCL Control Voltage 2V
RF Input Power, P_{IN} 26dBm
Junction Temperature ..... +150℃
Storage Temperature Range ..... -55℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility HBM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃
Operating Frequency Range ..... 0.1GHz to 3.8GHz
Supply Voltage, V_{DD} ..... 2.4V to 4.8V
Supply Voltage (MIPI), V_{IO} ..... 1.65V to 1.95V

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. PSMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

PS Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

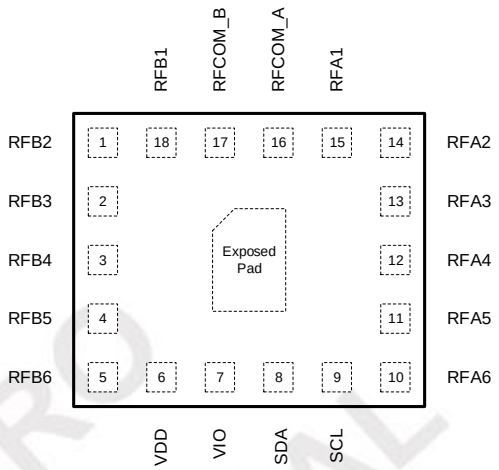


Figure 2. SGM72112B-18L

PIN DESCRIPTION

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	RFB2	RF Port B2.	10	RFA6	RF Port A6.
2	RFB3	RF Port B3.	11	RFA5	RF Port A5.
3	RFB4	RF Port B4.	12	RFA4	RF Port A4.
4	RFB5	RF Port B5.	13	RFA3	RF Port A3.
5	RFB6	RF Port B6.	14	RFA2	RF Port A2.
6	VDD	DC Power Supply	15	RFA1	RF Port A1.
7	VIO	Supply voltage for MIPI.	16	RFCOM_A	RF Common Port A.
8	SDA	RFFE Data Signal.	17	RFCOM_B	RF Common Port B.
9	SCL	RFFE Clock Signal.	18	RFB1	RF Port B1.
Exposed Pad	GND	Ground.			

Register_0 TRUTH TABLE (RFCOM_B)

Table 1. Register_0 Truth Table (RFCOM_B)

State	Mode	Register_0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	All Isolation	0	0	0	0	0	0	0	0
2	RFB1	0	0	0	0	0	0	0	1
3	RFB2	0	0	0	0	0	0	1	0
4	RFB3	0	0	0	0	0	0	1	1
5	RFB4	0	0	0	0	0	1	0	0
6	RFB5	0	0	0	0	0	1	0	1
7	RFB6	0	0	0	0	0	1	1	0
8	RFB6+5	0	0	0	0	0	1	1	1
9	RFB6+4	0	0	0	0	1	0	0	0

Register_0 TRUTH TABLE (RFCOM_B) (continued)

State	Mode	Register_0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
10	RFB6+3	0	0	0	0	1	0	0	1
11	RFB6+2	0	0	0	0	1	0	1	0
12	RFB6+1	0	0	0	0	1	0	1	1
13	RFB5+4	0	0	0	0	1	1	0	0
14	RFB5+3	0	0	0	0	1	1	0	1
15	RFB5+2	0	0	0	0	1	1	1	0
16	RFB5+1	0	0	0	0	1	1	1	1
17	RFB4+3	0	0	0	1	0	0	0	0
18	RFB4+2	0	0	0	1	0	0	0	1
19	RFB4+1	0	0	0	1	0	0	1	0
20	RFB3+2	0	0	0	1	0	0	1	1
21	RFB3+1	0	0	0	1	0	1	0	0
22	RFB2+1	0	0	0	1	0	1	0	1

Register_1 TRUTH TABLE (RFCOM_A)

Table 2. Register_1 TRUTH TABLE (RFCOM_A)

State	Mode	Register_0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	All Isolation	0	0	0	0	0	0	0	0
2	RFA1	0	0	0	0	0	0	0	1
3	RFA2	0	0	0	0	0	0	1	0
4	RFA3	0	0	0	0	0	0	1	1
5	RFA4	0	0	0	0	0	1	0	0
6	RFA5	0	0	0	0	0	1	0	1
7	RFA6	0	0	0	0	0	1	1	0
8	RFA6+5	0	0	0	0	0	1	1	1
9	RFA6+4	0	0	0	0	1	0	0	0
10	RFA6+3	0	0	0	0	1	0	0	1
11	RFA6+2	0	0	0	0	1	0	1	0
12	RFA6+1	0	0	0	0	1	0	1	1
13	RFA5+4	0	0	0	0	1	1	0	0
14	RFA5+3	0	0	0	0	1	1	0	1
15	RFA5+2	0	0	0	0	1	1	1	0
16	RFA5+1	0	0	0	0	1	1	1	1
17	RFA4+3	0	0	0	1	0	0	0	0
18	RFA4+2	0	0	0	1	0	0	0	1
19	RFA4+1	0	0	0	1	0	0	1	0
20	RFA3+2	0	0	0	1	0	0	1	1
21	RFA3+1	0	0	0	1	0	1	0	0
22	RFA2+1	0	0	0	1	0	1	0	1

ELECTRICAL CHARACTERISTICS

(Typical values, V_{DD} = 2.8V, T_A = +25℃, P_{IN} = 0dBm, 50Ω, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Specifications						
Supply Voltage	V_{DD}		2.4	2.8	4.8	V
Supply Current	I_{DD}			32	60	μA
V_{IO} Supply Voltage	V_{IO}		1.65	1.8	1.95	V
V_{IO} Supply Current	I_{IO}			4.8	10	μA
Control Voltage	V_{CTL_H}	High	0.8 × V_{IO}	V_{IO}	1.95	V
	V_{CTL_L}	Low	0		0.45	
Switching Time	t_{SW}	50% of control voltage to 90% of RF power		1	2	μs
Turn-On Time	t_{ON}	Time from V_{DD} = 0V to part on and RF at 90%		5	10	μs
RF Specifications						
Insertion Loss (RFCOM to All RF Ports)	IL	f_0 = 0.1GHz to 1.0GHz		0.40	0.6	dB
		f_0 = 1.0GHz to 2.0GHz		0.50	0.7	
		f_0 = 2.0GHz to 2.7GHz		0.60	0.8	
		f_0 = 2.7GHz to 3.8GHz		1.0	1.3	
Isolation (RFCOM_A to any OFF RFA port; RFCOM_B to any OFF RFB port)	ISO	f_0 = 0.1GHz to 1.0GHz	22	25		dB
		f_0 = 1.0GHz to 2.0GHz	17	20		
		f_0 = 2.0GHz to 2.7GHz	14	17		
		f_0 = 2.7GHz to 3.8GHz	12	15		
Isolation (RFCOM_A to RFCOM_B)	ISO	f_0 = 0.1GHz to 1.0GHz	27	30		dB
		f_0 = 1.0GHz to 2.0GHz	21	24		
		f_0 = 2.0GHz to 2.7GHz	19	22		
		f_0 = 2.7GHz to 3.8GHz	15	18		
0.1dB Compression Point (RFCOM to All RF Ports)	$P_{0.1dB}$	f_0 = 0.1GHz to 3.8GHz		25		dBm

MIPI READ AND WRITE TIMING

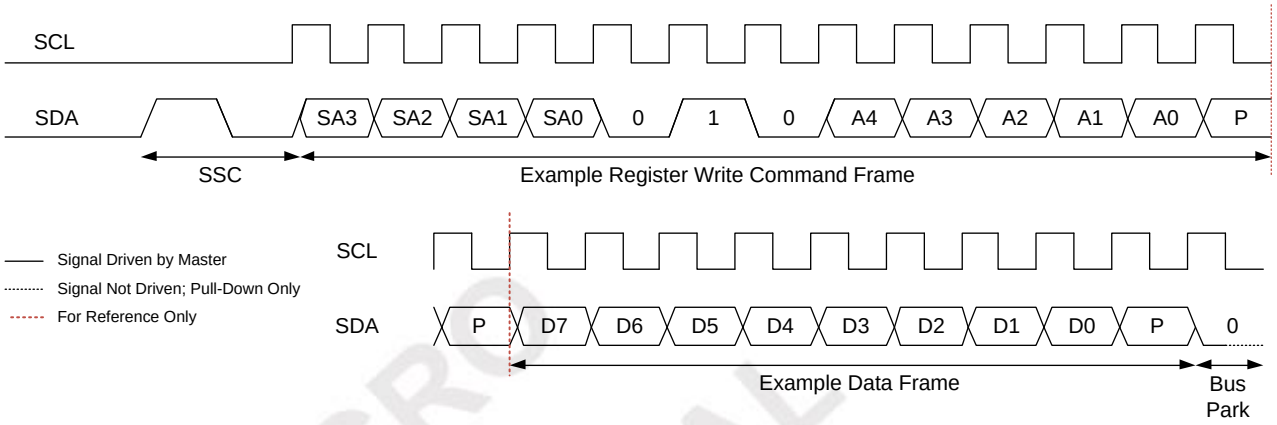


Figure 3. Register Write Command Timing Diagram

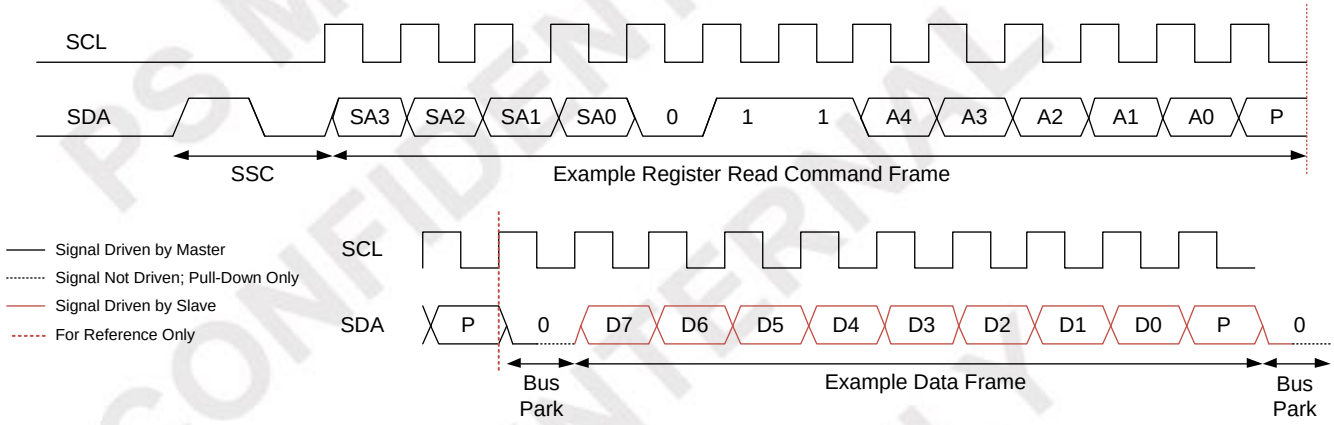


Figure 4. Register Read Command Timing Diagram

COMMAND SEQUENCE BIT DEFINITIONS

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data[3:0]	Y	Y	-	-	-	-	-	-
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	-	Data[7:0]	Y	Y	-	-	-
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	Y	Y	-	-	-

Legends:

SSC = Sequence start command

SA = Slave address

D = Register Address

A = Data bits

C = Command frame bits

BPC = Bus park cycle

REGISTER MAPS

Register_0

Register Address: 0x0000; R/W

Table 3. Register_0 Register Details

Bit(s)	Bit Name	Description	Default	R/W
D[7:0]	MODE_CTRL	See Table 1 section.	0000 0000	R/W

Register_1

Register Address: 0x0001; R/W

Table 4. Register_1 Register Details

Bit(s)	Bit Name	Description	Default	R/W
D[7:0]	MODE_CTRL	See Table 2 section.	0000 0000	R/W

PM_TRIG

Register Address: 0x001C; R/W and W

Table 7. PM_TRIG Register Details

Bit(s)	Bit Name	Description	Default	Type
D[7]	PWR_MODE_1	0: Normal 1: Low power	0	R/W
D[6]	PWR_MODE_0	0: Active - Normal 1: Startup - All registers are reset to the default	0	R/W
D[5]	TRIGGER_MASK_2	0: TRIGGER_2 enabled 1: TRIGGER_2 disabled If any one of the three TRIGGER_MASK_x is set to logic '1', the corresponding trigger is disabled, in that case data written to a register associated with the trigger goes directly to the destination register. Otherwise, if the TRIGGER_MASK_x is set to logic '0', incoming data is written to the shadow register, and the destination register is unchanged until its corresponding trigger is asserted.	0	R/W
D[4]	TRIGGER_MASK_1	0: TRIGGER_1 enabled 1: TRIGGER_1 disabled	0	R/W
D[3]	TRIGGER_MASK_0	0: TRIGGER_0 enabled 1: TRIGGER_0 disabled	0	R/W
D[2]	TRIGGER_2	0: Keep its associated destination registers unchanged. 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_2 is set to logic '0'.	0	W
D[1]	TRIGGER_1	0: Keep its associated destination registers unchanged. 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_1 is set to logic '0'.	0	W
D[0]	TRIGGER_0	0: Keep its associated destination registers unchanged. 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_0 is set to logic '0'.	0	W

REGISTER MAPS (continued)

PM_TRIG

Register Address: 0x001C; R/W and W

Table 7. PM_TRIG Register Details

Bit(s)	Bit Name	Description	Default	Type
D[7]	PWR_MODE_1	0: Normal 1: Low power	0	R/W
D[6]	PWR_MODE_0	0: Active - Normal 1: Startup - All registers are reset to the default	0	R/W
D[5]	TRIGGER_MASK_2	0: TRIGGER_2 enabled 1: TRIGGER_2 disabled If any one of the three TRIGGER_MASK_x is set to logic '1', the corresponding trigger is disabled, in that case data written to a register associated with the trigger goes directly to the destination register. Otherwise, if the TRIGGER_MASK_x is set to logic '0', incoming data is written to the shadow register, and the destination register is unchanged until its corresponding trigger is asserted.	0	R/W
D[4]	TRIGGER_MASK_1	0: TRIGGER_1 enabled 1: TRIGGER_1 disabled	0	R/W
D[3]	TRIGGER_MASK_0	0: TRIGGER_0 enabled 1: TRIGGER_0 disabled	0	R/W
D[2]	TRIGGER_2	0: Keep its associated destination registers unchanged. 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_2 is set to logic '0'.	0	W
D[1]	TRIGGER_1	0: Keep its associated destination registers unchanged. 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_1 is set to logic '0'.	0	W
D[0]	TRIGGER_0	0: Keep its associated destination registers unchanged. 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_0 is set to logic '0'.	0	W

PRODUCT_ID

Register Address: 0x001D; R

Table 8. PRODUCT_ID Register Details

Bit(s)	Bit Name	Description	Default	Type
D[7:0]	PRODUCT_ID	Product ID.	0000 0000	R

MANUFACTURER_ID

Register Address: 0x001E; R

Table 9. MANUFCTURER_ID Register Details

Bit(s)	Bit Name	Description	Default	Type
D[7:0]	MANUFACTURER_ID [7:0]	Lower eight bits of MIPI registered Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	0100 1010	R

MAN_USID

Register Address: 0x001F; R and R/W

Table 10. MAN_USID Register Details

Bit(s)	Bit Name	Description	Default	Type
D[7:6]	Reserved	Reserved	00	R
D[5:4]	MANUFACTURER_ID [9:8]	Upper two bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	00	R
D[3:0]	USID	USID of the device	1011	R/W

TYPICAL APPLICATION CIRCUIT

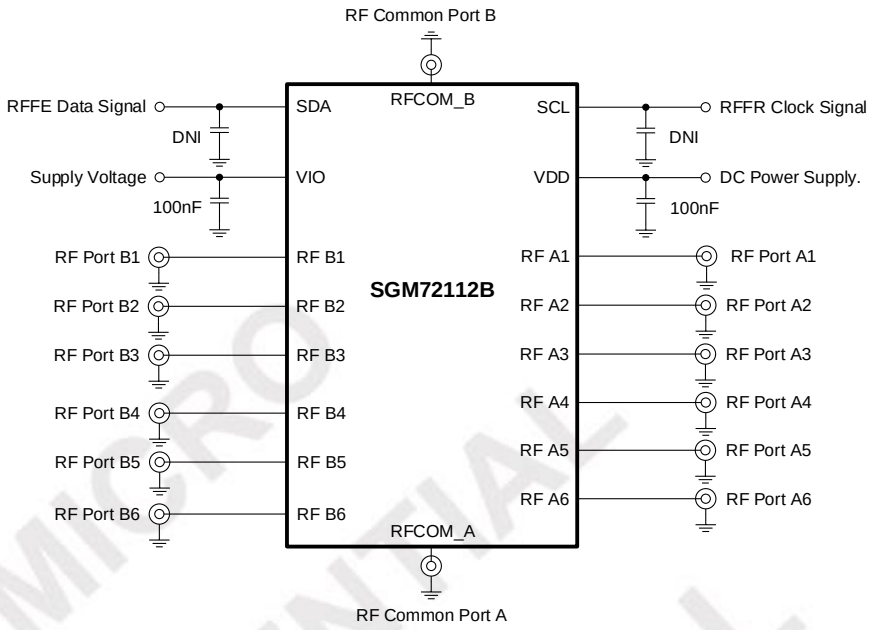


Figure 5. SGM72112B Typical Application Circuit

EVALUATION BOARD LAYOUT

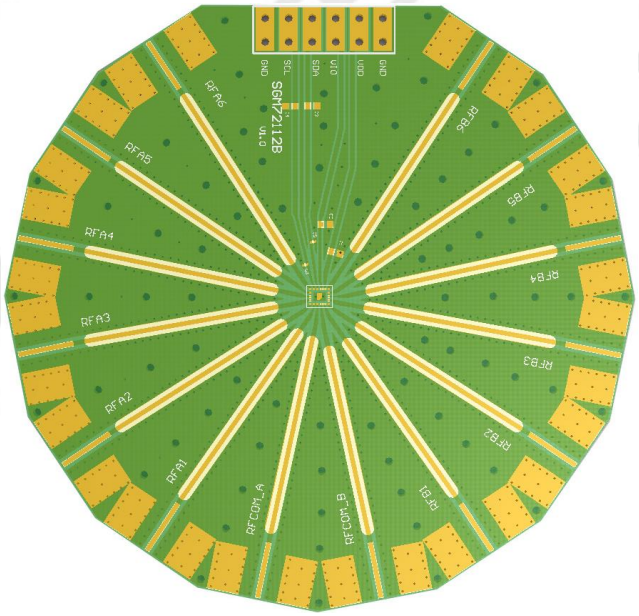
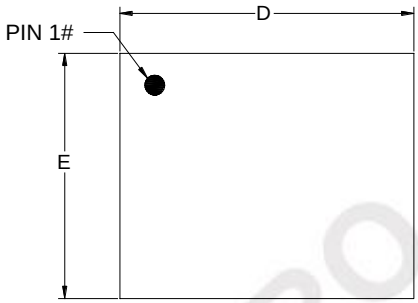


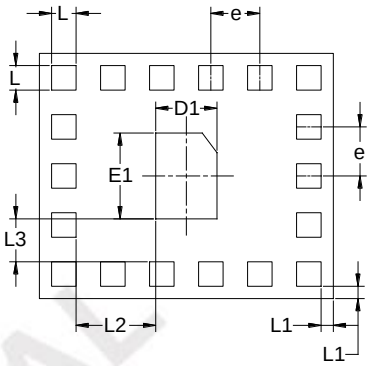
Figure 6. SGM72112B Evaluation Board Layout

PACKAGE OUTLINE DIMENSIONS

ULGA-2.4×2-18L

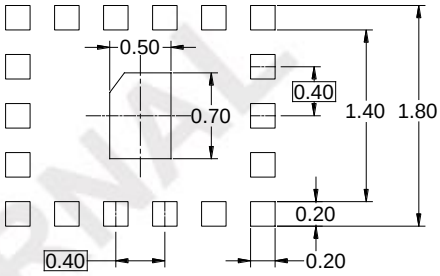


TOP VIEW



BOTTOM VIEW

SIDE VIEW



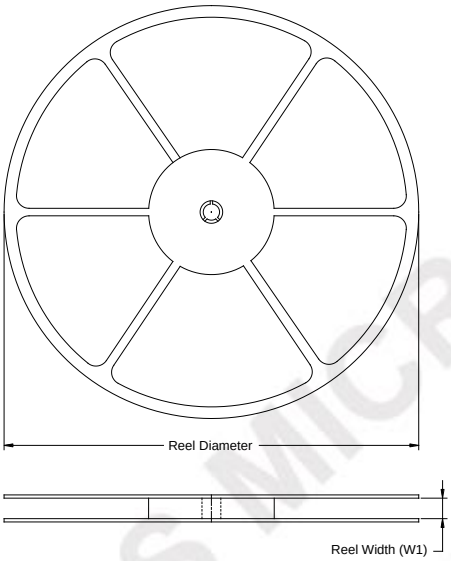
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.500	0.550	0.600
A1	0.140	0.170	0.200
A2		0.380 BSC	
D	2.300	2.400	2.500
E	1.900	2.000	2.100
D1		0.500	
E1		0.700	
e		0.400 BSC	
L		0.200	
L1		0.100	
L2		0.650	
L3		0.350	

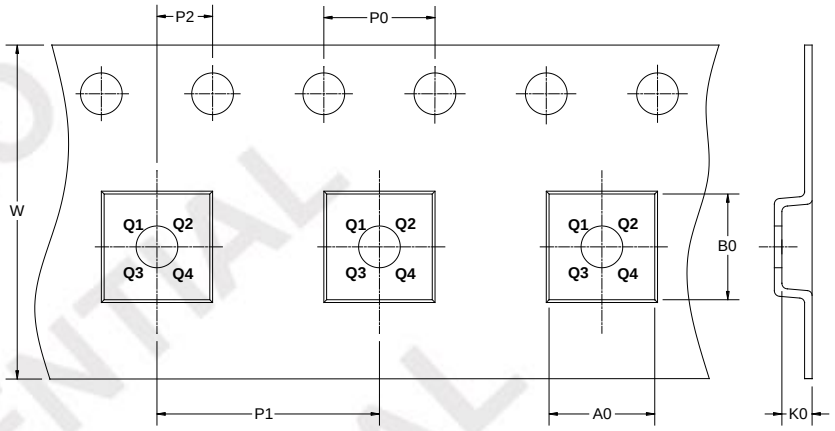
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

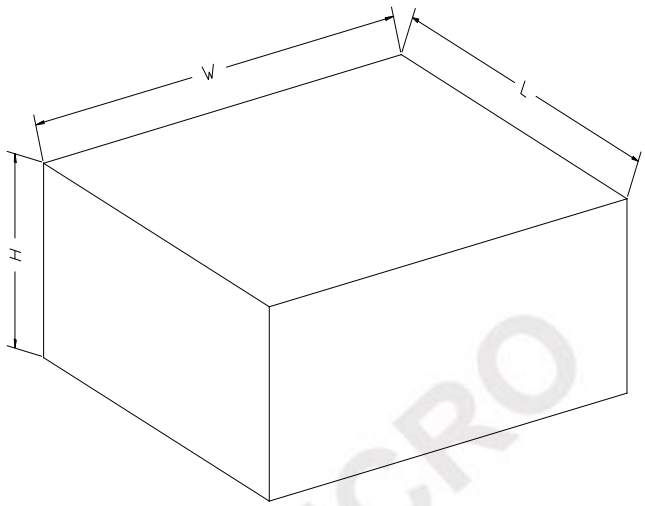
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
ULGA-2.4×2-18L	7″	9.5	2.25	2.65	0.75	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002

Weedspread

For the latest specifications or product information:

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