XBM3212 Series

Li-ion/Polymer 2-Cell Protector

GENERAL DESCRIPTION

XBM3212 Series is a protection IC for 2 serial-cell lithium-ion / lithium polymer recharge able batteries and includes high accuracy voltage detection circuits and delay circuits.

XBM3212 Series is suitable for protecting 2 serial-cell rechargeable lithium-ion / lithium polymer battery packs from overcharge, over-discharge, overcurrent and short-circuiting.

FEATURES

- Manufactured with High Voltage Tolerant Process Maximum Rating 30V
- Low supply current
- 2-Cell voltage7.2V Typ. 8μA(I_q)
- 2-Cell voltage4.0V Typ. 3.3μA(I_{sd})
- SOT23-6 Package
- Variety of detector threshold
- Over-charge detector threshold-V_{cu}:3.6V-4.5V step of 0.1V ±25mV
- Overcharge Release Voltage-V_{cL}=V_{cu}-0.2V ±50mV
- Over-discharge detector threshold V_{DL}:2.1V-3.0V step of 0.1V ±80mV
- Over-discharge Release Voltage-V_{DR} ±100mV
- Discharge-current threshold1 0.1V
- Short detector threshold 1.0V (Fixed)
- Charge-current threshold -0.1V
- Over-discharge self-recovery function
- Broken line protection function
- Over-charge detector Output Delay 1s
- Over-discharge detector Output Delay 100ms
- Discharge-current detector Output Delay 8ms
- Charge-current detector Output Delay 8ms
- Short Circuit detector Output Delay 130μs
- 0V Battery Charging Function
- ESD HBM: 4KV
- RoHS Compliant and Lead Pb Free

APPLICATIONS

- Power Tools
- E-Bike
- Power Bank
- Power Amplifier
- 2 Cell Lithium-ion or Lithium polymer rechargeable battery pack
- Lithium iron phosphate battery

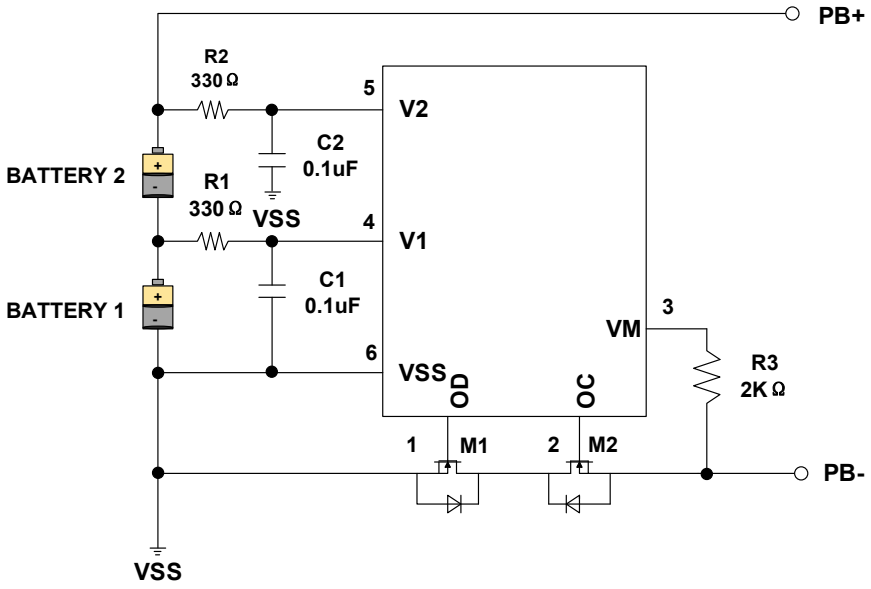


Figure 1. Typical Application Circuit

ORDERING INFORMATION

PART NUMBER	OCV [VCU] (V)	OCRV [VCL] (V)	ODV [VDL] (V)	ODRV [VDR] (V)	TOP MARK
XBM3212RKK	3.65±25mV	3.45±50mV	2.10±80mV	2.50±100mV	YWTxxx
XBM3212DBA	4.28±25mV	4.08±50mV	2.9±80mV	3.0±100mV	YWTxxx
XBM3212DGB	4.28±25mV	4.08±50mV	2.4±80mV	2.95±100mV	YWTxxx
XBM3212DCA	4.28±25mV	4.08±50mV	2.8±80mV	3.0±100mV	YWTxxx
XBM3212BCA	4.25±25mV	4.05±50mV	2.8±80mV	3.0±100mV	YWTxxx
XBM3212JFG	4.425±25mV	4.225±50mV	2.5±80mV	2.7±100mV	YWTxxx

Note: “YWTxxx” is manufacture date code, “Y” means the year, “W” means the week, “T” means the times of odering, “xxx” is internal product code of XySemi.

PIN CONFIGURATION

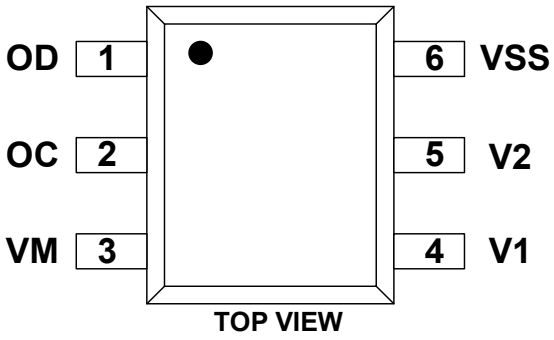


Figure 2. PIN Configuration

PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	OD	Connection pin of discharge control FET gate (CMOS output)
2	OC	Connection pin of charge control FET gate (CMOS output)
3	VM	Voltage detection pin between VM pin and VSS pin （Overcurrent / charger detection pin)
4	V1	Positive terminal Pin for Cell-1
5	V2	Positive terminal Pin for Cell-2
6	VSS	VSS pin. Ground pin for the IC

ABSOLUTE MAXIMUM RATINGS

(NOTE: DO NOT EXCEED THESE LIMITS TO PREVENT DAMAGE TO THE DEVICE. EXPOSURE TO ABSOLUTE MAXIMUM RATING CONDITIONS FOR LONG PERIODS MAY AFFECT DEVICE RELIABIL-

PARAMETER	VALUE	UNIT
V2; VM	-0.3~30	V
OC	VSS-0.3~VSS+30	V
OD	VSS+0.3~V2+0.3	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C
Power Dissipation at T=25°C	0.25	W
Package Thermal Resistance (Junction to Ambient) θJA	350	°C/W
Package Thermal Resistance (Junction to Case) θJC	50	°C/W
ESD(HBM)	4000	V

ELECTRICAL CHARACTERISTICS

Typical and limits appearing in normal type apply for TA = 25˚C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Detection Voltage						
Charger Detection Voltage	V_{CHA}		-0.08	-0.10	-0.12	V
Discharger Detection Voltage	V_{DIS}		0.08	0.10	0.12	V
Current Consumption						
Current Consumption in Normal Operation	I_{OPE}	VDD=7.2V VM =0V		8	10	μA
Current Consumption in Power Down	I_{PD}	VDD=4.0V VM pin floating		3.3	5	μA
Detection Delay Time						
Overcharge Voltage Detection DelayTime	t_{CU}		800	1000	1200	mS
Overdischarge Voltage Detection Delay Time	t_{DL}		80	100	120	mS
Overdischarge Current Detection Delay Time	t_{IOV}		6	8	10	mS
Overcharge Current Detection Delay Time	t_{ICV}		6	8	10	mS
Load Short-Circuiting Detection Delay Time	*t_{SHORT}		100	130	160	μS

Note1: *---The parameter is guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM

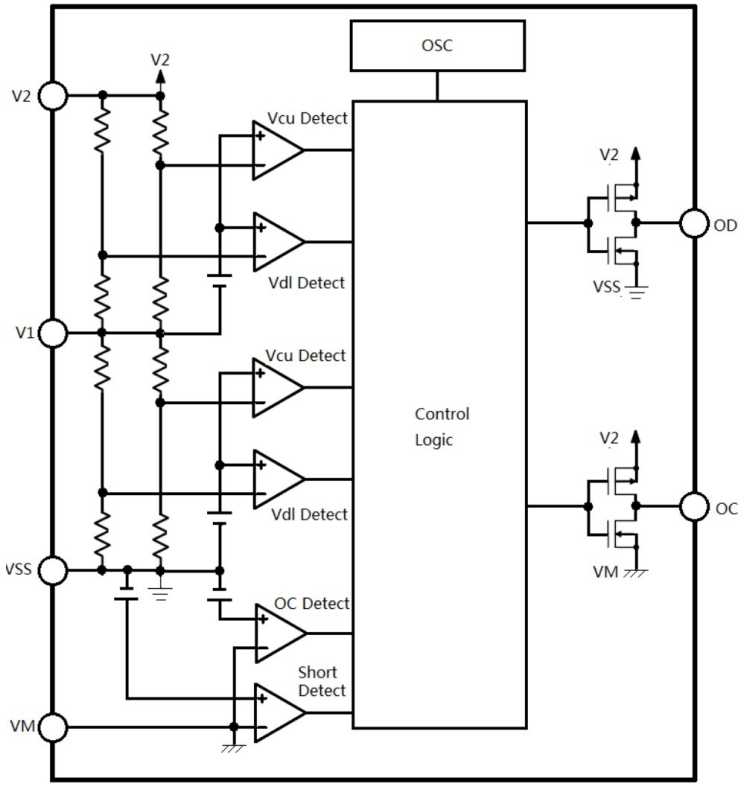


Figure 3. Functional Block Diagram

OPERATION

Over-charge detectors

While the cell is charged, the voltage between V1 pin and VSS pin (voltage of the Cell-1), the voltage between V2 pin and V1 pin (voltage of the Cell-2) are supervised. If at least one of the cells' voltage becomes equal or more than the over-charge detector threshold, the over-charge is detected, and an external charge control N-MOSFET turns off with OC pin being at "L" level via an external pull-down resister and charge stops.

To reset the over-charge and make the OC pin level to "H" again after detecting over-charge, in such conditions that a time when all the cells' voltages are down to a level lower than over-charge released voltage. The output voltage of OC pin becomes "H", and it makes an external N-MOSFET turns on, and charge cycle is available. The over charge detectors have hysteresis. Internal fixed output delay times for overcharge detection and release from overcharge exist. Even if one of voltage of Cells keeps its level more than the over-charge detector threshold, and output delay time passes, overcharge voltage is detected. Even when the voltage of each cell becomes equal or higher level than V_{CU} if these voltages would be back to a level lower than the overcharge detector threshold within a time period of the output delay time, the overcharge is not detected. Besides, after detecting over-charge, each cell voltage is lower than the overcharge detector released voltage, even if just one of cells' voltage becomes equal or more than the over-charge released voltage within the released output delay time, overcharge is not released.

Over-discharge detectors

While the cells are discharged, the volt-age between V1 pin and VSS pin (the voltage of Cell-1), the voltage between V2 pin and V1 pin (Cell-2 voltage) are supervised. If at least one of the cells' voltage becomes equal or less than the over-discharge detector threshold, the over-discharge is detected and discharge stops by the external discharge control N-MOSFET turning off with the OD pin being at "L". The condition to release over-discharge voltage detector is that after detecting over-discharge voltage, all the cells' voltage becomes higher than the over-discharge released voltage, OD pin becomes "H" level, and by turning on the external N-MOSFET, discharge becomes possible. The over-discharge detectors have hysteres-is.

Internal fixed output delay times for overcharge detection and release from over-charge exist. If at least one of the voltage of Cells is down to equal or lower than the over-discharge detector threshold, if the voltage of each Cell would be back to a level higher than the over-discharge detector threshold within a time period of the output delay time, the over-discharge is not detected. Output delay time for release from over-discharge is also set internally. After detecting over-discharge, supply current would be reduced and be into standby by halting unnecessary circuits and consumption current of the IC itself is made as small as possible.

Discharge-current Detector, & Short Circuit Protector

When the discharge is acceptable, VM voltage is supervised, if the load is short and VM voltage becomes equal or more than excess discharge current threshold, and equal or less than short detector threshold, the status becomes excess discharge current detected condition. If VM voltage becomes equal or more than short circuit detector threshold, the status becomes short circuit detected, then OD pin outputs "L" and by turning off the external MOSFET, large current flow is prevented. The excess discharge current detector and short detector has the fixed output delay time.

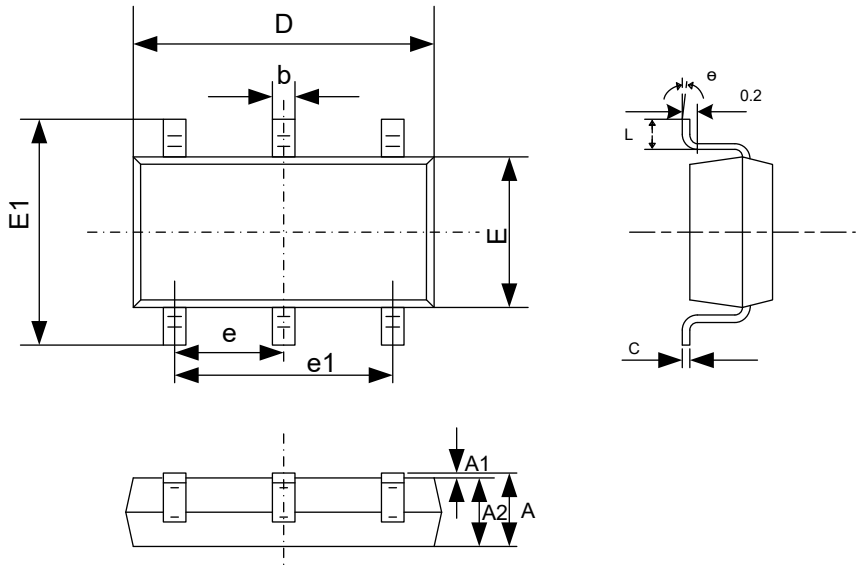
Charge-current detector

When the charge is acceptable, VM voltage is supervised, if the VM voltage becomes equal or more than excess charge current threshold the status becomes excess charge current detected condition. then OC pin outputs "L" and by turning off the external MOSFET, large current flow is prevented. Output delay of excess charge current is internally fixed.

Over-discharge self-recovery function

In normal working conditions, when the battery voltage drops below the discharge detection voltage, and the duration of this state exceeds the excess discharge detection delay time, the chip will turn off the MOSFET (OD terminal) for discharge control and stop discharging.

PACKAGE OUTLINE(SOT23-6)



Symbol	Dimensions In Millimetres		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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