

General Features

- Low On-Resistance
- 100% avalanche tested
- Fast Switching Speed
- Excellent package for good heat dissipation

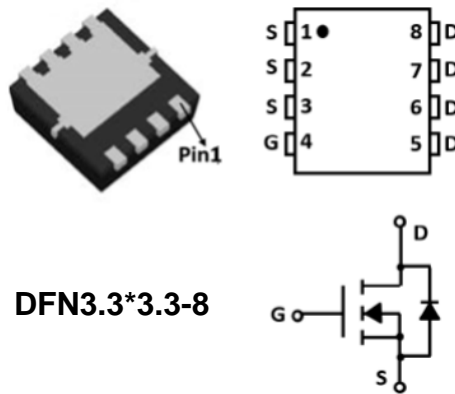
Application

- DC/DC Converters
- On board power for server
- Synchronous rectification

Product Summary



V_{DS}	40	V
$R_{DS(on), Typ @ V_{GS}=10V}$	6.0	m Ω
I_D	40	A



DFN3.3*3.3-8

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	40	A
		$T_C = 100^\circ\text{C}$	32	A
I_{DM}	Pulsed Drain Current ^{note1}		160	A
EAS	Single Pulsed Avalanche Energy		50	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	65	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.92	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	LIMITS			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	40	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$	---	---	1	μA
		$T_J=125^\circ C$	---	---	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.1	1.6	2.4	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
$R_{DS(on)}^{①}$	Drain-Source On-state Resistance	$V_{GS}=4.5V, I_{DS}=20A$	---	7.5	12	$m\Omega$
		$V_{GS}=10V, I_{DS}=30A$	---	6.0	8.5	$m\Omega$
Diode Characteristics						
$V_{SD}^{①}$	Diode Forward Voltage	$I_{SD}=20A, V_{GS}=0V$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD}=20A, di_{SD}/dt=100A/\mu s$	---	14	---	ns
Q_{rr}	Reverse Recovery Charge		---	32	---	nC
Dynamic Characteristics ^②						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	---	1.2	---	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=20V,$ Frequency=1.0MHz	---	1733	---	pF
C_{oss}	Output Capacitance		---	283	---	
C_{rss}	Reverse Transfer Capacitance		---	141	---	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=20V, I_{DS}=20A,$ $V_{GEN}=10V, R_G=4.7\Omega$	---	6	---	ns
t_r	Turn-on Rise Time		---	10	---	
$t_{d(OFF)}$	Turn-off Delay Time		---	24	---	
t_f	Turn-off Fall Time		---	5	---	
Gate Charge Characteristics ^②						
Q_g	Total Gate Charge	$V_{DS}=32V, V_{GS}=10V,$ $I_{DS}=20A$	---	18	23	nC
Q_{gs}	Gate-Source Charge		---	2.5	---	
Q_{gd}	Gate-Drain Charge		---	5	---	

Notes:①Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

②Guaranteed by design, not subject to production testing.

Test Circuit

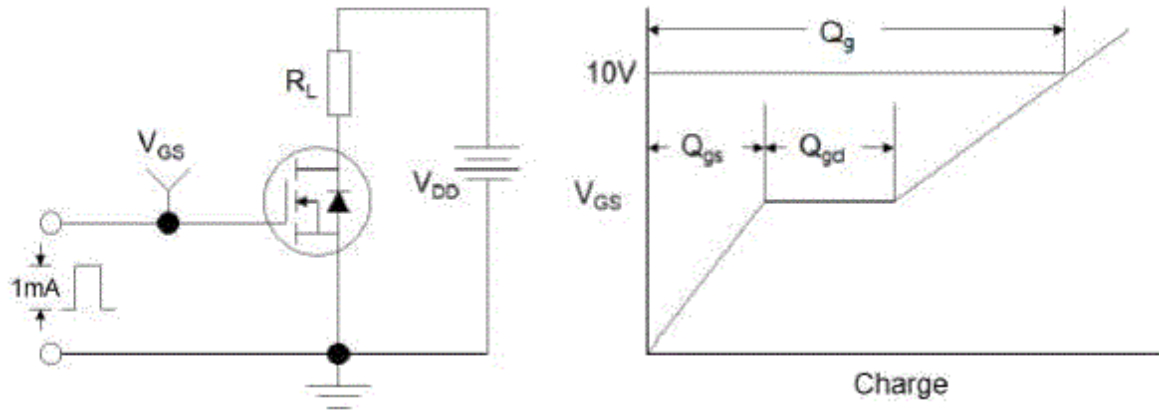


Figure1:Gate Charge Test Circuit & Waveform

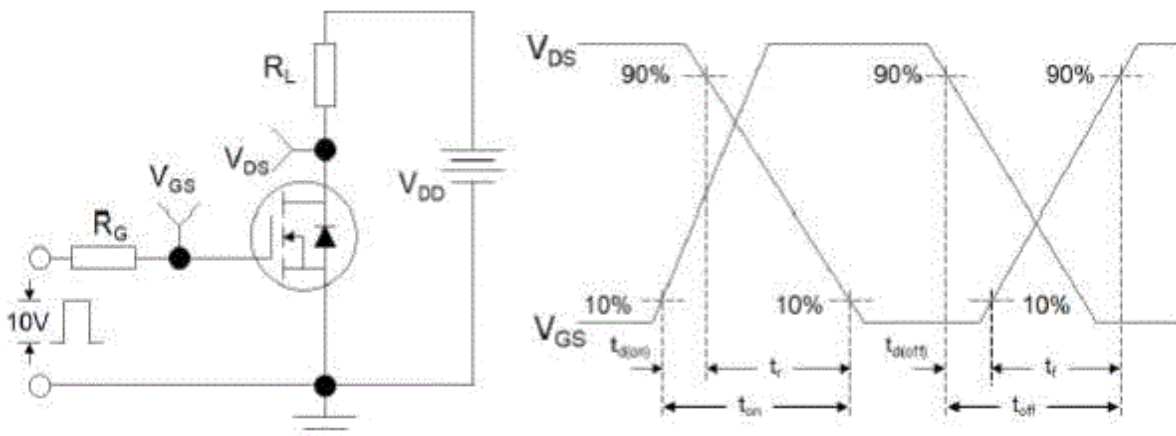


Figure 2: Resistive Switching Test Circuit & Waveforms

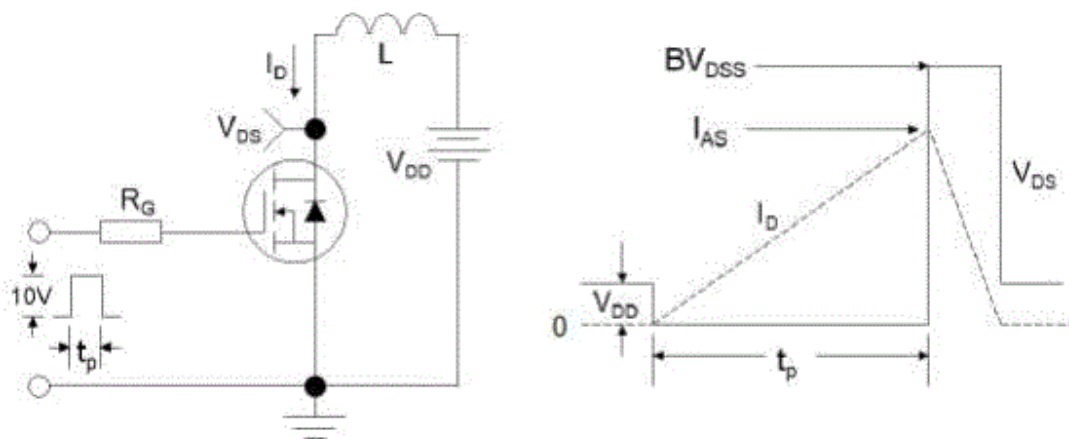
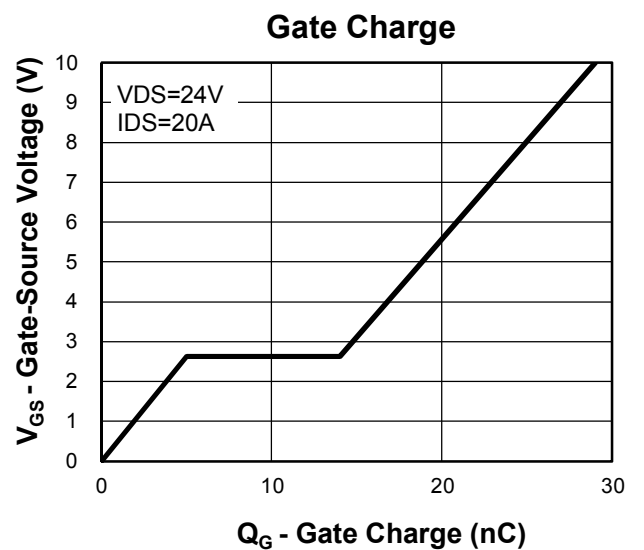
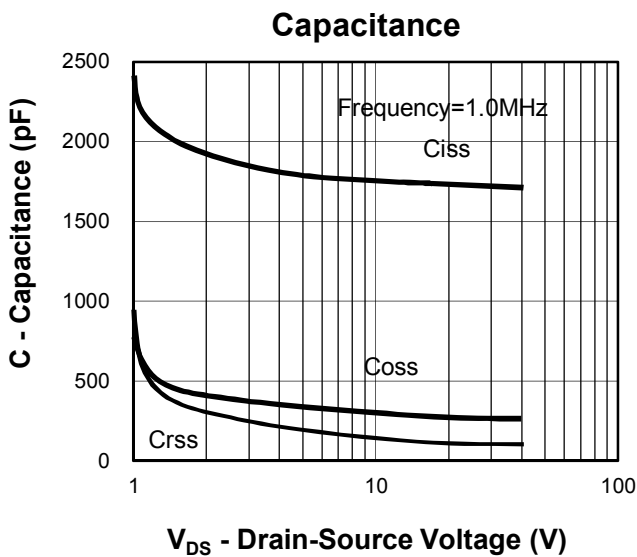
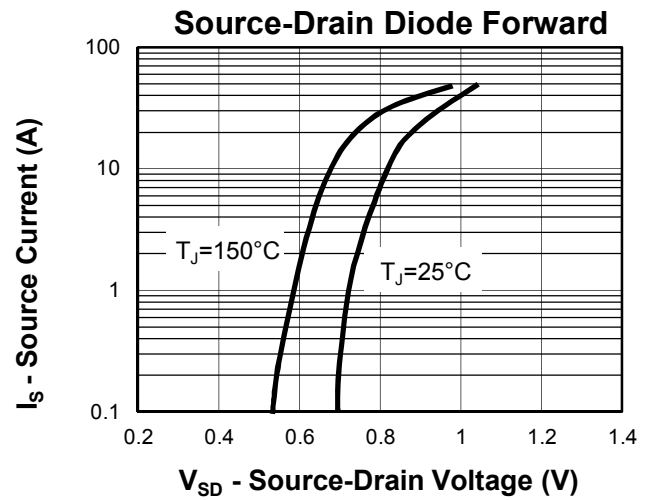
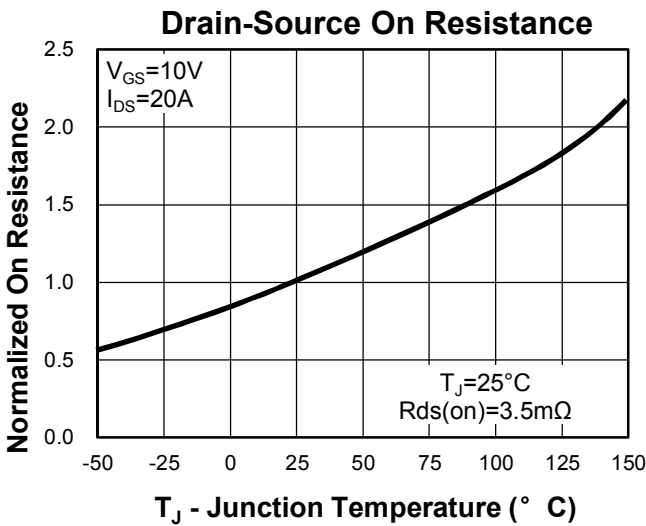
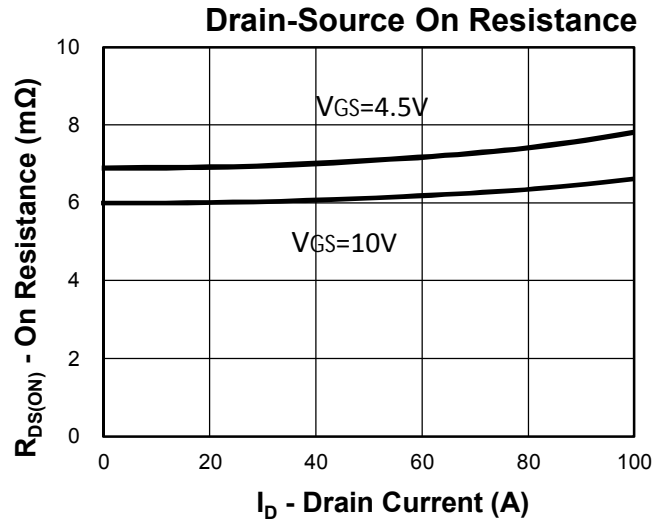
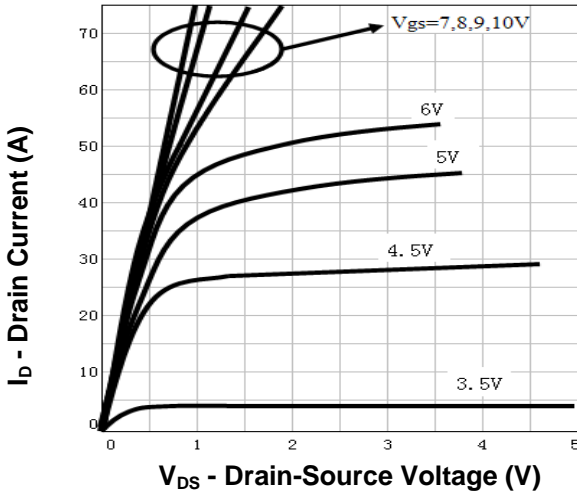
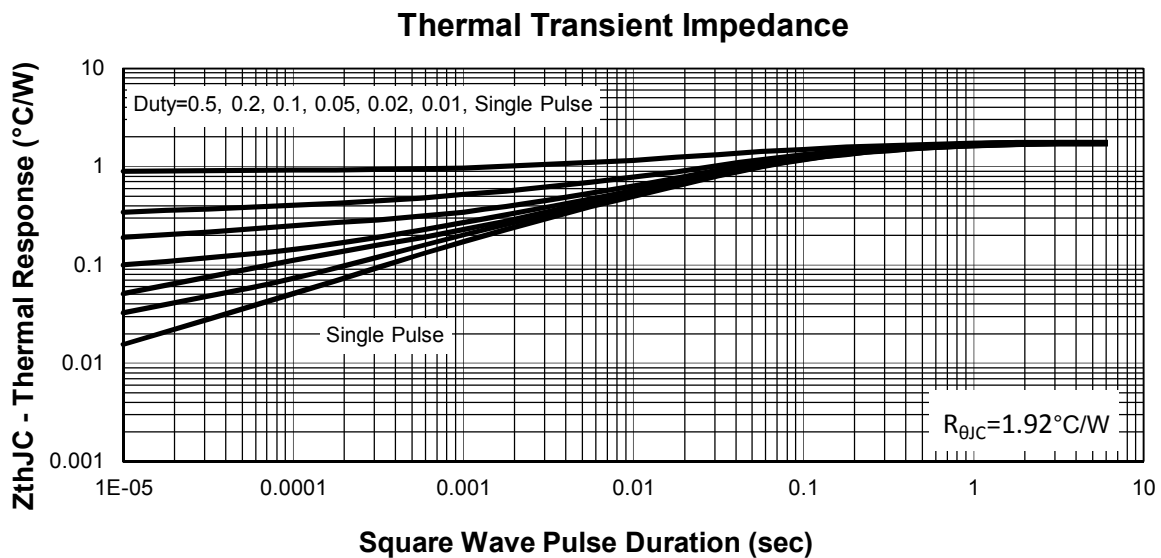
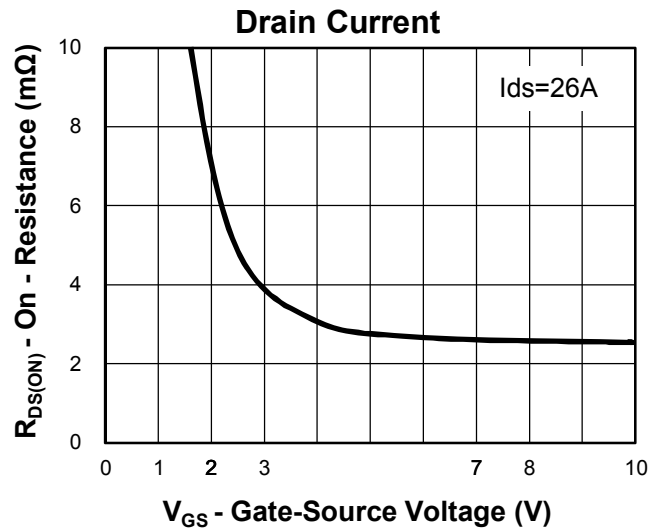
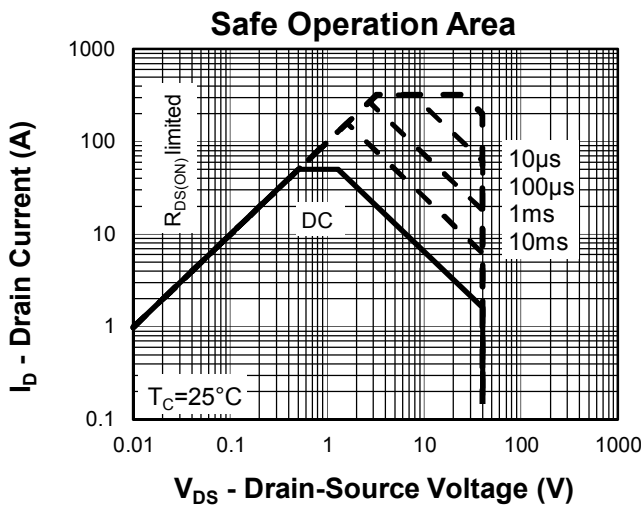
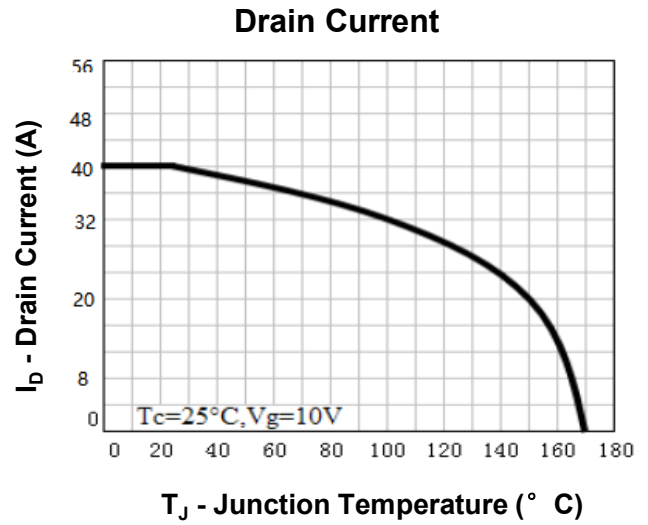
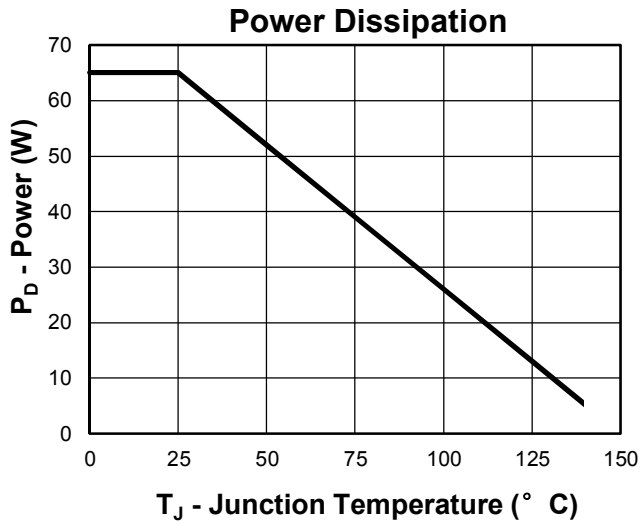


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



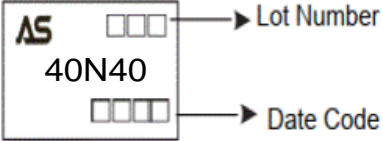
Typical Electrical and Thermal Characteristics (Curves)





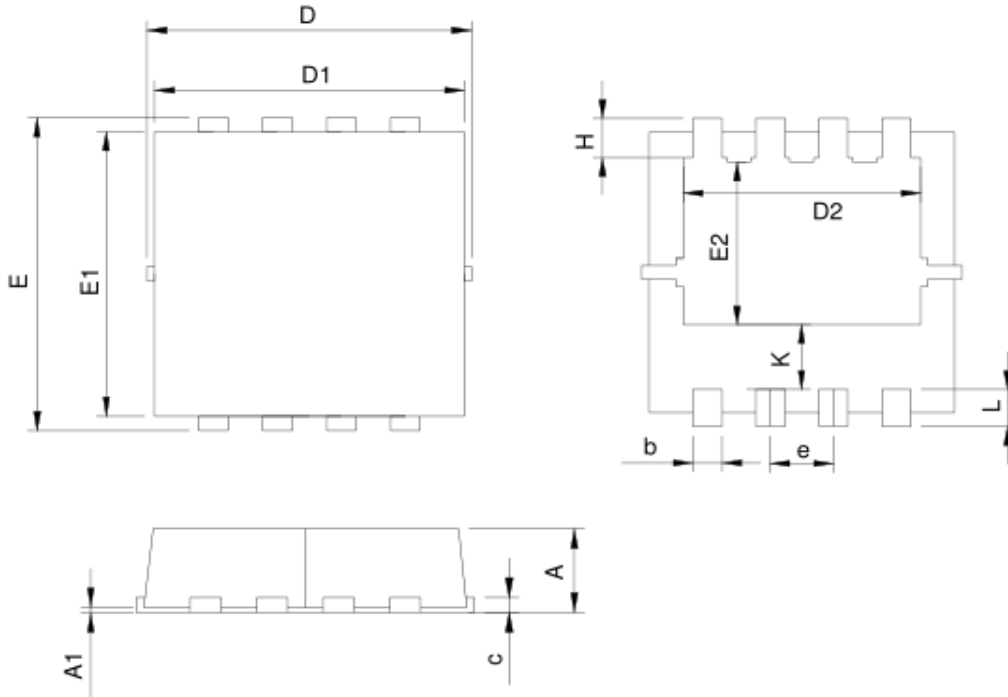
Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM40N40E-R	40N40	DFN3.3*3.3-8	Tape&Reel	5000/Reel

PACKAGE	MARKING
DFN3.3x3.3-8	 <p>AS □□ → Lot Number 40N40 □□□□ → Date Code</p>

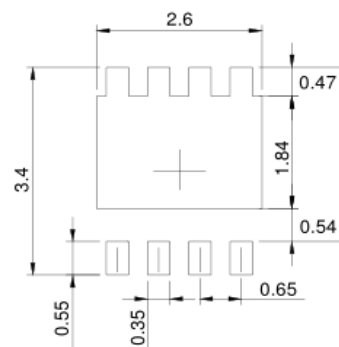


Dimensions(DFN3.3x3.3-8)



SYMBOL	DFN3.3x3.3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.00	0.028	0.039
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.010	0.014
c	0.14	0.20	0.006	0.008
D	3.10	3.50	0.122	0.138
D1	3.05	3.25	0.120	0.128
D2	2.35	2.55	0.093	0.100
E	3.10	3.50	0.122	0.138
E1	2.90	3.10	0.114	0.122
E2	1.64	1.84	0.065	0.072
e	0.65 BSC		0.026 BSC	
H	0.32	0.52	0.013	0.020
K	0.59	0.79	0.023	0.031
L	0.25	0.55	0.010	0.022

RECOMMENDED LAND PATTERN



UNIT: mm

IMPORTANT NOTICE

Xi'an Ascend Semiconductor incorporated MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Xi'an Ascend Semiconductor Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Xi'an Ascend Semiconductor Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Xi'an Ascend Semiconductor Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume .

all risks of such use and will agree to hold Ascendsemi Incorporated and all the companies whose products are represented on Xi'an Ascend Semiconductor Incorporated website, harmless against all damages.

Xi'an Ascend Semiconductor Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Xi'an Ascend Semiconductor Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Xi'an Ascend Semiconductor Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

www.ascendsemi.com