WNM6012

Single N-Channel, 60V, 250mA, Power MOSFET

V_{DS} (V)	Max $R_{DS(on)}$ (Ω)
60	7.5@ V_{GS}=10V
	9.5@ V_{GS}=4.5V
	24.0@ V_{GS}=2.5V
ESD Rating：2000V HBM	
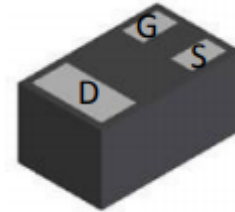
DFN1006-3L

Description

The WNM6012 is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WNM6012 is Pb-free.

Pin configuration (Top view)
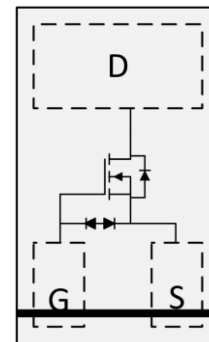
Features

- Trench Technology

- Supper high density cell design

- Excellent ON resistance

- Extremely Low Threshold Voltage

- Small package DFN1006-3L
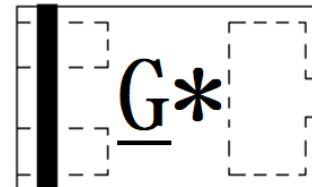
<u>G</u> = Device Code

* = Month(A~Z)

Marking

Applications

Order information

- DC/DC converters

- Power supply converters circuit

- Load/Power Switching for portable device

Device	Package	Shipping
WNM6012-3/TR	DFN1006-3L	10K/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A=25°C	I_D	250	mA
	T_A=70°C		200	
Pulsed Drain Current [c]		I_{DM}	500	
Maximum Power Dissipation [b]	T_A=25°C	P_D	1008	mW
	T_A=70°C		645	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

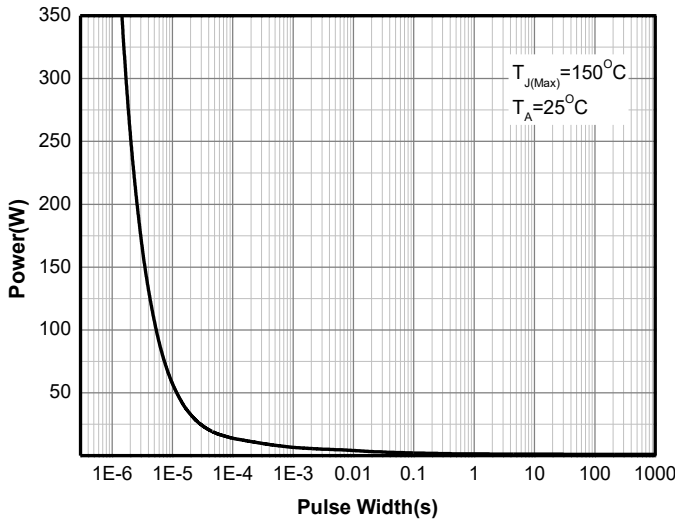| Single Operation				
Parameter		Symbol	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	94	°C/W
	Steady State		124	
Junction-to-Ambient Thermal Resistance [b]	t ≤ 10 s	$R_{\theta JA}$	221	
	Steady State		299	

Note:

a   The value of $R_{\theta JA}$ is measured with the device mounted on 1-inch2 (6.45cm2) with 2oz.(0.071mm thick) Copper pad on a 1.5*1.5 inch2, 0.06-inch thick FR4 PCB, in a still air environment with T_A =25°C. The power dissipation P_D is based on $R_{\theta JA}$ value and the $T_{J(MAX)}$=150°C. The value in any given application is determined by the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

b   The value of $R_{\theta JA}$ is measured with the device mounted on FR-4 minimum pad board, in a still air environment with T_A =25°C. The power dissipation P_D is based on $R_{\theta JA}$ value and the $T_{J(MAX)}$=150°C. The value in any given application is determined by the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.

c   Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d   The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

## Electronics Characteristics (Ta=25ºC, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0$ V, $I_D = 250uA$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V$, $V_{GS} = 0V$			1	uA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm20V$			±10	uA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250uA$	1.0	1.5	2.3	V
Drain-to-source On-resistance[d]	$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 150mA$		4.4	7.5	Ω
		$V_{GS} = 4.5V$, $I_D = 100mA$		4.7	9.5	
		$V_{GS} = 2.5V$, $I_D = 10mA$		7.9	24.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS} = 0$ V,		9.4		pF
Output Capacitance	C_{OSS}	$f = 1.0MHz$,		2.2		
Reverse Transfer Capacitance	C_{RSS}	$V_{DS} = 25$ V		0.7		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10$ V,		3.4		nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{DS} = 30V$,		0.4		
Gate-to-Source Charge	Q_{GS}	$I_D = 150m$ A		0.8		
Gate-to-Drain Charge	Q_{GD}			0.3		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	$V_{GS} = 10V$,		2.0		ns
Rise Time	tr	$V_{DS} = 30$ V,		5.0		
Turn-Off Delay Time	td(OFF)	$I_D = 150m$ A ,		6.8		
Fall Time	tf	$R_G = 10Ω$		60.0		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = 200mA$		0.9	1.2	V

Typical Characteristics (Ta=25°C, unless otherwise noted)
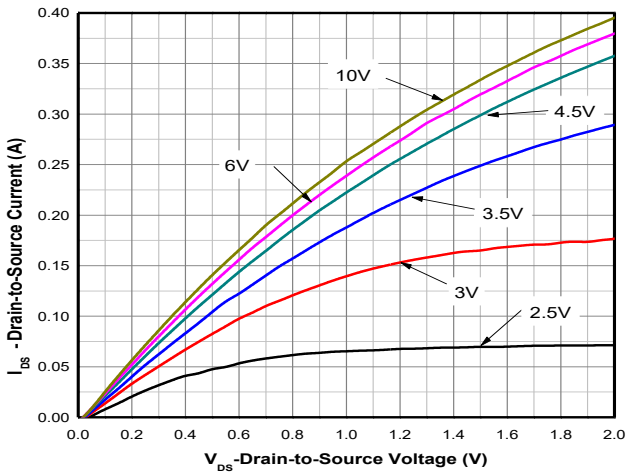
Output Characteristics [d]
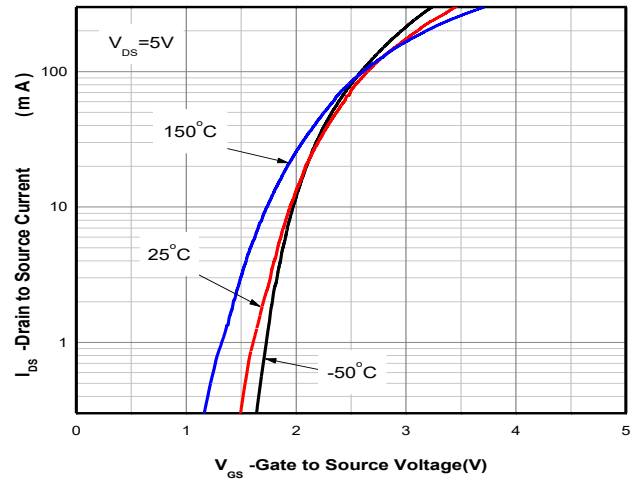
Transfer Characteristics [d]
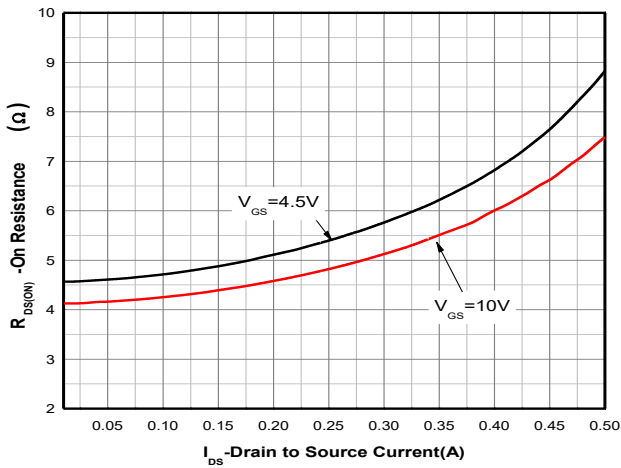
On-Resistance vs. Drain Current [d]
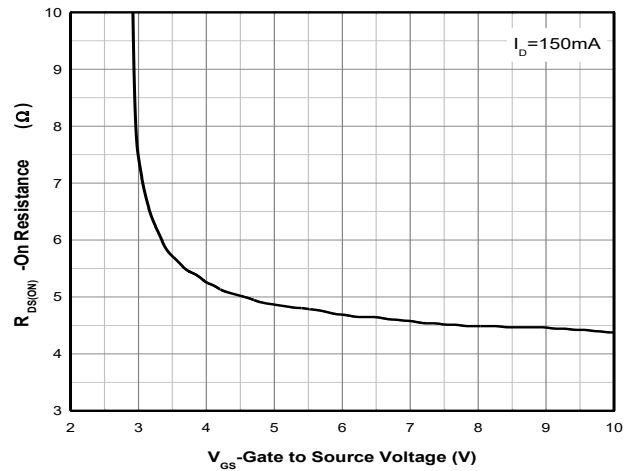
On-Resistance vs. Gate-to-Source Voltage [d]
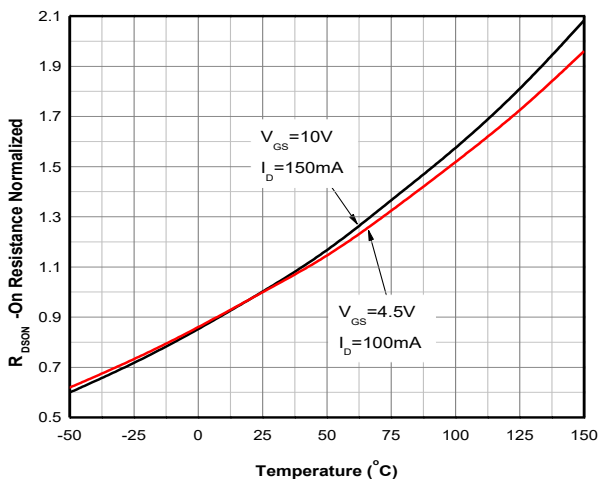
On-Resistance vs. Junction Temperature [d]
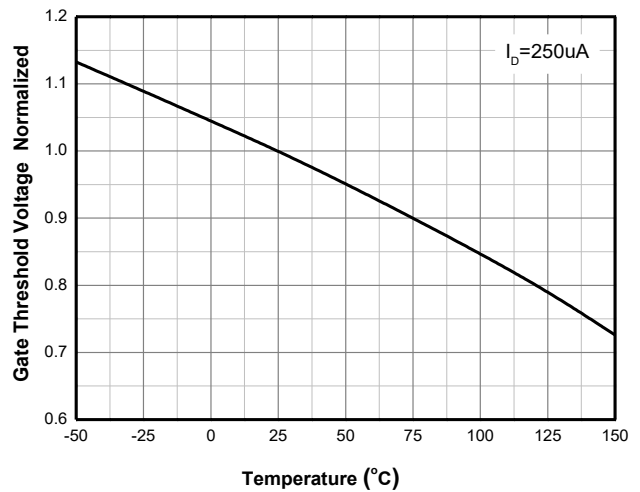
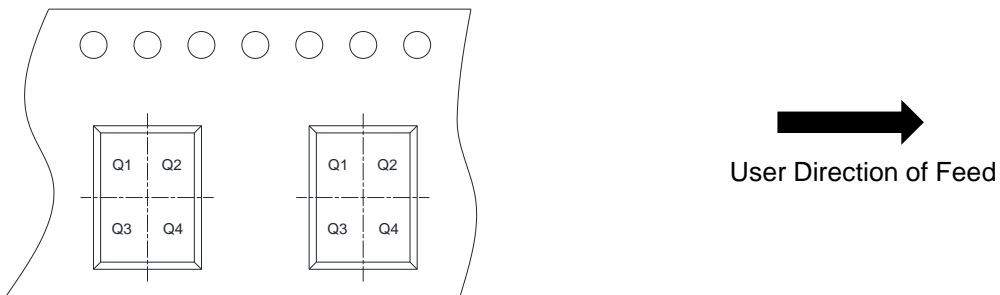**Threshold Voltage vs. Temperature**
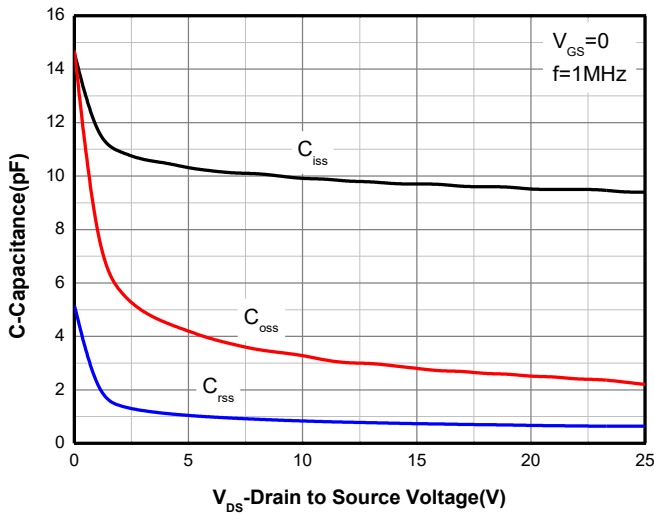
Capacitance
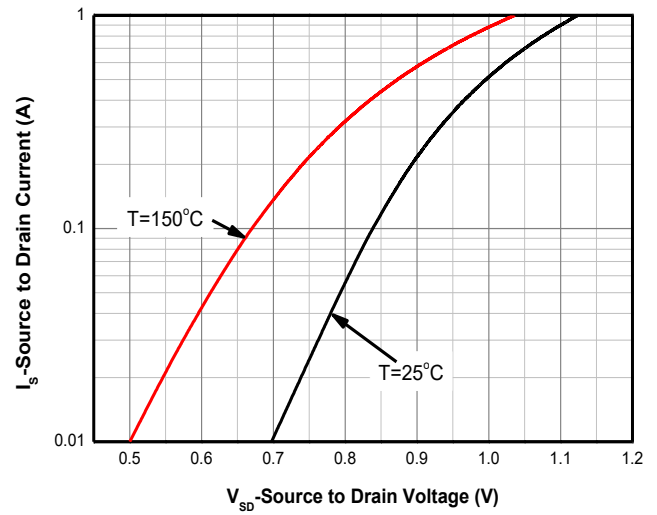
Body Diode Forward Voltage

Single Pulse power
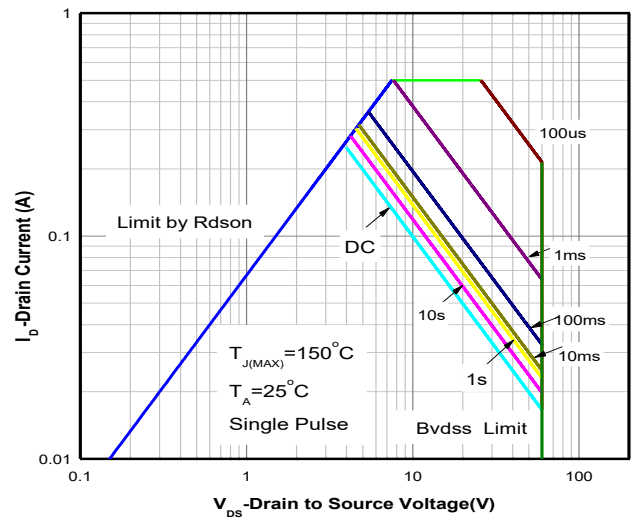
Safe Operating Power
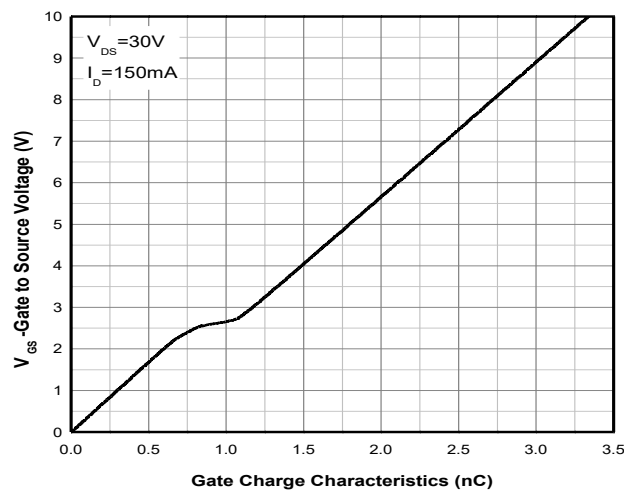
Gate Charge Characteristics
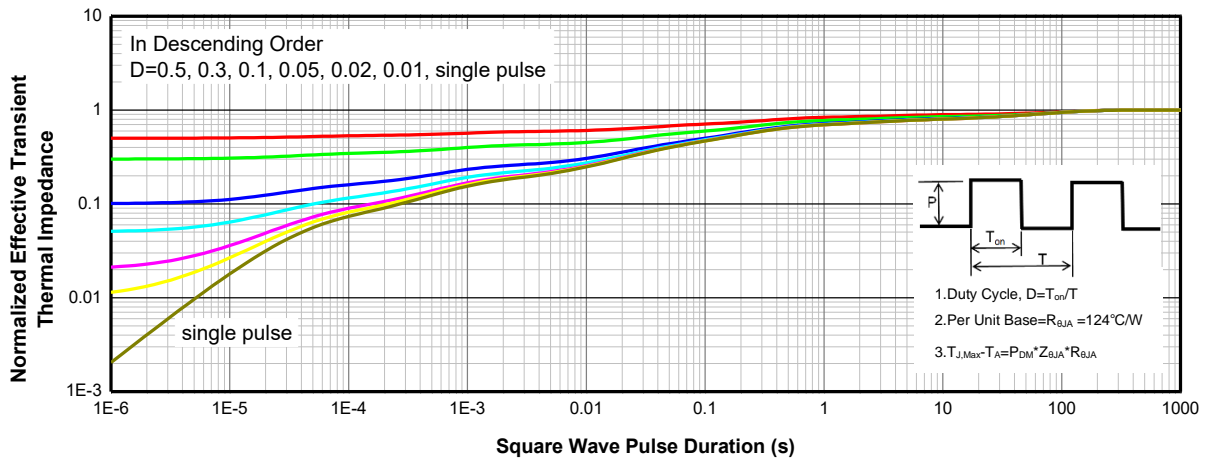
Transient thermal response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

DFN1006-3L
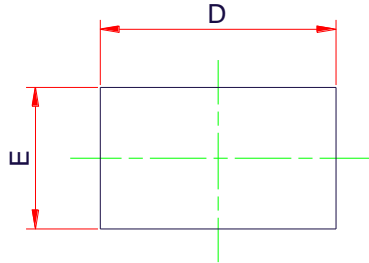
TOP VIEW
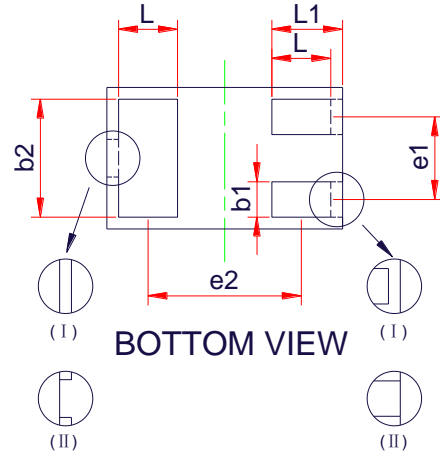
BOTTOM VIEW
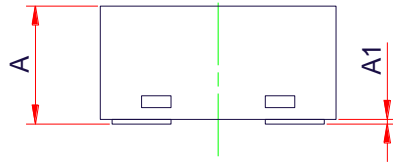
SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.36	-	0.50
A1	0.00	-	0.05
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b1	0.10	0.15	0.20
b2	0.40	0.50	0.60
L	0.20	0.25	0.30
L1	0.20	0.30	0.40
e1	0.35Ref		
e2	0.65 Ref		

TAPE AND REEL INFORMATION

Reel Dimensions
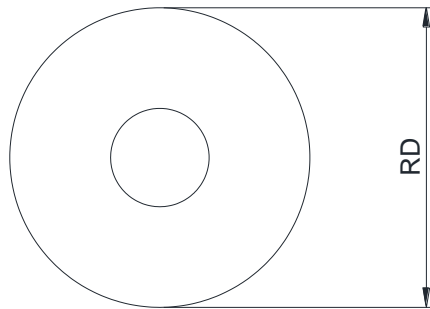
Tape Dimensions
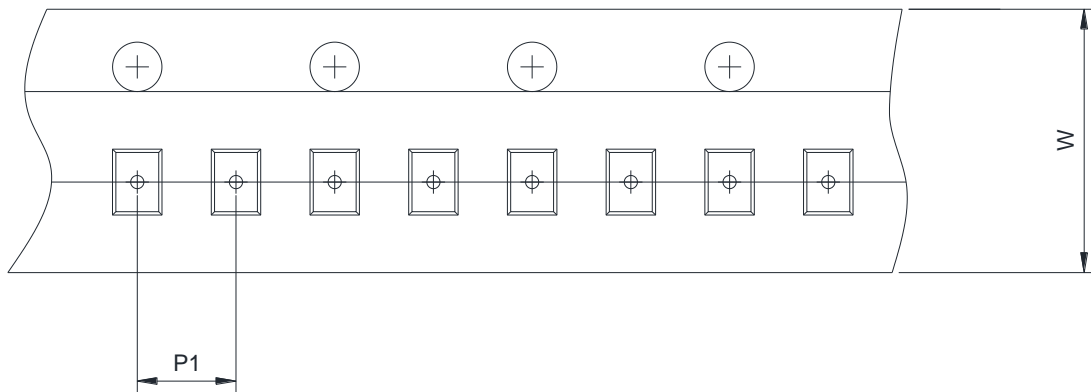
Quadrant Assignments For PIN1 Orientation In Tape

User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☑ 2mm	☐ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☐ Q2	☑ Q3	☑ Q4