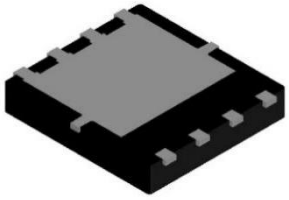
WNM4014

Single N-Channel, 100V, 48A, Power MOSFET

Http://www.sh-willsemi.com

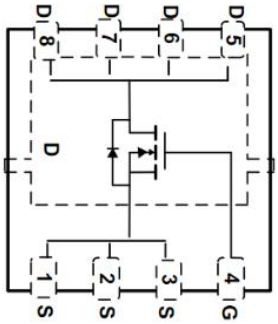
V_{DS} (V)	Typical $R_{DS(on)}$ (mΩ)
100	5.6@ V_{GS}=10V
	7.0@ V_{GS}=4.5V



PDFN5X6-8L

Description

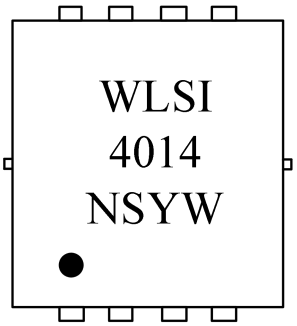
The WNM4014 is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WNM4014 is Pb-free.



Pin configuration (Top view)

Features

- Trench Technology
- Supper high density cell design
- Low ON resistance
- Package PDFN5X6-8L



4014 = Device Code
NS = Special Code
Y = Year
W = Week(A~Z)

Marking

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
WNM4014-8/TR	PDFN5X6-8L	3000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [d]	T_C=25°C	I_D	48	A
	T_C=100°C		43	A
Pulsed Drain Current [c]		I_{DM}	185	A
Continuous Drain Current	T_A=25°C	I_{DSM}	21	A
	T_A=70°C		17	
Avalanche Energy L=0.3mH		E_{AS}	118	mJ
Power Dissipation [b]	T_C=25°C	P_D	63	W
	T_C=100°C		25	
Power Dissipation [a]	T_A=25°C	P_{DSM}	6.0	W
	T_A=70°C		3.8	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	16	21	°C/W
	Steady State		42	53	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	1.6	2	

Note:

a The value of $R_{\theta JA}$ is measured with the device mounted on 1-inch^2 (6.45cm^2) with 2oz.(0.071mm thick) Copper pad on a 1.5*1.5 inch^2, 0.06-inch thick FR4 PCB, in a still air environment with T_A =25°C. The power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C. The value in any given application is determined by the user's specific board design.

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

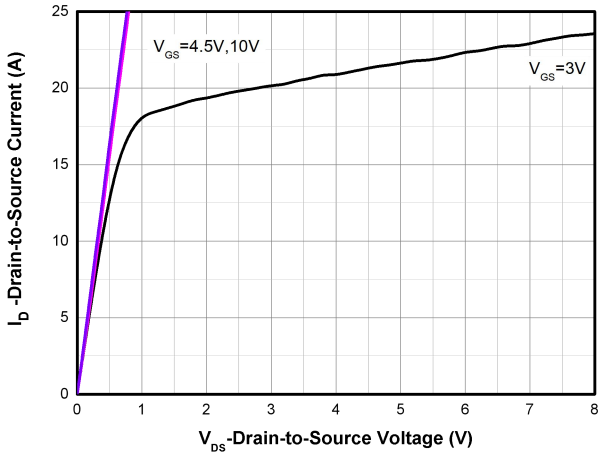
d The maximum current rating by source bonding technology.

e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

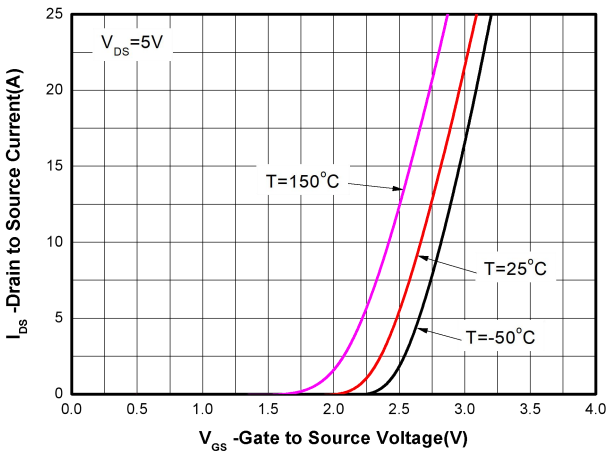
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =80V, V_{GS} = 0V			1	uA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	1.2	1.7	2.5	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D = 20A		5.6	7.0	mΩ
		V_{GS} = 4.5V, I_D = 15A		7.0	10.0	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS} = 30 V		2960		pF
Output Capacitance	C_{OSS}			1303		
Reverse Transfer Capacitance	C_{RSS}			67		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50V, I_D = 20A		55		nC
Threshold Gate Charge	$Q_{G(TH)}$			5.0		
Gate-to-Source Charge	Q_{GS}			9.3		
Gate-to-Drain Charge	Q_{GD}			13.2		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	td(ON)	V_{GS} = 10 V, V_{DS} = 50 V, R_L=2.5 Ω , R_G=3Ω		38		ns
Rise Time	tr			24		
Turn-Off Delay Time	td(OFF)			95		
Fall Time	tf			15		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1A		0.8	1.2	V

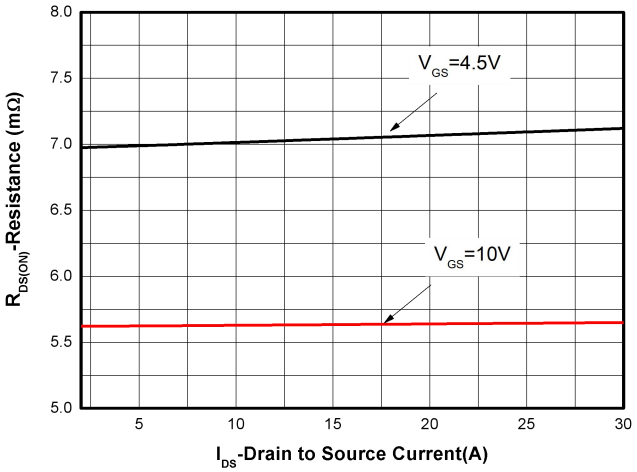
Typical Characteristics (Ta=25°C, unless otherwise noted)



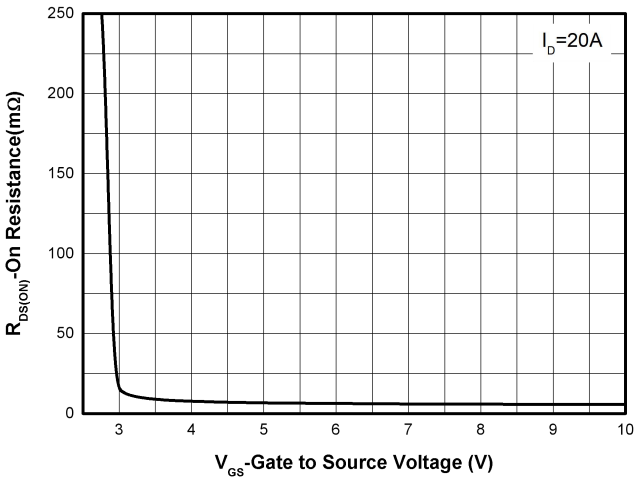
Output Characteristics



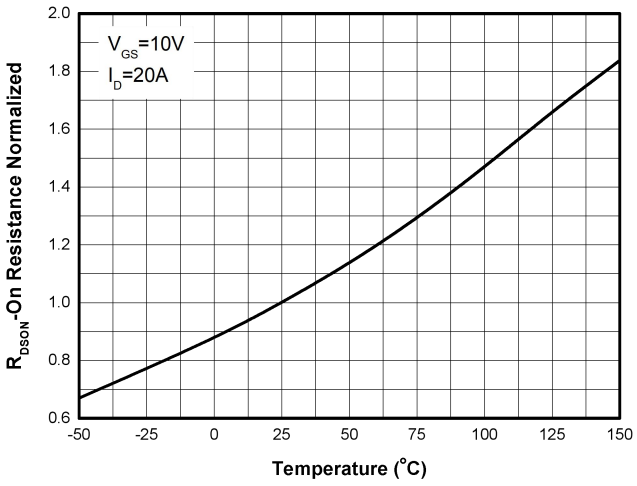
Transfer Characteristics



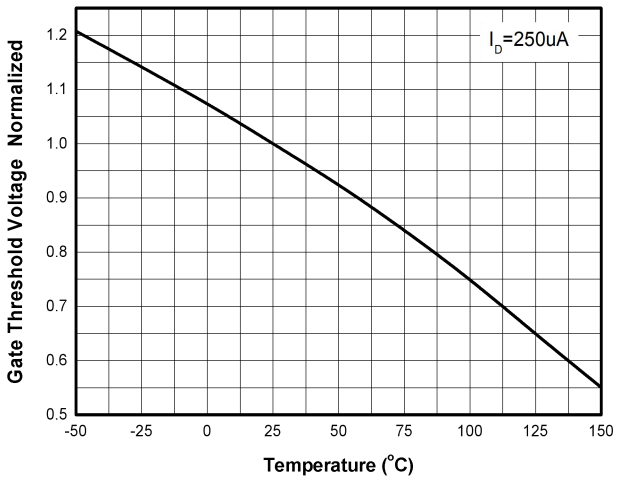
On-Resistance vs. Drain Current



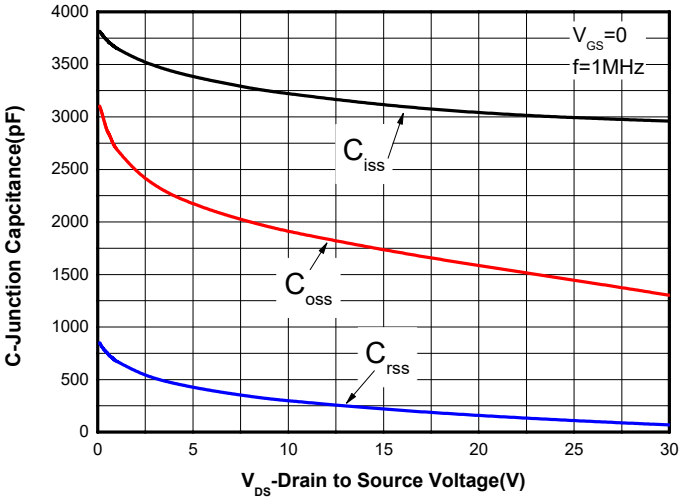
On-Resistance vs. Gate-to-Source Voltage



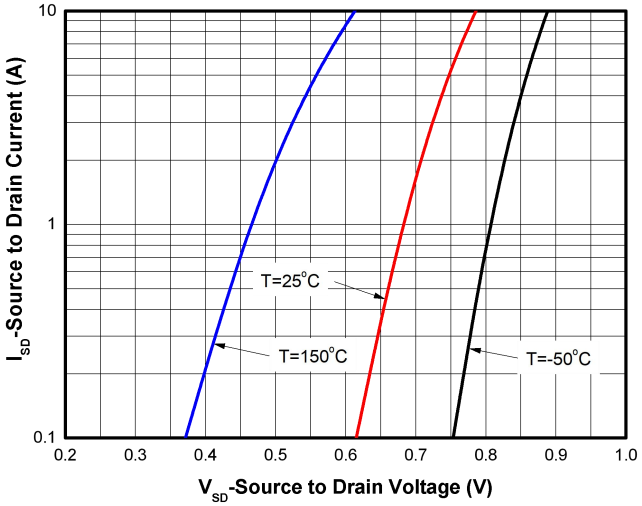
On-Resistance vs. Junction Temperature



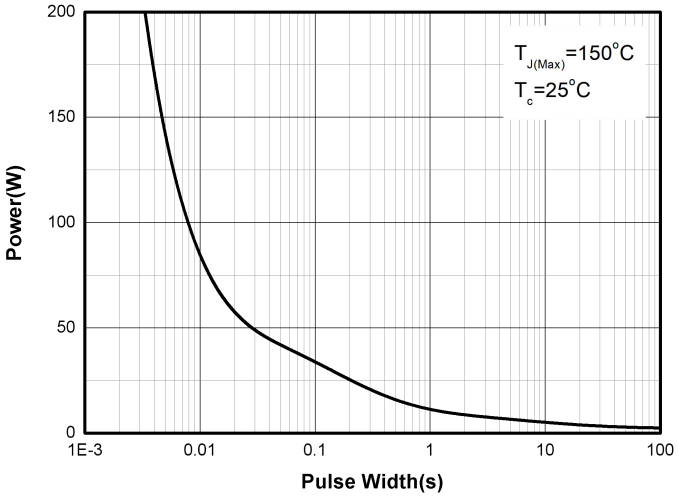
Threshold Voltage vs. Temperature



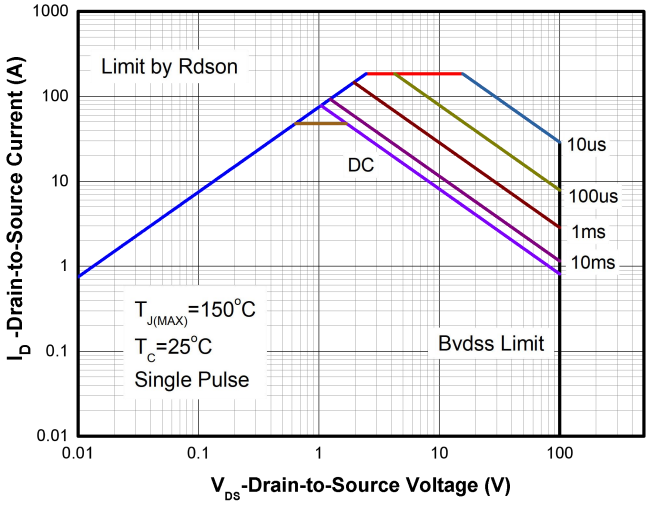
Capacitance



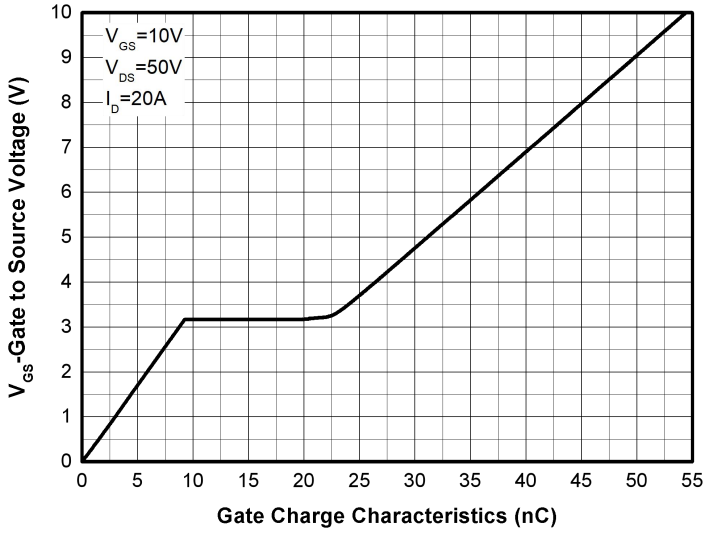
Body Diode Forward Voltage



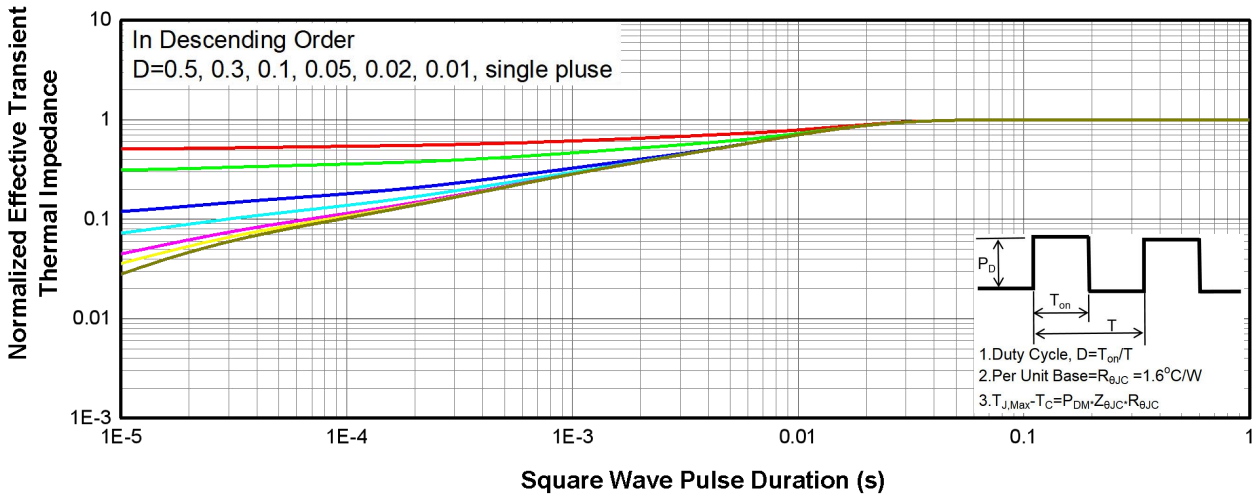
Single Pulse power



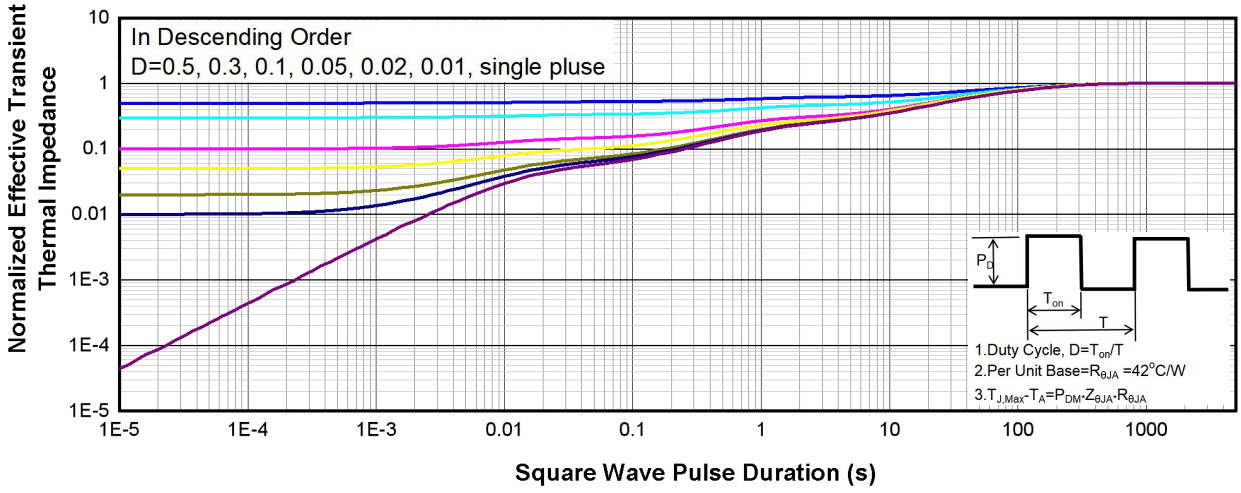
Safe Operating Power



Gate Charge Characteristics



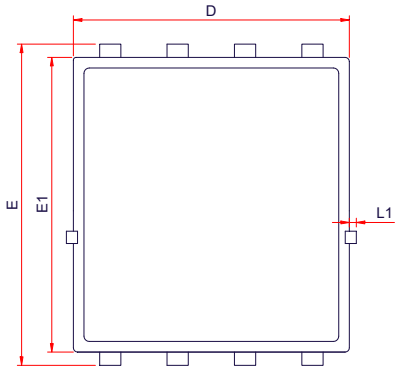
Transient Thermal Response (Junction-to-Case)



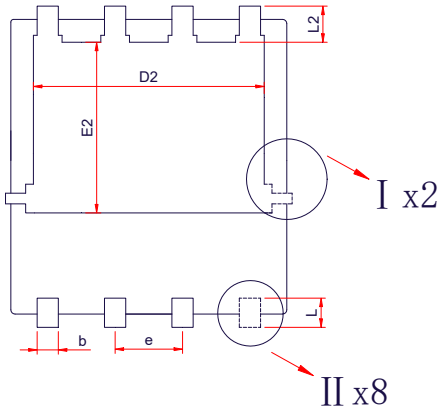
Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

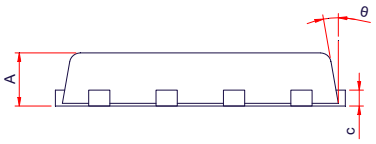
PDFN5X6-8L



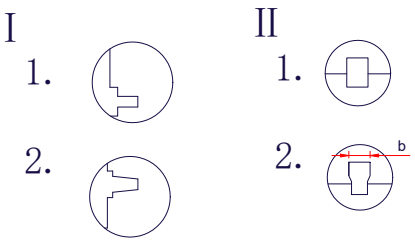
TOP VIEW



BOTTOM VIEW



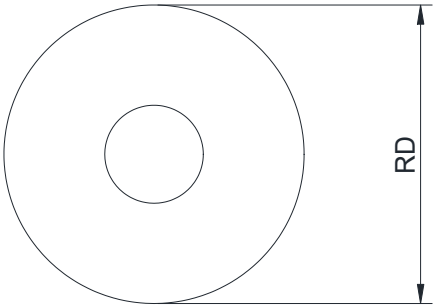
SIDE VIEW



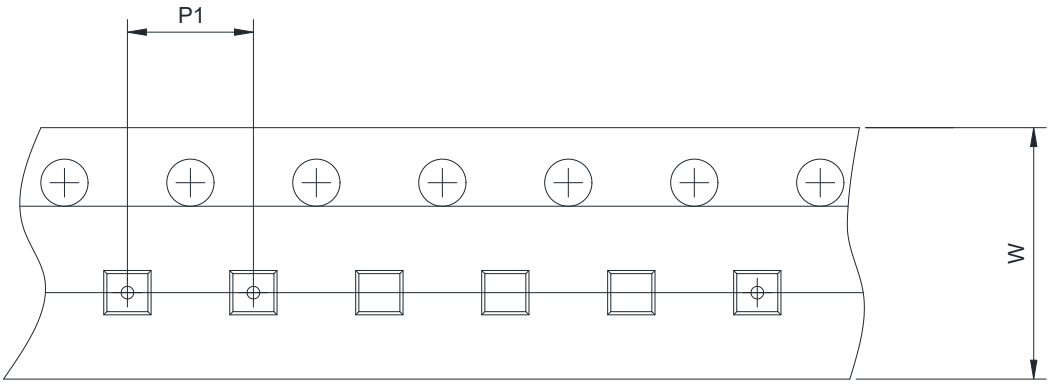
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.85	0.95	1.00
c	0.15	-	0.34
D	4.80	-	5.30
D2	3.82	-	4.45
E	5.90	-	6.15
E1	5.45	-	5.80
E2	3.18	3.45	3.73
e	1.27BSC		
b	0.30	0.40	0.50
L	0.45	-	0.71
L1	0.00	-	0.15
L2	0.68Ref		
θ	0°	-	12°

TAPE AND REEL INFORMATION

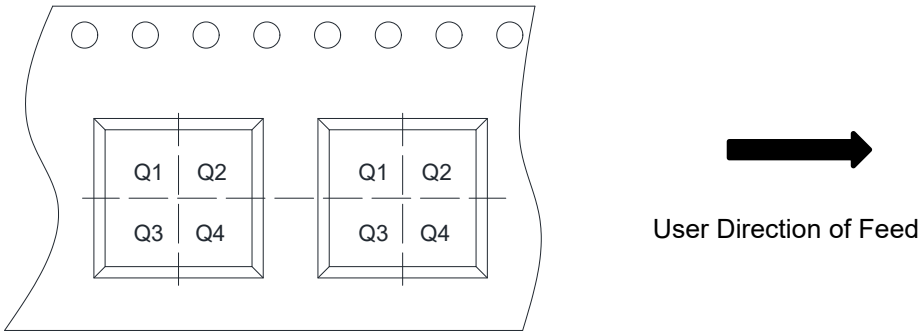
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4