

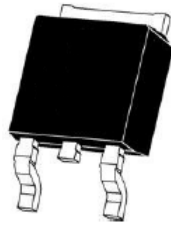


## General Features

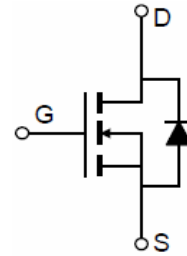
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

## Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply



TO-252-2L top view



Schematic diagram

## Product Summary

$V_{DS}$	60	V
$R_{DS(on), Typ} @ V_{GS}=10V$	12	m $\Omega$
$I_D$	45	A

## Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	45	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_{D(100^\circ\text{C})}$	35	A
Pulsed Drain Current	$I_{DM}$	180	A
Maximum Power Dissipation	$P_D$	80	W
Derating factor		0.53	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	115	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	12	15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	14	17	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =25V, I <sub>D</sub> =20A	24	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	1920	-	PF
Output Capacitance	C <sub>oss</sub>		-	221	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	70	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =2A, R <sub>L</sub> =15Ω V <sub>GS</sub> =10V, R <sub>G</sub> =2.5Ω	-	25	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	5	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	50	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	6	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =30V, I <sub>D</sub> =50A, V <sub>GS</sub> =10V	-	30	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	10	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =40A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	45	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 40A	-	50	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100A/μs (Note 3)	-	100	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω

## Typical Electrical and Thermal Characteristics (Curves)

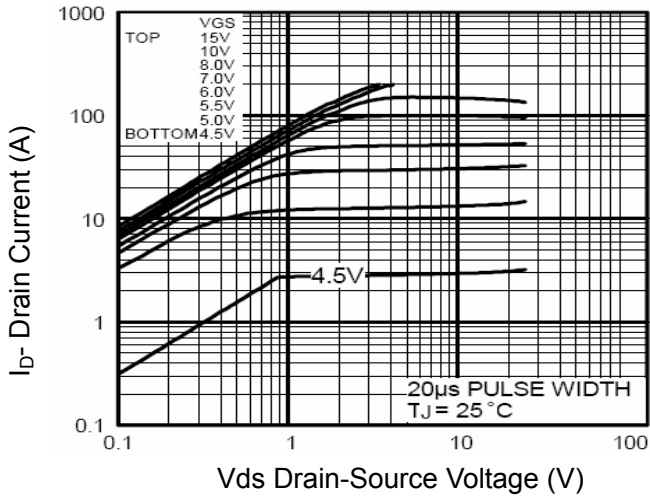


Figure 1 Output Characteristics

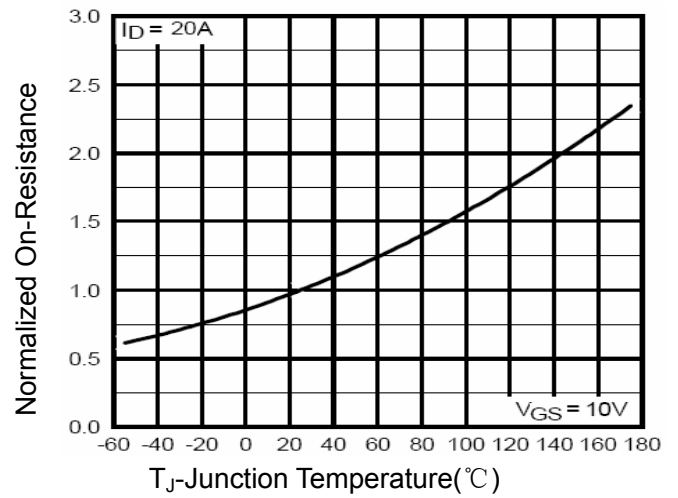


Figure 4  $R_{dson}$ -Junction Temperature

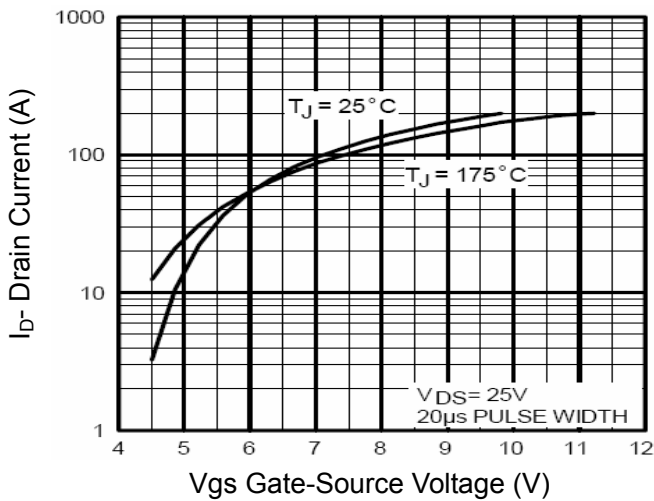


Figure 2 Transfer Characteristics

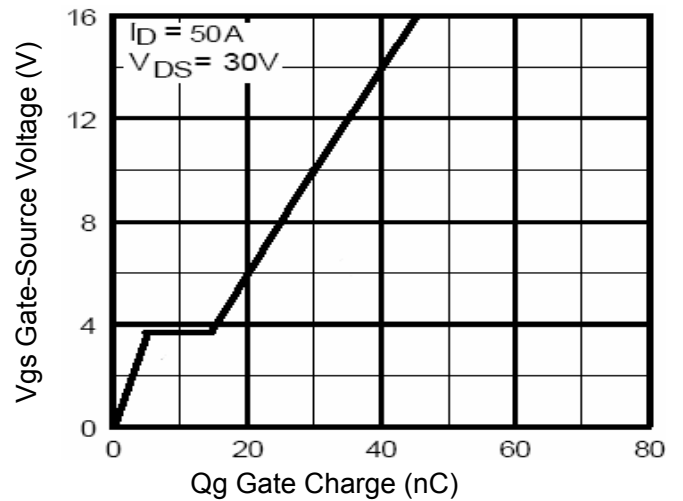


Figure 5 Gate Charge

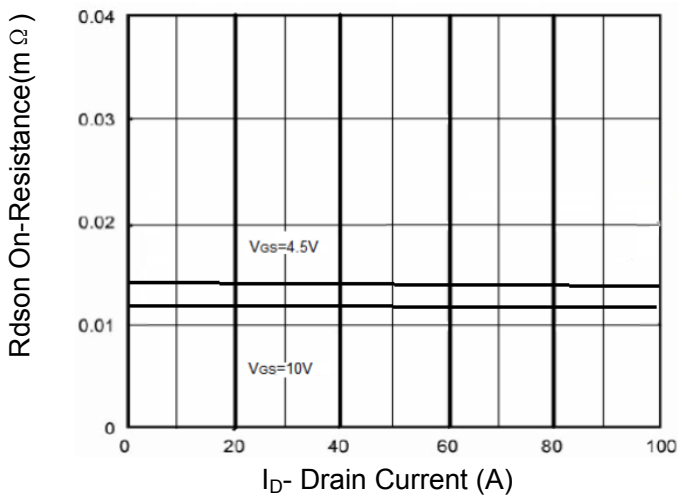


Figure 3  $R_{dson}$ - Drain Current

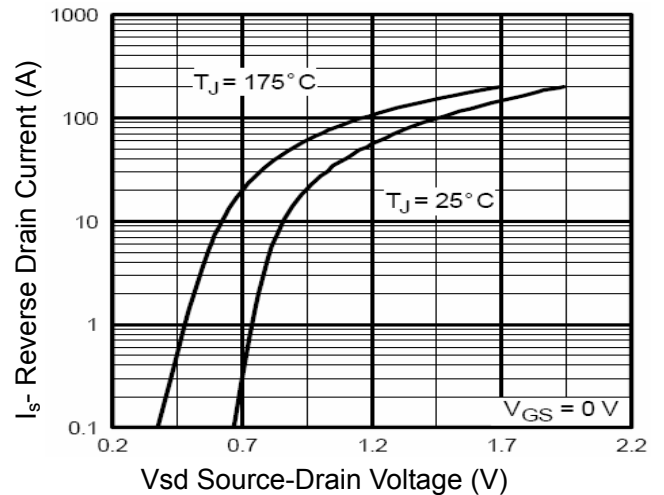
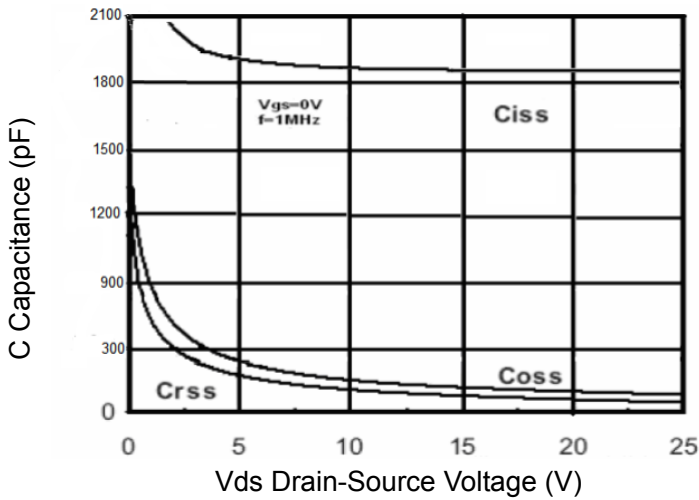
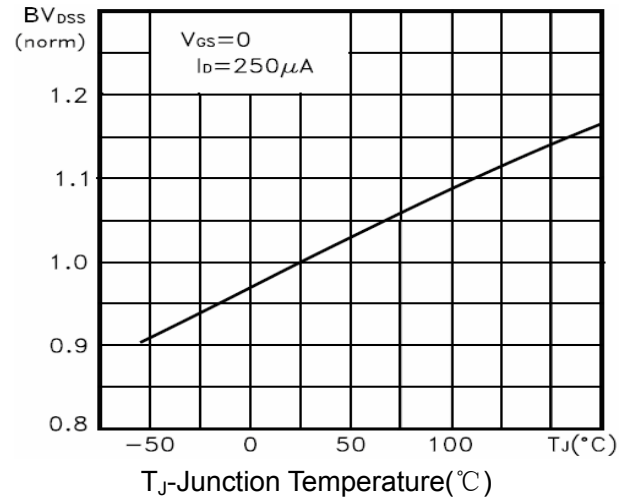


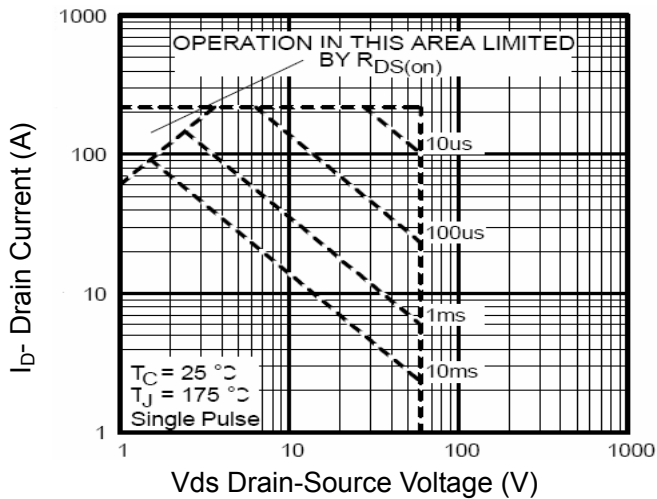
Figure 6 Source- Drain Diode Forward



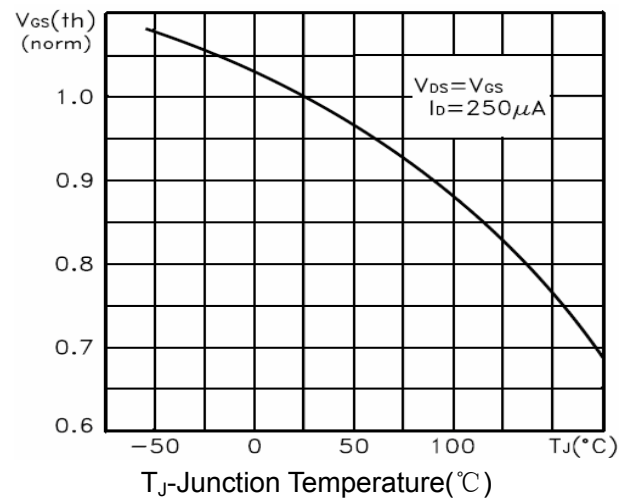
**Figure 7 Capacitance vs Vds**



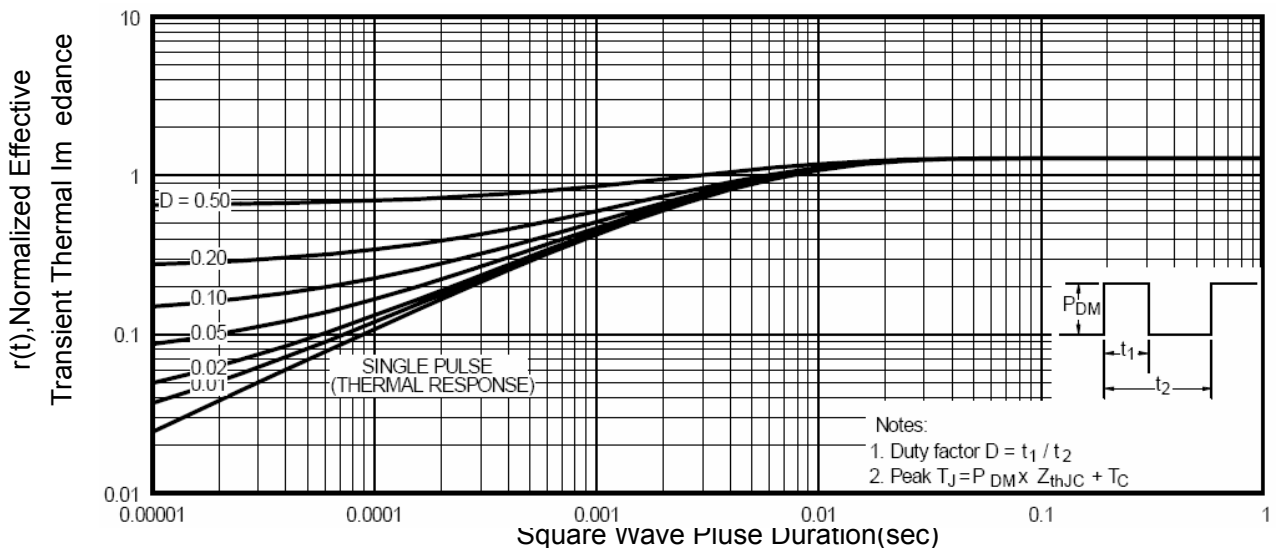
**Figure 9  $BV_{DSS}$  vs Junction Temperature**



**Figure 8 Safe Operation Area**



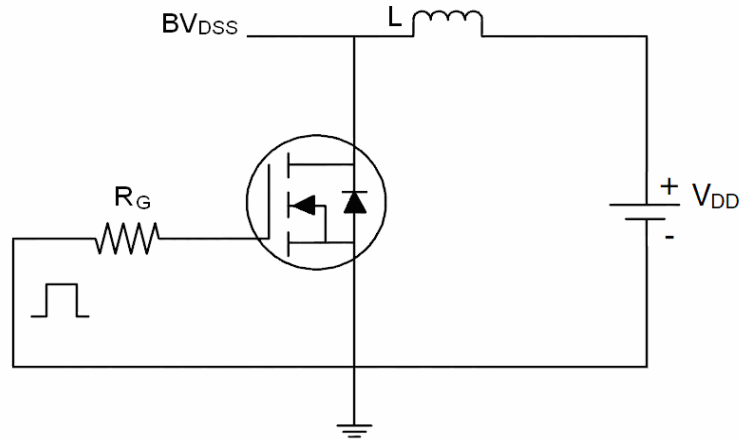
**Figure 10  $V_{GS(th)}$  vs Junction Temperature**



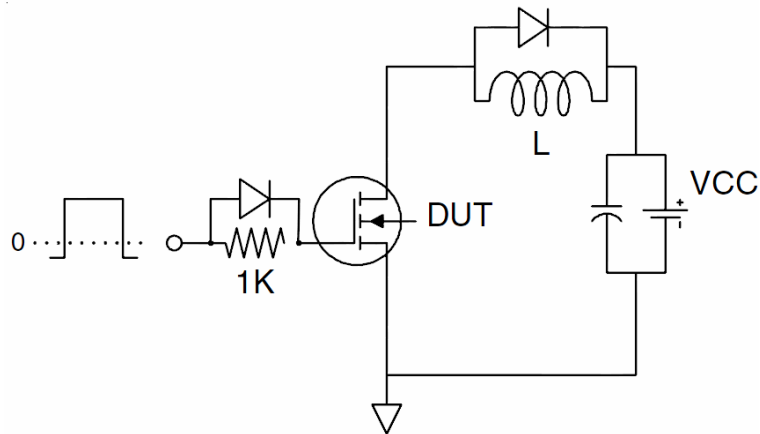
**Figure 11 Normalized Maximum Transient Thermal Impedance**

### Test Circuit

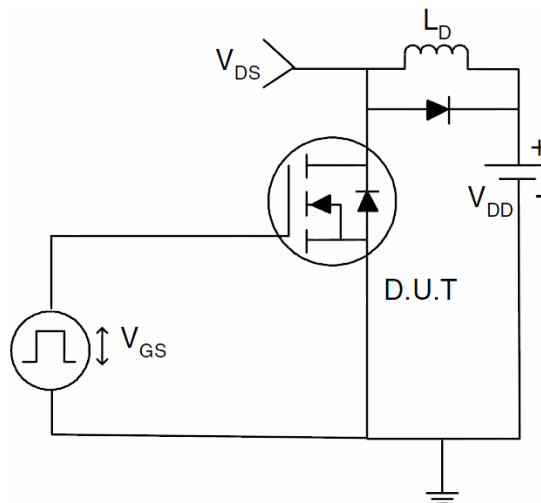
#### 1) $E_{AS}$ Test Circuit



#### 2) Gate Charge Test Circuit

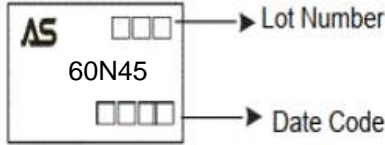


#### 3) Switch Time Test Circuit

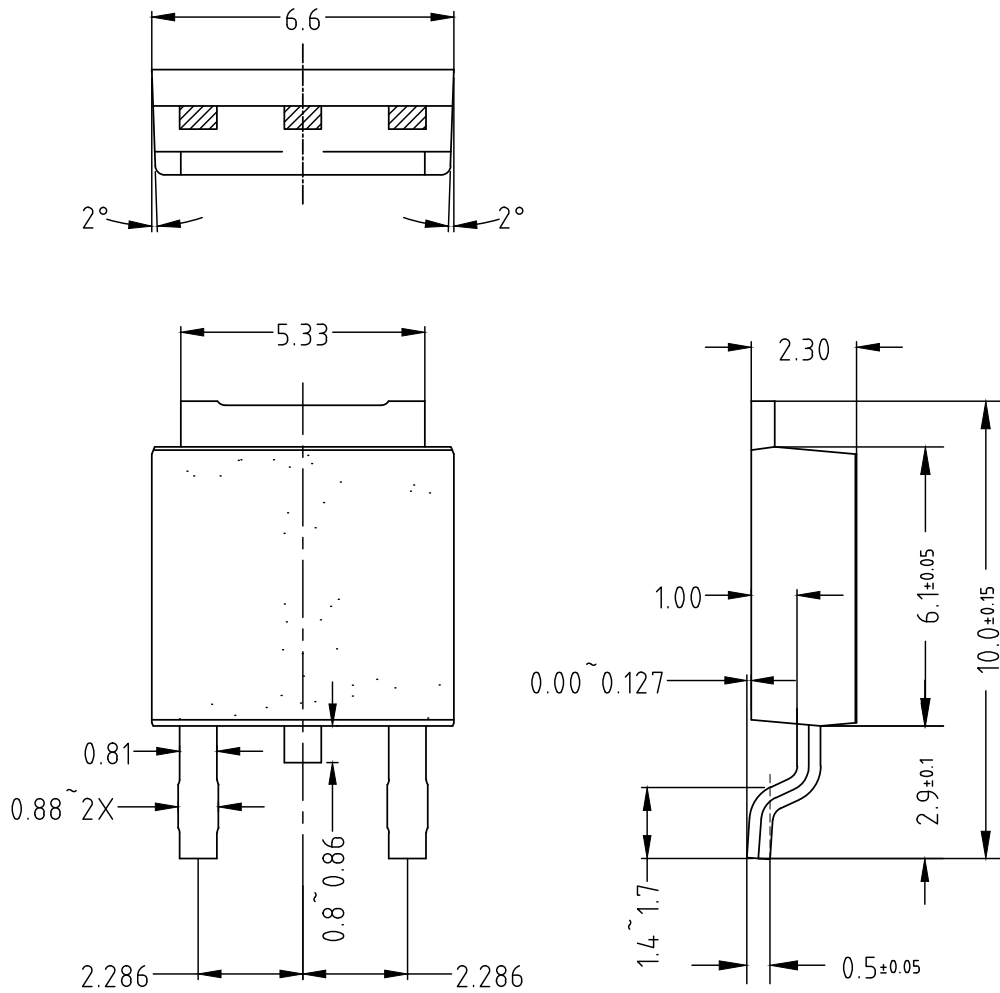


### Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM60N45KQ-R	60N45	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 <p>The diagram shows a rectangular marking area on a TO-252 package. It contains the 'AS' logo, the part number '60N45', and two sets of three empty boxes. The top set of boxes is labeled 'Lot Number' and the bottom set is labeled 'Date Code'.</p>

### TO-252



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