BCT644B
2:1 MIPI D-PHY,C-PHY(2.0Gbps) 4-Data Lane Switch

GENERAL DESCRIPTION

The BCT644B is a four-data-lane, MIPI, D-PHY, C-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The BCT644B is designed for the MIPI specification and allows connection to a CSI or DSI module.

APPLICATIONS

Cellular Phones, Smart Phones
Displays

FEATURES

- Switch Type: SPDT(10x)
- Signal Types: MIPI, D-PHY,C-PHY
- V_{CC}:1.65 to 4.5V
- Input Signals: 0 to V_{CC}
- R_{ON}: 7.7Ω Typical HS MIPI
  8.8Ω Typical LP MIPI
- ΔR_{ON}: 0.6Ω Typical
- R_{ON_FLAT}: 0.3Ω Typical
- I_{CCZ}: 0.5uA Maximum
- I_{CC}: 26uA Typical
- Q_{IRR}:-32dB Typical
- X_{TALK}:-45dB Typical
- Differential Bandwidth:2.0GHz Typical
- C_{ON}:5.2pF
- 36-Ball WLCSP Package

ORDERING INFORMATION

Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT644BEWX-TR	WLCSP-36	-40°C to +85°C	644B XXXXX	3000

Mark Note: "XXXXX" in Marking will be appeared as the batch code.

TYPICAL OPERATING CIRCUIT

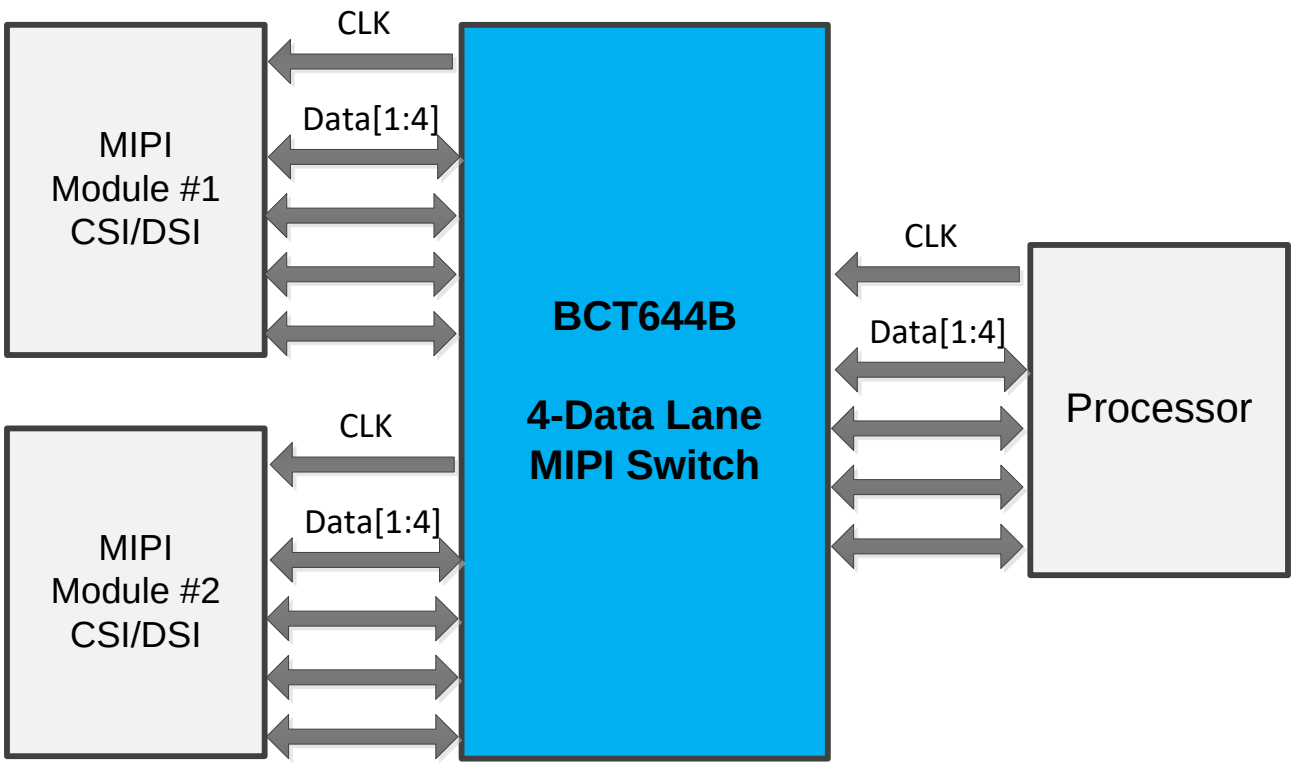


Figure 1. Application Block Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})…….....-0.5V to +5.25V
DC Input Voltage (SEL, /OE)[1].....-0.5V to V_{CC}V
DC Switch I/O Voltage.....-0.5V to 5.25V
DC Input Diode Current.....-50mA
DC Output Current …….....50mA
Storage Temperature Range.....-65℃ to +150℃
Junction Temperature.....150℃
Operating Temperature Range.....-40℃ to +85℃
Lead Temperature (Soldering, 10 sec).....260℃
ESD Susceptibility
All Pins.....4KV
I/O to GND.....4KV
Power to GND..... .....8KV

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Broadchip recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Broadchip reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Broadchip sales office to get the latest datasheet.

RECOMMENDED OPERATING CONDTIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.65	4.5	V
V_{CTRL}	Control Input Voltage(SEL, /OE)(2)		0	V_{CC}	V
V_{SW}	Switch I/O Voltage (CLKn, CLKAn, CLKBn, Dn, DAn, DBn)	HS Mode	0.1	0.3	V
		LP Mode	0	1.2	
T_A	Operating Temperature		-40	+85	℃

Notes：

1. The input and output negative ratings maybe exceed if the input and output diode current ratings are observed.
2. The control input must be held HIGH or LOW; it must not float.

PIN CONFIGURATION

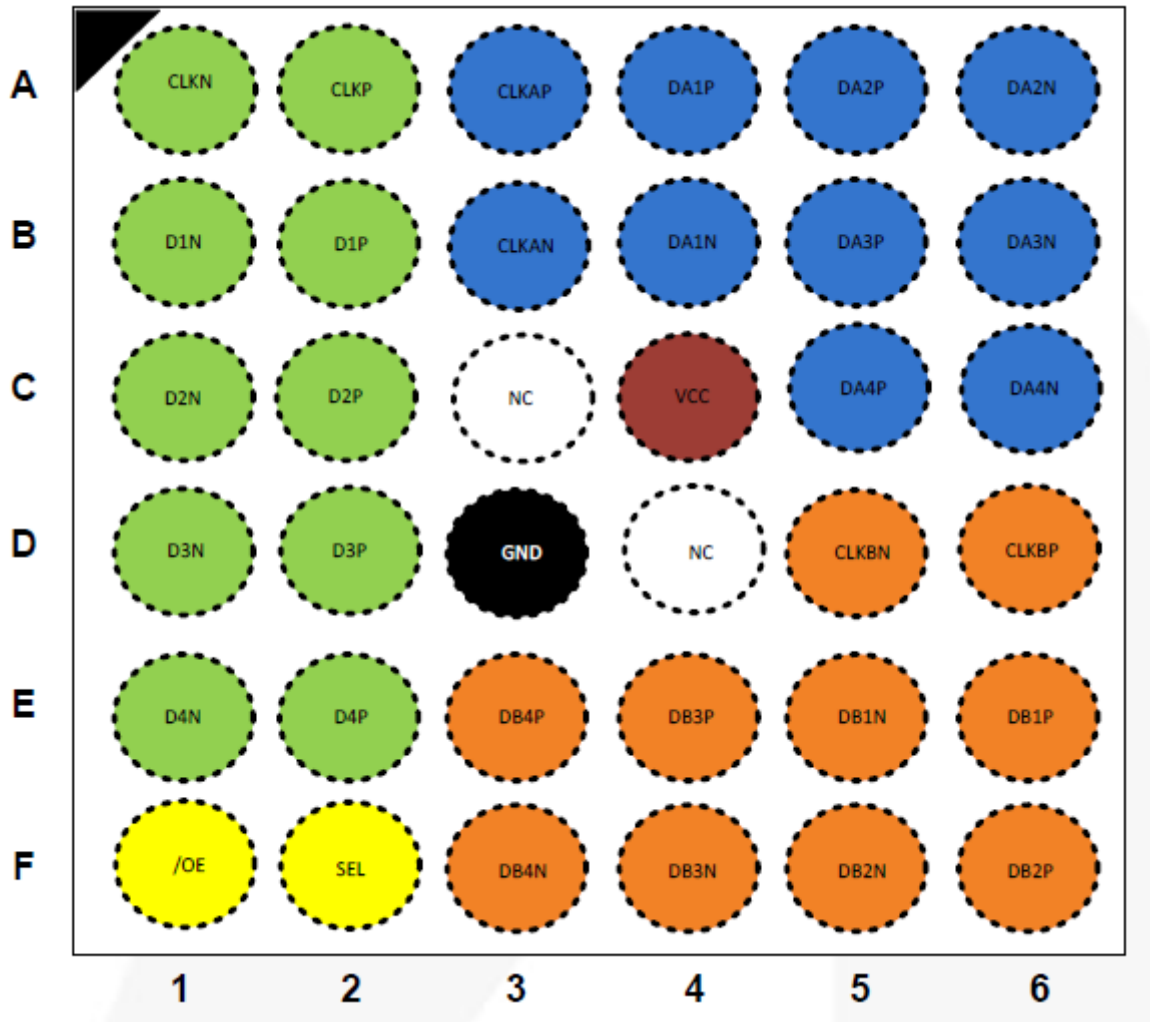


Figure2. Pin Configuration(Top Through View)

Table 1. Ball-to-Pin Mappings

Ball	Pin Name
A1	CLKN
A2	CLKP
A3	CLKAP
A4	DA1P
A5	DA2P
A6	DA2N
B1	D1N
B2	D1P
B3	CLKAN
B4	DA1N
B5	DA3P
B6	DA3N
C1	D2N
C2	D2P
C3	NC
C4	VCC
C5	DA4P
C6	DA4N
D1	D3N
D2	D3P
D3	GND
D4	NC
D5	CLKBN
D6	CLKBP
E1	D4N
E2	D4P
E3	DB4P
E4	DB3P
E5	DB1N
E6	DB1P
F1	/OE
F2	SEL
F3	DB4N
F4	DB3N
F5	DB2N
F6	DB2P

TRUTH TABLE

SEL	/OE	Function
LOW	LOW	CLKP=CLKAP, CLKN=CLKAN, DN(P/N)=DAN(P/N)
HIGH	LOW	CLKP=CLKBP, CLKN=CLKBN, DN(P/N)=DBN(P/N)
X	HIGH	DAN(P/N), DBN(P/N) Data Ports High Impedance

PIN DESCRIPTION

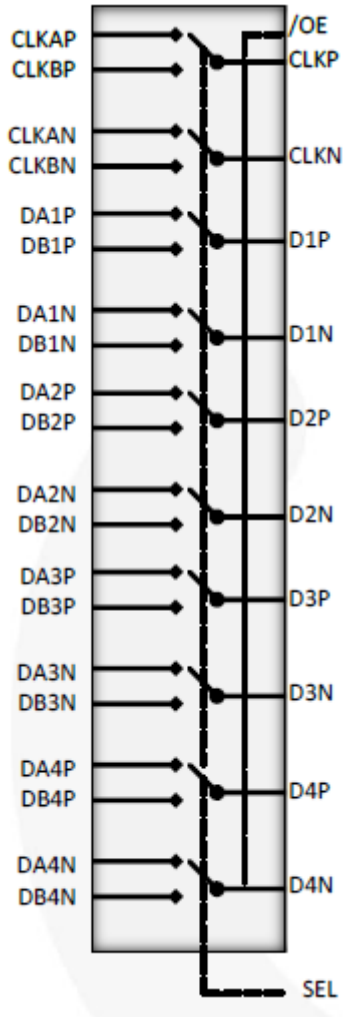


Figure 3. Analog Symbol

Pin Name	Description	
CLKP/N	Common Clock Path	
D1P/N	Common Data Path1	
D2P/N	Common Data Path2	
D3P/N	Common Data Path3	
D4P/N	Common Data Path4	
CLKAP/N	A-Side Clock Path	
DA1P/N	A-Side Data Path 1	
DA2P/N	A-Side Data Path 2	
DA3P/N	A-Side Data Path 3	
DA4P/N	A-Side Data Path 4	
CLKBP/N	B-Side Clock Path	
DB1P/N	B-Side Data Path 1	
DB2P/N	B-Side Data Path 2	
DB3P/N	B-Side Data Path 3	
DB4P/N	B-Side Data Path 4	
SEL	SEL=0	CLKP=CLKAP, CLKN=CLKAN, DN(P/N)=DAN(P/N)
	SEL=1	CLKP=CLKBP, CLKN=CLKBN, DN(P/N)=DBN(P/N)
/OE	Output Enable	
VCC	Power	
GND	Ground	
NC	No Connect	

DC ELECTRICAL CHARACTERISTICS

(All typical values are T_A = 25℃, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Input Leakage(SEL, /OE)	I_{IN}	V_{SW}=0 to 4.3V	1.65 to 4.5	-100		100	nA
Input Voltage High	V_{IH}	V_{IN}=0 to V_{CC}	1.65 to 4.5	1.0			V
Input Voltage Low	V_{IL}	V_{IN}=0 to V_{CC}	1.65 to 4.5			0.4	V
Off leakage Current of Port CLKAn, DAn, CLKBn, DBn	$I_{NO(OFF)}$ $I_{NC(OFF)}$	CLKn, Dn=0.3V; V_{CC}-0.3V; CLKAn, DAn, or CLKBn; DBn=V_{CC}-0.3V, 0.3V, or Floating; /OE=0V	1.65 to 4.5	-100		100	nA
On leakage Current of Common Ports(CLKAn, Dn)	$I_{A(ON)}$	CLKn, Dn=0.3V; Vcc-0.3V; CLKAn, DAn, or CLKBn; DBn=V_{CC}-0.3V, 0.3V, or Floating; /OE=0V	1.65 to 4.5	-100		100	nA
Power-Off Leakage Current	I_{OFF}	CLKn, Dn or CLKAn, DAn, or CLKBn; DBn; V_{IN}=0V to 4.5V; V_{CC}=0V	0	-100		100	nA
Off-State Leakage	I_{OZ}	0≤CLKn, Dn, CLKAn, DAn, CLKBn, DBn≤ 3.6V; /OE=High	4.5	-100		100	nA
Switch On Resistance for HS MIPI Applications(3)	$R_{ON\_MIPI\_HS}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8--4.5		7.7		Ω
Switch On Resistance for LP MIPI Applications(3)	$R_{ON\_MIPI\_LP}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0, 0.6, 1.2V	1.8-4.5		8.8		Ω
On Resistance Matching Between HS MIPI Channels(4)	$\Delta R_{ON\_MIPI\_HS}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8-4.5		0.6		Ω

DC ELECTRICAL CHARACTERISTICS

(All typical values are T_A = 25℃, unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
On Resistance Matching Between LP MIPI Channels(4)	$\Delta R_{ON\_MIPI\_LP}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.0, 0.6, 1.2V	1.8-4.5		0.6		Ω
On Resistance Flatness for HS MIPI Signals(4)	$R_{ON\_FLAT\_MIPI\_HS}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8-4.5		0.3		Ω
On Resistance Flatness for LP MIPI Signals(4)	$R_{ON\_FLAT\_MIPI\_LP}$	I_{ON}=-10mA, /OE=0V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.0, 0.6, 1.2V	1.8-4.5		1.5		Ω
Quiescent Hi-Z Supply Current	I_{CCZ}	V_{IN}=0 or V_{CC}, I_{OUT}=0	4.5			0.5	uA
Quiescent Supply Current	I_{CC}	V_{IN}=0 or V_{CC}, I_{OUT}=0	2.8		26		uA
Increase in I_{CC} Current Per Control Voltage and V_{CC}	I_{CCT}	$V_{SEL, /OE}$=1.65V	4.5			4	uA
			2.5			0.1	

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).
4. Guaranteed by characterization

AC ELECTRICAL CHARACTERISTICS

(All values are for V_{CC}=3.3V at T_A=25℃ unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Initalization Time VCC to Output(5)	t_{INIT}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5			100	us
			1.8			150	
Enable Turn-On Time, /OE to Output	t_{EN}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		120	200	ns
			1.8		250	500	
Disable Turn-off Time, /OE to Output	t_{DIS}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		25	50	ns
			1.8		50	90	
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		50	100	ns
			1.8		75	125	

AC ELECTRICAL CHARACTERISTICS

(All values are for V_{CC}=3.3V at T_A=25℃ unless otherwise specified.)

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω, C_L=5pF, V_{SW}=1.2V	2.5 to 4.5		50	200	ns
			1.8		200	325	
Break-Before-Make Time	t_{BBM}	C_L=5pF, R_L=50Ω, V_{SW}=1.2V		10	50		ns
Off Isolation for MIPI(5)	O_{IRR}	f=750MHz, R_L=50Ω, /OE=V_{CC} ,V_{SW}=-1dBm (200mV_{PP})	1.65 to 4.5		-32		dB
Crosstalk for MIPI(5)	Xtalk	f=750MHz, R_L=50Ω, /OE=V_{CC} ,V_{SW}=-1dBm (200mV_{PP})	1.65 to 4.5		-45		dB
Differential -3db Bandwidth(5)	BW	C_L=0pF, R_L=50Ω	3.0	1.5	2.0		GHz

Note:
5. Guaranteed by characterization.

HIGH-SPEED-RELATED AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Channel-to-Channel Single-Ended Skew(6)	$t_{SK(O)}$	TDR-Based Method (V_{SW}=0.2V_{PP}, C_L=C_{ON})	3.3		6	20	ps
Skew of Opposite Transitions of the Same Output(6)	$t_{SK(P)}$	TDR-Based Method (V_{SW}=0.2V_{PP}, C_L=C_{ON})	3.3		6	20	ps

Notes:
6. Guaranteed by characterization.

CAPACITANCE

PARAMETER	SYM	CONDITIONS	V_{CC} (V)	MIN	TYP	MAX	UNITS
Control Pin Input Capacitance(7)	C_{IN}	V_{CC}=0V, f=1MHz	0		2.1		pF
Output On Capacitance(7)	C_{ON}	V_{CC}=3.3V, /OE=0V, f=1MHz	3.3		5.2		
Output Off Capacitance(7)	C_{OFF}	V_{CC} and /OE=3.3V, f=1MHz	3.3		2.0		

Note:
7. Guaranteed by characterization.

TEST DIAGRAMS

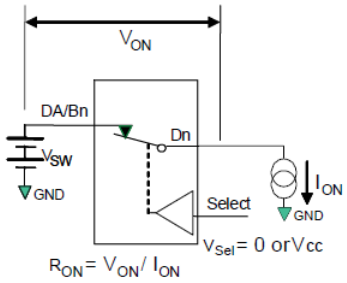


Figure 4. On Resistance

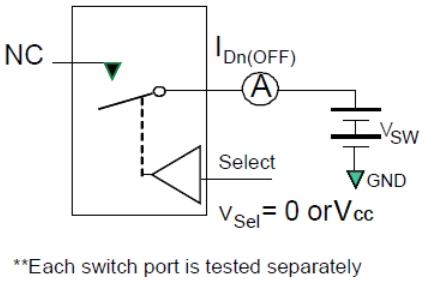


Figure 5. Off Leakage

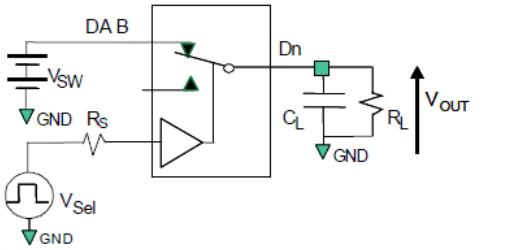


Figure 6. AC Test Circuit Board

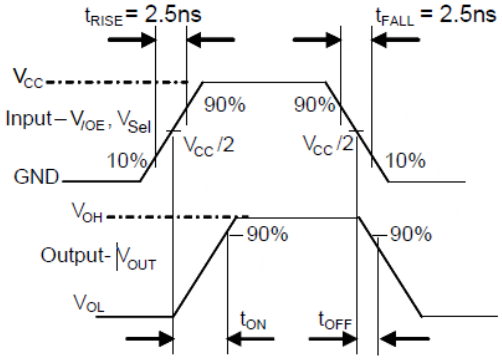


Figure 7. Turn-On/Turn-Off waveform

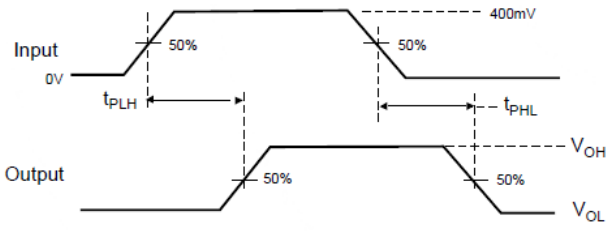


Figure 8. Propagation Delay($t_R$$t_F$-500ps)

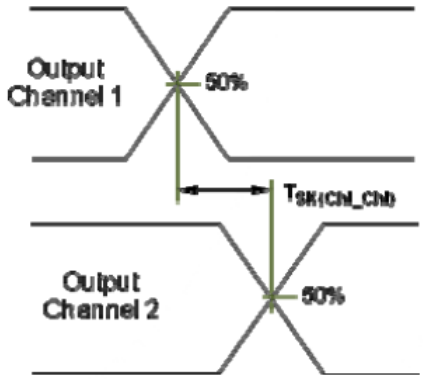


Figure 9. Channel to Channel Skew

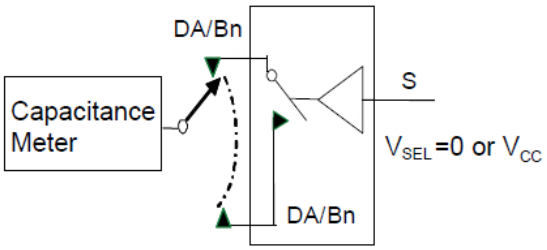


Figure 10. Channel Off Capacitance

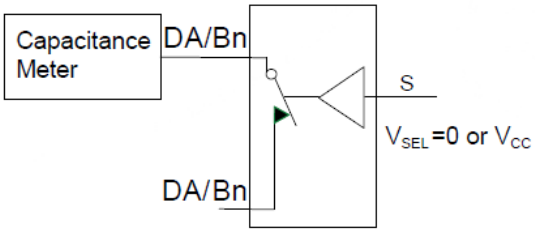


Figure 11. Channel On Capacitance

TEST DIAGRAMS(CONTINUED)

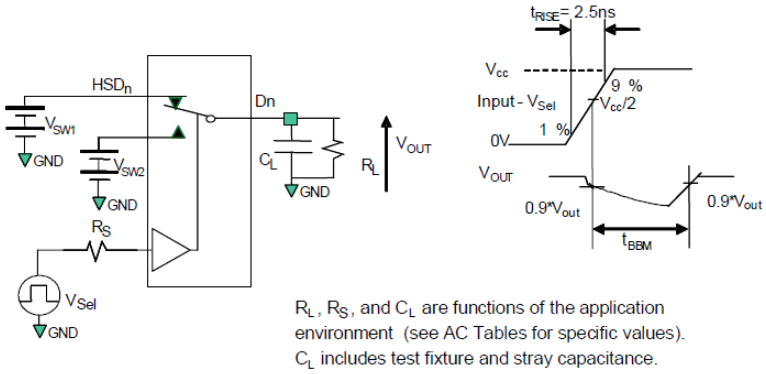
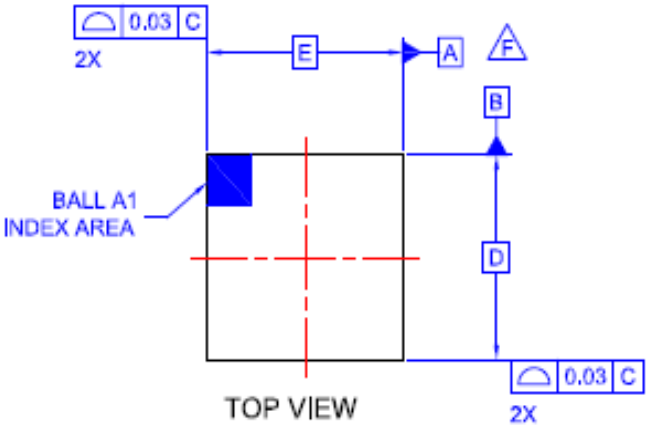
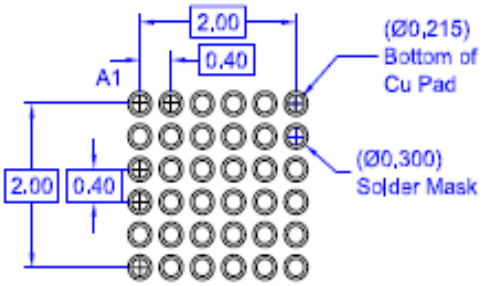


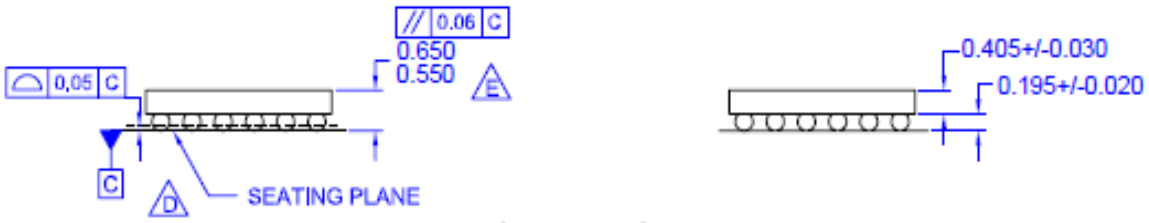
Figure 12. Break-Before-Make Interval Timing

PACKAGE OUTLINE DIMENSIONS

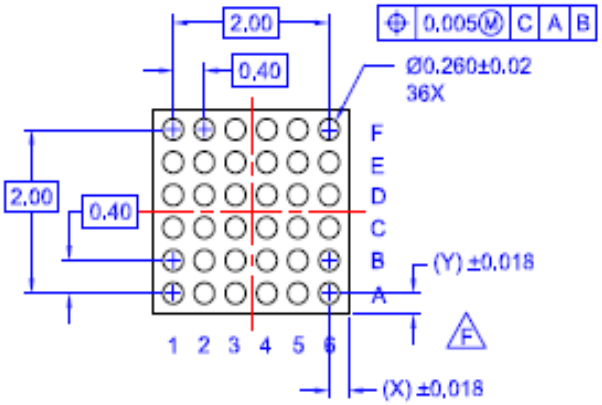




RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14,5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 495 ± 39 MICRONS (456-534 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC036AB REV1.

Product	Package	D	E	X	Y
BCT644BEWX-TR	36-Ball WLCSP, 2.375mm x 2.375 mm, 0.4mm Pitch	2.375mm	2.375mm	0.18mm	0.18mm