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November 2013

FDL100N50F

N-Channel UniFETTM FRFET[®] MOSFET 500 V, 100 A, 55 m Ω

Features

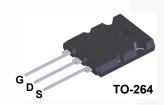
- $R_{DS(on)}$ = 43 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 50 A
- Low Gate Charge (Typ. 238 nC)
- Low C_{rss} (Typ. 64 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability
- · RoHS Compliant

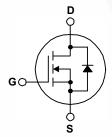
Applications

- · Uninterruptible Power Supply
- · AC-DC Power Supply

Description

UniFETTM MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





MOSFET Maximum Ratings $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol		Parameter		FDL100N50F	Unit
V_{DSS}	Drain to Source Voltage	Drain to Source Voltage		500	V
V_{GSS}	Gate to Source Voltage	Gate to Source Voltage		±30	V
	- Continuous (T _C = 25°C)			100	А
ID	Drain Current	- Continuous (T _C = 100°C)		60	_ A
I _{DM}	Drain Current	Drain Current - Pulsed (Note 1)		400	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		(Note 2)	5000	mJ
I _{AR}	Avalanche Current (Note 1)		(Note 1)	100	Α
E _{AR}	Repetitive Avalanche Ener	Repetitive Avalanche Energy (Note 1)		73.5	mJ
dv/dt	Peak Diode Recovery dv/d	t	(Note 3)	20	V/ns
Б	$(T_C = 25^{\circ}C)$			2500	W
P_{D}	Power Dissipation - Derate Above 25°C			20	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T _L	Maximum Lead Temperatu	re for Soldering, 1/8" from Case for 5 So	econds	300	οС

Thermal Characteristics

Symbol	Parameter	FDL100N50F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.05	°C/W
$R_{\theta,JA}$	Thermal Resistance, Junction to Ambient, Max.	30	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDL100N50F	FDL100N50F	TO-264	Tube	N/A	N/A	25 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_C = 25^{\circ}C$	500	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.5	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	10	μA
IDSS Zero Gate voltage Drain Current	$V_{DS} = 400 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	100	μΑ	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 50 A	-	0.043	0.055	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 50 A	-	95	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 25 V V - 0 V		-	12000	-	pF
C _{oss}	Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		-	1700	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12		-	64	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DD} = 400 V, I _D = 50 A,		-	238	-	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V		-	74	-	nC
Q_{qd}	Gate to Drain "Miller" Charge		(Note 4)	-	95	-	nC

Switching Characteristics

_						
$t_{d(on)}$	Turn-On Delay Time	V _{DD} = 250 V, I _D = 50 A,	-	63	-	ns
t _r		$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	186	-	ns
t _{d(off)}	Turn-Off Delay Time		- /	202	-	ns
t _f	Turn-Off Fall Time	(Note 4)	- /	105	-	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode	Maximum Continuous Drain to Source Diode Forward Current		-	100	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	400	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 100 A	-	-	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 100 A	-	250	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.5	-	uC

Notes

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 1 mH, I_{AS} = 100 A, V_{DD} = 50 V, R_{G} = 25 Ω , starting T_{J} = 25°C.
- 3. I $_{SD}$ \leq 100 A, di/dt \leq 200 A/ $\mu s,~V_{DD}$ \leq BV $_{DSS},$ starting T $_{J}$ = 25°C.
- Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

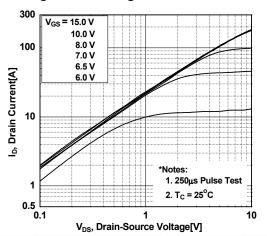


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

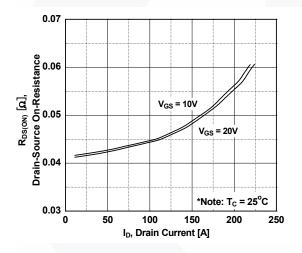


Figure 5. Capacitance Characteristics

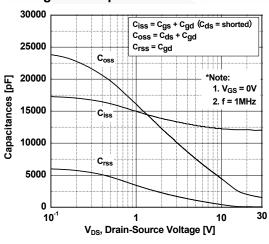


Figure 2. Transfer Characteristics

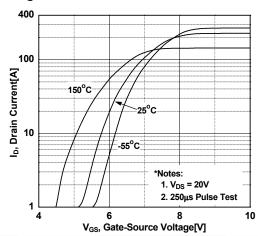


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

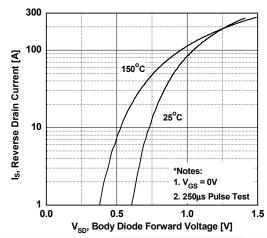
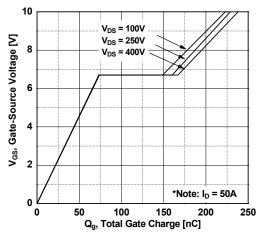


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

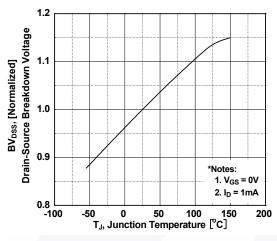


Figure 9. Maximum Safe Operating Area

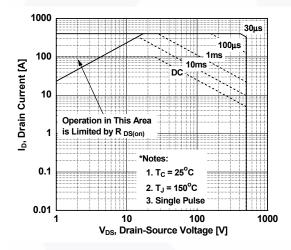


Figure 8. On-Resistance Variation vs. Temperature

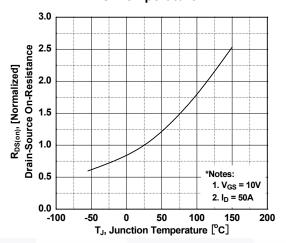


Figure 10. Maximum Drain Current vs. Case Temperature

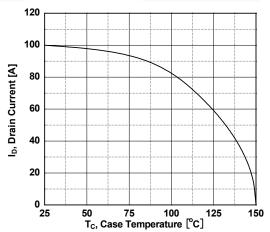
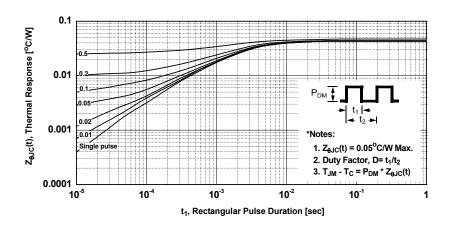


Figure 11. Transient Thermal Response Curve



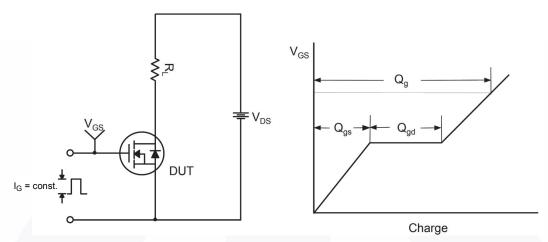


Figure 12. Gate Charge Test Circuit & Waveform

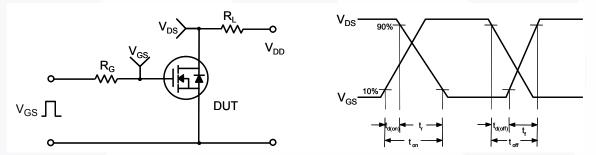


Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

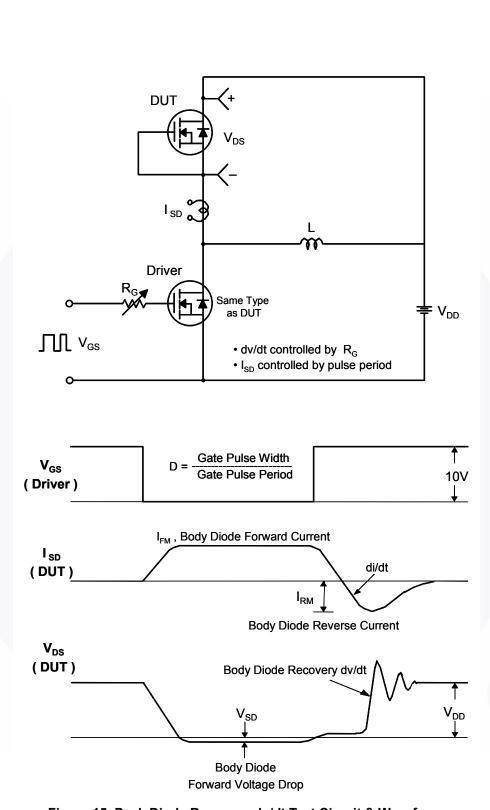
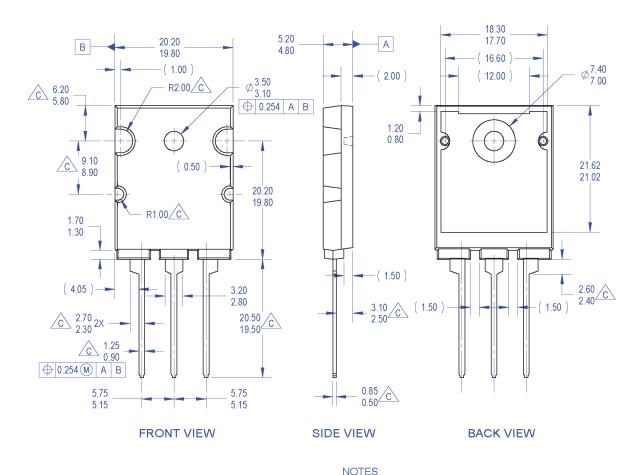
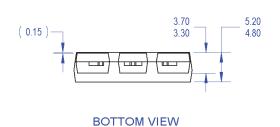


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions





- - A. PACKAGE REFERENCE: JEDEC TO264 VARIATION AA. B. ALL DIMENSIONS ARE IN MILLIMETERS.
- OUT OF JEDEC STANDARD VALUE.
 DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- DIMENSIONS ARE EXCLUSIVE OF BURRS
- MOLD FLASH AND TIE BAR PROTRUSIONS. THIS PACKAGE IS INTENDED ONLY FOR
- "FS PKG CODE AR"
- G. DRAWING FILE NAME: TO264A03REV1

Figure 16. TO264, Molded, 3-Lead, Jedec Variation AA

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