40V N-Channel MOSFET

PRODUCT SUMMARY

V_{DS}	40V
I_D (at V_{GS}=10V)	40A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 5.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 7mΩ

100% UIS Tested
100% R_g Tested

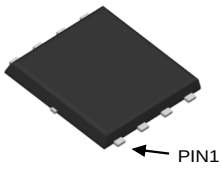
- Trench Power αMOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

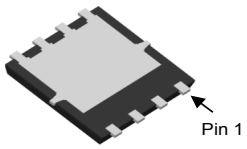
- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

PDFN5X6-8L

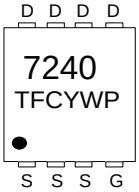
Top View



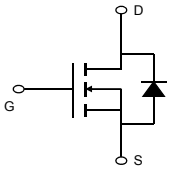
Bottom View



Top View



Equivalent Circuit



Y :year code W :week code

Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25℃	I_D	40	A
Pulsed Drain Current [C]		I_{DM}	144	
Continuous Drain Current	T_A=25℃	I_{DSM}	19	A
Avalanche Current [C]		I_{AS}, I_{AR}	40	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	80	mJ
Power Dissipation [B]	T_C=25℃	P_D	36.7	W
Power Dissipation [A]	T_A=25℃	P_{DSM}	3.1	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	75	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.8	3.4	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.4	1.9	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	144			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		4.2	5.5	mΩ
		V_{GS}=4.5V, I_D=15A		5.6	7	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		67		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current [G]				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz	1460	1830	2200	pF
C_{oss}	Output Capacitance		365	521	680	pF
C_{rss}	Reverse Transfer Capacitance		20	43	73	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=20A	22	27.8	35	nC
Q_g(4.5V)	Total Gate Charge		10	12.8	15	nC
Q_{gs}	Gate Source Charge		3	3.9	5	nC
Q_{gd}	Gate Drain Charge		2	6	10	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1Ω, R_{GEN}=3Ω		7.2		ns
t_r	Turn-On Rise Time			3		ns
$t_{D(off)}$	Turn-Off DelayTime			23		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs	11	16.5	21	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs	28	40	52	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design, and the maximum temperature of 150℃ may be u sed if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T_J =25℃.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

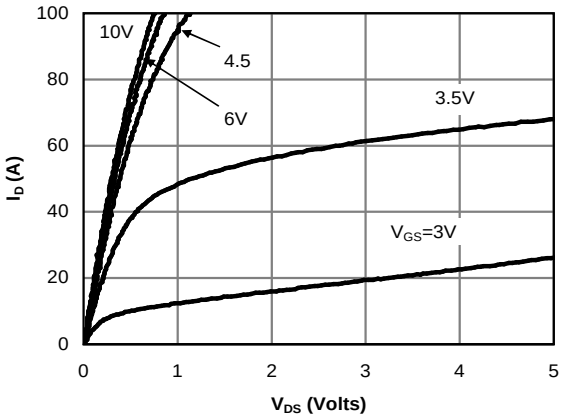


Fig 1: On-Region Characteristics (Note E)

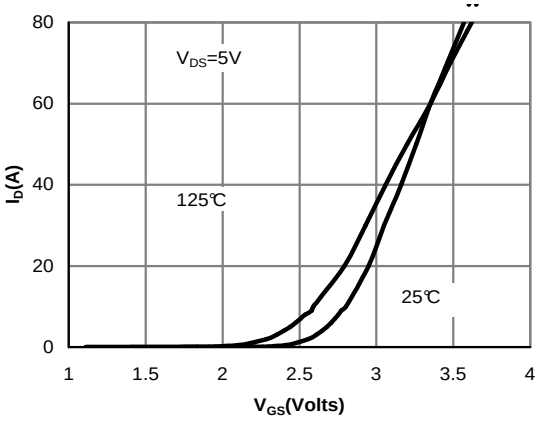


Figure 2: Transfer Characteristics (Note E)

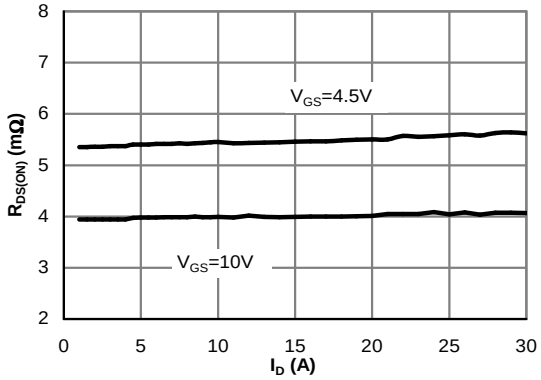


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

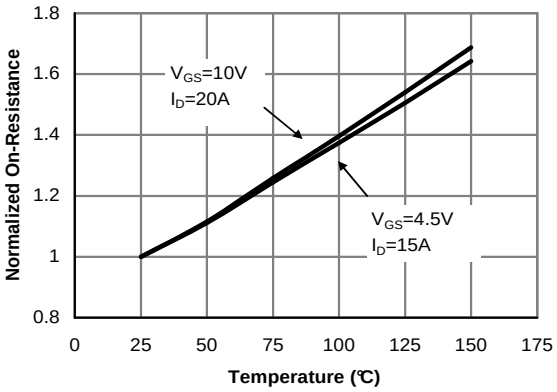


Figure 4: On-Resistance vs. Junction Temperature (Note E)

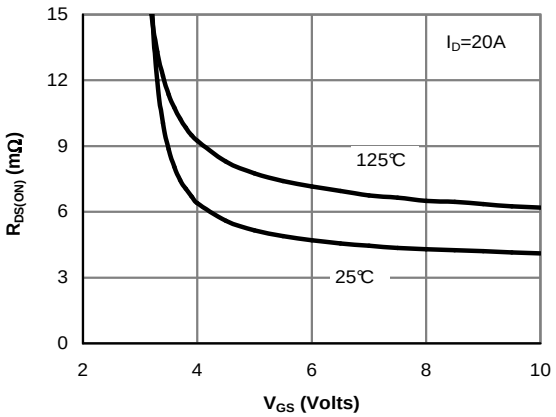


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

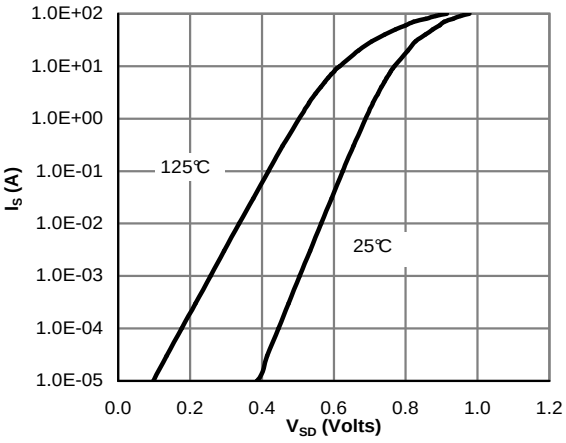


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

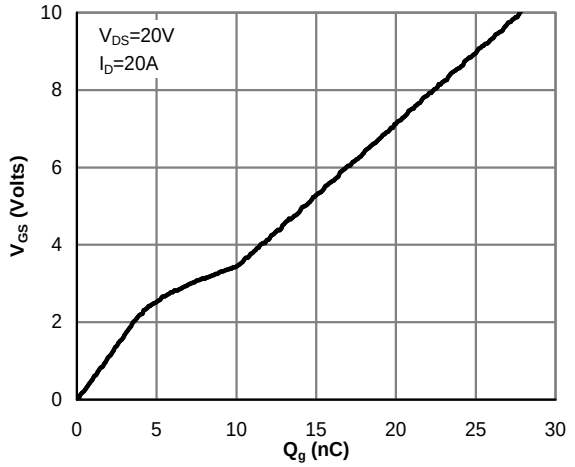


Figure 7: Gate-Charge Characteristics

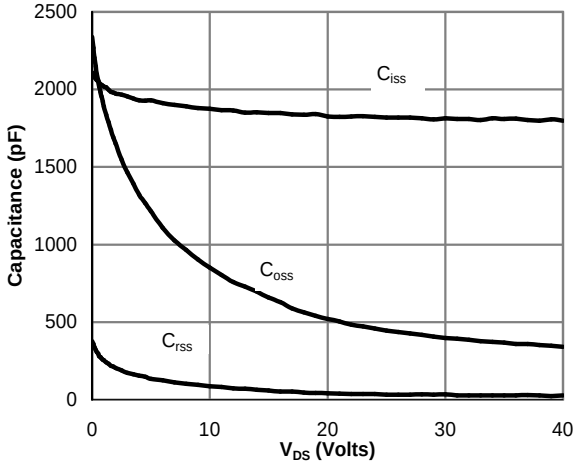


Figure 8: Capacitance Characteristics

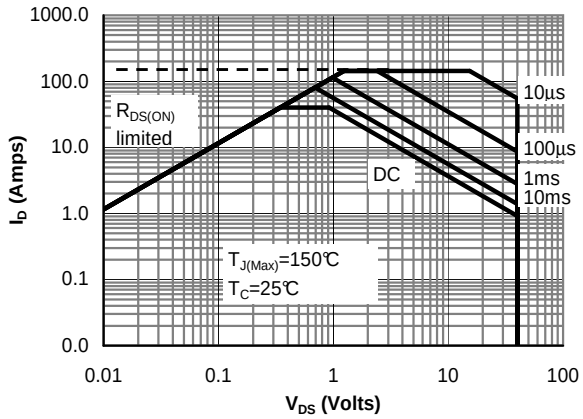


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

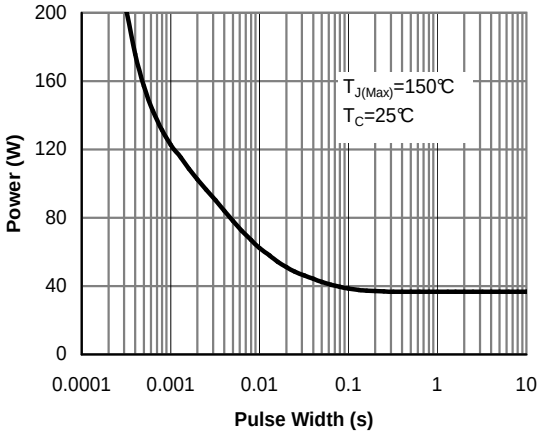


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

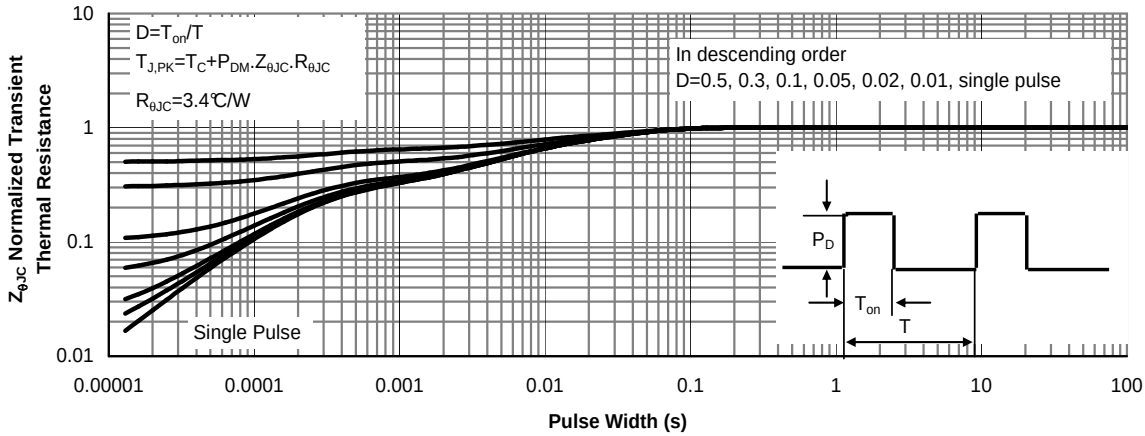


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

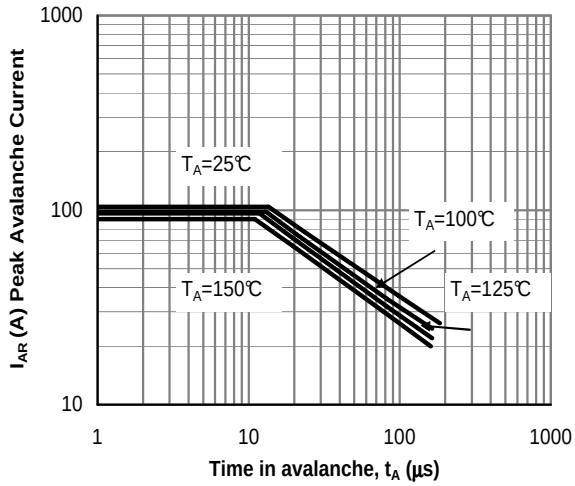


Figure 12: Single Pulse Avalanche capability (Note C)

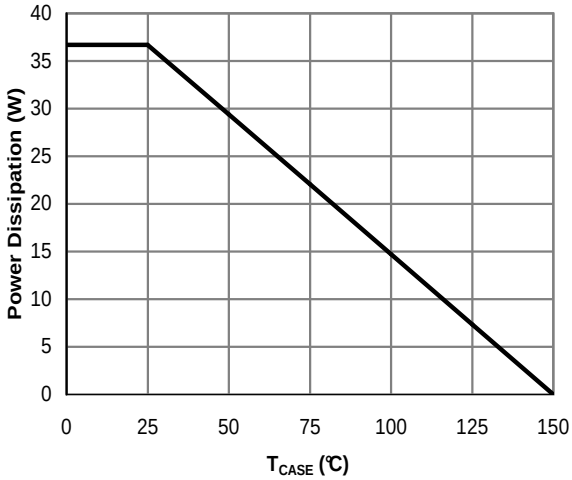


Figure 13: Power De-rating (Note F)

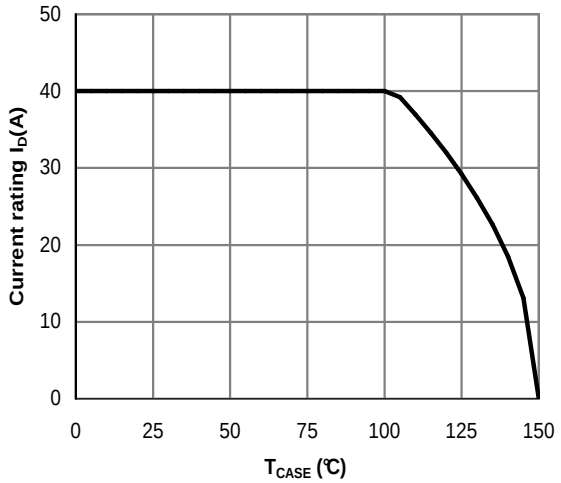


Figure 14: Current De-rating (Note F)

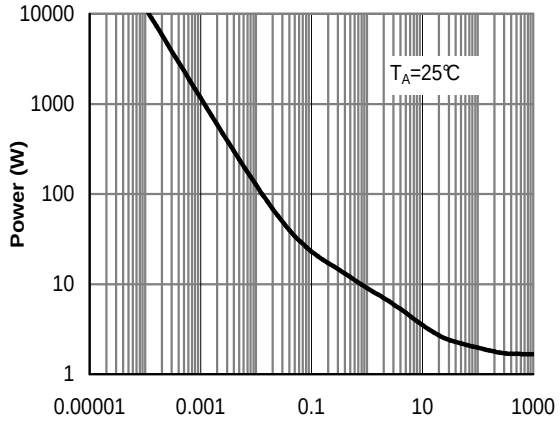


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

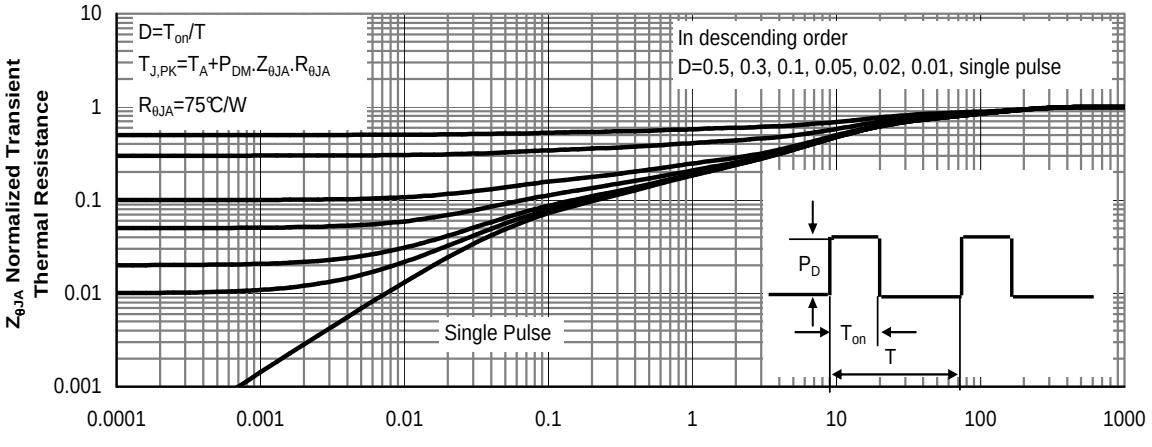
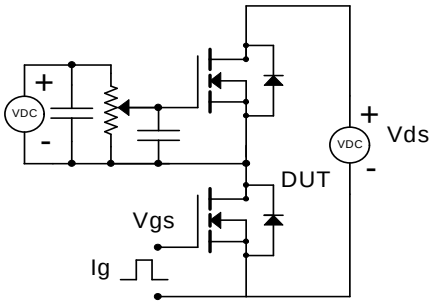
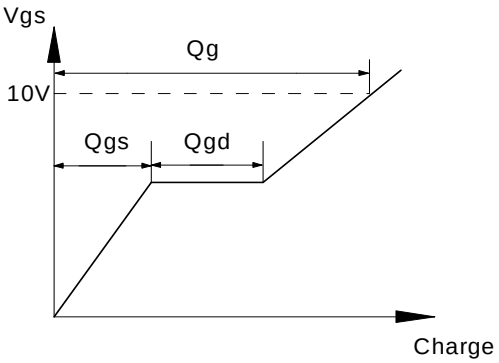


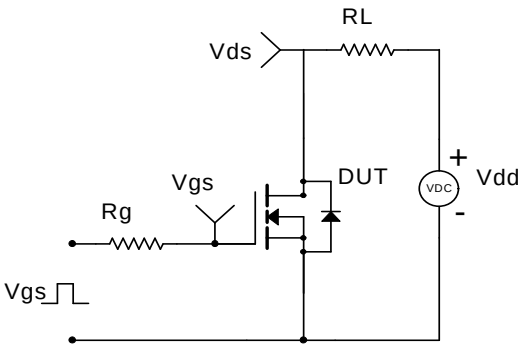
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

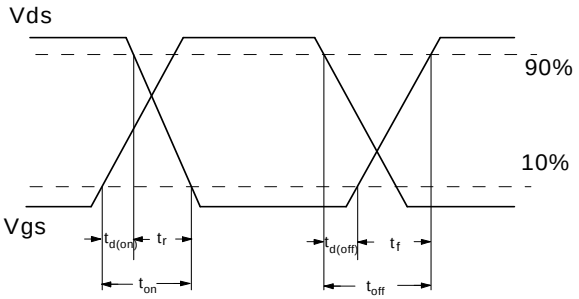
Gate Charge Test Circuit & Waveform



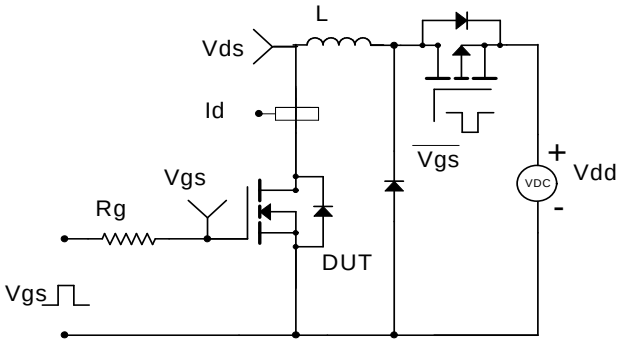


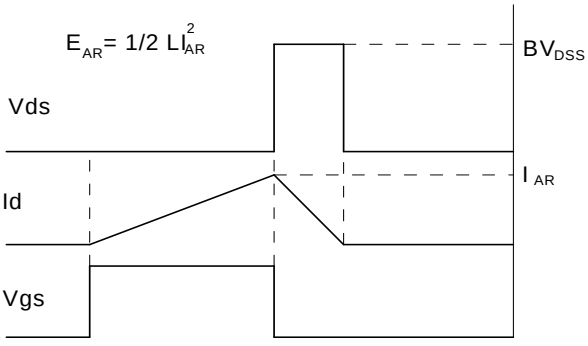
Resistive Switching Test Circuit & Waveforms



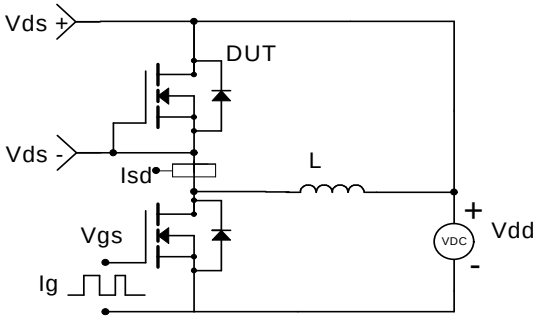


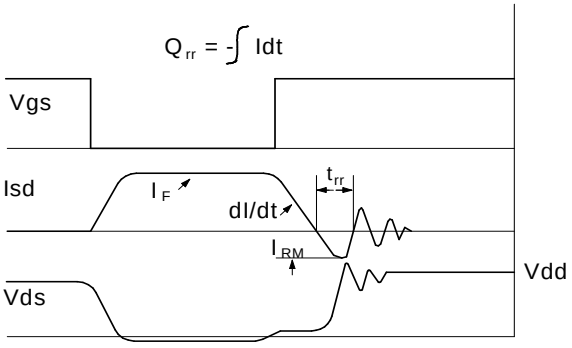
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



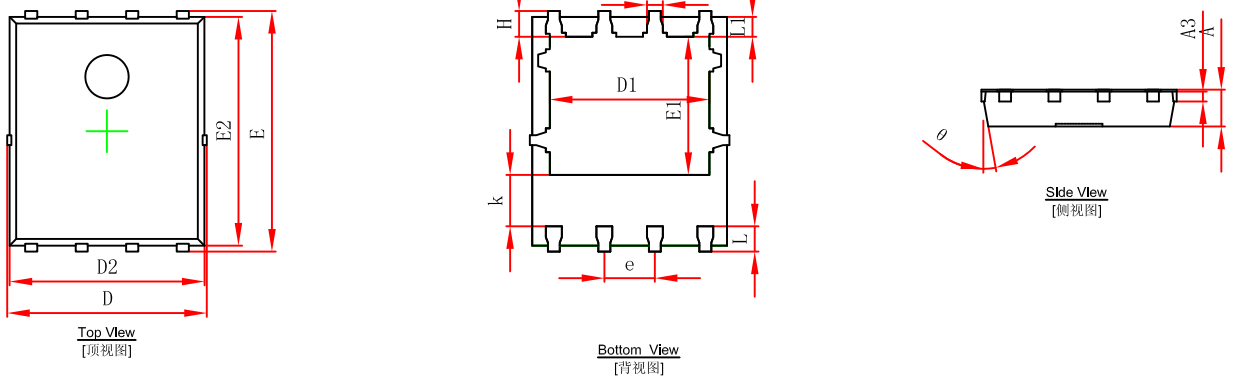


Diode Recovery Test Circuit & Waveforms



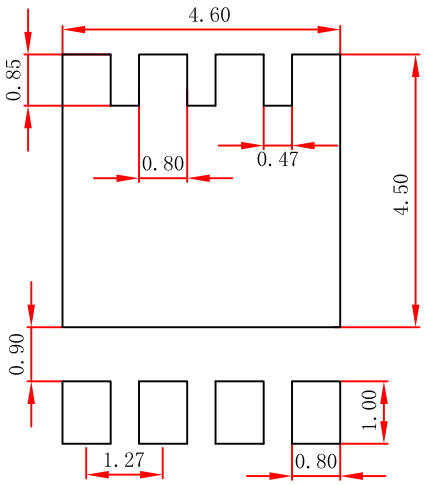


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.