

28V N-Channel MOSFET

PRODUCT SUMMARY

$V_{DS} (V) = 28V$
 $I_D = 12A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 9.9m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 14m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested
100% R_g Tested

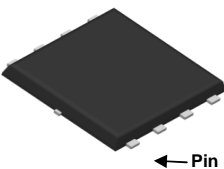
- Trench Power α MOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

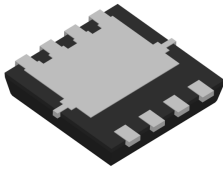
- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

DFN 3x3_EP

Top View

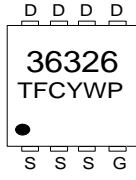


Bottom View



← Pin 1

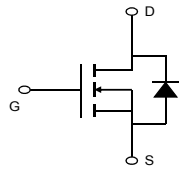
Top View



36326
TFCYW P

S S S G

Equivalent Circuit



Y :year code W :week code

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
36326	36326	PDFN3x3-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	28	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	12	A
Pulsed Drain Current ^C	I_{DM}	36	
Continuous Drain Current ^A	I_{DSM}	12	A
Avalanche Current ^C	I_{AR}	10	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	7	mJ
Power Dissipation ^B	P_D	19	W
Power Dissipation ^A	P_{DSM}	3.1	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	40	$^\circ C/W$
Maximum Junction-to-Ambient ^A		60	75	$^\circ C/W$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	4.5	5.4	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	28			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =25V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±12V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.50	0.85	1.20	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	80			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A		8.5	9.9	mΩ
		V _{GS} =4.5V, I _D =10A		10	14	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =12A		45		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		688		pF
C _{oss}	Output Capacitance			305		pF
C _{rss}	Reverse Transfer Capacitance			24		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =12A		12		nC
Q _g (4.5V)	Total Gate Charge			5.5		nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.3		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.25Ω, R _{GEN} =3Ω		3.5		ns
t _r	Turn-On Rise Time			3.0		ns
t _{D(off)}	Turn-Off DelayTime			15		ns
t _f	Turn-Off Fall Time			3.0		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, di/dt=500A/μs	5.6	7	8	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =12A, di/dt=500A/μs	6.4	8	9.6	nC

A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

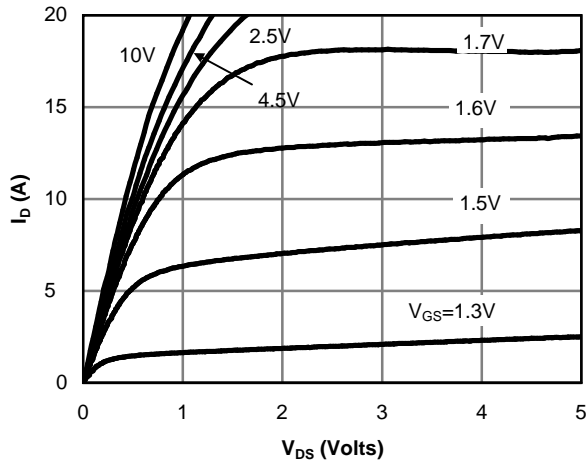


Fig 1: On-Region Characteristics

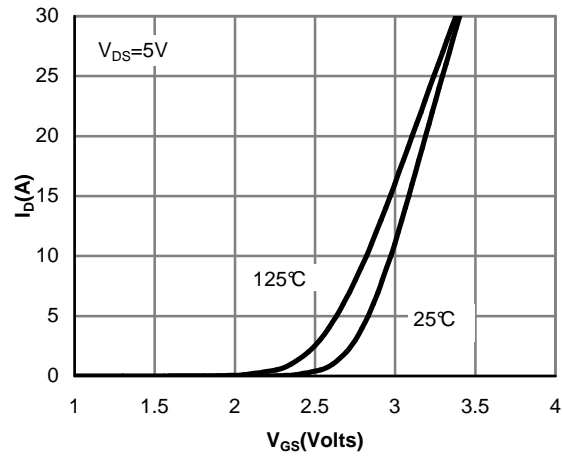


Figure 2: Transfer Characteristics

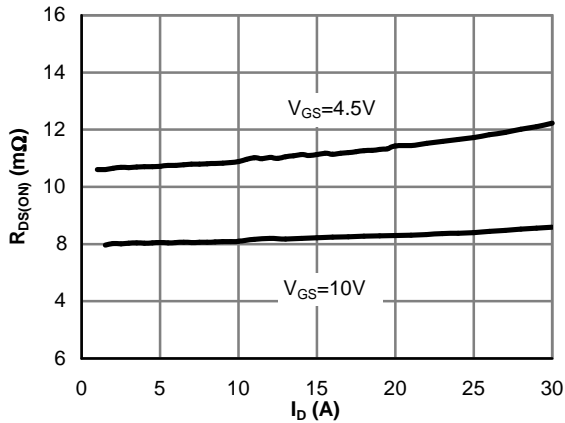


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

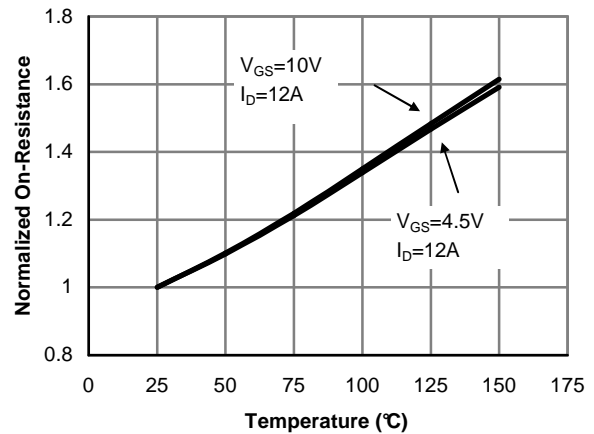


Figure 4: On-Resistance vs. Junction Temperature

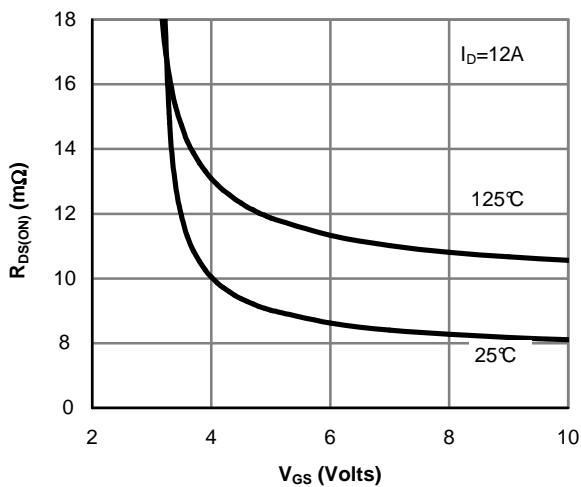


Figure 5: On-Resistance vs. Gate-Source Voltage

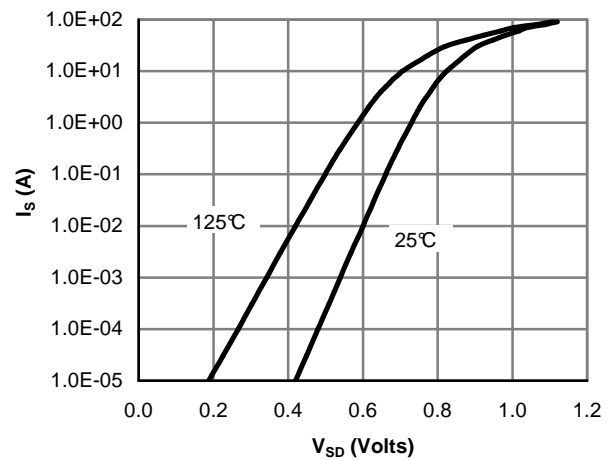


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

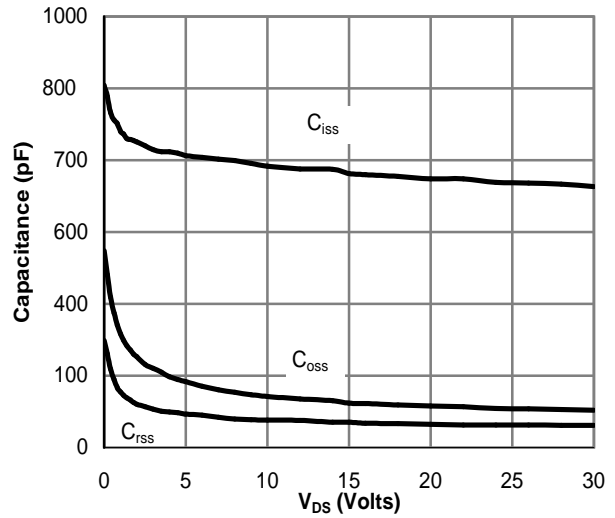
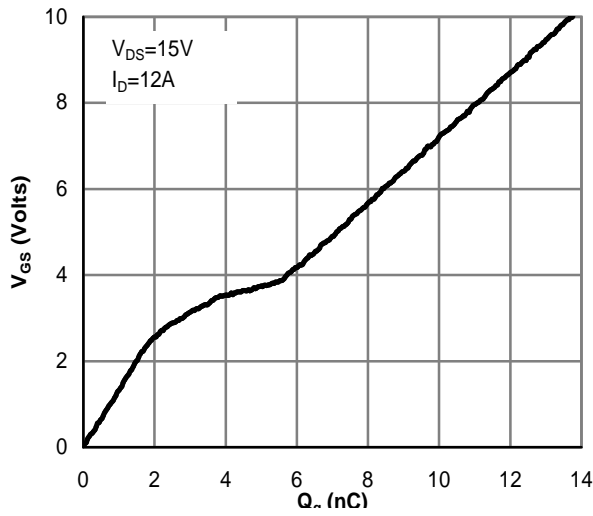


Figure 8: Capacitance Characteristics

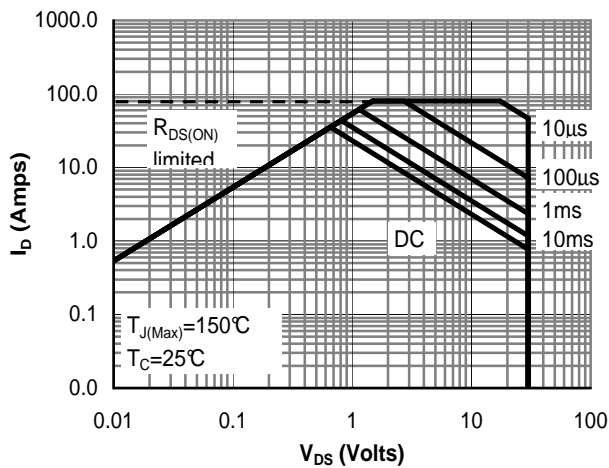


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

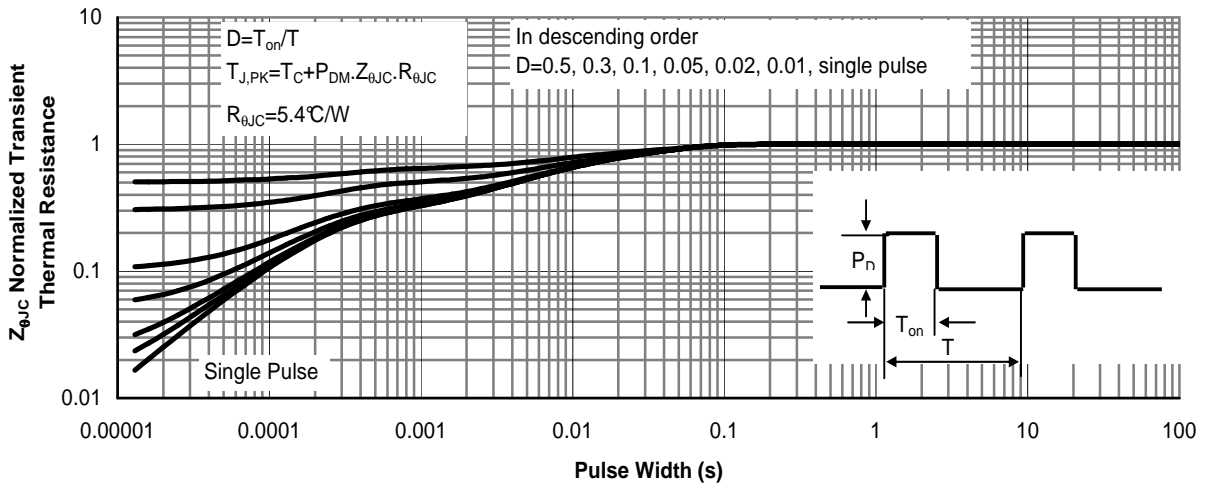
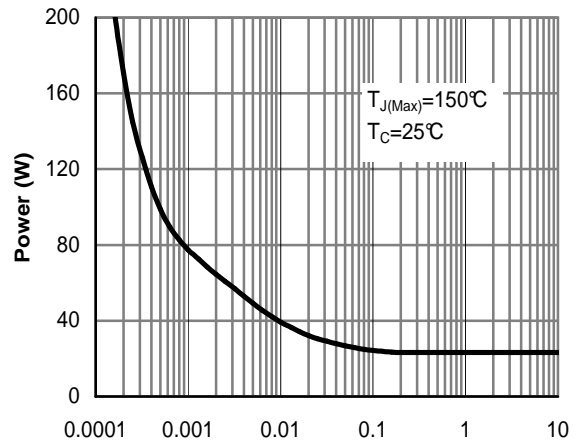


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

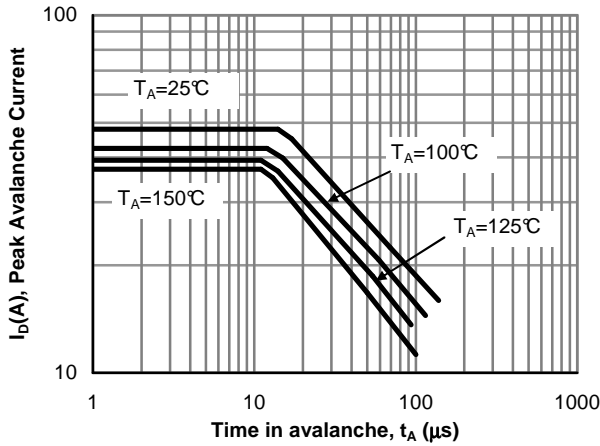


Figure 12: Single Pulse Avalanche capability (Note C)

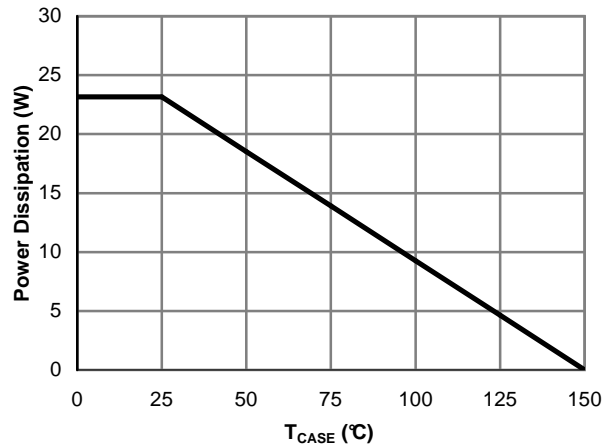


Figure 13: Power De-rating (Note F)

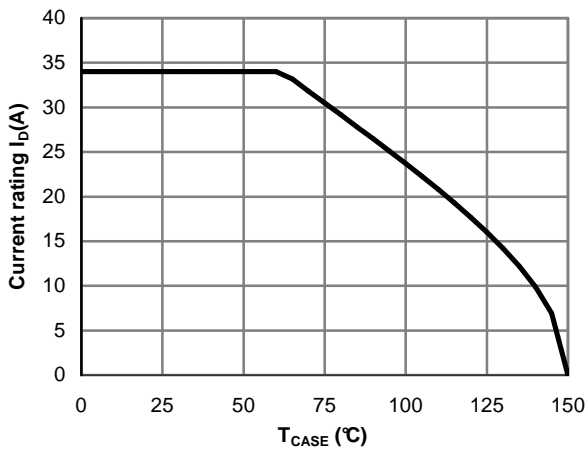


Figure 14: Current De-rating (Note F)

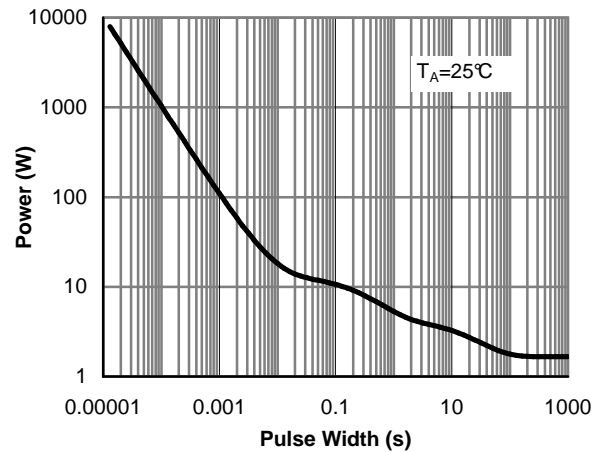


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

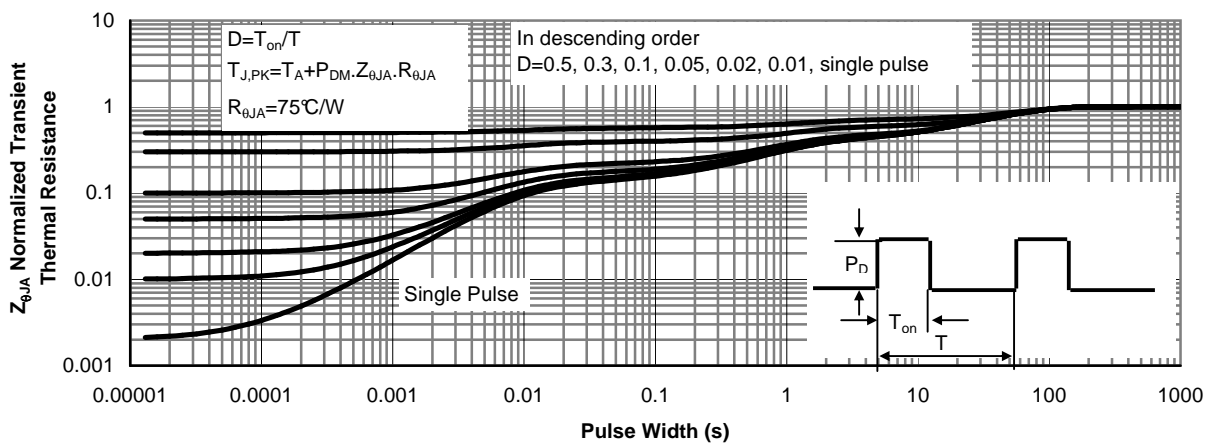
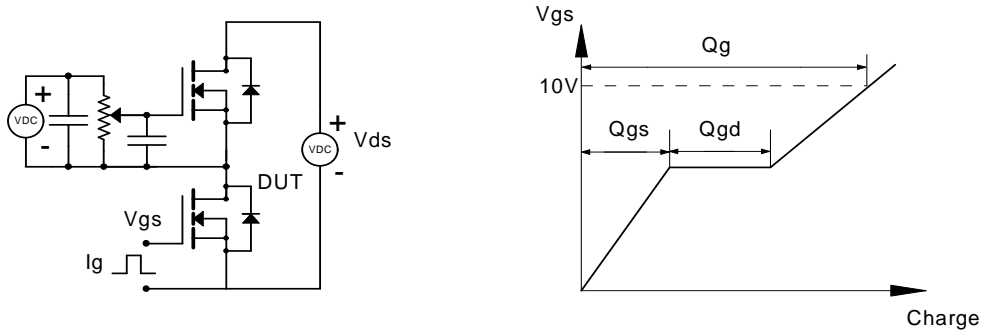
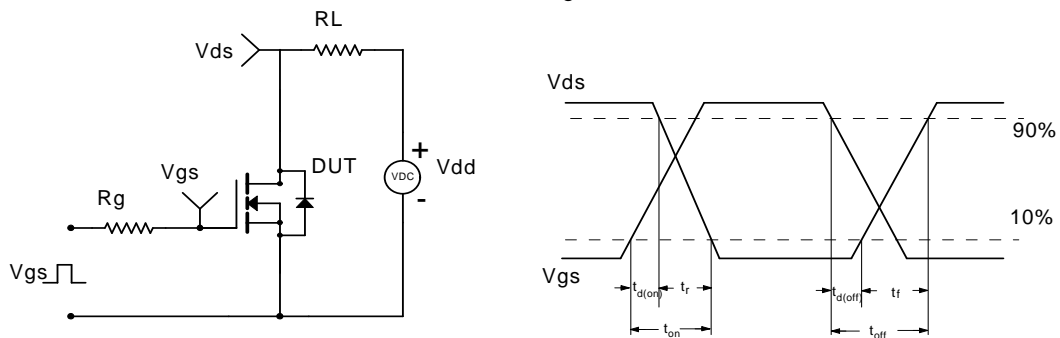


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

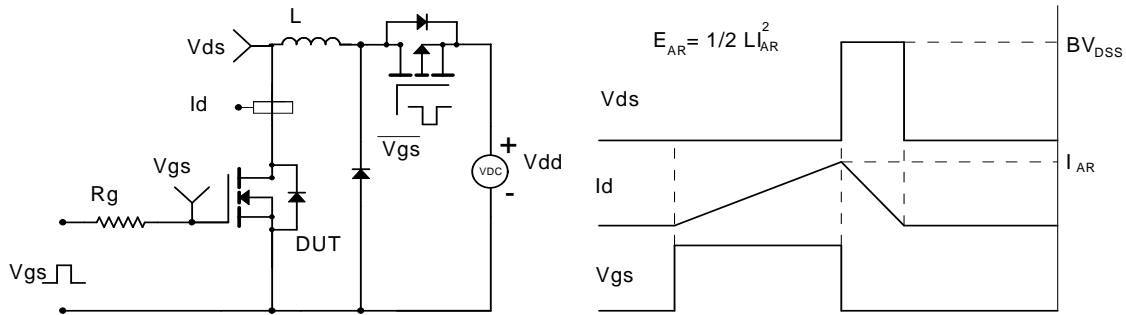
Gate Charge Test Circuit & Waveform



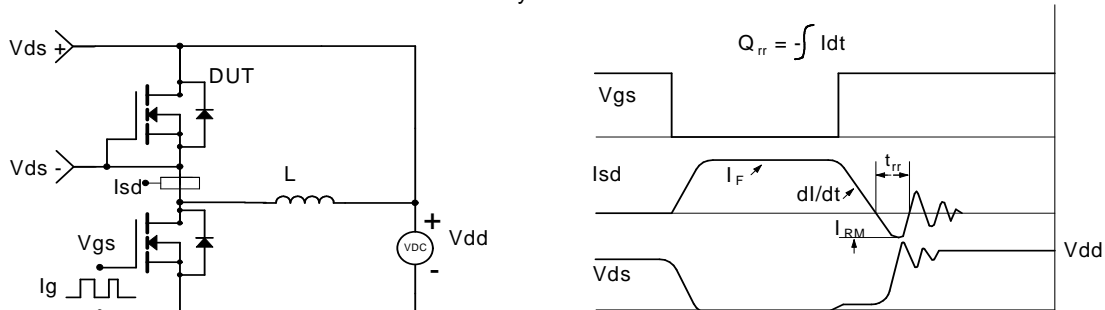
Resistive Switching Test Circuit & Waveforms



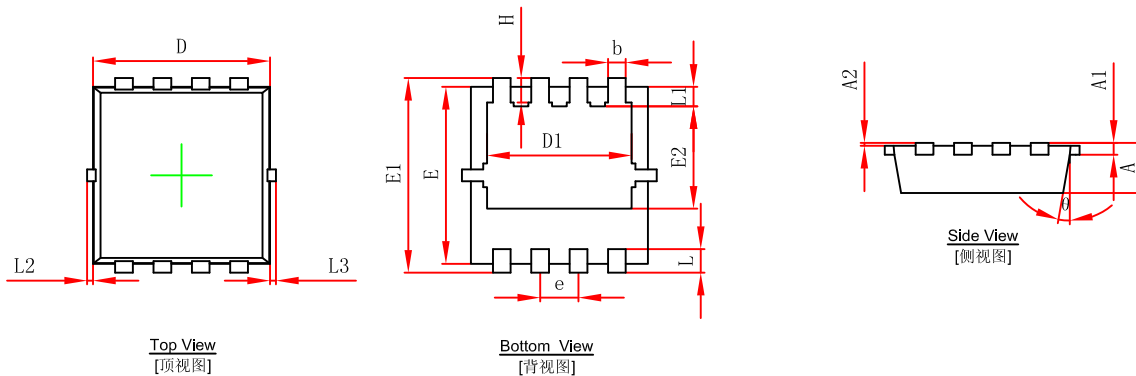
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

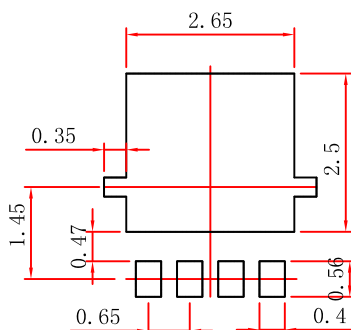


PDFNWB3.3x3.3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.05 mm.
 3. The pad layout is for reference purposes only.