

N-Channel Enhancement Mode Power MOSFET

**Description**

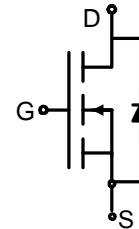
The 30115 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V.

**General Features**

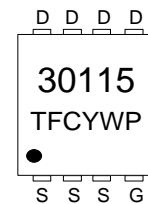
- $V_{DS} = 30V, I_D = 115A$
- $R_{DS(ON)} < 6.0m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} < 4.0m\Omega @ V_{GS}=10V$
- High power and current handing capability
- Lead free product is acquired
- Surface mount package

**Application**

- Battery Switch
- Load switch
- Power management

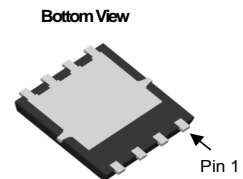
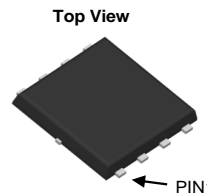


Schematic diagram



Y : year code W : week code

Pin assignment



PDFN5X6-8L

**Absolute Maximum Ratings ( $T_A=25^\circ C$  unless otherwise noted)**

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_J = 150^\circ C$ )	$T_A = 25^\circ C$	$I_D$	115	A
	$T_A = 70^\circ C$		25	
Drain Current-Pulsed (Note 1)		$I_{DM}$	180	A
Maximum Power Dissipation		$P_D$	60	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	2.0	$^\circ C/W$
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**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.7	2.0	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	2.8	4.0	mΩ
		V <sub>GS</sub> =5V, I <sub>D</sub> =20A	-	4.7	6.0	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	20	-	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	2225	-	PF
Output Capacitance	C <sub>oss</sub>		-	986	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	100	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, I <sub>D</sub> =20A V <sub>GS</sub> =10V, R <sub>GEN</sub> =3.0Ω	-	15	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	5	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	35	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	9	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	6.0	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	5.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	29.5	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	115	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs (Note 3)	-	24	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	30	-	uC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=15V, V<sub>G</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω

Figure 1 Output Characteristics

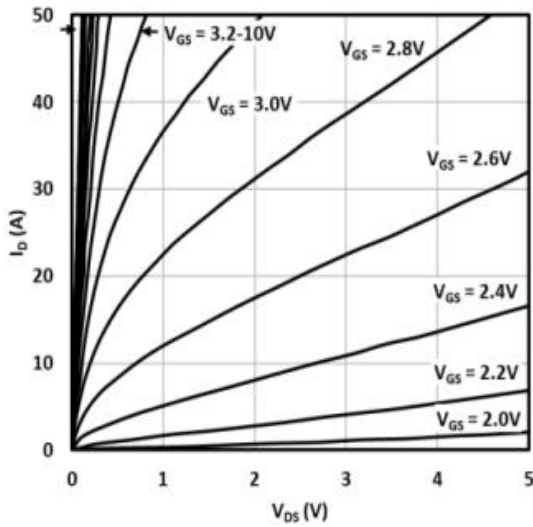


Figure 2 Transfer Characteristics

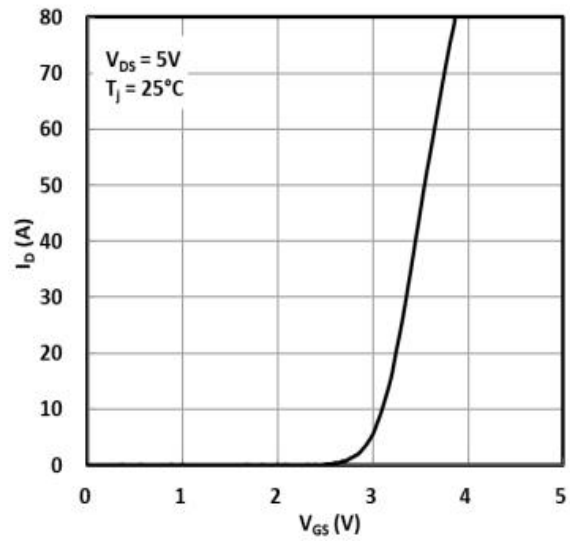


Figure 3 On-resistance vs.gate voltage

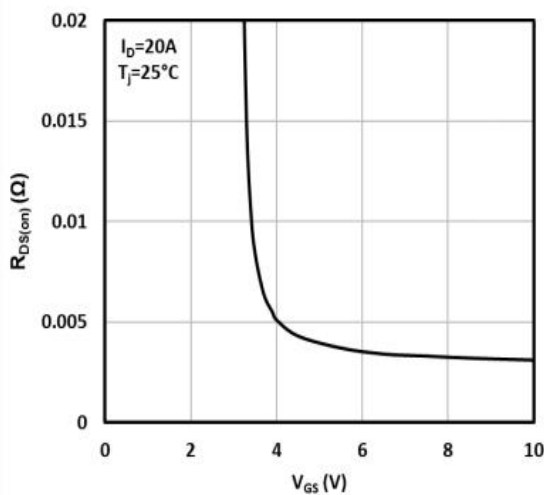


Figure 4 On-resistance vs.drain current

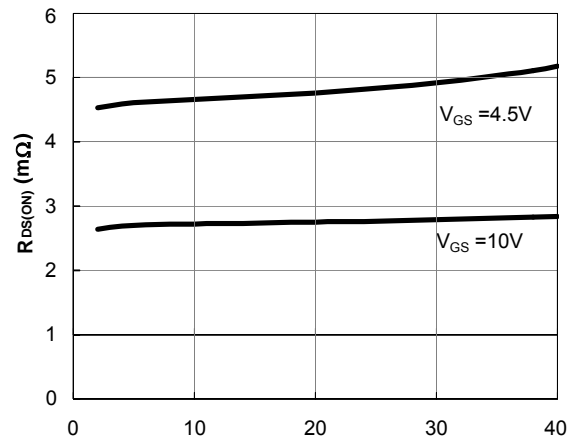


Figure 5 Source-to-drain diode forward characteristics

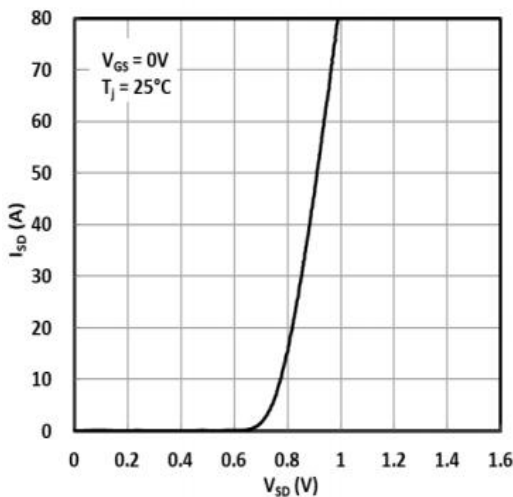


Figure 6 Capacitance vs drain-to-source Voltage

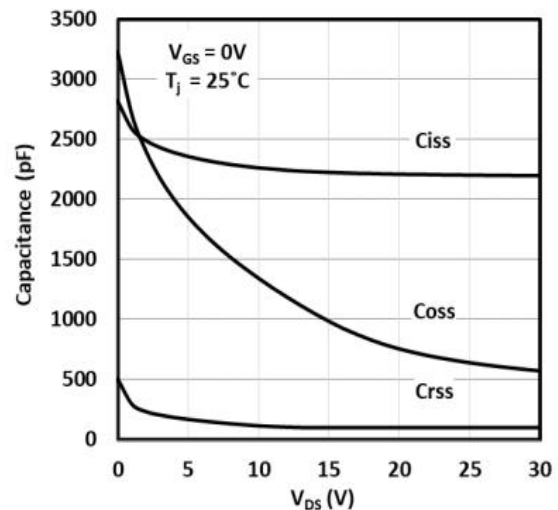


Figure 7 Gate-to-source voltage vs.gate charge

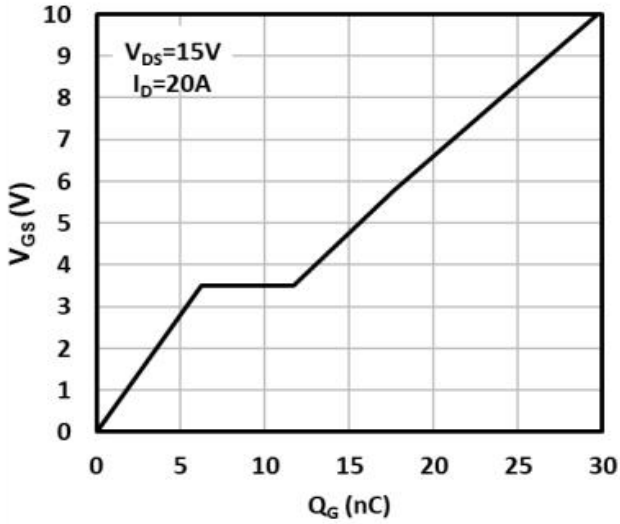


Figure 8 Maximum drain current vs.case temperature

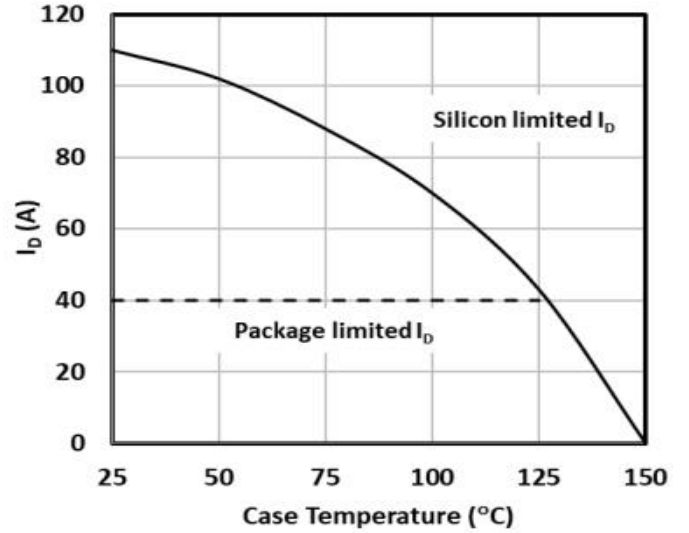
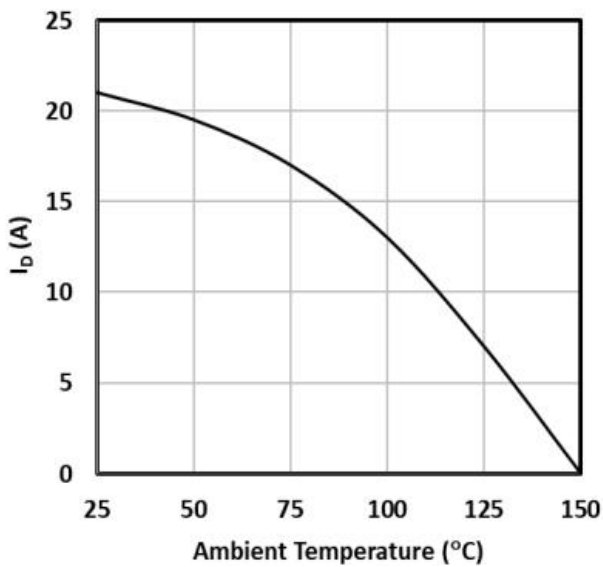
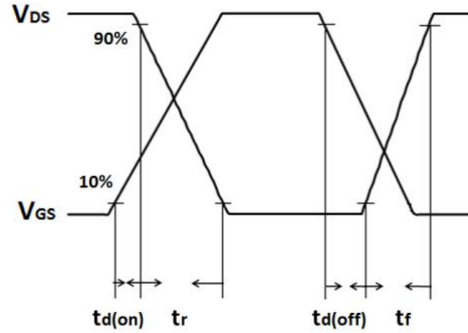
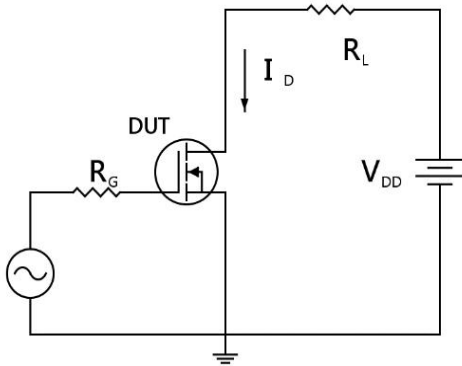


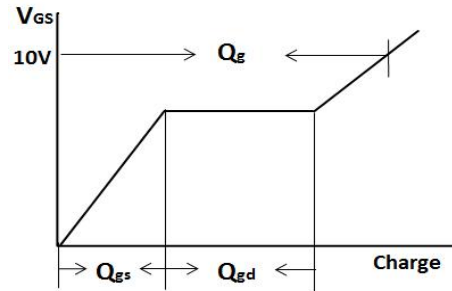
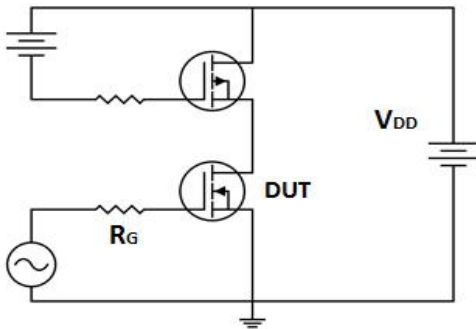
Figure 9 Maximum drain current vs. ambient temperature



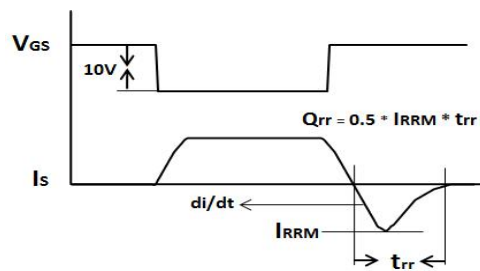
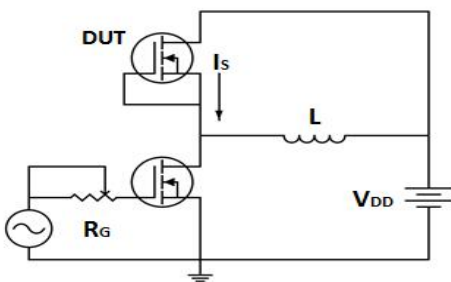
Resistive switching time test circuit & waveforms



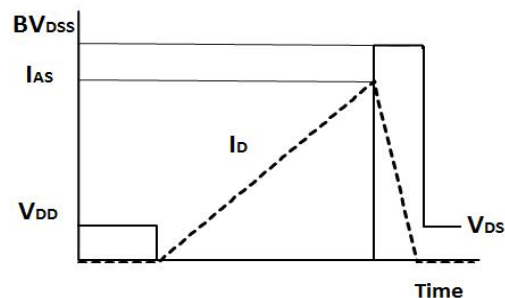
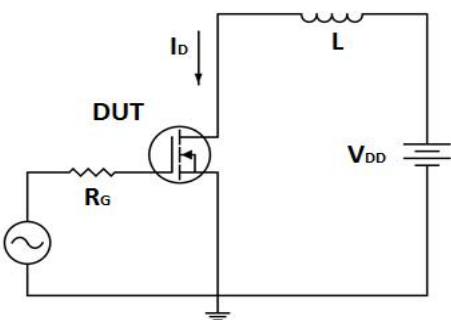
Gate charge test circuit & waveforms



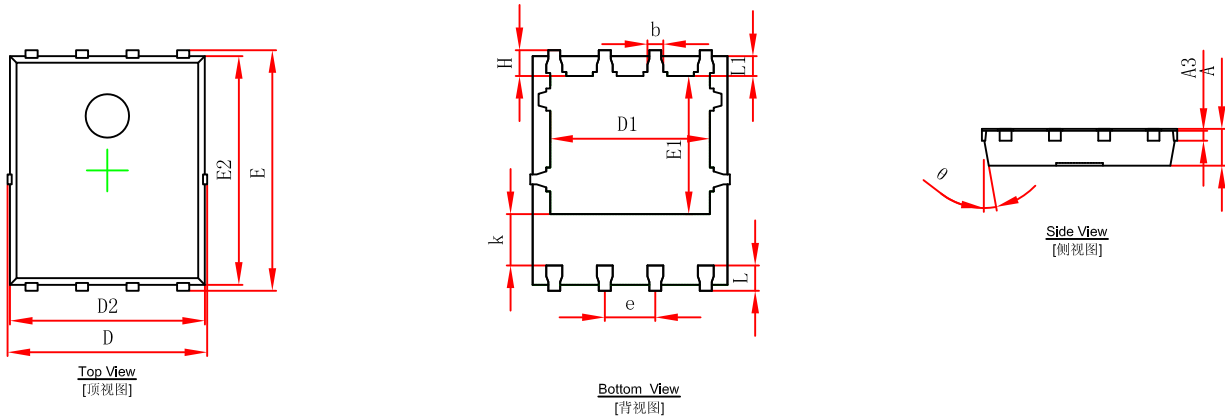
Peak diode recovery dv/dt circuit & waveforms



Unclamped inductive switching test circuit & waveforms

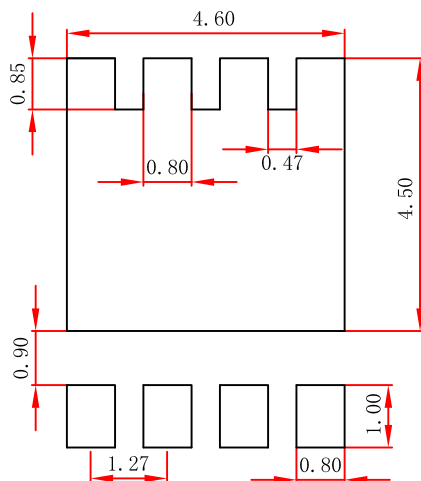


PDFNWB5x6-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

PDFNWB5x6-8L Suggested Pad Layout



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance: ±0.05mm.  
 3. The pad layout is for reference purposes only.