178ball FBGASpecification

16Gb LPDDR3 (x32)

Document Title

FBGA
16Gb (x32) LPDDR3

Revision History

Revision No.	History	Draft Date	Remark
0.1	- Initial Draft	May. 2019	Preliminary

FEATURES

[FBGA]

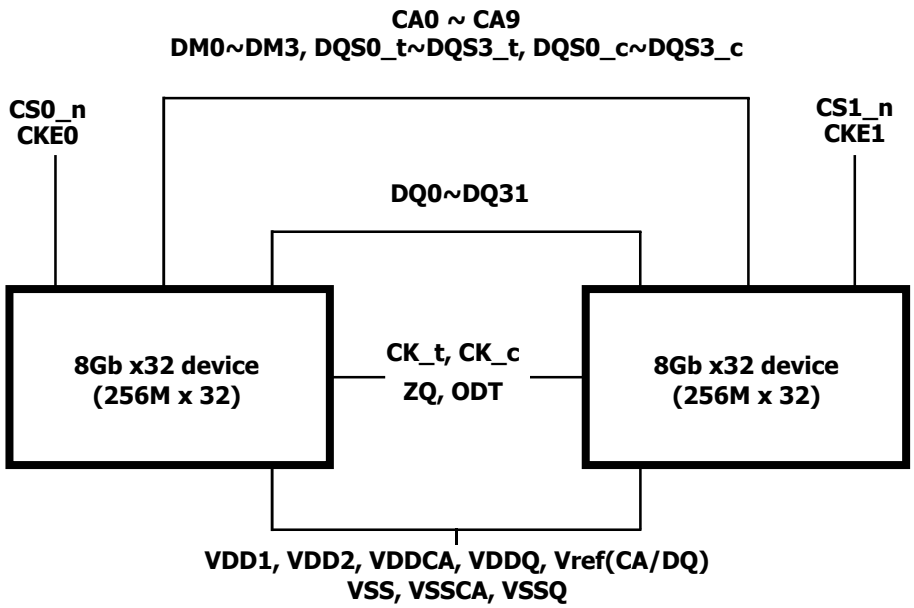
● OperationTemperature
- -25°C ~85°C

● Package
- 178-ballFBGA
- 11.0x11.5mm^2, 1.00t, 0.65mm pitch
- Lead & HalogenFree

[LPDDR3]

- VDD1 = 1.8V (1.7V to1.95V)
- VDD2, VDDCA and VDDQ = 1.2V (1.14V to1.30)
- HSUL_12 interface (High Speed Unterminated Logic1.2V)
- Doubledataratearchitectureforcommand,addressanddataBus;
  - allcontrolandaddressexceptCS_n,CKElatchedatbothrisingandfallingedgeoftheclock
  - CS_n,CKElatchedatrisingedgeoftheclock
  - twodataaccessesperclockcycle
- Differential clock inputs (CK_t,CK_c)
- Bi-directional differential data strobe (DQS_t,DQS_c)
  - Sourcesynchronousdatatransactionalignedtobi-directionaldifferentialdatastrobe(DQS_t,DQS_c)
  - Dataoutputsalignedtotheedgeofthedatastrobe(DQS_t,DQS_c)whenREADoperation
  - Datainputsalignedtothecenterofthedatastrobe(DQS_t,DQS_c)whenWRITEoperation
- DMmaskswritedataatthebothrisingandfallingedgeofthedatastrobe
- Programmable RL (Read Latency) and WL (WriteLatency)
- Programmable burst length:8
- Auto refresh and self refreshsupported
- All bankautorefreshandperbankautorefreshsupported
- AutoTCSR(TemperatureCompensatedSelfRefresh)
- PASR(PartialArraySelfRefresh)byBankMaskandSegmentMask
- DS (DriveStrength)
- ZQ(Calibration)
- ODT (On DieTermination)

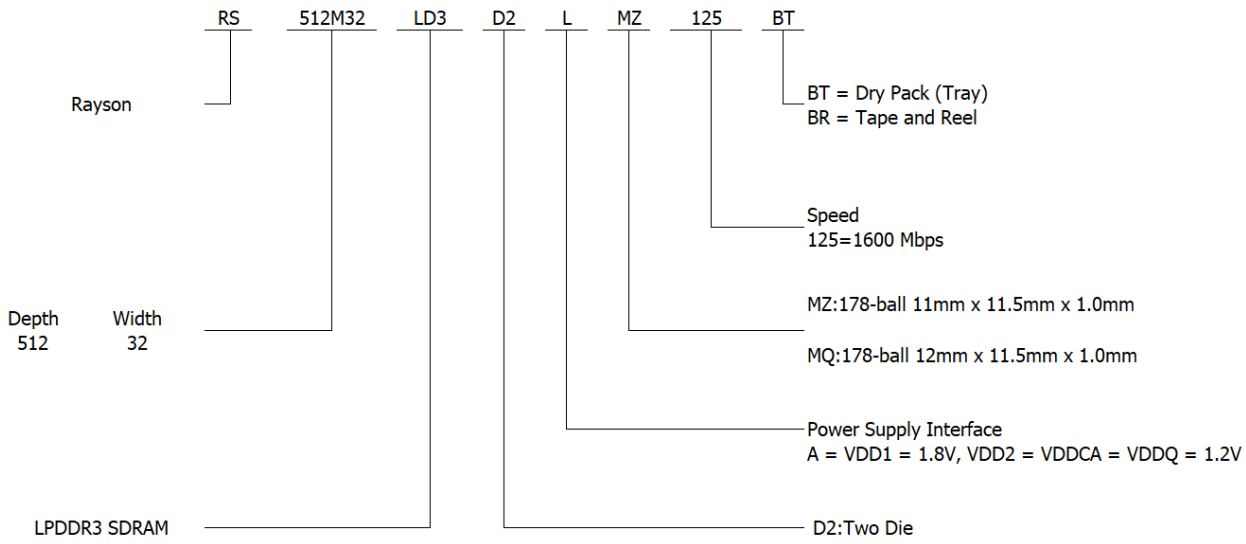
Functional Block Diagram



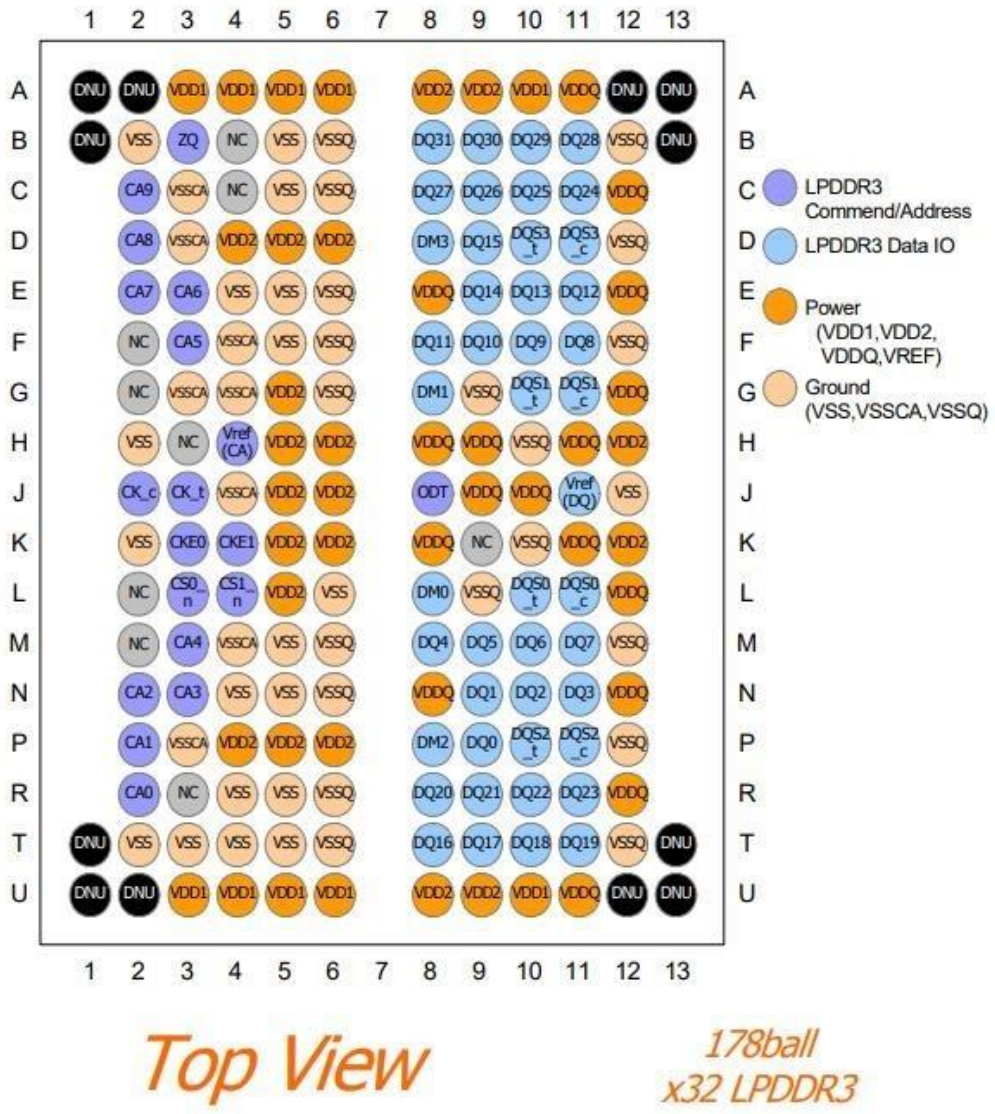
Note
1. Totalcurrentconsumptionisdependenttouseroperatingconditions.ACandDCCharacteristicsshownin thisspecificationarebasedonasingledie.Seethesectionof"DCParametersandOperatingConditions"

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
RS512M32LD3D2LMZ-125BT	LPDDR3	1.8V/1.2/1.2/1.2	16Gb(x 32)	DDR3 1600	178Ball FBGA (Lead & Halogen Free)



Ball ASSIGNMENT



Note

1.1. J8 will be used as "ODT". Users who don't use ODT Function can assign J8 as VSSQ.

2. InsidethechipVDDCAandVDD2aretied.F2,G2,H3,L2andM2arenotconnectedtothechip.Itfully guaranteesDRAMoperationeventhereisaVDDCAinputvoltage.

Pin Description

SYMBOL	DESCRIPTION	Type
CS0	Chip Select	Input
CK_c, CK_t	Differential Clocks	Input
CKE0	Clock Enable	Input
CA0 ~ CA9	Command / Address	Input
DQ0 ~ DQ31	Data I/O	Input/Output
DM0 ~ DM3	Input Data Mask	Input/Output
DQS0_t ~ DQS3_t	Differential Data Strobe (rising edge)	Input/Output
DQS0_c ~ DQS3_c	Differential Data Strobe (falling edge)	Input/Output
ZQ	Drive Strength Calibration	Input/Output
VDD1	Core Power Supply	Power
VDD2	Core Power Supply	Power
VSS	Ground	Ground
VDDQ	I/O Power Supply	Power
VDDCA	CA Power Supply	Power
VSSCA	CA Ground	Ground
VSSQ	I/O Ground	Ground
VREF	Reference Voltage	Power
ODT	On Die Termination Enable	Input

Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit
Input capacitance, CK_t and CK_c	CCK	1.5	3.0	pF
Input capacitance, all other input-only pins	CI	0.5	3.0	pF
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	2.0	3.5	pF
Input/Output Capacitance ZQ	CZQ	1.5	3.0	pF

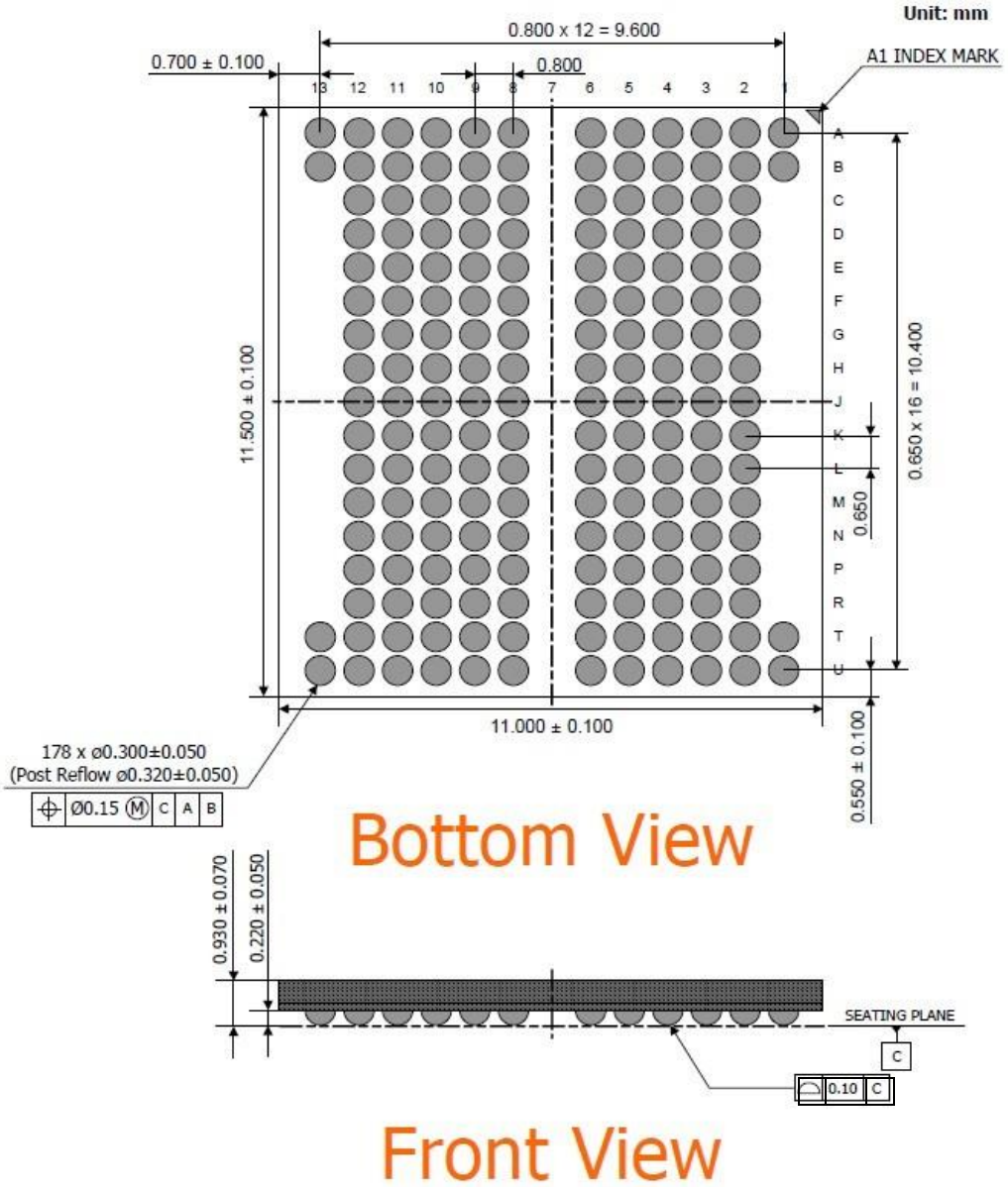
(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:

1. This parameter applies to both die andpackage.
2. Thisparameteris notsubjecttoproductiontest.It isverifiedbydesignandcharacterization.Thecapacitanceismeasured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pinsfloating).
3. CI applies to CS_n, CKE,CA0-CA9.
4. DM loading matches DQ andDQS.
5. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3Ohm typical)
6. MaximumexternalloadcapacitanceonZQ pin,includingpackaging,board,pin,resistor,andotherLPDDR3devices:5pF.

PACKAGE INFORMATION

178 Ball 0.65mm pitch 11.0mm x 11.5mm [t = 1.00mm max] FBGA



8Gb LPDDR3 SDRAM

Input/Output Functional Description

SYMBOL	TYPE	DESCRIPTION
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined bythecrosspointofarisingCK_tandafallingCK_c.ThenegativeClockedgeisdefinedby the crosspoint of a falling CK_t and a risingCK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code.CS_n is sampled at the positive Clock edge.
CA0 - CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ0 - DQ15(x16) DQ0 - DQ31(x32)	I/O	**Data Input/Output:** Bi-directional data bus
DQS0_t, DQS1_t, DQS0_c, DQS1_c (x16) DQS0_t - DQS3_t, DQS0_c - DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c tothedataonDQ8-DQ15,DQS2_tandDQS2_ctothedataonDQ16-DQ23,DQS3_tand DQS3_c to the data on DQ24 -DQ31.
DM0-DM1 (x16) DM0-DM3 (x32)	Input	**InputDataMask:**DMistheinputmasksignalforwritedata.Inputdataismaskedwhen DMissampledHIGHcoincidentwiththatinputdataduringaWriteaccess.DMissampled onbothedgesofDQS_t.AlthoughDMisforinputonly,theDMloadingshallmatchtheDQ and DQS_t (orDQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. Forx32devices,DM2istheinputdatamasksignalforthedataonDQ16-23andDM3isthe input data mask signal for the data onDQ24-31.
ODT	Input	**On-Die Termination:** This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
VDD1	Supply	**Core Power Supply 1**
VDD2	Supply	**Core Power Supply 2**
VDDCA	Supply	**Input Receiver Power Supply**: Power for CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VDDQ	Supply	**I/O Power Supply**: Power supply for data input/output buffers.
VREFCA	Supply	**ReferenceVoltageforCACommandandControlInputReceiver**:Referencevoltage for all CA0-9, CKE, CS_n, CK_t and CK_c input buffers.
VREFDQ	Supply	**ReferenceVoltageforDQInputReceiver**:ReferencevoltageforallDatainputbuffers.
VSS	Supply	**Ground**
VSSCA	Supply	**Ground for Input Receivers**
VSSQ	Supply	**I/O Ground**: Ground for data input/output buffers
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

Functional Description

LPDDR3-SDRAM is a high-speed synchronous DRAM device internally configured as an 8-bank memory.

These devices contain the following number of bits:
8 Gb has 8,589,934,592 bits

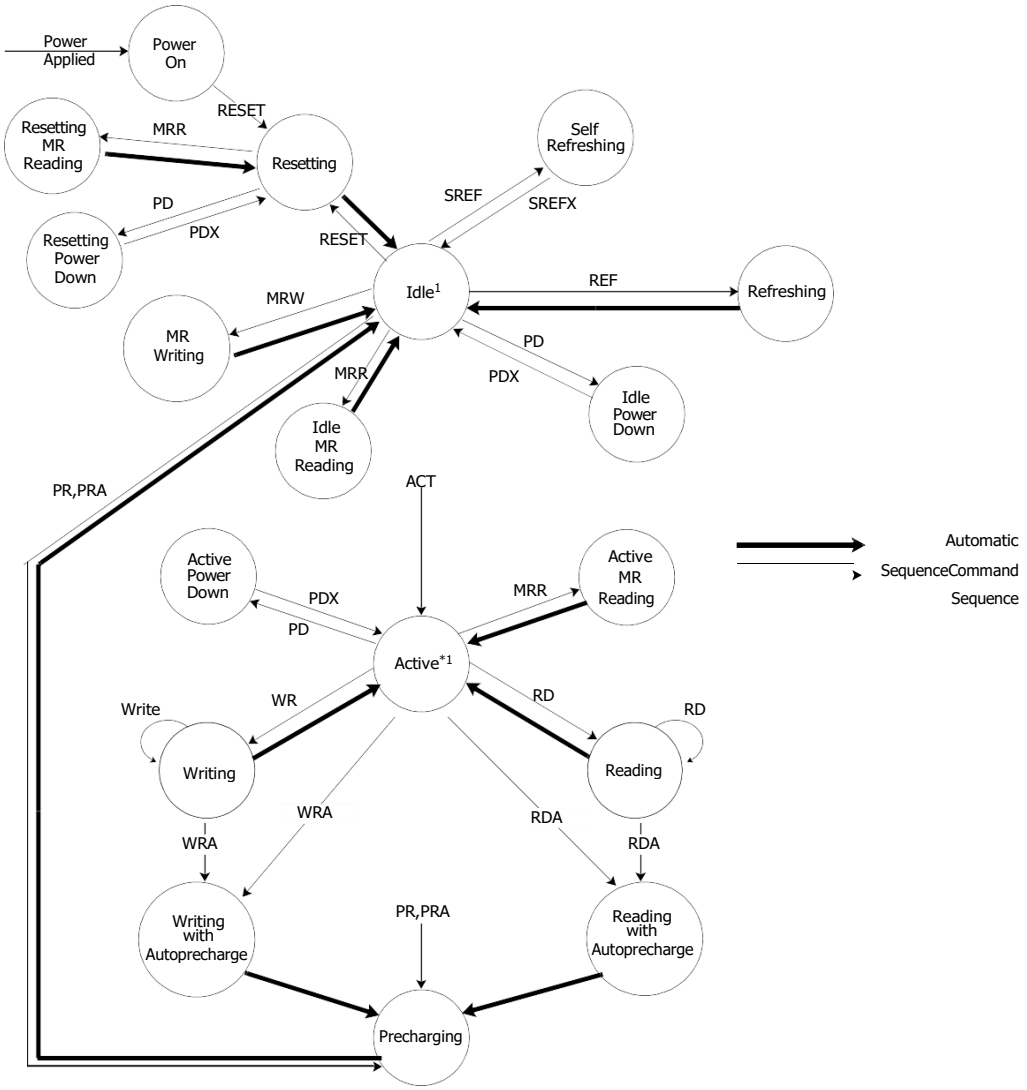
LPDDR3devicesuseadoubledataratearchitectureontheCommand/Address(CA)bustoreducethenumberofinput pinsinthesystem.The10-bitCAbuscontainscommand,address,andbankinformation.Eachcommandusesoneclock cycle,duringwhichcommandinformationistransferredonboththepositiveandnegativeedgeoftheclock. ThesedevicesalsouseadoubledataratearchitectureontheDQpinstoachievehighspeedoperation.Thedoubledata ratearchitectureisessentiallyan8nprefetcharchitecturewithaninterfacedesignedtotransfertwodatabitsperDQ everyclockcycleattheI/Opins.Asinglereadorwriteaccessforthe LPDDR3SDRAMeffectivelyconsistsofasingle 8n-bitwide,oneclockcycledatatransferattheinternalDRAMcoreandeightcorrespondingn-bitwide,one-half-clock- cycle data transfers at the I/Opins.
ReadandwriteaccessestotheLPDDR3SDRAMsareburstoriented;accessesstartataselectedlocationandcontinue foraprogrammednumberoflocationsinaprogrammedsequence.Accessesbeginwiththeregistrationofan Activate command,whichisthenfollowedbyaReadorWritecommand.TheaddressandBAbitsregisteredcoincidentwiththe Activatecommandareusedtoselecttherowandthebanktobeaccessed.Theaddressbitsregisteredcoincidentwith theReadorWritecommandareusedtoselectthebankandthestartingcolumnlocationfortheburstaccess. Priortonormaloperation,theLPDDR3SDRAMmustbeinitialized.Thefollowingsectionprovidesdetailedinformation coveringdeviceinitialization,registerdefinition,commanddescriptionanddeviceoperation.

LPDDR3 SDRAM Addressing

Density		8Gb
Number of Banks		8
Bank Addresses		BA0 - BA2
t_{REFI}(us)[2]		3.9
x16	Row Addresses	R0 - R14
	Column Addresses[1]	C0 - C10
x32	Row Addresses	R0 - R14
	Column Addresses[1]	C0 - C9

Note:
1. Theleast-significantcolumnaddressC0isnottransmittedontheCAbus,andisimpliedtobezero.
2. tREFI values for all bank refresh is Tc = 0 ~ 85 °C, Tc means Operating CaseTemperature.
3. Row and Column Address values on the CA bus which are not used are "don'tcare".
4. NomemorypresentataddresseswithR13=R14=HIGH.ACTcommandwithR13=R14=HIGHisignored(NOP).Writeto R13=R14=HIGH is ignored(NOP).

STATE DIAGRAM



PR(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)

RESET=ResetisachievedthroughMRWcommand
MRW=ModeRegisterWrite
MRR = Mode Register Read

PD = Enter Power Down
PDX = Exit Power Down
SREF = Enter Self Refresh
SREFX = Exit Self Refresh
REF = Refresh

Note:
1. In the Idle state, all banks areprecharged.
2. In the case of MRW to enter CA Training mode or Write Leveling Mode, the state machine will not automatically return to the Idle state.InthesecasesanadditionalMRWcommandisrequiredtoexiteitheroperatingmodeandreturntotheIdlestate.Seesections "CA Training"or "WriteLeveling".
3. Terminated bursts are not allowed. For these state transitions, the burst operation must be completed before the transition can occur.
4. Use caution with this diagram. It is intended to provide a floorplan of the possible state transitions and commands to control them, not all details. In particular, situations involving more than one bank are not capturediSn full detail.

Power-up, Initialization and Power-off

Voltage Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

1. Voltage Ramp

Whileapplyingpower(afterTa),CKEmustbeheldLOW(≤0.2×VDDCA),andallotherinputsmustbebetween VILmin andVIHmax.Thedevice outputsremainatHigh-ZwhileCKEisheldLOW.
Followingthecompletionofthevoltageramp(Tb),CKEmustbemaintainedLOW.DQ,DM,DQS_tandDQS_cvoltage levelsmustbebetweenVSSQandVDDQduringvoltageramptoavoidlatchup.CK_t,CK_c,CS_n,andCAinputlevels mustbebetweenVSSCAandVDDCAduringvoltageramptoavoidlatch-up.Voltageramppowersupplyrequirements are provided in the table "Voltage RampConditions".

After…	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2-200mV.
	VDD1 and VDD2 must be greater than VDDCA-200mV.
	VDD1 and VDD2 must be greater than VDDQ-200mV.
	VREF must always be less than all other supply voltages.

Note:
1. Ta is the point when any power supply firstreaches 300mV.
2. Noted conditions apply between Ta and power-off (controlledor uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined operatingranges.
4. Power ramp duration tINIT0 (Tb - Ta) must not exceed20ms.
5. The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed100mV.

BeginningatTb,CKEmustremainLOWforatleasttINIT1,afterwhichCKEcanbeassertedHIGH.Theclockmustbe stableatleasttINIT2priortothefirstCKELOW-to-HIGHtransition(Tc).CKE,CS_n,andCAinputsmustobservesetup andholdrequirements(tIS,tIH)withrespecttothefirstrisingclockedge(aswellastosubsequentfallingandrising edges).
IfanyMRRcommandsareissued,theclockperiodmustbewithintherangedefinedfortCKb.MRWcommandscanbe issuedatnormalclockfrequenciesaslongasallACtimingsaremet.SomeACparameters(forexample,tDQSCK) could have relaxed timings (such as t DQSCKb) before the system is appropriately configured. While keeping CKE HIGH,NOPcommandsmustbeissuedforatleasttINIT3(Td).TheODTinputsignalmaybeinundefinedstateuntilt ISbeforeCKEisregisteredHIGH.WhenCKEisregisteredHIGH,theODTinputsignalshallbestaticallyheldateither LOWorHIGH.TheODTinputsignalremainsstaticuntilthepowerupinitializationsequenceisfinished,includingthe expiration oftZQINIT.

2. ResetCommand

After tINIT3 is satisfied, the MRW RESET command must be issued (Td).
AnoptionalPRECHARGEALLcommandcanbeissuedpriortotheMRWRESETcommand.WaitatleasttINIT4while keepingCKEassertedandissuingNOPcommands.OnlyNOPcommandsareallowedduringtimetINIT4.

3. MRRs and Device Auto Initialization (DAI)Polling

AftertINIT4issatisfied(Te),onlyMRRcommandsandpower-downentry/exitcommandsaresupported.AfterTe,CKE cangoLOWinalignmentwithpower-downentryandexitspecifications.MRRcommandsareonlyvalidatthistimeif the CAbus does not need to be trained. may only begin after time Tf. User may issue MRR command to poll the DAI bitwhichwillindicateifdeviceautoinitializationiscomplete;onceDAIbitindicatescompletion,SDRAMisinidlestate. Devicewillalsobeinidlestateaftert INIT5(max)hasexpired(whetherornotDAIbithasbeenreadbyMRRcommand). AsthememoryoutputbuffersarenotproperlyconfiguredbyTe,someACparametersmusthaverelaxedtimingsbefore the system is appropriatelyconfigured.

4. ZQCalibration

IfCATrainingisnotrequired,theMRWinitializationcalibration(ZQ_CAL)commandcanbeissuedtothememory

(

MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. See the section of "Mode Regis- ter Write - CA Training Mode" for the CA Training command. No other CA commands (other than RESET or NOP) may beissuedpriortothecompletionofCATraining.AtthecompletionofCATraining(Tf'),theMRWinitializationcalibra-t ion(ZQ_CAL)commandcanbe issuedtothememory(MR10).

Thiscommandisusedtocalibrateoutputimpedanceoverprocess,voltage,andtemperature.Insystemswheremore thanoneLPDDR3deviceexistsonthesamebus,thecontrollermustnotoverlapMRWZQ_CALcommands.Thedevice is readyfornormaloperationaftertZQINIT.

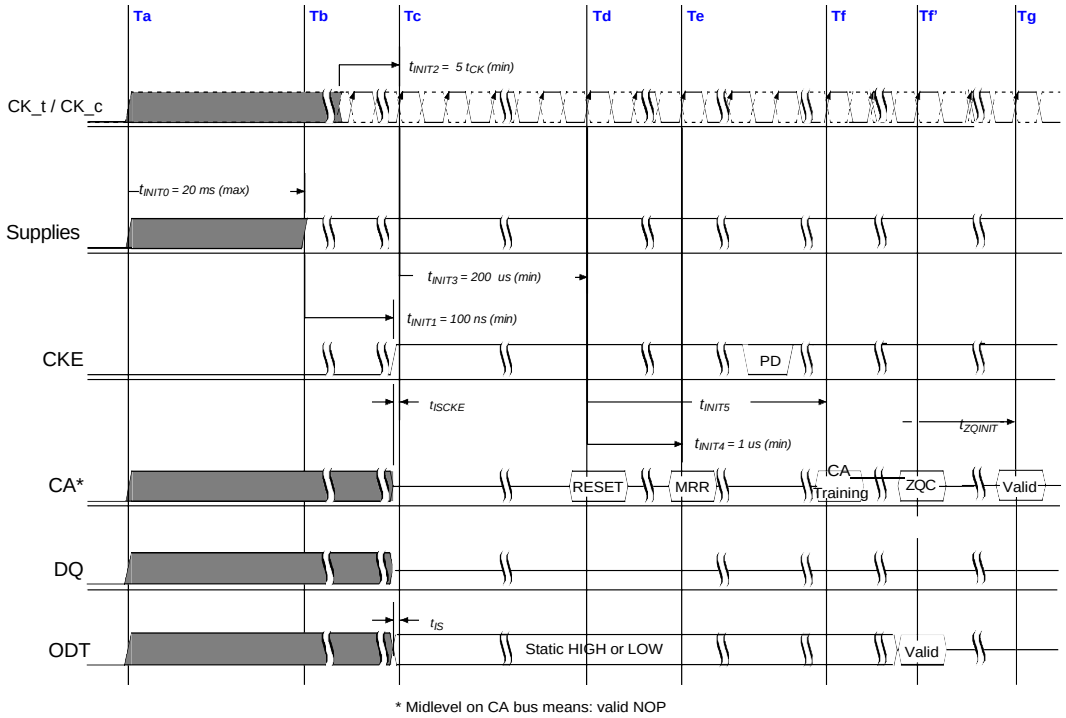
5. NormalOperation

AftertZQINIT(Tg),MRWcommandsmustbeusedtoproperlyconfigurethememory(forexampletheoutputbuffer drivestrength,latencies,etc.).Specifically,MR1,MR2,andMR3mustbesettoconfigurethememoryforthetargetf requency and memoryconfiguration.

Aftertheinitializationsequenceiscomplete,thedeviceisreadyforanyvalidcommand.AfterTg,theclockfrequency canbechangedusingtheproceduredescribedintheLPDDR3specification.

Table. Timing Parameters for initialization

Symbol	Parameter	Value		Unit
		min	max	
tINIT0	Maximum Voltage Ramp Time	-	20	ms
tINIT1	Minimum CKE low time after completion of voltage ramp	100	-	ns
tINIT2	Minimum stable clock before first CKE high	5	-	tCK
tINIT3	Minimum idle time after first CKE assertion	200	-	us
tINIT4	Minimum idle time after Reset command	1	-	us
tINIT5	Maximum duration of Device Auto-Initialization	-	10	us
tZQINIT	ZQ Initial Calibration for LPDDR3 devices	1	-	us
tCKb	Clock cycle time during boot	18	100	ns



* Midlevel on CA bus means: valid NOP

Figure. Power Ramp and Initialization Sequence

Notes
1. High-Z on the CA bus indicatesNOP.
2. For tINIT values, see the table "Timing Parameters forInitialization".
3. After RESET command (time Te), RTT is disabled until ODT function is enabled by MRW to MR11following Tg.
4. CA Training isoptional.

Initialization After Reset (without Power ramp)

IftheRESETcommandisissuedbeforeorafterthepower-upinitializationsequence,there-initializationproceduremust begin atTd.

Power-off Sequence

The following procedure is required to power off the device.
Whilepoweringoff,CKEmustbeheldLOW(≤0.2×VDDCA);allotherinputsmustbebetweenVILminandVIHmax.The deviceoutputsremainatHigh-ZwhileCKEisheldLOW.
DQ,DM,DQS_t,andDQS_cvoltagelevelsmustbebetweenVSSQandVDDQduringthepower-offsequencetoavoidlatch-up.CK_t,CK_c,CS_n,andCAinputlevelsmustbebetweenVSSCAandVDDCAduringthepower-offsequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see the table "Power Supply Conditions").

Table. Power Supply Conditions

Between…	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2—200mV
	VDD1 must be greater than VDDCA—200mV
	VDD1 must be greater than VDDQ—200mV
	VREF must always be less than all other supply voltages

The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:
AtTx,whenthepowersupplydropsbelowtheminimumvaluesspecified,allpowersuppliesmustbeturnedoffandall power-supplycurrentcapacitymustbeatzero,exceptforanystaticchargeremaininginthesystem.
AfterTz(thepointatwhichallpowersuppliesfirstreach300mV),thedevicemustpoweroff.ThetimebetweenTxa ndTzmustnotexceed10ms.Duringthisperiod,therelativevoltagebetweenpowersuppliesisuncontrolled.VDD1a ndVDD2mustdecreasewithaslopelowerthan0.5V/µsbetweenTxandTz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table. Power-Off Timing

Symbol	Parameter	Value		Unit
		min	max	
tPOFF	Maximum power-off ramp time	-	2	sec

Mode Register Definition

TablebelowshowsthemoderegistersforLPDDR3SDRAM.Eachregisterisdenotedas"R"ifitcanbereadbutnotwritten,"W"ifitcanbewrittenbutnotread,and"R/W"ifitcanbereadandwritten.AModeRegisterReadcommandshallbeusedtoreadamoderegister.AModeRegisterWritecommandshallbeusedtowriteamoderegister.

Table. Mode Register Assignment

MR #	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	RL3	WL setB	(RFU)	RZQI (Optional)		(RFU)		DAI	go to MR0
1	01H	Device Feature1	W	nWR (for AP)			(RFU)	BT	BL			go to MR1
2	02H	Device Feature 2	W	WR Lev	WL Select	(RFU)	nWRE	RL & WL				go to MR2
3	03H	I/O Config-1	W	(RFU)				DS				go to MR3
4	04H	Device Tempera-ture	R	TUF	(RFU)				Refresh Rate			go to MR4
5	05H	Basic Config-1	R	Manufacturer ID								go to MR5
6	06H	Basic Config-2	R	Revision ID1								go to MR6
7	07H	Basic Config-3	R	Revision ID2								go to MR7
8	08H	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	0AH	Calibration	W	Calibration Code								go to MR10
11	0BH	ODT	W	(RFU)					PD CTL	DQ ODT		go to MR11
16	10H	PASR_Bank	W	PASR Bank Mask								go to MR16
17	11H	PASR_Segment	W	PASR Segment Mask								go to MR17
32	20H	DQ Calibration Pattern A	R	See the section "DQ Calibration"								go to MR32
40	28H	DQ Calibration Pattern B	R	See the section "DQ Calibration"								go to MR40
41	29H	CA TrainingEntry for CA0-3,CA5-8	W	See the section "Mode Register Write - CA Training Mode"								go to MR41
42	2AH	CA Training Exit	W	See the section "Mode Register Write - CA Training Mode"								go to MR42
48	30H	CA Training Entry for CA4, 9	W	See the section "Mode Register Write - CA Training Mode"								go to MR48
63	3FH	Reset	W	X								go to MR63

Note:
1. RFU bits shall be set to `0' during Mode Registerwrites.
2. RFU bits shall be read as `0' during ModeRegister reads.
3. AllModeRegistersthatarespecifiedas RFUor write-onlyshallreturnundefineddatawhen readandDQS_t,DQS_cshallbetog- gled.
4. All Mode Registers that are specified as RFU shall not bewritten.
5. Writestoread-onlyregistersshallhavenoimpactsonthefunctionalityofthedevice.

MR0 Device Information (MA<7:0> = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI (Optional)		(RFU)		DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0B: DAI complete 1B: DAI still in progress
RZQI (Built in Self Test for RZQ Information)	Read-only	OP4:OP3	00B: RZQ self test not supported 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B:ZQ-pinself testcompleted,noerrorcondi-tion detected (ZQ-pin may not connect toVDD or float nor short to GND)
WL (Set B) Support	Read-only	OP<6>	0B: DRAM does not support WL (Set B) 1B: DRAM supports WL (Set B)
RL3 Option Support	Read-only	OP<7>	0B : DRAM does not support RL=3, nWR=3, WL=1 1B : DRAM supports RL=3, nWR=3, WL=1 for frequencies <=166

Note:
1. RZQI, if supported, will be set upon completion of the MRW ZQ InitializationCalibration command.
2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. InthecaseofpossibleassemblyerroreitherOP[4:3]=01orOP[4:3]=10perNote4),theLPDDR3devicewilldefaultto factory trimsettingsforRON,andwill ignoreZQcalibrationcommands.Ineithercase,thesystemmaynotfunctionasintended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-ohm+/-1%).

MR1 Device Feature 1 (MA<7:0> = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)	BT	BL		

BL	Write-only	OP<2:0>	011B: BL8 (default)
			100B: Reserved
			All others: reserved
BT	Write-only	OP<3>	0B: Don't care
nWR	Write-only	OP<7:5>	If nWRE (in MR2 OP4) = 0
			001B : nWR=3 (optional)
			100B : nWR=6
			110B : nWR=8
			111B : nWR=9
			If nWRE (in MR2 OP4) = 1
			000B : nWR=10 (default)
			001B : nWR=11
			010B : nWR=12
			100B : nWR=14
			110B : nWR=16
			All others: reserved

Note:
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table. Burst Sequence by BL and BT

C2	C1	C0	BT	BL	Burst Cycle Number and Burst Address Sequence							
					1	2	3	4	5	6	7	8
0B	0B	0B	seq	8	0	1	2	3	4	5	6	7
0B	1B	0B			2	3	4	5	6	7	0	1
1B	0B	0B			4	5	6	7	0	1	2	3
1B	1B	0B			6	7	0	1	2	3	4	5

Note:
1. C0 inputs are not present on CA bus. Those areimplied zero.
2. For BL=8, the burst address represents C2 -C0.

MR2 Device Feature 2 (MA<7:0> = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WL Select	(RFU)	nWRE	RL & WL			

RL & WL	Write-only	OP<3:0>	If OP<6> =0 (WL Set A, default) 0001B: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 6 (≤ 667 MHz, default) 1001B: RL = 11 / WL = 6 (≤ 733MHz) 1010B: RL = 12 / WL = 6 (≤ 800MHz) 1100B: RL = 14 / WL = 8 (≤ 933MHz) 1110B: RL = 16 / WL = 8 (≤ 1066 MHz) All others: reserved If OP<6> =1 (WL Set B, optional[2]) 0001B: RL = 3 / WL = 1 (≤ 166 MHz, optional[1]) 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 8 (≤ 667 MHz, default) 1001B: RL = 11 / WL = 9 (≤ 733MHz) 1010B: RL = 12 / WL = 9 (≤ 800MHz) 1100B: RL = 14 / WL = 11 (≤ 933MHz) 1110B: RL = 16 / WL = 13 (≤ 1066MHz) All others: reserved
nWRE	Write-only	OP<4>	0B : Enable nWR programing ≤ 9 1B : Enable nWR programing > 9 (default)
WL Select	Write-only	OP<6>	0B : Select WL Set A (default) 1B : Select WL Set B (optional[2])
Write Leveling	Write-only	OP<7>	0B : Disabled (default) 1B : Enabled

Note:
1. See MR0,OP<7>.
2. See MR0,OP<6>

MR3 I/O Configuration 1 (MA<7:0> = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			
DS	Write-only	OP<3:0>	0000B: reserved				
			0001B: 34.3Ωtypical pull-down/pull-up				
			0010B: 40Ωtypical pull-down/pull-up (default)				
			0011B: 48Ωtypical pull-down/pull-up				
			0100B: reserved for 60Ωtypical pull-down/pull-up				
			0110B: reserved for 80Ωtypical pull-down/pull-up				
			1001B: 34.3Ωtypical pull-down, 40ΩTypical Pull-up (optional[1])				
			1010B: 40Ωtypical pull-down, 48ΩTypical Pull-up (optional[1])				
			1011B: 34.3Ωtypical pull-down, 48ΩTypical Pull-up (optional[1])				
			All others: reserved				

Note:
1. Please contact us, for the supportability of the optionalfeature.

MR4 Device Temperature (MA<7:0> = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		
Refresh Rate	Read-only	OP<2:0>	000B: Low temperature operating limit exceeded				
			001B: 4 x tREFI, 4 x tREFIpb, 4 x tREFW				
			010B: 2 x tREFI, 2 x tREFIpb, 2 x tREFW				
			011B: 1 x tREFI, 1 x tREFIpb, 1 x tREFW (≤85°C)				
			100B: 1/2 x tREFI, 1/2 x tREFIpb, 1/2 x tREFW, do not de-rate AC timing				
			101B: 1/4 x tREFI, 1/4 x tREFIpb, 1/4 x tREFW, do not de-rate AC timing				
			110B: 1/4 x tREFI, 1/4 x tREFIpb, 1/4 x tREFW, de-rate AC timing				
			111B: High temperature operating limit exceeded				
Temperature Update Flag (TUF)	Read-only	OP<7>	0B: OP<2:0> value has not changed since last read of MR4 1B: OP<2:0> value has changed since last read of MR4				

Note:
1.A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' atpower-up.
3. If OP2 equals '1', the device temperature is greaterthan 85ºC.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last readof MR4.
5. LPDDR3mightnotoperateproperlywhenOP[2:0]=000Bor111B.
6.For specified operating temperature range and maximum operating temperature refer to the section of Operating Temperature Range.
7.LPDDR3 devices shall be de-rated by adding derating values to the following core timing parameters: tRCD, tRC, tRAS, tRP and tRRD.tDQSCKshallbede-ratedaccordingtothetDQSCKde-ratingin"ACtimingtable".Prevailingclockfrequencyspecandrelated setup and hold timings shall remainunchanged.
8. See the section of Temperature Sensor for information on the recommended frequencyof reading MR4.

MR5BasicConfiguration1(MA<7:0>=05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Company ID	Read-only	OP<7:0>	0000 0110B: Hynix Semiconductor	

MR6BasicConfiguration2(MA<7:0>=06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 1							

Revision ID1	Read-only	OP<7:0>	00000011B	

MR7BasicConfiguration3(MA<7:0>=07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID 2							

Revision ID2	Read-only	OP<7:0>	00000000B: A-version	

MR8BasicConfiguration4(MA<7:0>=08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP<1:0>	11B: S8
			All Others : Reserved
Density	Read-only	OP<5:2>	0110B : 4Gb
			0111B : 8Gb
			1000B : 16Gb
			All Others : Reserved
I/O width	Read-only	OP<7:6>	00B: x32
			01B: x16
			All Others : Reserved

MR9 Test Mode (MA<7:0> = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

MR10 Calibration (MA<7:0> = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write Only	OP<7:0>	1111 1111B: Calibration command after initialization
			1010 1011B: Long Calibration
			0101 0110B: Short Calibration
			1100 0011B: ZQ Reset
			others: reserved

Note:
1. Host processor shall not write MR10 with "Reserved"values
2. LPDDR3devicesshallignorecalibrationcommandwhena"Reserved"valueis writtenintoMR10.
3. See AC timing table for the calibrationlatency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQRESET command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to thedevice.
5. LPDDR3 devices that do not support calibration shall ignore theZQ Calibration command.
6. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pinconnection.

MR11 ODT (MA<7:0> = 0BH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)					PD Control	DQ ODT	

DQ ODT	Write Only	OP<1:0>	00B : Disable (Default)
			01B : RZQ/4 (See the Note 1.)
			10B : RZQ/2
			11B : RZQ/1
Power Down Control	Write Only	OP<2>	0B : ODT disabled by DRAM during power down
			1B : ODT enabled by DRAM during power down

Note:
1. RZQ/4 shall be supported for LPDDR3-1866 devices. RZQ/4 support is optional for LPDDR3-1333 and LPDDR3-1600 devices. Consult manufacturer specifications for RZQ/4 support for LPDDR3-1333 and LPDDR3-1600.

MR12:15 (Reserved) (MA<7:0> = 0CH - 0FH)

MR16 PASR Bank Mask (MA<7:0> = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

Bank <7:0> Mask	Write-only	OP<7:0>	0B : refresh enable to the bank (=unmasked, default) 1B : refresh blocked (=masked)

OP	Bank Mask	LPDDR3 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

MR17 PASR Segment Mask (MA<7:0> = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment <7:0> Mask	Write-only	OP<7:0>	0B : refresh enable to the segment (=unmasked, default) 1B : refresh blocked (=masked)

Segment	OP	Segment Mask	4Gb R13:11	6Gb[2] R14:12	8Gb R14:12	12Gb[2] R14:12	16Gb R14:12
0	0	XXXXXXX1	000B				
1	1	XXXXXX1X	001B				
2	2	XXXXX1XX	010B				
3	3	XXXX1XXX	011B				
4	4	XXX1XXXX	100B				
5	5	XX1XXXXX	101B				
6	6	X1XXXXXX	110B				
7	7	1XXXXXXX	111B				

Note:
1. This table indicates the range of row addresses in each masked segment. X is do not care for a particular segment.

MR18:31 (Reserved) (MA<7:0> = 12H - 1FH)

MR32 DQ Calibration Pattern A (MA<7:0> = 20H): MRR only
Reads to MR32 return DQ Calibration Pattern A. See the section of DQ Calibration.

MR33:39 (Reserved) (MA<7:0> = 21H - 27H)

MR40 DQ Calibration Pattern B (MA<7:0> = 28H): MRR only
Reads to MR40 return DQ Calibration Pattern B. See the section of DQ Calibration.

MR41 CA Calibration Mode Entry for CA0-3, CA5-8 (MA<7:0> = 29H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
A4							

See the section of CA Calibration.

MR42 CA Calibration Mode Exit (MA<7:0> = 2AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
A8							

See the section of CA Calibration.

MR43:47 (Reserved) (MA<7:0> = 2BH - 2FH)

MR48 CA Calibration Mode Entry for CA4, 9 (MA<7:0> = 30H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
C0							

See the section of CA Calibration.

MR49:62 (Reserved) (MA<7:0> = 31H - 3EH)

MR63 Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X or 0xFC							

Note: For additional information on MRW RESET, see Mode Register Write Command section.

TRUTHTABLES

Operationortimingthatisnotspecifiedisillegalandaftersuchanevent,inordertoguaranteeproperoperation,the LPDDR3devicemustbepowereddownandthenrestartedthroughthespecifiedinitializationsequencebeforenormal operation cancontinue.

COMMAND TRUTH TABLE

Command	SDR Command Pins (2)			DDR CA Pins (10)										CK_t edge
	CKE		CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	falling
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	rising
			X	MA6	MA7	X								falling
Refresh (per bank)	H	H	L	L	L	H	L	X						rising
			X	X										falling
Refresh (all bank)	H	H	L	L	L	H	H	X						rising
			X	X										falling
Enter Self Refresh	H	L	L	L	L	H	X							rising
			X	X										falling
Active (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	rising
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	falling
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	rising
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	rising
			X	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	falling
Precharge (perbank, all bank)[11]	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	rising
			X	X	X	X	X	X	X	X	X	X	X	falling
NOP	H	H	L	H	H	H	X							rising
			X	X										falling
Maintain SREF, PD (NOP)[4]	L	L	X	H	H	H	X							rising
			X	X										falling
NOP	H	H	H	X										rising
			X	X										falling
Maintain PD, SREF (NOP)[4]	L	L	X	X										rising
			X	X										falling
Enter Power Down	H	L	H	X										rising
			X	X										falling
Exit PD, SREF	L	H	H	X										rising
			X	X										falling

Note:

1. All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of theclock.
2. BankaddressesBA0,BA1,BA2(BA)determinewhichbankistobeoperatedupon.
3. AP"high"duringaREADor WRITEcommandindicatesthatanauto-prechargewill occurto thebankassociatedwiththeREADor WRITEcommand.
4. "X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, or SREF, in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exitprocedure.
5. Self refresh exit isasynchronous.
6. VREF must be between 0 and VDDQ during SelfRefreshoperation.
7. CAxr refers to command/address bit "x" on the rising edgeofclock.
8. CAxf refers to command/address bit "x" on the falling edge ofclock.
9. CS_n and CKE are sampled at the rising edge ofclock.
10. Theleast-significantcolumnaddressC0isnottransmittedon theCAbus,andis impliedtobezero.
11. AB"high"duringPrechargecommandindicatesthatallbankPrechargewill occur.Inthiscase,BankAddressisdo-not-care.
12. When CS_n is HIGH, LPDDR3 CA bus can befloated.

CKE TRUTH TABLE

Current State[3]	CKE_{n-1}[4]	CKE_n[4]	CS_n[5]	Command n[6]	Operationn[6]	Next State	Notes
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Powe Down	
	L	H	H	NOP	Exit Active Power Down	Active	7
Idl Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	7
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	7,9
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	8
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power-Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	11
	H	L	L	Enter Self Refresh	Enter Self Refresh	Self Refresh	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
	H	H	Refer to the Command Truth Table				

Note:
1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere inthis document.
2. 'X' means 'Don'tcare'.
3. "Currentstate"isthestateoftheLPDDR3deviceimmediatelypriortoclockedgen.
4. "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previousclock edge.
5. "CS_n" is the logic state of CS_n at the clock rising edgen.
6. "Commandn"isthecommandregisteredatclockedgeN, and"Operationn"is aresultof"Commandn".
7. PowerDownexittime(tXP)shouldelapsebeforeacommandotherthanNOPis issued.Theclockmusttoggleatleast twice during the tXP period.
8. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued. The clock must toggle at least t wice during the tXSRtime.
9. UponexitingResettingPowerDown,thedevicewillreturntotheIdlestateiftINIT5hasexpired.
10. Inthecaseof ODTdisabled,allDQoutputshallbeHi-Z.InthecaseofODTenabled,all DQshallbe terminatedto VDDQ.

Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current State	
Idle	Activate	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Write value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	8
	Precharge	Deactive row in bank or banks	Precharging	9, 12
Row Active	Read	Select Column, and start read burst	Reading	
	Write	Select Column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10,11
	Write	Select column, and start write burst	Writing	10,11,13
Writing	Write	Select Column, and start new write burst	Writing	10,11
	Read	Select column, and start read burst	Reading	10,11,14
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:

1. ThetableapplieswhenbothCKE_{n-1}andCKE_nareHIGH,andaftertXSRortXPhasbeenmetifthepreviousstatewasPowerDown.
2. All states and sequences not shown are illegal orreserved.
3. Current StateDefinitions:
   Idle: The bank or banks have been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
   Reading: A READ burst has been initiated, with Auto Precharge disabled.
   Writing: A WRITE burst has been initiated, with Auto Precharge disabled.
4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to theotherbankshouldbeissuedonanyclock edgeoccurringduringthesestates.Allowablecommandstotheotherbanksaredeter- mined by its current state and Table "Current State Bank n - Command to Bank n", and according to Table "Current State Bank n - Command to Bankm".
   Precharging:startswiththeregistrationofaPRECHARGEcommandandendswhentRPismet.OncetRPismet,thebankwill be in the idlestate.
   Row Activating: starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
   Read with AP Enabled: starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. Thefollowingstatesmustnotbeinterruptedbyanyexecutablecommand;NOPcommandsmustbe appliedto eachpositiveclock edge during thesestates.
   Refreshing(PerBank):startswithregistrationofaREFRESH(PerBank)commandandendswhentRFCpbismet.OncetRFCpbis met, the bank will be in an 'idle'state.
   Refreshing (All Bank): starts with registration of a REFRESH(All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.

Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
PrechargingAll:startswiththeregistrationofaPRECHARGEALLcommandandendswhentRPismet.OncetRPismet,thebank will be in the idlestate.

6. Bank-specific; requires that the bank is idle and no bursts are inprogress.
7. Not bank-specific; requires that all banks are idle and no bursts are inprogress.
8. Not bank-specific reset command is achieved through MODE REGISTER WRITEcommand.
9. Thiscommandmayormaynotbebankspecific.Ifallbanks arebeingprecharged,theymustbein a validstateforprecharging.
10. AcommandotherthanNOPshouldnotbeissuedtothesamebankwhileaREADorWRITEburstwithAutoPrechargeisenabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Prechargedisabled.
12. If a Precharge command is issued to a bank in the Idle state, tRP shallstill apply.
13. A Write command may be applied after the completion of the Read burst, burst terminates arenot permitted.
14. A Read command may be applied after the completion of the Write burst, burst terminates arenot permitted.

Current State Bank n - Command to Bank m

Current State of Bank n	Commandfor Bank m	Operation	Next State for Bank m	Note
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Readingor Active MRReading	9,10,12
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7,16
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13
	Write	Select column, and start write burst to Bank m	Writing	7,15,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13,16
	Write	Select column, and start write burst to Bank m	Writing	7,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Power On	Reset	Begin Device Auto-Initialization	Resetting	11, 14
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note:
1. The table applies when both CKE_{n-1} and CKE_n are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or PowerDown.
2. All states and sequences not shown are illegal orreserved.
3. Current StateDefinitions:
   Idle: the bank has been precharged, and tRP has been met.
   Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Reading: a READ burst has been initiated, with Auto Precharge disabled.
   Writing: a WRITE burst has been initiated, with Auto Precharge disabled.
4. REFRESH,SELFREFRESH,andMODEREGISTERWRITEcommandsmayonlybeissuedwhenall bankareidle.
5. Thefollowingstatesmustnotbeinterruptedbyanyexecutablecommand;NOPcommandsmustbeappliedduringeachclockcycle whilein thesestates:
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Row Active state.
   MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
6. tRRDmustbemetbetweenActivatecommandtoBanknandasubsequentActivatecommandtoBankm.

7. READsorWRITEslistedintheCommandcolumnincludeREADsandWRITEswithAutoPrechargeenabledandREADsandWRITEs with Auto Prechargedisabled.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. MRRisallowedduringtheRowActivatingstateandMRWisprohibitedduringtheRowActivatingstate.(RowActivatingstartswith registrationofanActivatecommandandendswhentRCDismet.)
10. MRRisallowedduringthePrechargingstate.(PrechargingstartswithregistrationofaPrechargecommandandendswhentRPis met.
11. Not bank-specific; requires that all banks are idle and no bursts are inprogress.
12. ThenextstateforBankmdependsonthecurrentstateofBankm(Idle,RowActivating,Precharging,orActive).Thereadershall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD andtRP respectively.
13. ReadwithautoprechargeenabledoraWritewithautoprechargeenabledmaybefollowedbyanyvalidcommandtootherbanks provided that the timing restrictions in the section of Precharge and Auto Precharge clarification arefollowed.
14. Reset command is achieved through MODE REGISTER WRITEcommand.
15. A Write command may be applied after the completion of the Read burst, burst terminates arenot permitted.
16. A Read command may be applied after the completionof the Write burst, burst terminates are not permitted.

DATA MASK TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Note:
1. Used to mask write data, provided coincident with the corresponding data.

Absolute Maximum DC Ratings

Stressesgreaterthanthoselistedmaycausepermanentdamagetothedevice.Thisisastressratingonly,andfunc-tionaloperationofthedeviceattheseoranyotherconditions above thoseindicatedintheoperationalsectionsofthis specificationisnotimplied.Exposuretoabsolutemaximumratingconditionsforextendedperiodsmayaffectreliability.

Parameter	Symbol	Min	Max	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	1
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	1, 2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	1, 3
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	°C	4

Note:

1. See the section "Power-up, Initialization, and Power-off" for relationships between powersupplies.
2. VREFCA≤0.6x VDDCA;however,VREFCAmaybe≥VDDCAprovidedthatVREFCA≤300mV.
3. VREFDQ≤0.7x VDDQ; however,VREFDQmaybe≥VDDQprovidedthatVREFDQ≤300mV.
4. StorageTemperatureisthecase surfacetemperatureonthecenter/topsideof thedevice.Forthemeasurementconditions,please refer to JESD51-2standard.

AC and DC Operating Conditions

Operationortimingthatisnotspecifiedisillegal,andaftersuchanevent,inordertoguaranteeproperoperation,the LPDDR3Devicemustbepowereddownandthenrestartedthroughthespecializedinitializationsequencebeforenormal operation cancontinue.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power 1	VDD1	1.70	1.80	1.95	V
Core Power 2	VDD2	1.14	1.20	1.30	V
Input Buffer Power	VDDCA	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

Note :

1. VDD1 uses significantly less current thanVDD2.
2. ThevoltagerangeisforDCvoltageonly.DCisdefinedasthevoltagesuppliedattheDRAMandisinclusiveof allnoiseupto 1MHz at the DRAM package ball.

Input Leakage Current

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage current	IL	-2	2	uA	2
VREF supply leakage current	IVREF	-1	1	uA	1

Note:

1. ForCA,CKE,CS_n,CK_t,CK_c.Anyinput0V≤VIN ≤VDDCA(Allotherpinsnotundertest=0V)
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c outputleakage specification.
3. Theminimumlimitrequirementisfortestingpurposes.Theleakagecurrenton VREFCAandVREFDQpinsshouldbeminimal.
4. VREFDQ = VDDQ/2 or VREFCA = VDDCA/2. (All other pins not under test= 0V)

Operating Temperature

Parameter		Symbol	Min	Max	Unit	Note
Operating Temperature	Standard	T_{OPER}	-25	85	°C	1

Note:

1.Operating Temperature is the case surface temperature on the center-top side of the LPDDR3 device. For the measurement conditions, please refer to JESD51-2 standard.

AC and DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended CA and CS_n Signals

Parameter	Symbol	LPDDR3 1600/1333		Unit	Note
		Min	Max		
AC Input Logic High	VIHCA	VREF + 0.150	Note 2	V	1,2
AC Input Logic Low	VILCA	Note 2	VREF - 0.150	V	1,2
DC Input Logic High	VIHCA	VREF + 0.100	VDDCA	V	1
DC Input Logic Low	VILCA	VSSCA	VREF - 0.100	V	1
Reference Voltage for CA and CS_n Inputs	VREFCA(DC)	0.49 * VDDCA	0.51 * VDDCA	V	3,4

Note:
1. For CA and CS_n input only pins. VREF =VREFCA(DC).
2. See the section "Overshoot and UndershootSpecifications".
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12mV).
4. For reference: approx. VDDCA/2 +/- 12mV.

AC and DC Logic Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Note
CKE Input High Level	VIHCKE	0.65 * VDDCA	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.35 * VDDCA	V	1

Note: 1. See the section "Overshoot and Undershoot Specifications".

AC and DC Logic Input Levels for Single-Ended Data (DQ and DM) Signals

Parameter	Symbol	LPDDR3 1600/1333		Unit	Note
		Min	Max		
AC Input High Voltage	VIHDQ	VREF + 0.150	Note 2	V	1,2
AC Input Low Voltage	VILDQ	Note 2	VREF - 0.150	V	1,2
DC Input High Voltage	VIHDQ	VREF + 0.100	VDDQ	V	1
DC Input Low Voltage	VILDQ	VSSCA	VREF - 0.100	V	1
Reference Voltage for DQ and DM Inputs	VREFDQ(DC) (DQ ODT disabled)	0.49 * VDDQ	0.51*VDDQ	V	3,4
Reference Voltage for DQ and DM Inputs	VREFDQ(DC) (DQODT enabled)	0.5 * Vodtr - 0.01 * VDDQ	0.5 * Vodtr + 0.01 * VDDQ	V	3,5,6

Note:
1. For DQ input only pins. VREF =VREFDQ(DC).
2. See the section of Overshoot and UndershootSpecifications.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12mV).
4. For reference: approx. VDDQ/2 +/- 12mV.
5. For reference: approx. VODTR/2 +/- 12mV.
6. ThenominalmoderegisterprogrammedvalueforRODTandthenominalcontrolleroutputimpedanceRONareusedforthecalcu- lation of VODTR. For testing purposes a controller RON value of 50 Ω isused.
   Vodtr = (2 * RON + RTT) / (RON + RTT) * VDDQ

VREF Tolerances

Thedc-tolerancelimitsandac-noiselimitsforthereferencevoltagesVREFCAandVREFDQareillustratedinFigurebe-low.Itshowsavalidreferencevoltage VREF(t)asafunctionoftime.(VREFstandsforVREFCAandVREFDQlikewise). VDDstandsforVDDCSforVREFCAandVDDQforVREFDQ.VREF(DC)isthelinearaverageofVREF(t)overaverylong periodoftime(e.g.1sec)andisspecifiedasafractionofthelinearaverageofVDDCAorVDDQalsooveraverylong periodoftime(e.g.1sec).Thisaveragehastomeetthemin/maxrequirementsinTable"ElectricalCharacteristicsand OperatingConditions".FurthermoreVREF(t)maytemporarilydeviatefromVREF(DC)bynomorethan+/-1%VDD.V REF(t)cannottracknoiseonVDDQorVDDCAif thiswouldsendVREF outsidethesespecifications.

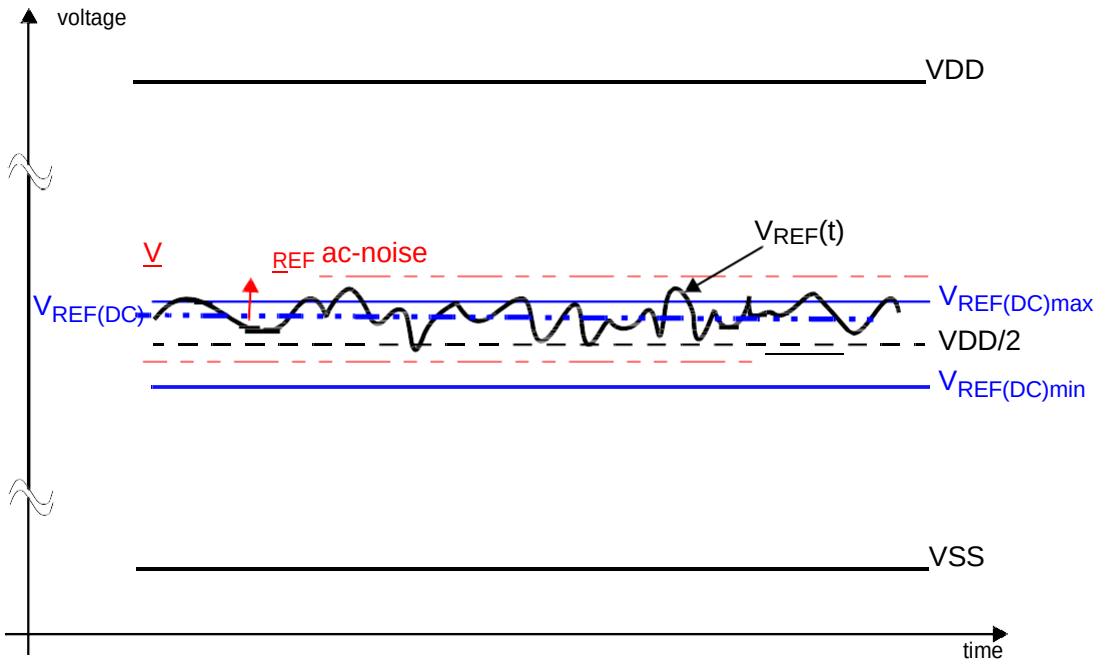


Figure. Illustration of VREF(DC) tolerance and VREF ac-noise limits

ThevoltagelevelsforsetupandholdtimemeasurementsVIH(AC),VIH(DC),VIL(AC)andVIL(DC)aredependentonV REF."VREF"shallbe understoodasVREF(DC),asdefinedinFigure above.

Thisclarifiesthatdc-variationsofVRefaffecttheabsolutevoltageasignalhastoreachtoachieveavalidhighorlowl evelandthereforethetimetowhichsetupandholdismeasured.Systemtimingandvoltagebudgetsneedtoaccount forVREF(DC)deviationsfromtheoptimumpositionwithinthedata-eyeoftheinputsignals.

ThisalsoclarifiesthattheLPDDR3setup/holdspecificationandderatingvaluesneedtoincludetimeandvoltageasso-ciatedwithVREFac-noise.TimingandvoltageeffectsduetoAC-noiseonVREFuptothespecifiedlimit(+/-1%ofVD D) are included in LPDDR3 timings and their associated deratings.

Input Signal

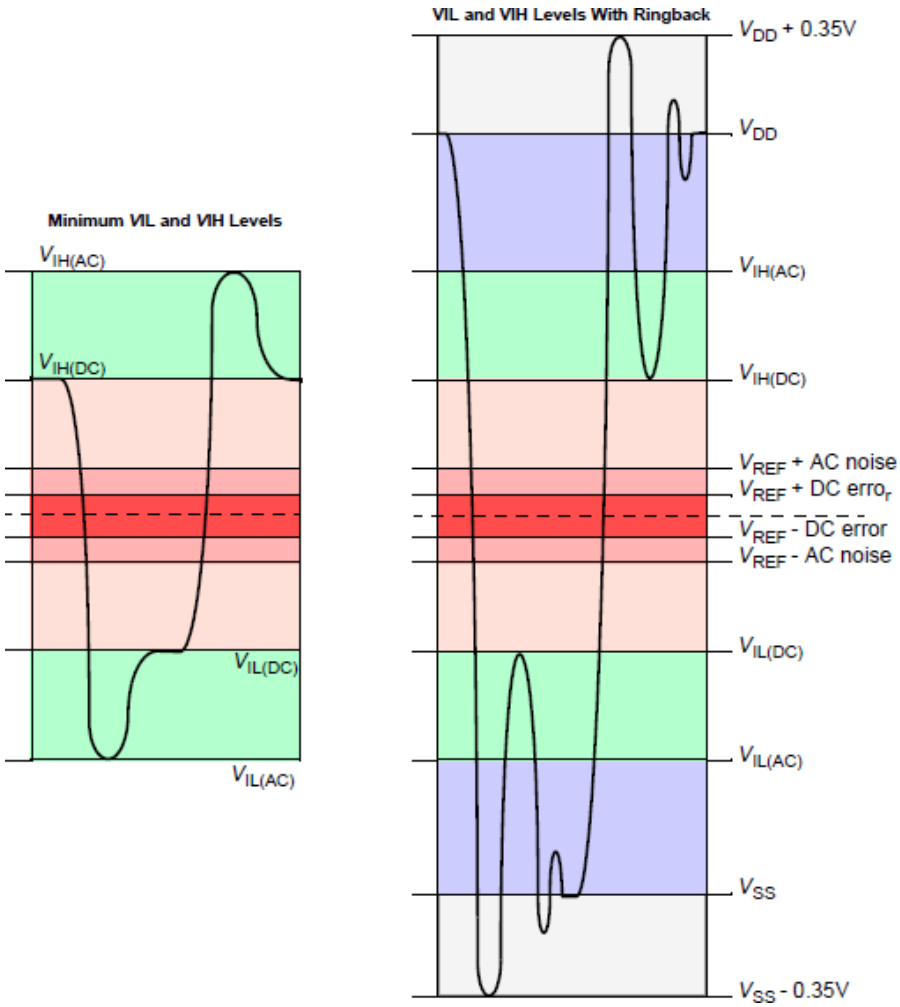


Figure. LPDDR3 Input signal

Note:
1. Numbers reflect nominalvalues.
2. For CA0-9, CK_t, CK_c and CS_n, VDD stands for VDDCA. For DQ, DM/DNV, DQS_t and DQS_c, VDD stands forVDDQ.
3. ForCA0-9,CK_t,CK_candCS_n,VSSstandsforVSSCA.ForDQ,DM/DNV,DQS_tandDQS_c,VSSstandsfor VSSQ.

AC and DC Logic Input Levels for Differential Signals

DifferentialSignalDefinition

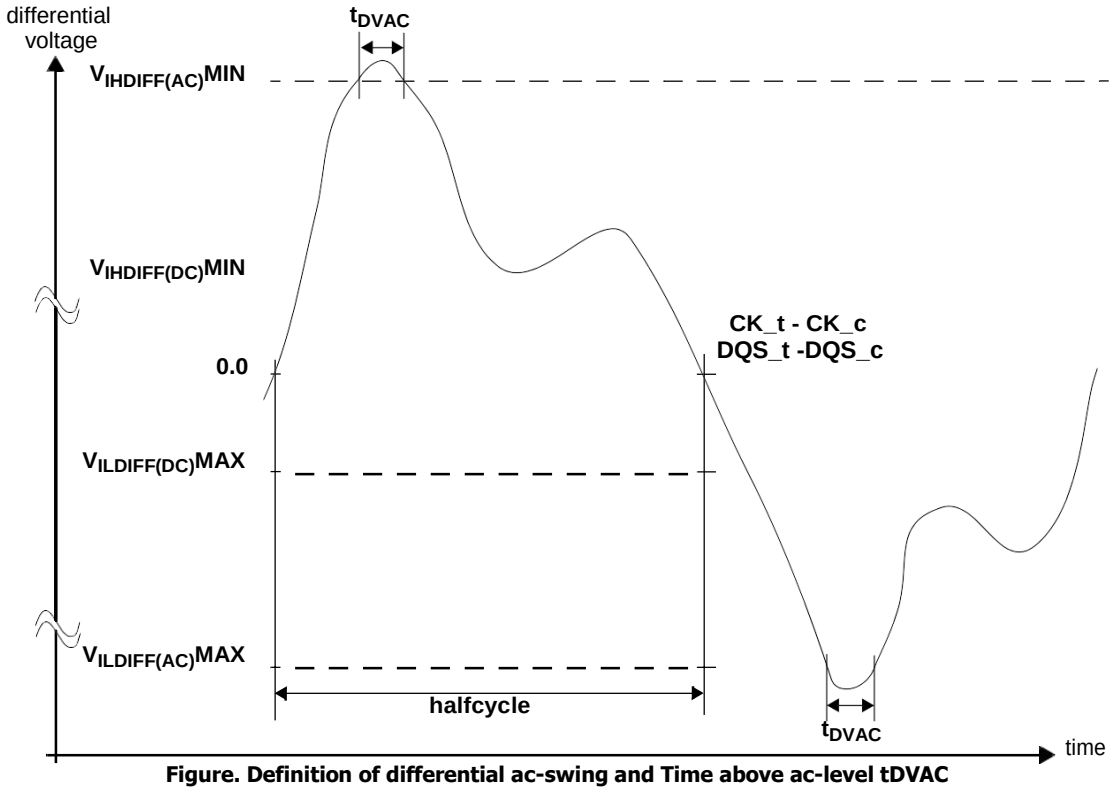


Figure. Definition of differential ac-swing and Time above ac-level tDVAC

Differential swing requirements for clock and strobe

Parameter	Symbol	Min	Max	Unit	Note
DC Differential Input High	VIHDIFF(DC)	2 x (VIH(DC) - VREF)	Note 3	V	1
DC Differential Input Low	VILDIFF(DC)	Note 3	2 x (VIL(DC) - VREF)	V	1
AC Differential Input High	VIHDIFF(AC)	2 x (VIH(AC) - VREF)	Note 3	V	2
AC Differential Input Low	VILDIFF(AC)	Note 3	2 x (VIL(AC) - VREF)	V	2

Note:
1.Used to define a differential signal slew-rate. For CK_t - CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2.For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits(VIH(dc)max,VIL(dc)min) forsingle-endedsignalsaswellasthelimitationsforovershootandundershoot.Referto thesection of "Overshoot and UndershootSpecifications".
4. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref= VrefDQ(DC).

Table. Allowed time before ringback (tDVAC) for DQS_t - DQS_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ |VIH/Ldiff(ac)|= 300mV	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 300mV
	1600Mbps	1333Mbps
	MIN	MIN
> 8.0	48	58
8.0	48	58
7.0	46	56
6.0	43	53
5.0	40	50
4.0	35	45
3.0	27	37
<3.0	27	37

Table. Allowed time before ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	t_{DVAC} [ps] @ |VIH/Ldiff(ac)|= 300mV	t_{DVAC} [ps] @ |VIH/Ldiff(ac)| = 300mV
	1600Mbps	1333Mbps
	MIN	MIN
> 8.0	48	58
8.0	48	58
7.0	46	56
6.0	43	53
5.0	40	50
4.0	35	45
3.0	27	37
<3.0	27	37

Single-ended Requirements for Differential Signals

Eachindividualcomponentofadifferentialsignal(CK_t,DQS_t,CK_c,orDQS_c)hasalsotocomplywith certain requirements for single-endedsignals.

CK_t and CK_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle.

DQS_t, DQS_c shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

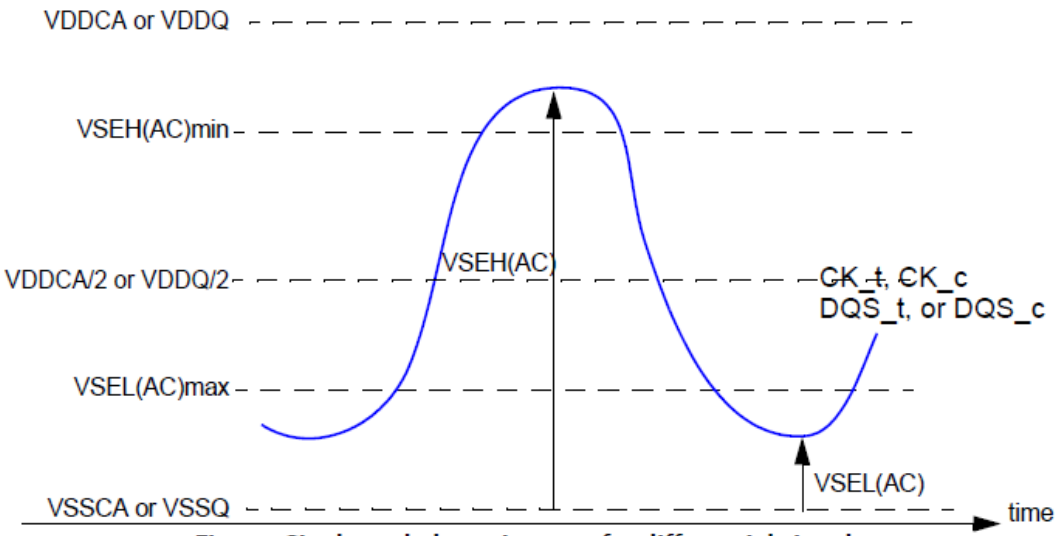


Figure. Single-ended requirement for differential signals

NotethatwhileCAandDQsignalrequirementsarewithrespecttoVREF,thesingle-endedcomponentsof differentialsignalshavearequirementwithrespecttoVDDQ/2forDQS_t,DQS_CandVDDCA/2forCK_t, CK_c; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measuresetuptime.Forsingle-endedcomponentsofdifferentialsignalstherequirementtoreach V SEL(AC)max, VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of thesesignals.

Table. Single-ended Levels for Clock and Strobe

Parameter	Symbol	Min	Max	Unit	Note
Single-ended High Level for strobes	VSEH (AC150)	(VDDQ/2) + 0.150	Note 3	V	1, 2
Single-ended High Level for CK_t and CK_c		(VDDCA/2) + 0.150	Note 3	V	1, 2
Single-ended Low Level for strobes	VSEL (AC150)	Note 3	(VDDQ / 2) - 0.150	V	1, 2
Single-ended Low Level for CK_t and CK_c		Note 3	(VDDCA / 2) - 0.150	V	1, 2
Single-ended High Level for strobes	VSEH (AC135)	(VDDQ/2) + 0.135	Note 3	V	1, 2
Single-ended High Level for CK_t and CK_c		(VDDCA/2) + 0.135	Note 3	V	1, 2
Single-ended Low Level for strobes	VSEL (AC135)	Note 3	(VDDQ / 2) - 0.135	V	1, 2
Single-ended Low Level for CK_t and CK_c		Note 3	(VDDCA / 2) - 0.135	V	1, 2

Note:
1. ForCK_t,CK_cuseVSEH/VSEL(AC)ofCA;for strobes(DQS0_t,DQS0_c,DQS1_t,DQS1_c,DQS2_t,DQS2_c,DQS3_t,DQS3_c) use VIH/VIL(AC) ofDQs.
2. IH(AC)/VIL(AC)forDQsisbasedonVREFDQ;VSEH(AC)/VSEL(AC)forCAisbasedonVREFCA;ifareducedac-highorac-lowlevel is used for a signal group, then the reduced level applies alsohere.
3. Thesevaluesarenotdefined,howeverthesingle-endedsignalsCK_t,CK_c,DQS0_t,DQS0_c,DQS1_t,DQS1_c,DQS2_t,DQS2_c, DQS3_t,DQS3_cneedtobewithintherespectivelimits(VIH(DC)max,VIL(DC)min)forsingle-endedsignalsaswellasthelimitations forovershootandundershoot.RefertothesectionofOvershootandUndershootSpecifications.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in "Single-end- ed Levels for Clock and Strobe". The differential input cross point voltage VIX is measured from the actual cross p oint of true and complement signals to the mid level between of VDD and VSS.

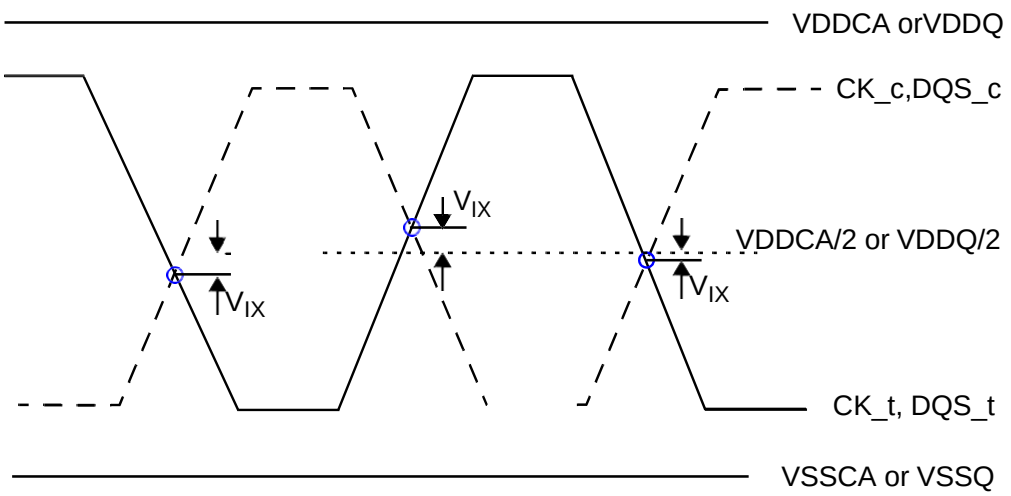


Figure. VIX definition

Table. Cross Point Voltage for Differential Input Signals (Clock and Strobe)

Parameter	Symbol	Min	Max	Unit	Note
Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t and CK_c	VIXCA	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t and DQS_c	VIXDQ	-120	120	mV	1, 2

Note:

1. The typical value of VIX(AC) is expected to be about 0.5 x VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, VREF = VREFCA(DC). For DQS_t and DQS_c, VREF= VREFDQ(DC).

Slew Rate Definitions for Single-ended Input Signals

See"CAandCS_nSetup,HoldandDerating"forsingle-endedslewratedefinitionsforaddressandcommandsignals.
See"DataSetup,HoldandSlewRateDerating"forsingle-endedslewratedefinitionsfordatasignals.

Slew Rate Definitions for Differential Input Signals

Inputslewratefordifferentialsignals(CK_t,CK_candDQS_t,DQS_c)aredefinedandmeasuredasshowninthetable and figurebelow.

Table. Differential Input Slew Rate Definition

Parameter	Measured		Defined by
	From	To	
Differential Input Slew Rate for Rising Edge (CK_t - CK_c and DQS_t - DQS_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / Delta TRdiff
Differential Input Slew Rate for Falling Edge (CK_t - CK_c and DQS_t - DQS_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / Delta TFdiff

Note: 1. The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds.

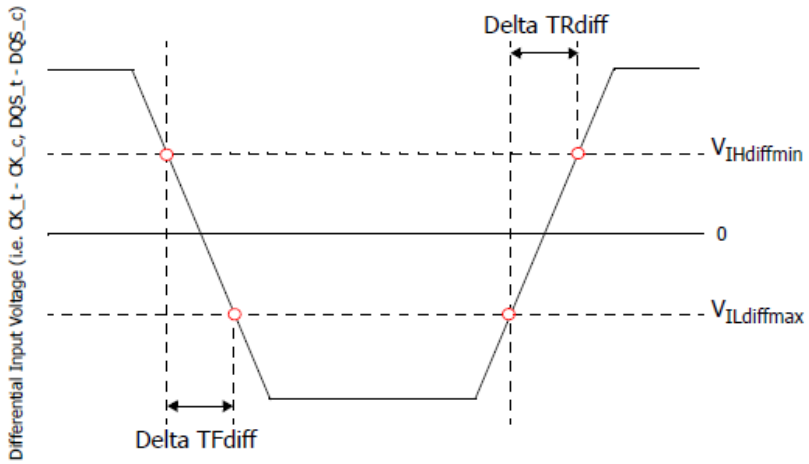


Figure. Differential Input Slew Rate Definition for CK_t, CK_c and DQS_t, DQS_c

AC and DC Output Measurement Levels

Single Ended AC and DC Output Levels

Parameter		Symbol	Levels	Unit	Note
DC Output Logic High Measurement Level (for IV curve linearity)		VOH(DC)	0.9 x VDDQ	V	1
DC Output Logic Low Measurement Level (for IV curve linearity)		VOL(DC) ODT disabled	0.1 x VDDQ	V	2
		VOL(DC) ODT enabled	VDDQ * [0.1 + 0.9 * (RON/ (RTT+RON))]	V	3
AC Output Logic High Measurement Level (for output slew rate)		VOH(AC)	VREFDQ + 0.12	V	
AC Output Logic Low Measurement Level (for output slew rate)		VOL(AC)	VREFDQ - 0.12	V	
Output Leakage current (DQ, DM, DQS_t and DQS_c) (DQ, DQS_t and DQS_c are disabled; 0V ≤VOUT ≤VDDQ)	Min	I_{OZ}	-5	uA	
	Max		5	uA	
Delta RON between pull-up and pull-down for DQ and DM	Min	MM_{PUPD}	-15	%	
	Max		15	%	

Note:
1. IOH = -0.1mA,
2. IOL =0.1mA
3. The min value is derived when using RTT, min and RON,max (+/- 30% uncalibrated,+/-15% calibrated).

Differential AC and DC Output Levels (DQS_t, DQS_c)

Parameter	Symbol	Levels	Unit	Note
AC Differential Output High measurement Level (for Output SR)	VOHdiff(AC)	+ 0.20 x VDDQ	V	
AC Differential Output Low measurement Level (for Output SR)	VOLdiff(AC)	- 0.20 x VDDQ	V	

Note:
1. IOH = -0.1mA,
2. IOL = 0.1mA

Single Ended Output Slew Rate

Withthereferenceloadfortimingmeasurements,outputslewrateforfallingandrisingedgesisdefinedandmeasuredbetweenVOL(AC)andVOH(AC)forsingleendedsignalsasshowninbelowTableandFigure.

Parameter	Measured		Defined by
	From	To	
Single Ended Output Slew Rate for Rising Edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / Delta TRse
Single Ended Output Slew Rate for Falling Edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / Delta TFse

Note: Output slew rate is verified by design and characterization and may not be subject to production test.

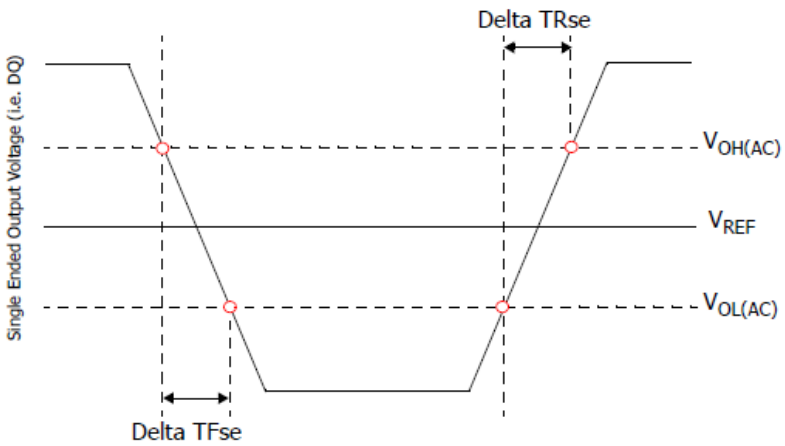


Figure. Single Ended Output Slew Rate Definition

Table. Output Slew Rate (Single Ended)

Parameter	Symbol	Min	Max	Unit	Note
Single-ended Output Slew Rate (RON = 40Ω+/- 30%)	SRQse	1.5	4.0	V/ns	
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4		

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

Note:

1. Measured with output referenceload.
2. Theratio ofpull-uptopull-downslewrateisspecifiedforthesametemperatureand voltage, overtheentiretemperature andvoltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC)and VOH(AC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per databyte switching.

Differential Output Slew Rate

Withthereferenceloadfortimingmeasurements,outputslewrateforfallingandrisingedgesisdefinedandmeasured betweenVOLdiff(AC)andVOHdiff(AC)fordifferentialsignalsasshowninbelowTableandFigure.

Parameter	Measured		Defined by
	From	To	
Differential Output Slew Rate for Rising Edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / Delta TRdiff
Differential Output Slew Rate for Falling Edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / Delta TFdiff

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

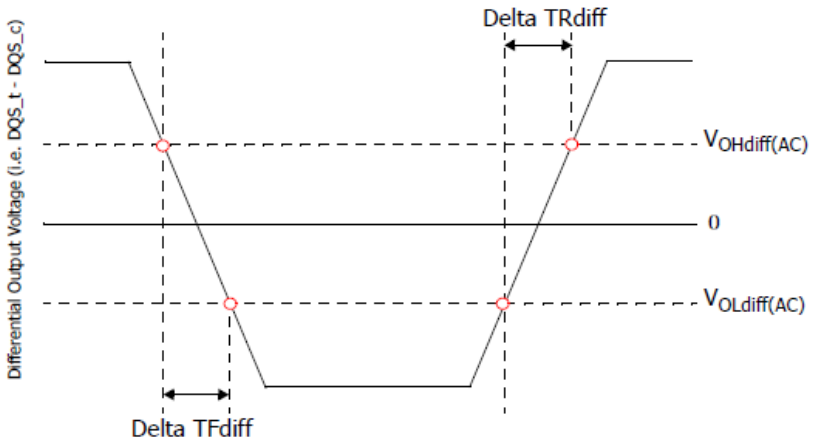


Figure. Differential Output Slew Rate Definition

Table. Output Slew Rate (Differential)

Parameter	Symbol	Min	Max	Unit	Note
Differential Output Slew Rate (RON = 40Ω+/- 30%)	SRQdiff	3.0	8.0	V/ns	

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

Note:

1. Measured with output referenceload.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC)and VOH(AC).
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byteswitching.

Overshoot and Undershoot Specifications

Parameter	1600	1333	Unit
Maximum peak amplitude allowed for overshoot area	0.35		V
Maximum peak amplitude allowed for undershoot area	0.35		V
Maximum overshoot area above VDD	0.10	0.12	V-ns
Maximum undershoot area below VSS	0.10	0.12	V-ns

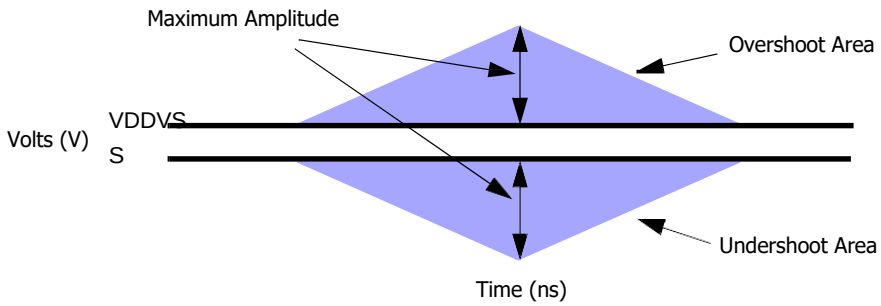


Figure.OvershootandUndershootDefinition

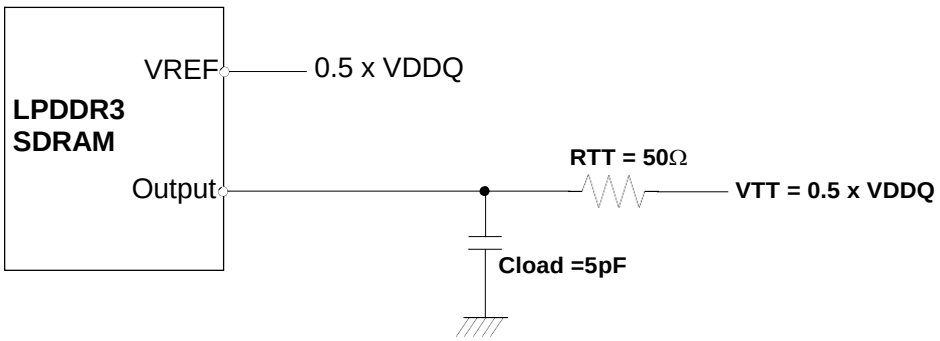
Note:

1. VDDstandsforVDDCAforCA0-9,CK_t,CK_c,CS_n,andCKE.VDDstandsforVDDQforDQ,DM,ODT,DQS_t,andDQS_c.
2. VSSstandsforVSSCAforCA0-9,CK_t,CK_c,CS_n,andCKE.VSSstandsforVSSQforDQ,DM,ODT,DQS_t,andDQS_c.
3. Absolute maximum requirementsapply.
4. Maximum peak amplitude values are referenced from actual VDD andVSS values.
5. Maximum area values are referenced from maximum operating VDD andVSS values.

Output Buffer Characteristics

HSUL_12 Driver Output Timing Reference Load

These'TimingReferenceLoads'arenotintendedasapreciserepresentationofanyparticularsystemenvironmentor adepictionoftheactualloadpresentedbyaproductiontester.Systemdesignersshouldu seIBISorothersimulation toolstocorrelatethetimingreferenceloadtoasystemenvironment.Manufacturerscorrelatetotheirproductiontest conditions,generallyoneormorecoaxialtransmissionlinesterminatedatthetesterelectronics.



Note: 1. All output timing parameter values (like t_{DQSCK}, t_{DQSQ}, t_{QHS}, t_{HZ}, t_{RPRE}etc.) are reported with respect to this reference load. This reference load is also used to report slewrate.

Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

$RONPU$ and $RONPD$ resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note 1: This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note 1: This is under the condition that RON_{PU} is turned off

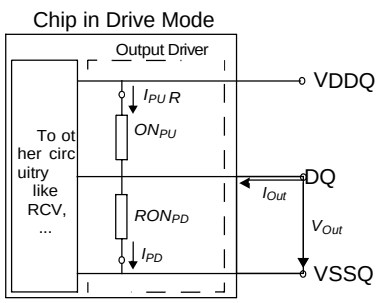


Figure. Output Driver: Definition of Voltages and Currents

RON_{PU} and RON_{PD} Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table - Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Typ	Max	Unit	Notes
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
Mismatch between pull-up and pull-down	MM_{PUPD}		-15.00		+15.00	%	1,2,3,4,5

Note:

1.Acrossentireoperatingtemperaturerange,aftercalibration. 2.
RZQ =240Ω.

3. Thetolerancelimitsarespecifiedaftercalibrationwithfixedvoltageandtemperature.Forbehaviorofthetoler-a nce limits if temperature or voltage changes after calibration, see following section on voltage and temperature se nsitivity.

4. Pull-downandpull-upoutputdriverimpedancesarerecommendedtobecalibratedat0.5xVDDQ.

5. Measurementdefinitionformismatchbetweenpull-upandpull-do wn,MMPUPD:MeasureRON_{PU}andRON_{PD},bothat0.5xVDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

6. Output driver strength measured withoutODT.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table. Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Notes
RONPD	0.5 x VDDQ	85 - (*dRONdT* x |*ΔT*|) - (*dRONdV* x |*ΔV*|)	115+(*dRONdT* x |*ΔT*|)+(*dRONdV* x |*ΔV*|)	%	1,2
RONPU					
RTT	0.5 x VDDQ	85 - (*dRTTdT* x |*ΔT*|) - (*dRTTdV* x |*ΔV*|)	115 + (*dRTTdT* x |*ΔT*|) + (*dRTTdV* x |*ΔV*|)	%	1,2

Note
1. *ΔT=T-T*(@calibration),*ΔV=V-V*(@calibration)
2. dRONdTanddRONdVarenotsubjecttoproductiontestbutareverifiedbydesign andcharacterization.

Table. Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV
dRTTdT	RTT Temperature Sensitivity	0.00	0.75	% / C
dRTTdV	RTT Voltage Sensitivity	0.00	0.20	% / mV

RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table. Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Notes
34.3Ω	RON40PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON40PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω (optional)	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω (optional)	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1

Note:
1. Across entire operating temperature range, without calibration.

RZQ I-V Curve

Table. RZQ I-V Curve

Voltage(V)	RON = 240Ω(RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ω]				Current [mA] / RON [Ω]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

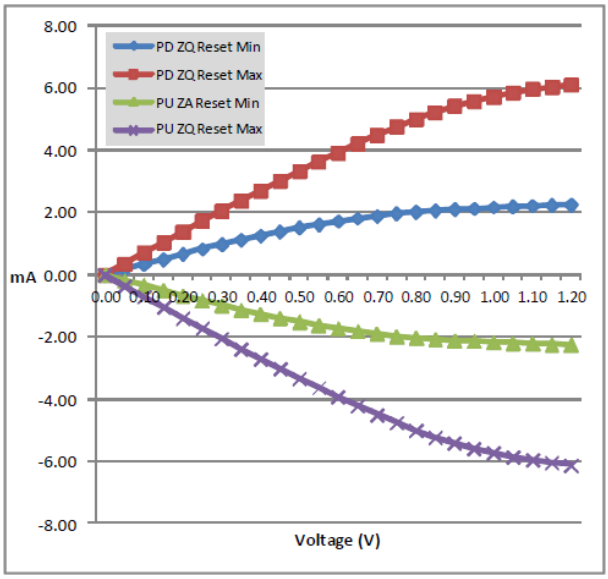


Figure. I-V Curve After ZQ Reset

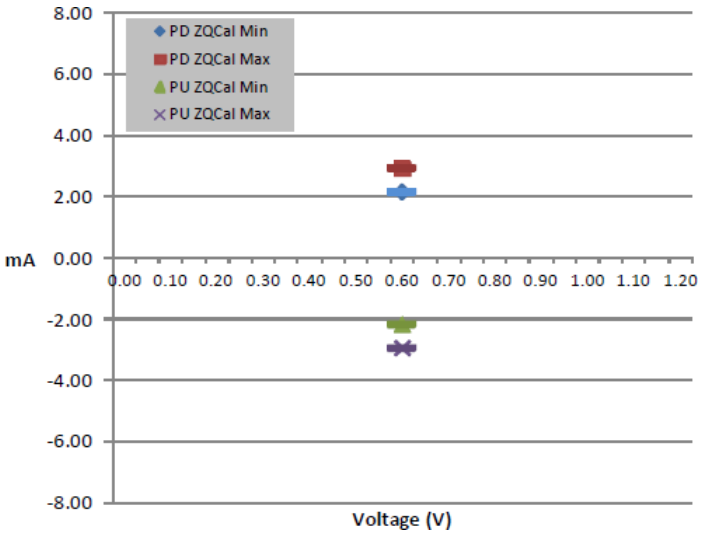


Figure. I-V Curve After Calibration

ODT Levels and I-V Characteristics

On-DieTerminationeffectiveresistance,RTT,isdefinedbymoderegisterMR11[1:0].ODTisappliedtotheDQ,DM, andDQS_t/DQS_cpins.Afunctionalrepresentationoftheon-dieterminationisshowninthefigurebelow.RTTisde- fined by the followingformula:

RTTPU = (VDDQ - VOut) / | IOut |

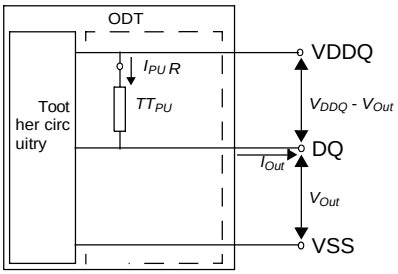


Table. ODT DC Electrical Characteristics, assuming RZQ = 240 ohm after proper ZQ calibration

RTT (ohm)	VOUT (V)	IOUT	
		Min (mA)	Max (mA)
RZQ/1	0.6	-2.17	-2.94
RZQ/2	0.6	-4.34	-5.88
RZQ/4	0.6	-8.68	-11.76

Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit	Note
Input capacitance, CK_t and CK_c	CCK	0.5	1.2	pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	0	0.15	pF	1,2,3
Input capacitance, all other input-only pins	CI	0.5	1.1	pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	-0.2	0.2	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	1.0	1.8	pF	1,2,6,7
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	0	0.2	pF	1,2,7,8
Input/output capacitance delta, DQ and DM	CDIO	-0.25	0.25	pF	1,2,7,9
Input/Output Capacitance ZQ	CZQ	0	2.0	pF	1,2

(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

Note:

1. This parameter applies to die device only (does not includepackage capacitance).
2. Thisparameteris notsubjecttoproductiontest.It isverifiedbydesignandcharacterization.Thecapacitanceismeasured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pinsfloating).
3. Absolute value of CCK_t -CCK_c.
4. CI applies to CS_n, CKE,CA0-CA9.
5. CDI = CI - 0.5 * (CCK_t +CCK_c)
6. DM loading matches DQ andDQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3Ohm typical)
8. Absolute value of CDQS_t andCDQS_c.
9. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) inbyte-lane.

IDD Specification Parameters and Test Conditions

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: $V_{IN} \leq V_{IL}$(DC) MAX HIGH:

VIN $\geq V_{IH}$(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level.

SWITCHING: See tables below.

Table. Switching for CA Input Signals

Switching for CA								
	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) / CK_c (Rising)	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) / CK_c (Rising)	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) / CK_c (Rising)	CK_t (Rising) /CK_c (Falling)	CK_t (Falling) / CK_c (Rising)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note:

1. CS_n must always be drivenHIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW once per clock for theCA bus.
3. Theabovepattern(N,N+1,N+2,N+3...) isusedcontinuouslyduringIDDmeasurementforIDDvaluesthatrequireswitching on the CAbus.

Table. Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQs
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N+3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+3	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N+4	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N+4	Read_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+7	NOP	HLH	LHLHLHL	L

Note:
1. Data strobe (DQS) is changing between HIGH and LOW every clockcycle.
2. The above pattern (N, N+1, ...) is used continuously during IDD measurement forIDD4R.

Table. Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA[0:2]	CA[3:9]	All DQs
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N+3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N+3	NOP	HLL	HLHLLHL	L
Rising	HIGH	LOW	N+4	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N+4	Write_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N+6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N+7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N+7	NOP	HLL	LHLHLHL	L

Note:
1. Data strobe (DQS) is changing between HIGH and LOW every clockcycle.
2. Data masking (DM) must always be drivenLOW.
3. The above pattern (N, N+1…) is used continuously during IDD measurement forIDD4W.

IDD specifications (1/2)

- All IDD values are single-die-equivalent values. Total current consumption is dependent on user operating condition.

Parameter / Condition	Symbol	Power Supply	1600	Unit	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD0_1$	VDD1	18	mA	
	$IDD0_2$	VDD2 VDDCA	28	mA	
	$IDD0_{IN}$	VDDQ	0.2	mA	4
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS_n is HIGH; All banks are idle; CAbusinputsareswitching;Databusinputsare stable ODTdisabled	$IDD2P_1$	VDD1	0.9	mA	
	$IDD2P_2$	VDD2 VDDCA	3	mA	
	$IDD2P_{IN}$	VDDQ	0.2	mA	4,8
Idle power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks areidle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2PS_1$	VDD1	0.9	mA	
	$IDD2PS_2$	VDD2 VDDCA	3	mA	
	$IDD2PS_{IN}$	VDDQ	0.2	mA	4,8
Idle non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2N_1$	VDD1	1.1	mA	
	$IDD2N_2$	VDD2 VDDCA	15	mA	
	$IDD2N_{IN}$	VDDQ	0.2	mA	4
Idle non-power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2NS_1$	VDD1	1.1	mA	
	$IDD2NS_2$	VDD2 VDDCA	15	mA	
	$IDD2NS_{IN}$	VDDQ	0.2	mA	4
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3P_1$	VDD1	3.3	mA	
	$IDD3P_2$	VDD2 VDDCA	6	mA	
	$IDD3P_{IN}$	VDDQ	0.2	mA	4,8
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3PS_1$	VDD1	3.3	mA	
	$IDD3PS_2$	VDD2 VDDCA	6	mA	
	$IDD3PS_{IN}$	VDDQ	0.2	mA	4,8
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3N_1$	VDD1	3.3	mA	
	$IDD3N_2$	VDD2 VDDCA	18	mA	
	$IDD3N_{IN}$	VDDQ	0.2	mA	4

IDD specifications (2/2)

- All IDD values are single-die-equivalent values. Total current consumption is dependent on user operating condition.

Parameter / Test Condition	Symbol	Power Supply	1600		Unit	Note
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3NS_1$	VDD1	3		mA	
	$IDD3NS_2$	VDD2 VDDCA	15		mA	
	$IDD3NS_{IN}$	VDDQ	0.2		mA	4
Operating burst READ current: tCK = tCKmin; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	20	18	mA	
	$IDD4R_2$	VDD2 VDDCA	200	180	mA	
	$IDD4R_{IN}$	VDDQ	275	250	mA	
Operating burst WRITE current: tCK = tCKmin; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4W_1$	VDD1	16	14	mA	
	$IDD4W_2$	VDD2 VDDCA	180	160	mA	
	$IDD4W_{IN}$	VDDQ	55	50	mA	4
All-bank REFRESH burst current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD5_1$	VDD1	80		mA	
	$IDD5_2$	VDD2 VDDCA	120		mA	
	$IDD5_{IN}$	VDDQ	0.2		mA	4
All-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD5ab_1$	VDD1	5		mA	
	$IDD5ab_2$	VDD2 VDDCA	20		mA	
	$IDD5ab_{IN}$	VDDQ	0.2		mA	4
Per-bank REFRESH average current: tCK = tCKmin; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD5pb_1$	VDD1	5		mA	
	$IDD5pb_2$	VDD2 VDDCA	20		mA	
	$IDD5pb_{IN}$	VDDQ	0.2		mA	4
Self refresh current (0°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable Maximum 1x self refresh rate ODT disabled	$IDD6_1$	VDD1	4		mA	6
	$IDD6_2$	VDD2 VDDCA	7.7		mA	6
	$IDD6_{IN}$	VDDQ	0.2		mA	4,6,8

Note:

1. PublishedIDDvaluesarethemaximumofthedistributionofthearithmeticmean.
2. IDDcurrentspecificationsaretestedafterthedeviceis properlyinitialized.
3. The1xselfrefreshrateistherateatwhichthedeviceisrefreshedinternallyduringself refresh,beforegoingintotheelevated temperaturerange.
4. Measured currents are the summation of VDDQand VDDCA.
5. Guaranteedbydesignwithoutputload =TBDpFandRON=40ohm.
6. Thisis thegeneraldefinitionthatappliestofull-arraySELFREFRESH.
7. IDD6ET is a typical value, is sampled only, and is nottested.
8. For all IDD measurements, VIHCKE = 0.8 x VDDCA, VILCKE = 0.2 xVDDCA.
9. DPD(DeepPowerdown)functionisan optionalfeature.PleasecontactSKhynixformoreinformationtousethisfeature

AC TIMING PARAMETERS (1/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Maximum clock Frequency		-	800	667	MHz	
Clock Timing						
Average Clock Period	tCK(avg)	min	1.25	1.5	ns	
		max	100			
Average high pulse width	tCH(avg)	min	0.45		tCK(avg)	
		max	0.55			
Average low pulse width	tCL(avg)	min	0.45		tCK(avg)	
		max	0.55			
Absolute Clock Period	tCK(abs)	min	tCK(avg)min + tJIT(per)min		ns	
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min	0.43		tCK(avg)	
		max	0.57			
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min	0.43		tCK(avg)	
		max	0.57			
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min	-70	-80	ps	
		max	70	80		
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max	140	160	ps	
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min	min((tCH(abs)min - tCH(avg)min), (tCL(abs)min - tCL(avg)min)) * tCK(avg)		ps	
		max	max((tCH(abs)max - tCH(avg)max), (tCH(abs)max- tCL(avg)max)) * tCK(avg)			
Cumulative error across 2 cycles	tERR(2per), allowed	min	-103	-118	ps	
		max	103	118		
Cumulative error across 3 cycles	tERR(3per), allowed	min	-122	-140	ps	
		max	122	140		
Cumulative error across 4 cycles	tERR(4per), allowed	min	-136	-155	ps	
		max	136	155		
Cumulative error across 5 cycles	tERR(5per), allowed	min	-147	-168	ps	
		max	147	168		
Cumulative error across 6 cycles	tERR(6per), allowed	min	-155	-177	ps	
		max	155	177		
Cumulative error across 7 cycles	tERR(7per), allowed	min	-163	-186	ps	
		max	163	186		
Cumulative error across 8 cycles	tERR(8per), allowed	min	-169	-193	ps	
		max	169	193		
Cumulative error across 9 cycles	tERR(9per), allowed	min	-175	-200	ps	
		max	175	200		
Cumulative error across 10 cycles	tERR(10per), allowed	min	-180	-205	ps	
		max	180	205		

AC TIMING PARAMETERS (2/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Clock Timing (continued)						
Cumulative error across 11 cycles	tERR(11per), allowed	min	-184	-210	ps	
		max	184	210		
Cumulative error across 12 cycles	tERR(12per), allowed	min	-188	-215	ps	
		max	188	215		
Cumulative error across n cycles (n = 13, 14 ,. . . ,20)	tERR(nper), allowed	min	tERR(nper),allowed min = (1 + 0.68ln(n)) * tJIT(per),allowed min		ps	
		max	tERR(nper),allowed max = (1 + 0.68ln(n)) * tJIT(per),allowed max			
ZQ Calibration Parameters						
Initialization Calibration Time	tZQINIT	min	1		us	
Long Calibration Time	tZQCL	min	360		ns	
Short Calibration Time	tZQCS	min	90		ns	
Calibration Reset Time	tZQRESET	min	max(50ns, 3nCK)		ns	
Read Parameters						3
DQS output access time from CK/CK#	tDQSCK	min	2.5		ns	
		max	5.5			
DQSCK Delta short	tDQSCKDS	max	220	265	ps	4
DQSCK Delta Medium	tDQSCKDM	max	511	593	ps	5
DQSCK Delta Long	tDQSCKDL	max	614	733	ps	6
DQS-DQ skew	tDQSQ	max	135	165	ps	
DQS Output High Pulse Width	tQSH	min	tCH(abs) - 0.05		tCK(avg)	
DQS Output Low Pulse Width	tQSL	min	tCL(abs) - 0.05		tCK(avg)	
DQ/DQS output hold time from DQS	tQH	min	MIN (tQSH, tQSL)		ps	
Read preamble	tRPRE	min	0.9		tCK(avg)	7,10
Read postamble	tRPST	min	0.3		tCK(avg)	7,11
DQS low-Z from clock	tLZ(DQS)	min	tDQSCK(min) - 300		ps	7
DQ low-Z from clock	tLZ(DQ)	min	tDQSCK(min) - 300		ps	7
DQS high-Z from clock	tHZ(DQS)	max	tDQSCK(max) - 100		ps	7
DQ high-Z from clock	tHZ(DQ)	max	tDQSCK(max) + (1.4 x tDQSQ-max)		ps	7

AC TIMING PARAMETERS (3/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Write Parameters						3
DQ and DM input setup time (Vref based)	tDS	min	150	175	ps	
DQ and DM input hold time (Vref based)	tDH	min	150	175	ps	
DQ and DM input pulse width	tDIPW	min	0.35		tCK(avg)	
Write command to 1st DQS latching transition	tDQSS	min	0.75		tCK(avg)	
		max	1.25			
DQS input high-level width	tDQSH	min	0.4		tCK(avg)	
DQS input low-level width	tDQSL	min	0.4		tCK(avg)	
DQS falling edge to CK setup time	tDSS	min	0.2		tCK(avg)	
DQS falling edge hold time from CK	tDSH	min	0.2		tCK(avg)	
Write postamble	tWPST	min	0.4		tCK(avg)	
Write preamble	tWPRE	min	0.8		tCK(avg)	
CKE Input Parameters						
CKE min. pulse width (high/low pulse width)	tCKE	min	max(7.5ns, 3nCK)		ns	
CKE input setup time	tISCKE	min	0.25		tCK(avg)	12
CKE input hold time	tIHCKE	min	0.25		tCK(avg)	13
Command path disable delay	tCPDED	min	2		tCK(avg)	
Command Address Input Parameters						3
Address and control input setup time	tISCA	min	150	175	ps	14
Address and control input hold time	tIHCA	min	150	175	ps	14
CS_n input setup time	tISCS	min	270	290	ps	14
CS_n input hold time	tIHCS	min	270	290	ps	14
Address and control input pulse width	tIPWCA	min	0.35		tCK(avg)	
CS_n input pulse width	tIPWCS	min	0.7		tCK(avg)	
Boot Parameters (10MHz-55MHz)						15,16, 17
Clock Cycle Time	tCKb	min	18		ns	
		max	100			
CKE Input Setup Time	tISCKEb	min	2.5		ns	
CKE Input Hold Time	tIHCKEb	min	2.5		ns	
Address & Control Input Setup Time	tISb	min	1150		ps	
Address & Control Input Hold Time	tIHb	min	1150		ps	
DQS Output Data Access Time from CK/CK#	tDQSCKb	min	2.0		ns	
		max	10.0			
Data Strobe Edge to Output Data Edge tDQSQb	tDQSQb	max	1.2		ns	
Mode Register Parameters						
MODE REGISTER Write command period	tMRW	min	10		tCK(avg)	
MODE REGISTER Read command period	tMRR	min	4		tCK(avg)	
Additional time after tXP has expired until MRR command may be issued	tMRRI	min	tRCD(MIN)		ns	

AC TIMING PARAMETERS (4/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
Core Parameters						18
Read Latency	RL	min	12	10	tCK(avg)	
Write Latency (Set A)	WL	min	6	6	tCK(avg)	
Write Latency (Set B)	WL	min	9	8	tCK(avg)	
ACTIVE to ACTIVE command period	tRC	min	tRAS+tRPab (with all-bank Precharge) tRAS+tRPpb (with per-bank Precharge)		ns	
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min	max(15ns, 3nCK)		ns	
Self refresh exit to next valid command delay	tXSR	min	max(tRFCab +10ns, 2nCK)		ns	
Exit power down to next valid command delay	tXP	min	max(7.5ns, 3nCK)		ns	
CAS to CAS delay	tCCD	min	4		tCK(avg)	
Internal Read to Precharge command delay	tRTP	min	max(7.5ns, 4nCK)		ns	
RAS to CAS Delay	tRCD	min	max(18ns, 3nCK)		ns	
Row Precharge Time (single bank)	tRPpb	min	max(18ns ,3nCK)		ns	
Row Precharge Time (all banks) - 8-bank	tRPab	min	max(21ns, 3nCK)		ns	
Row Active Time	tRAS	min	max(42ns, 3nCK)		ns	
		max	70,000			
Write Recovery Time	tWR	min	max(15ns, 4nCK)		ns	
Internal Write to Read Command Delay	tWTR	min	max(7.5ns, 4nCK)		ns	
Active bank A to Active bank B	tRRD	min	max(10ns, 2nCK)		ns	
Four Bank Activate Window	tFAW	min	max(50ns, 8nCK)		ns	
ODT Parameters						
Asynchronous RTT turn-on dely from ODT in- put	tODTon	min	1.75		ns	
		max	3.5			
Asynchronous RTT turn-off delay from ODT in- put	tODToff	min	1.75		ns	
		max	3.5			
Automatic RTT turn-on delay after READ data	tAODTon	max	tDQSCKmax + 1.4 * tDQSQ-max + tCK(avg,min)		ps	
Automatic RTT turn-off delay after READ data	tAODToff	min	tDQSCKmin - 300		ps	
RTT disable delay from power down and self-refresh	tODTd	min	12		ns	
RTTenabledelayfrompowerdownandselfre-freshexit	tODTe	max	12		ns	

AC TIMING PARAMETERS (5/5)

Parameter	Symbol	min max	LPDDR3 1600	LPDDR3 1333	Unit	Note
CA Training Parameters						
First CA calibratino command after CA calibration mode is programmed	tCAMRD	min	20		tCK(avg)	
First CA calibratino command after CKE is LOW	tCAENT	min	10		tCK(avg)	
CA calibration exit command after CKE is HIGH	tCAEXT	min	10		tCK(avg)	
CKE LOW after CA calibration mode is programmed	tCACKEL	min	10		tCK(avg)	
CKE HIGH after the last CA calibration results are driven	tCACKEH	min	10		tCK(avg)	
Data out delay after CA training calibration command is programmed	tADR	max	20		ns	
MRW CA exit command to DQ tri-state	tMRZ	min	3		ns	
CA calibration command to CA calibration command delay	tCACD	min	RU(tADR+2*tCK)		tCK(avg)	
Write Leveling Parameters						
DQS_t/DQS_cdelayafterwritelevelingmodeis programmed	tWLDQSEN	min	25		ns	
		max	-			
First DQS_t/DQS_c edge after write leveling mode is programmed	tWLMRD	min	40		ns	
		max	-			
Write leveling output delay	tWLO	min	0		ns	
		max	20			
Write leveling hold time	tWLH	min	150	135	ps	
Write leveling setup time	tWLS	min	150	135	ps	
Mode register set command delay	tMRD	min	Max(14ns, 10nCK)		ns	
		max	-			
Temperature De-Rating						17
tDQSCK De-Rating	tDQSCK (Derated)	max	5620		ps	
Core Timings Temperature De-Rating	tRCD (Derated)	min	tRCD + 1.875		ns	
	tRC (Derated)	min	tRC + 1.875		ns	
	tRAS (Derated)	min	tRAS + 1.875		ns	
	tRP (Derated)	min	tRP + 1.875		ns	
	tRRD (Derated)	min	tRRD + 1.875		ns	

Note:
1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine devicecapabilities.
2. All AC timings assume an input slew rate of 2V/ns.
3. Measured with 4V/ns differential CK_t/CK_c slew rate and nominalVIX.
4. All timing and voltage measurements are defined 'at theball'.
5. READ, WRITE, and input setup and hold values are referencedto VREF.
6. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clockjitter.
7. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clockjitter.
8. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not in clude clockjitter.
9. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure shows a method to calculate the point when deviceisno longerdrivingtHZ(DQS)andtHZ(DQ),orbeginsdrivingtLZ(DQS),tLZ(DQ)bymeasuringthesignalattwodifferent voltages. The actual voltage measurement points are not critical as long as the calculationis consistent.
10. Output TransitionTiming

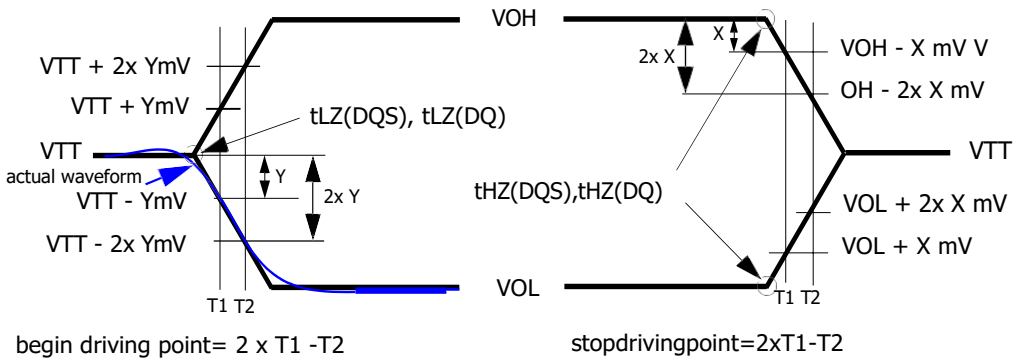


Figure. HSUL_12 Driver Output Reference Load for Timing and Slew Rate

11. TheparameterstLZ(DQS),tLZ(DQ),tHZ(DQS),andtHZ(DQ)aredefinedassingle-ended.ThetimingparameterstRPREandtRPST are determined from the differential signalDQS/DQS#.
12. MeasuredfromthepointwhenDQS_t/DQS_cbeginsdrivingthesignaltothepointwhenDQS_t/DQS_cbeginsdrivingthefirst rising strobeedge.
13. MeasuredfromthelastfallingstrobeedgeofDQS_t/DQS_ctothepointwhenDQS_t/DQS_cfinishesdrivingthesignal.
14. CKEinputsetuptimeismeasuredfromCKEreachingaHIGH/LOWvoltageleveltoCK_t/CK_ccrossing.
15. CKEinputholdtimeismeasuredfromCK_t/CK_ccrossingtoCKEreachingaHIGH/LOWvoltagelevel.
16. Input set-up/hold time for signal (CA[9:0],CS_n).
17. Toensuredeviceoperationbeforethedeviceisconfigured,anumberofACboot-timingparametersaredefined inthistable.Boot parametersymbolshavetheletterbappended(forexample,tCKduringbootistCKb).
18. The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as specified in "Mode RegisterDefinition".
19. Theoutputskew parametersaremeasuredwithdefaultoutputimpedancesettingsusingthereferenceload.
20. The minimum tCK column applies only when tCK is greaterthan 6ns.

CA and CS_n Setup, Hold and Derating

ForallinputsignalsCAandCS_nthetotaltIS(setuptime)andtIH(holdtime)requirediscalculatedbyaddingthe datasheettIS(base)andtIH(base)valuetotheΔtISandΔtIHderatingvaluerespectively.Example:tIS(totalsetupti me) = tIS(base) +ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and thefirstcrossingofVIH(AC)min.Setup(tIS)nominalslewrateforafallingsignalisdefinedastheslewratebetweent helastcrossingofVREF(DC)andthefirstcrossingofVIL(AC)max.Iftheactualsignalisalwaysearlierthanthenom-i nalslewratelinebetweenshaded`VREF(DC)toacregion',usenominalslewrateforderatingvalue.Iftheactualsig- nalislaterthanthenominalslewratelineanywherebetweenshaded`VREF(DC)toacregion',theslewrateofa t angentlinetotheactualsignalfromtheacleveltodclevelis usedforderatingvalue.

Hold(tIH)nominalslewrateforarisingsignalisdefinedastheslewratebetweenthelastcrossingofVIL(DC)maxand thefirstcrossingofVREF(DC).Hold(tIH)nominalslewrateforafallingsignalisdefinedastheslewratebetweenthe lastcrossingofVIH(DC)minandthefirstcrossingofVREF(DC).Iftheactualsignalisalwayslaterthanthenominals lewratelinebetweenshaded`DCtoVREF(DC)region',usenominalslewrateforderatingvalue.Iftheactualsignali searlierthanthenominalslewratelineanywherebetweenshaded`DCtoVREF(DC)region',theslewrateofatan-g entlinetotheactualsignalfromthedc leveltoVREF(DC)levelis usedforderatingvalue.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Althoughforslowslewratesthetotalsetuptimemightbenegative(i.e.avalidinputsignalwillnothavereachedVIH/ IL(AC)atthetimeoftherisingclocktransition)avalidinputsignalisstillrequiredtocompletethetransitionandreach VIH/IL(AC).

For slew rates in between the values listed in Table, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table. CA Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tIS(base)	75	100	VIH/L(AC)=VREF(DC)+/-150mV
tIS(base)	-	-	VIH/L(AC)=VREF(DC)+/-135mV
tIH(base)	100	125	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns CA slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table. CS_n Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tIS(base)	195	215	VIH/L(AC)=VREF(DC)+/-150mV
tIS(base)	-	-	VIH/L(AC)=VREF(DC)+/-135mV
tIH(base)	220	240	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns CS_n slew rate and 4V/ns differential CK_t/CK_c slew rate.

Table. Derating values tIS/tIH - ac/dc based AC150

		ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	0	0	13	13
	1.5							-25	-17	-25	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Derating values tIS/tIH - ac/dc based AC135

		ΔtISCA, ΔtIHCA, ΔtISCS, ΔtIHCS derating in [ps] AC/DC based AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25		
	3.0			23	17	23	17	23	17	23	17	34	29
	2.0					0	0	0	0	0	0	11	13
	1.5							-23	-17	-23	-17	-12	-4

Note 1: Cell contents shaded in red are defined as 'not supported'

Table. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} [ps] @150mV		t_{VAC} [ps] @150mV	
	1600Mbps		1333Mbps	
	MIN	MAX	MIN	MAX
> 4.0	48	-	58	-
4.0	48	-	58	-
3.5	46	-	56	-
3.0	43	-	53	-
2.5	40	-	50	-
2.0	35	-	45	-
1.5	27	-	37	-
<1.5	27	-	37	-

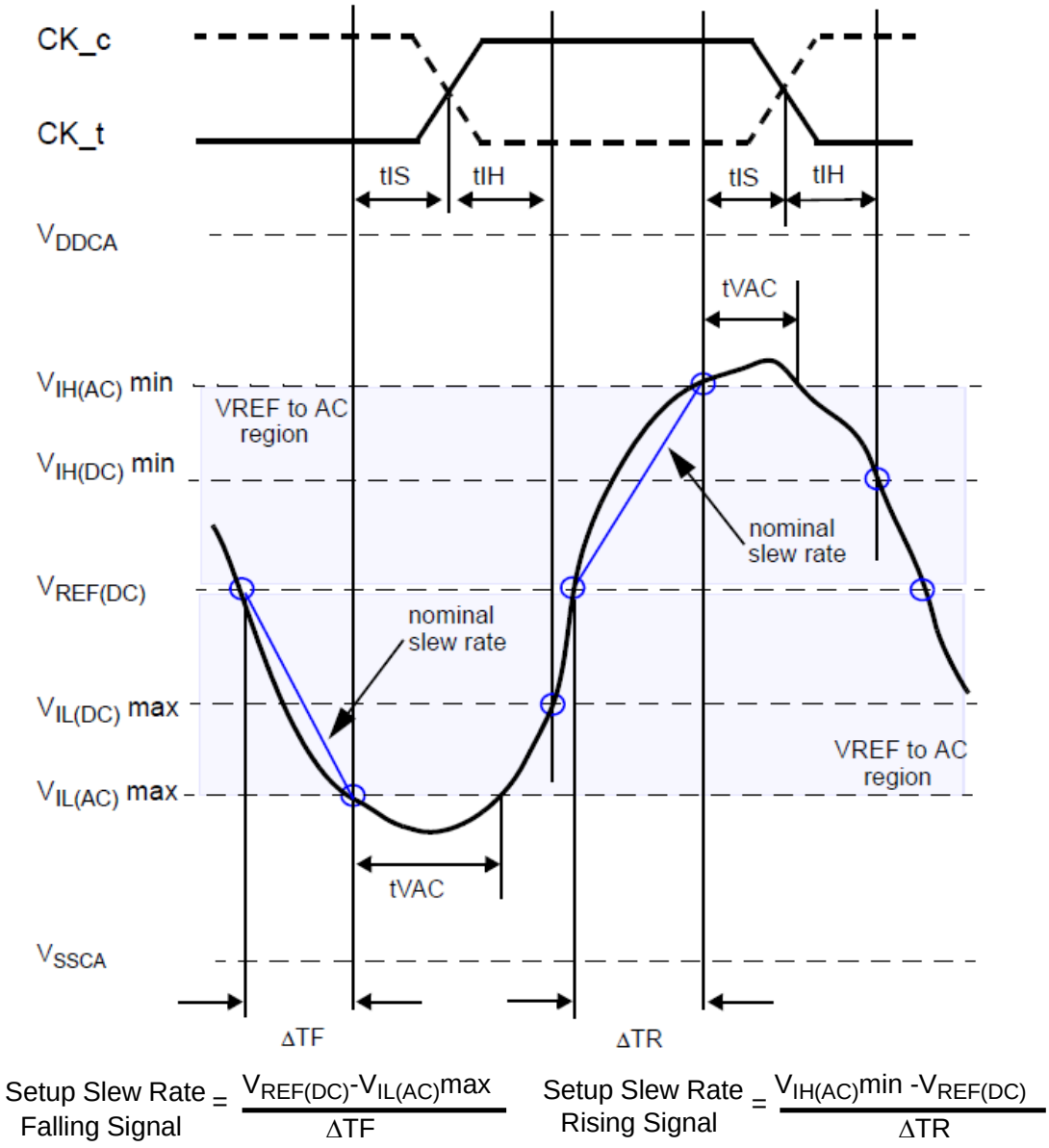
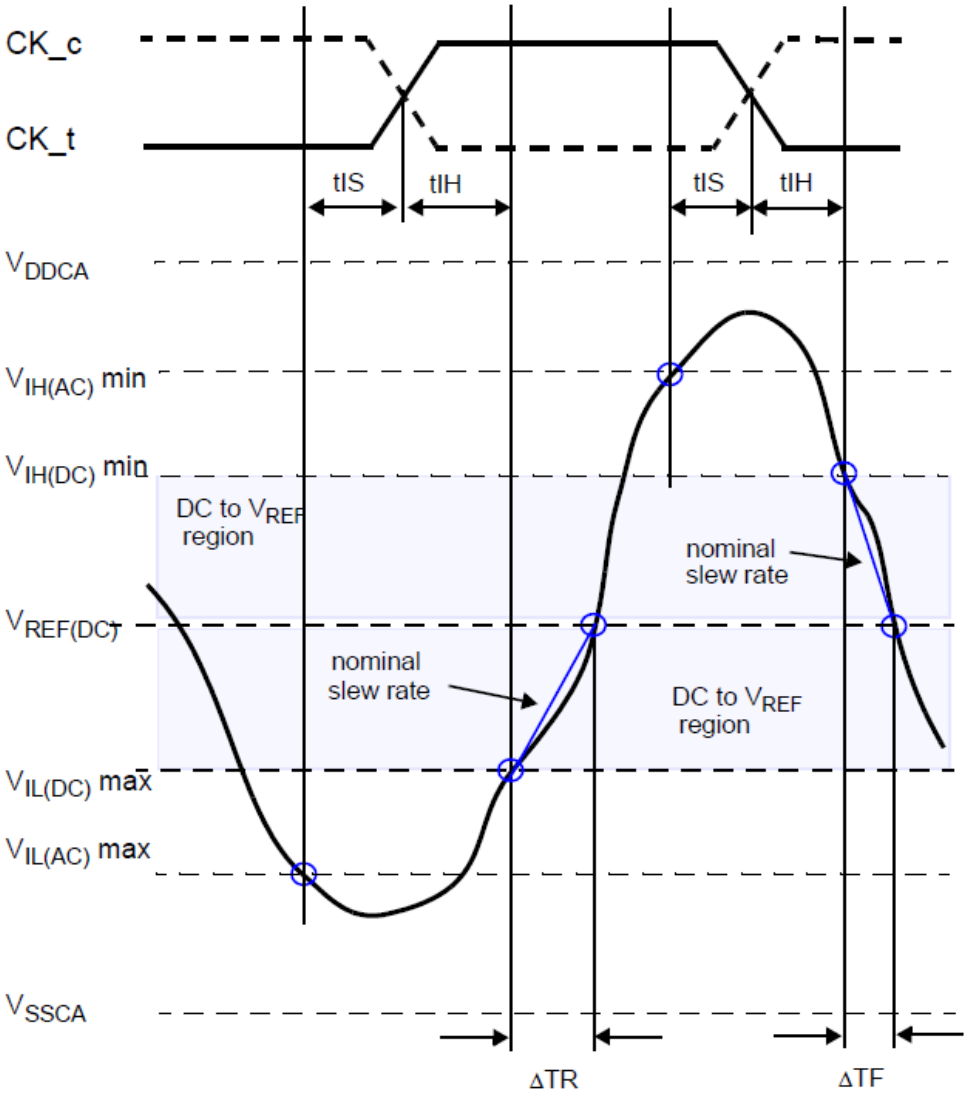


Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

Figure. Illustration of nominal slew rate for hold time tIH for CA and CS_n with respect to clock

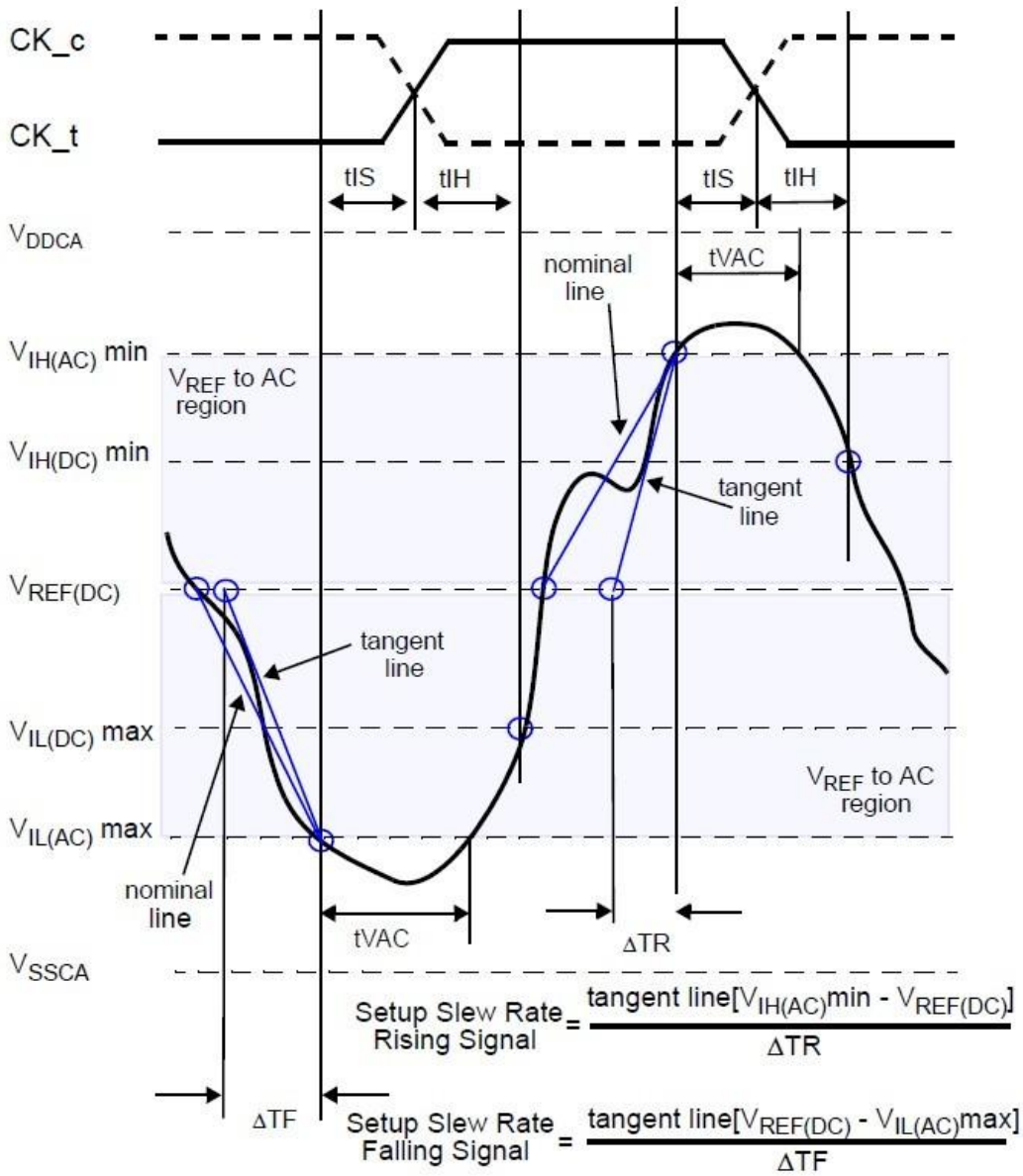
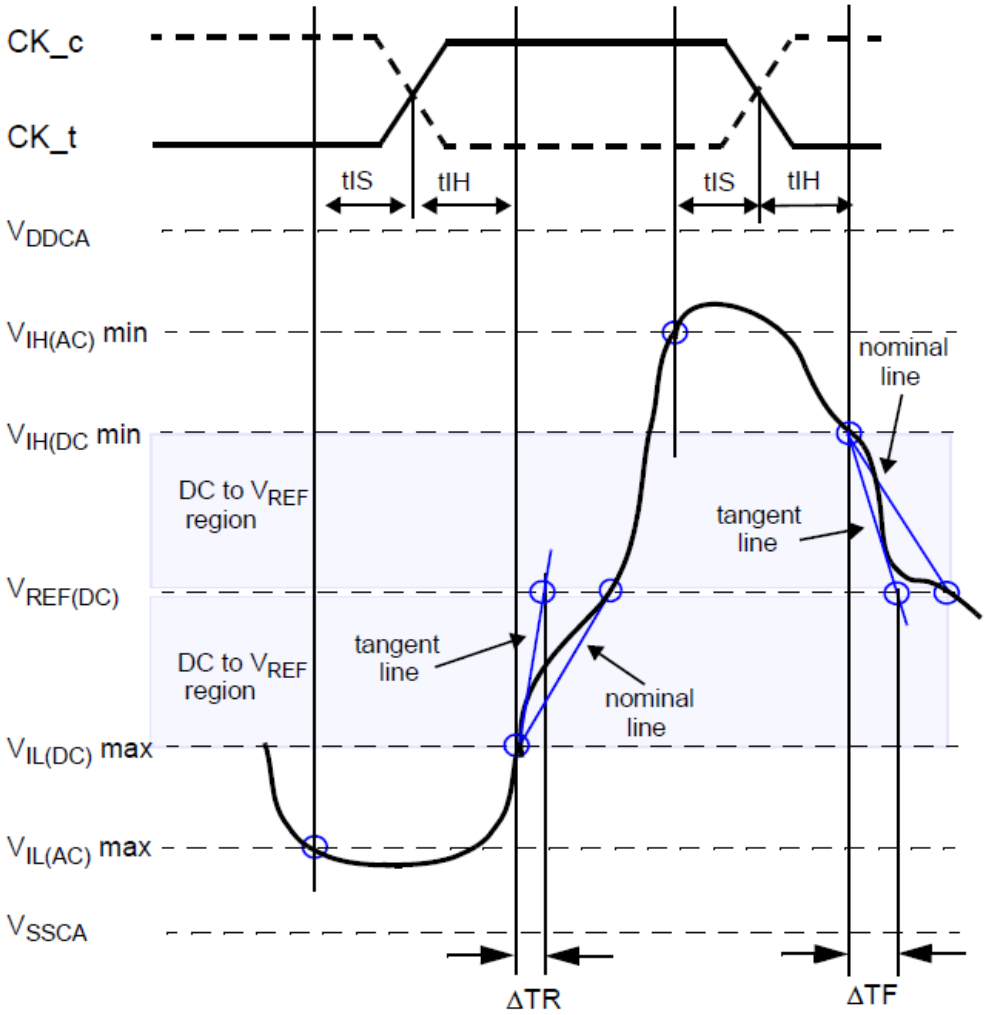


Figure. Illustration of tangent line for setup time t_{IS} for CA and CS_n with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}max]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(DC)}min - V_{REF(DC)}]}{\Delta TF}$$

Figure. Illustration of tangent line for hold time t_{IH} for CA and CS_n with respect to clock

Data Setup, Hold and Slew Rate Derating

Forallinputsignals(DQ,DM)thetotaltDS(setuptime)andtDH(holdtime)requirediscalculatedbyaddingthedata sheettDS(base)andtDH(base)valuetothe∆tDSand∆tDHderatingvaluerespectively. Example:tDS(totalsetupt ime) = tDS(base) +∆tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and thefirstcrossingofVIH(AC)min.Setup(tDS)nominalslewrateforafallingsignalisdefinedastheslewratebetween thelastcrossingofVREF(DC)andthefirstcrossingofVIL(AC)max.Iftheactualsignalisalwayssearlierthanthenom- inalslewratelinebetweenshaded`VREF(DC)toacregion',usenominalslewrateforderatingvalue.Iftheactualsig- nal is later than the nominal slew rate line anywhere between shaded `VREF(DC) to ac region', the slew rate of at angentlinetotheactualsignalfromtheacleveltodc levelis usedforderatingvalue.

Hold(tDH)nominalslewrateforarisingsignalisdefinedastheslewratebetweenthelastcrossingofVIL(DC)maxa ndthefirstcrossingofVREF(DC).Hold(tDH)nominalslewrateforafallingsignalisdefinedastheslewratebetweent helastcrossingofVIH(DC)minandthefirstcrossingofVREF(DC).Iftheactualsignalisalwayslaterthanthenominal slewratelinebetweenshaded`dcleveltoVREF(DC)region',usenominalslewrateforderatingvalue.Iftheactuals ignalisearlierthanthenominalslewratelineanywherebetweenshaded`dctoVREF(DC)region',theslewrateofa tangentlinetotheactualsignalfromthedcleveltoVREF(DC)levelisusedforderatingvalue.

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC.

Althoughforslowslewratesthetotalsetuptimemightbenegative(i.e.avalidinputsignalwillnothavereachedVIH/ IL(AC)atthetimeoftherisingclocktransition)avalidinputsignalisstillrequiredtocompletethetransitionandreach VIH/IL(AC).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

Table. Data Setup and Hold Base-Values

unit [ps]	LPDDR3 1600	LPDDR3 1333	Reference
tDS(base)	75	100	VIH/L(AC)=VREF(DC)+/-150mV
tDS(base)	-	-	VIH/L(AC)=VREF(DC)+/-135mV
tDH(base)	100	125	VIH/L(DC)=VREF(DC)+/-100mV

Note 1: AC/DC referenced for 2V/ns DQ, DM slew rate and 4V/ns differential DQS_t-DQS_c slew rate.

Table. Derating values LPDDR3 tDS/tDH - AC/DC based AC150

		ΔtDS, ΔtDH derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ,DM Slew rate V/ns	4.0	38	25	38	25	38	25	38	25	38	25		
	3.0			25	17	25	17	25	17	25	17	38	29
	2.0					0	0	0	0	0	0	13	13
	1.5							-25	-17	-25	-17	-12	-4

Note 1: Cellcontents shaded

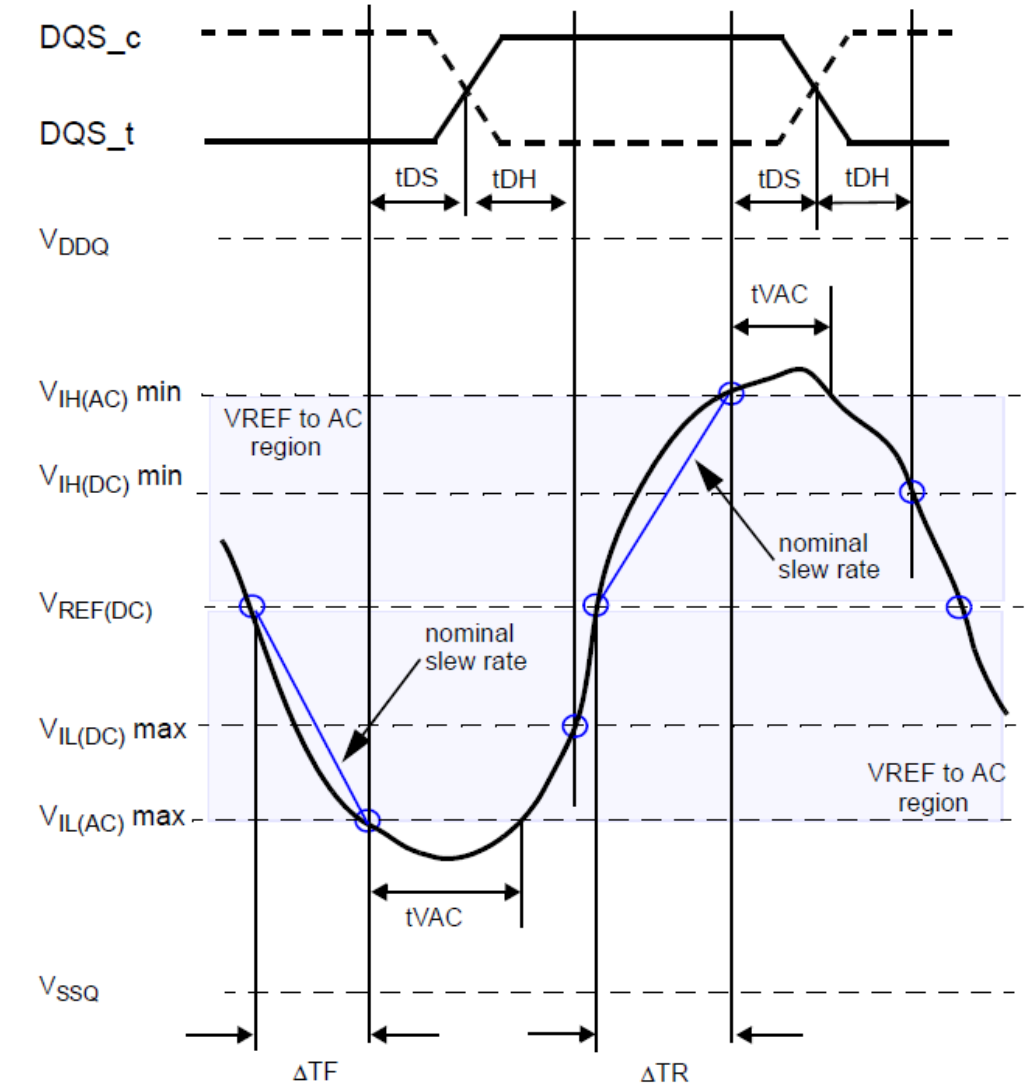
Table. Derating values LPDDR3 tDS/tDH - AC/DC based AC135

		ΔtDS, ΔtDH derating in [ps] AC/DC based AC135 Threshold -> VIH(ac)=VREF(dc)+135mV, VIL(ac)=VREF(dc)-135mV DC100 Threshold -> VIH(dc)=VREF(dc)+100mV, VIL(dc)=VREF(dc)-100mV											
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ,DM Slew rate V/ns	4.0	34	25	34	25	34	25	34	25	34	25		
	3.0			23	17	23	17	23	17	23	17	34	29
	2.0					0	0	0	0	0	0	11	13
	1.5							-23	-17	-23	-17	-12	-4

Note 1: Cellcontents shaded

Table. Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

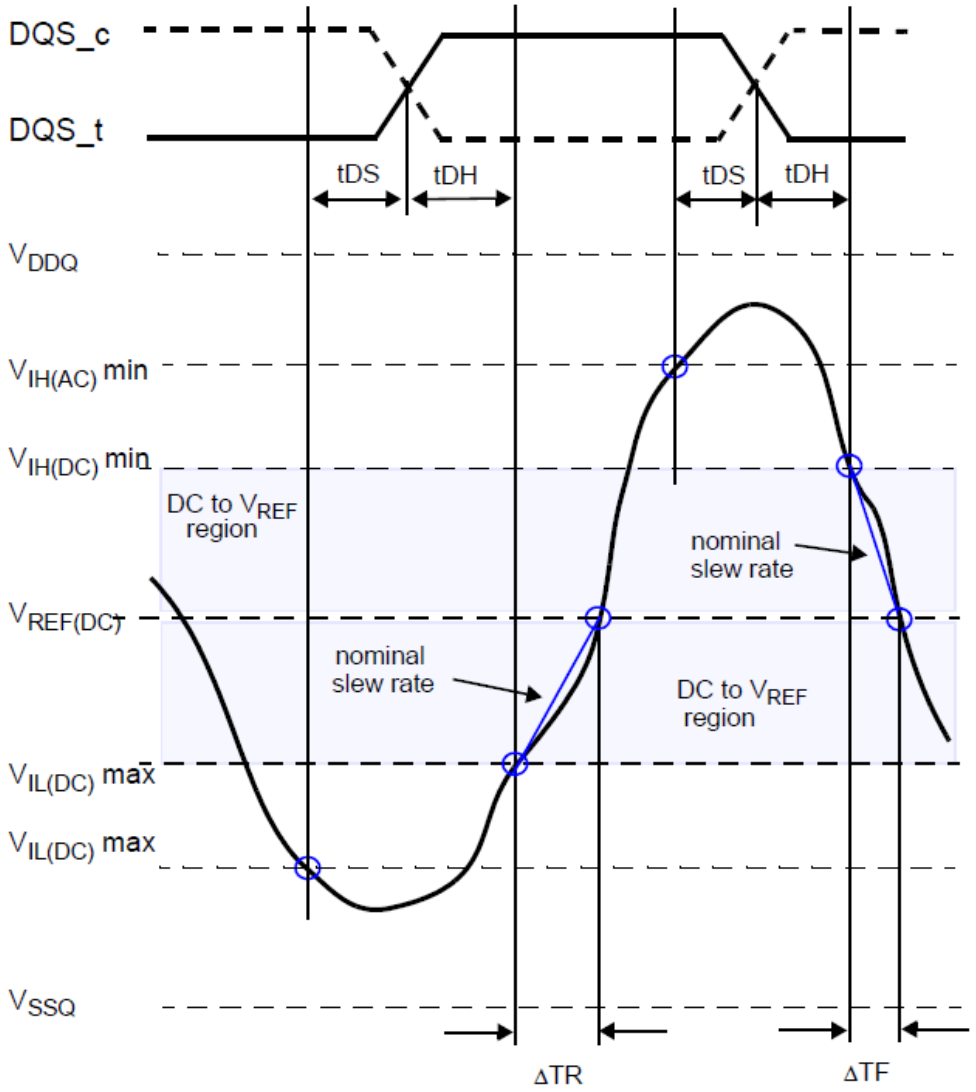
Slew Rate [V/ns]	t_{VAC} [ps] @150mV		t_{VAC} [ps] @150mV	
	1600Mbps		1333Mbps	
	MIN	MAX	MIN	MAX
> 4.0	48	-	58	-
4.0	48	-	58	-
3.5	46	-	56	-
3.0	43	-	53	-
2.5	40	-	50	-
2.0	35	-	45	-
1.5	27	-	37	-
<1.5	27	-	37	-



$$\text{Setup Slew Rate}_{\text{FallingSignal}} = \frac{V_{REF(DC)} - V_{IL(AC)}\text{max}}{\Delta TF}$$

$$\text{Setup Slew Rate}_{\text{Rising Signal}} = \frac{V_{IH(AC)}\text{min} - V_{REF(DC)}}{\Delta TR}$$

Figure. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)}min - V_{REF(DC)}}{\Delta TF}$$

Figure. Illustration of nominal slew rate for hold time t_{DH} for DQ with respect to strobe

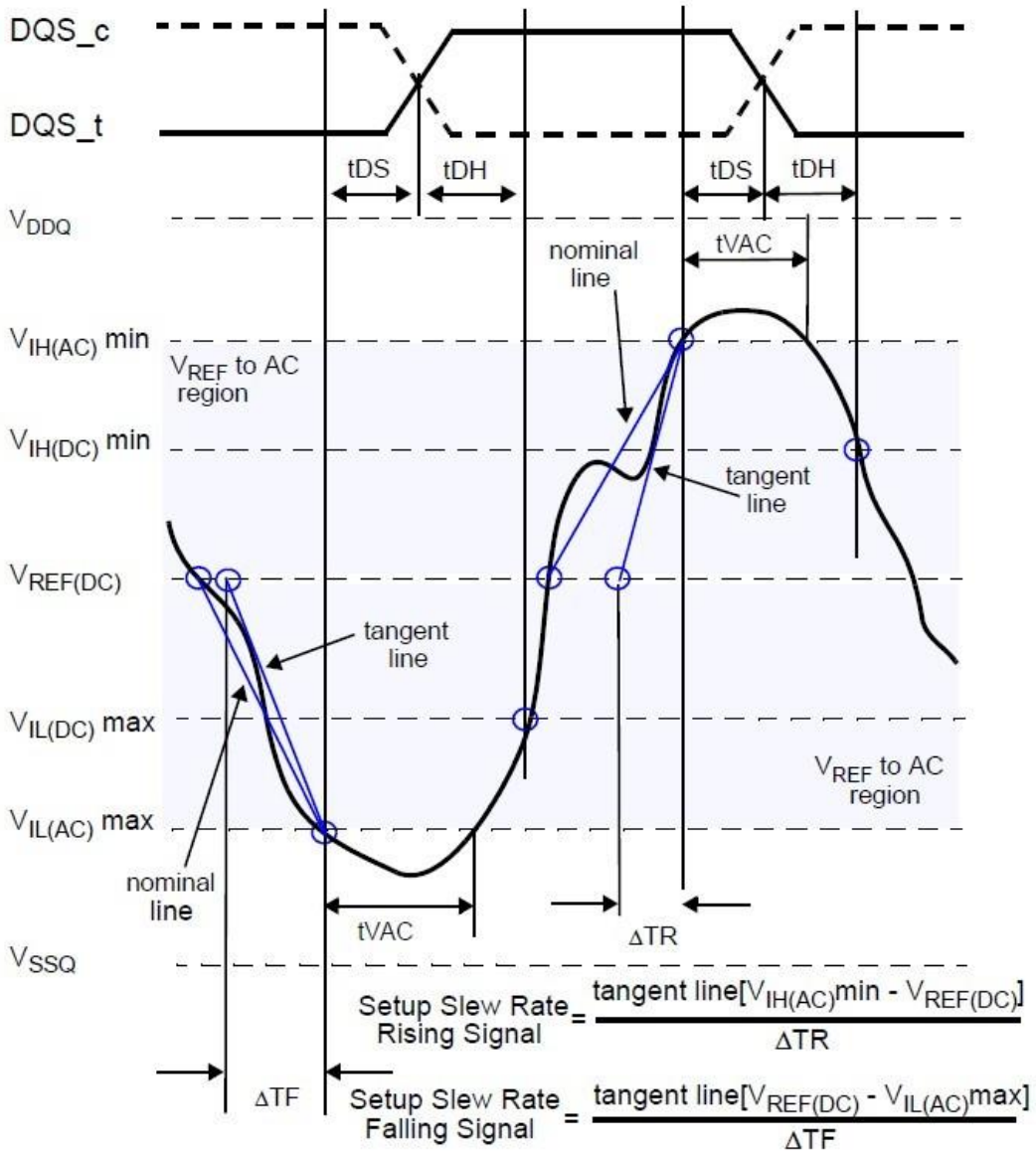
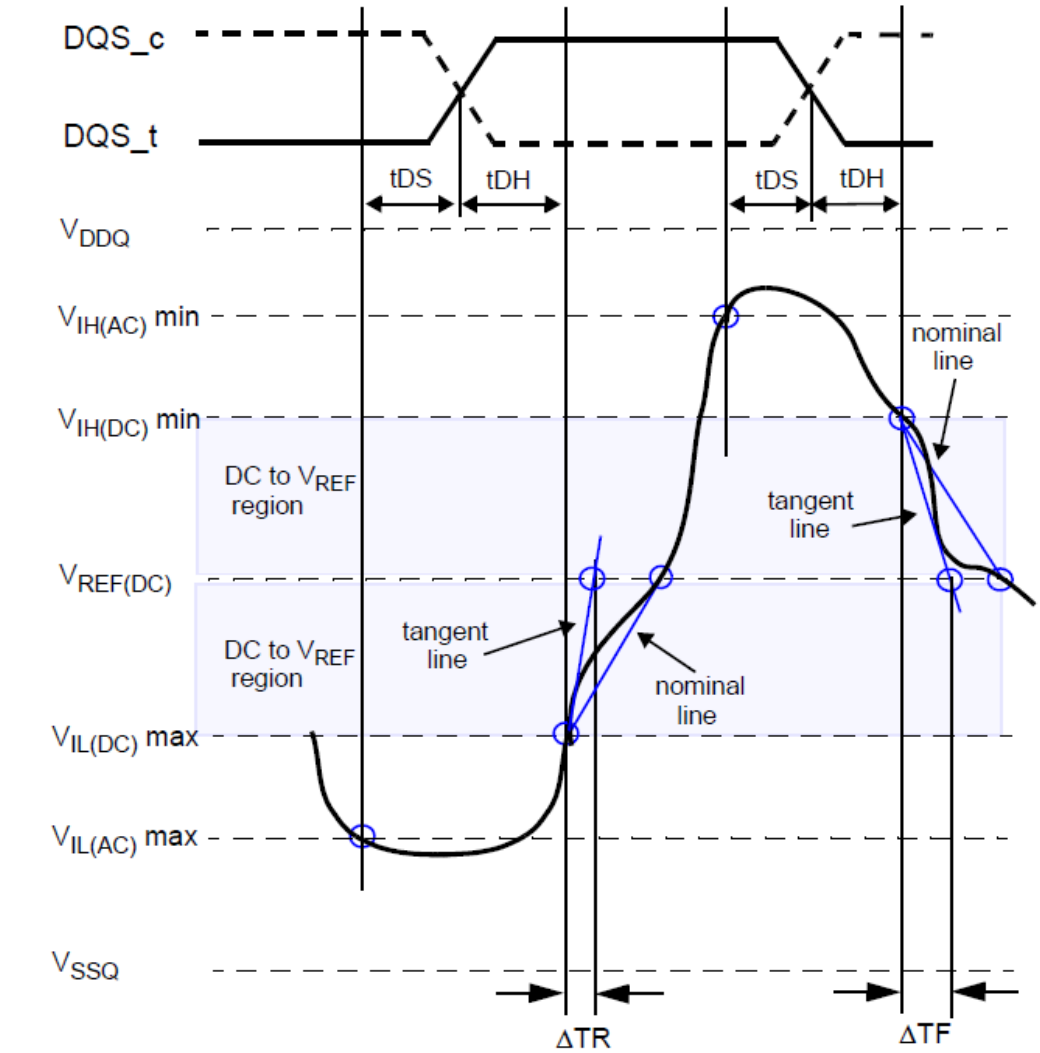


Figure. Illustration of tangent line for setup time t_{DS} for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}]}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta TF}$$

Figure. Illustration of tangent line for hold time t_{DH} for DQ with respect to strobe

Clock Specification

ThejitterspecifiedisarandomjittermeetingaGaussiandistribution.Inputclocksviolatingthemin/maxvaluesmay resultinmalfunctionoftheLPDDR3device.

Definition for tCK(avg) and nCK

tCK(avg)iscalculatedastheaverageclockperiodacrossanyconsecutive200cyclewindow,whereeachclockperiod is calculatedfromrisingedgetorisingedge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$
$$where \quad N = 200$$

Unit`tCK(avg)'representstheactualclockaveragetCK(avg)oftheinputclockunderoperation.Unit`nCK'represents oneclockcycleoftheinputclock,countingtheactualclockedges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specifications are met.

Definition for tCK(abs)

tCK(abs)isdefinedastheabsoluteclockperiod,asmeasuredfromonerisingedgetothenextconsecutiverising edge.tCK(abs)is notsubjecttoproductiontest.

Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$
$$where \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$
$$where \quad N = 200$$

Definition for tJIT(per)

tJIT(per)isthesingleperiodjitterdefinedasthelargestdeviationofanysignaltCKfromtCK(avg).
tJIT(per)=Min/maxof{tCK_i-tCK(avg)wherei= 1to200}.?
tJIT(per),act is the actual clock jitter for a given system.?
tJIT(per),allowed is the specified allowed clock period jitter.?
tJIT(per) is not subject to production test.

Definition for tJIT(cc)

tJIT(cc)isdefinedastheabsolutedifferenceinclockperiodbetweentwoconsecutiveclockcycles.
tJIT(cc)=Maxof|{tCK_{i+1}-tCK_i}|.?
tJIT(cc) defines the cycle to cycle jitter.?
tJIT(cc) is not subject to production test.

Definition for tERR(nper)

tERR(nper)isdefinedasthecumulativeerroracrossnmultipleconsecutivecyclesfromtCK(avg).
tERR(nper),actistheactualclockjitteroverncycles foragivensystem.?
tERR(nper),allowedisthespecifiedallowedclockperiodjitteroverncycles.? tERR(nper)is notsubjecttoproductiontest.

$$tERR(nper) = \left(\sum_{j=i}^{j+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),mincanbecalculatedbytheformulashownbelow:

$$tERR(nper), min = (1 + 0.68 LN(n)) \times tJIT(per), min$$

tERR(nper),maxcanbecaculatedbytheformulashownbelow:

$$tERR(nper), max = (1 + 0.68 LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value

Definition for duty cycle jitter tJIT(duty)
tJIT(duty)isdefinedwithabsoluteandaveragespecificationoftCH/tCL.

tJIT(duty),mincanbecaculatedbytheformulashownbelow:

$$tJIT(duty),min = MIN((tCH(abs),min - tCH(avg),min),(tCL(abs),min - tCL(avg),min)) \times tCK(avg)$$

tJIT(duty),maxcanbecaculatedbytheformulashownbelow:

$$tJIT(duty),max = MAX((tCH(abs),max - tCH(avg),max),(tCL(abs),max - tCL(avg),max)) \times tCK(avg)$$

Definition for tCK(abs), tCH(abs) and tCL(abs)
Theseparametersarespecifiedpertheiraveragevalues,howeveritisunderstoodthatthefollowingrelationship betweentheaveragetimingandtheabsoluteinstantaneoustimingholdsatalltimes.

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Note:
1. tCK(avg),min is expressed in ps for thistable
2. tJIT(duty),min is a negativevalue

Period Clock Jitter

LPDDR3devicescantoleratesomeclockperiodjitterwithoutcoretimingparameterde-rating.Thissectiondescribes devicetimingrequirementsinthepresenceofclockperiodjitter(tJIT(per))inexcessofthevaluesfoundin"ACtiming table"andhowtodeterminecycletimede-ratingandclockcyclede-rating.

Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measuredinnumbersofclockcycles.Whenthedeviceisoperatedwithclockjitterwithinthespecificationlimits,the LPDDR3deviceischaracterizedandverifiedtosupporttnPARAM=RU{tPARAM/tCK(avg)}.

Whenthedeviceisoperatedwithclockjitteroutsidespecificationlimits,thenumberofclocksortCK(avg)mayneedto be increasedbasedonthevaluesforeachcoretimingparameter.

Cycle time de-rating for core timing parameters

Foragivennumberofclocks(tnPARAM),foreachcoretimingparameter,averageclockperiod(tCK(avg))andactual cumulativeperioderror(tERR(tnPARAM),act)inexcessoftheallowedcumulativeperioderror (tERR(tnPARAM),allowed),theequationbelowcalculatestheamountofcycletimede-rating(inns)requiredifthe equationresultsinapositivevalueforacoretimingparameter(tCORE).

$$Cycle\ Time\ Derating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

Clock Cycle de-rating for core timing parameters

Foragivennumberofclocks(tnPARAM)foreachcoretimingparameter,clockcyclede-ratingshouldbespecifiedwith amount of period jitter(tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulativeperioderror(tERR(tnPARAM),act)inexcessoftheallowedcumulativeperioderror (tERR(tnPARAM),allowed),theequationbelowcalculatestheclockcyclederating(inclocks)requiredifttheequationre sultsinapositivevalueforacoretimingparameter(tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

Clock jitter effects on Command/Address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

Theseparametersaremeasuredfromacommand/addresssignal(CKE,CS,CA0-CA9)transitionedgetoitsrespec-t ive clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per),asthesetupandholdarerelativetotheclocksignalcrossingthatlatchesthecommand/address.Regardless ofclockjittervalues,thesevaluesshallbemet.

Clock jitter effects on Read timing parameters

tRPRE

Whenthedeviceisoperatedwithinputclockjitter,tRPREneedstobede-ratedbytheactualperiodjitter

(

tJIT(per),act,max)oftheinputclockinexcessoftheallowedperiodjitter(tJIT(per),allowed,max).Outputde-ratings arerelativetotheinputclock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

Theseparametersaremeasuredfromaspecificclockedgetoadatasignal(DMn,DQm:n=0,1,2,3,m=0-31)transi-tionandwillbemetwithrespecttothatclockedge.Therefore,theyarenotaffectedbytheamountofclockjittera pplied (i.e.tJIT(per)).

tQSH, tQSL

TheseparametersareaffectedbydutycyclejitterwhichisrepresentedbytCH(abs)minandtCL(abs)min.These parametersdetermineabsoluteData-ValidWindow(DVW)attheLPDDR3devicepin.
Absolute min DVW @ LPDDR3 device pin =
min{ (tQSH(abs)min – tDQSQmax) , (tQSL(abs)min – tDQSQmax) }
This minimum DVW shall be met at the target frequency regardless of clock jitter.

tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.
tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

Clock jitter effects on Write timing parameters

tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of c lock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

tDSS, tDSH

Theseparametersaremeasuredfromadatastrobesignal(DQSx_t,DQSx_c)crossingtoitsrespectiveclocksignal (CK_t/CK_c)crossing.Thespecvaluesarenotaffectedbytheamountofclockjitterapplied(i.e.tJIT(per),asthe setupandholdofthedatastrobesarerelativetothecorrespondingclocksignalcrossing.Regardlessofclockjitterval- ues, these values shall bemet.

tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal(CK_t/CK_c)crossing.Whenthedeviceisoperatedwithinputclockjitter,thisparameterneedstobede-ratedbythea ctualperiodjittertJIT(per),actoftheinputclockin excessoftheallowedperiodjittertJIT(per),allowed.

tDQSS(min,derated)canbecaculatedbytheformulashownbelow:

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

tDQSS(max,derated)canbecaculatedbytheformulashownbelow:

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

Refresh Requirements

Density		Symbol	8Gb	Unit
Number of Banks			8	-
Refresh Window Tcase <= 85'C		tREFW	32	ms
RefreshWindow 1/2-RateRefresh		tREFW	16	ms
RefreshWindow 1/4-RateRefresh		tREFW	8	ms
Required number of REFRESH commands (min)		R	8,192	-
average time between REFRESH commands (for referenceonly) Tcase <=85'C	REFab	tREFI	3.9	us
	REFpb	tREFIpb	0.4875	us
Refresh Cycle time		tRFCab	210	ns
Per Bank Refresh Cycle time		tRFCpb	90	ns
Burst Refresh Window = 4 x 8 x tRFCab		tREFBW	6.72	us

LPDDR3 Read and Write Latencies

Parameter	LPDDR3							Unit
	333	800	1066	1200	1333	1466	1600	
Max. Clock Frequency	166	400	533	600	667	733	800	NHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	MT/s
Average Clock Period	6	2.5	1.875	1.667	1.5	1.364	1.25	ns
Read Latency	3	6	8	9	10	11	12	tCK(avg)
Write Latency (Set A)	1	3	4	5	6	6	6	tCK(avg)
Write Latency (Set B)	1	3	4	5	8	9	9	tCK(avg)

Note:
1. RL=3/WL=1 setting is an optional feature. Refer to MR0OP<7>.
2. Write Latency (Set B) support is an optional feature. Refer toMR0 OP<6>.

Revision History

Rev. B – 2019/12/18

- Updated Operating temperature

Rev. A – 2018/11/14

- Initial release