LPDDR3 Mobile RAM

RS128M32LD3D1LMZ-125BT

Specifications

- Density: 4Gb
- Organization:
— ×16: 32M words × 16 bits × 8 banks
— ×32: 16M words × 32 bits × 8 banks
- Package: Bare Chip
- Power supply
— VDD1 = 1.70V to 1.95V
— VDD2, VDDCA, VDDQ = 1.14V to 1.30V
- Data rate: 1600Mbps max (RL = 12)
- 4KB page size
— Row address: R0 to R13
— Column address: C0 to C10 (×16 bits)
C0 to C9 (×32 bits)
- Eight internal banks for concurrent operation
- Interface: HSUL_12
- Burst lengths (BL): 8
- Burst type (BT)
— Sequential
- Read latency (RL): 3, 6, 8, 9, 10, 11, 12
- Precharge: auto precharge option for each burst access
- Programmable driver strength
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/32ms
— Average refresh period: 3.9µs
- Operating junction temperature range
— Tj = −25°C to +85°C

Features

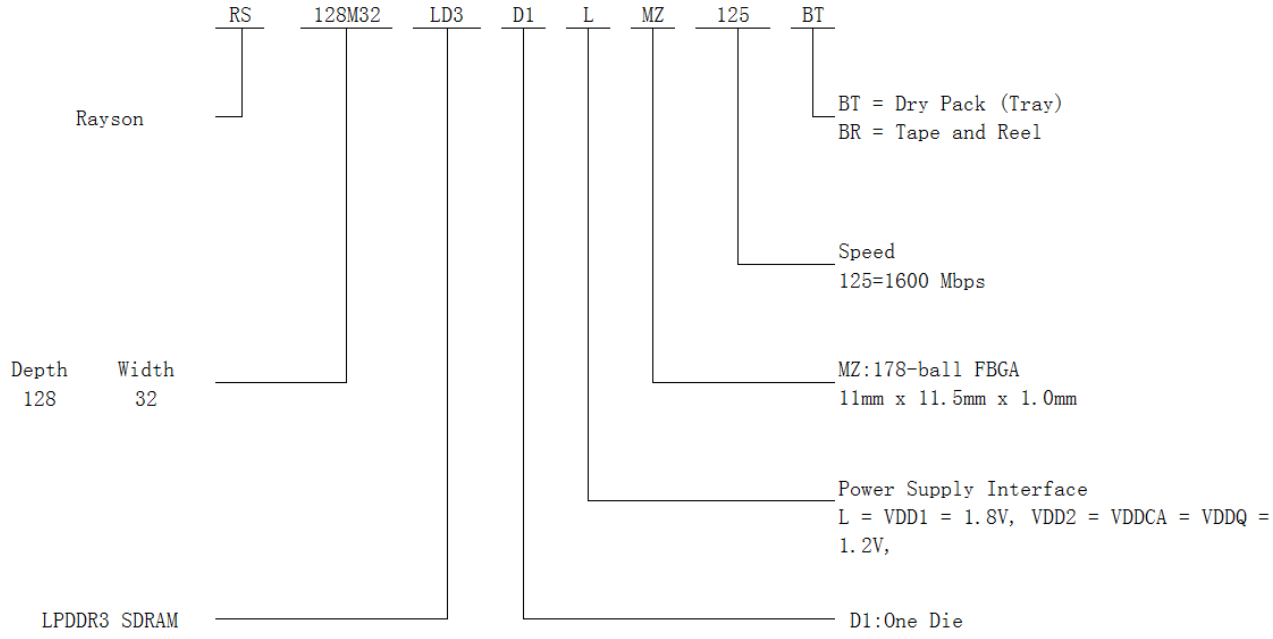
- Low power consumption
- JEDEC LPDDR3 compliant
- Per Bank Refresh
- Partial Array Self-Refresh (PASR)
— Bank Masking
— Segment Masking
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- On Die Termination (ODT) for better signal integrity
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Differential clock inputs (CK_t and CK_c)
- Bi-directional differential data strobe (DQS_t and DQS_c)
- Commands entered on both rising and falling CK_t edge; data and data mask referenced to both edges of DQS_t
- Data mask (DM) for write data
- CA training for CA input timing adjustment
- Write leveling for clock to DQ, DQS_t, DQS_c and DM timing adjustment

Part Numbering Information

Low Power memory devices are available in different configurations and densities.

Table 1: Ordering Information

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
RS128M32LD3D1LMZ	LPDDR3 4Gb	1.8V/1.2/1.2/1.2	4Gb (x32, 1CS)	DDR3 1333	178Ball FBGA (Lead & Halogen Free)



CONTENTS

Specifications 1
Features 1
Part Number Information 2
Ordering Information 3
Part Number 3
Pin Descriptions 5
Pin Capacitance 6
Pin Configurations 7
Package Drawing 8
Package Dlock Diagrams 8

1. Electrical Conditions 9
   - 1.1 Absolute Maximum Ratings 9
   - 1.2 Recommended DC Operating Conditions 9
2. Electrical Specifications 10
   - 2.1 DC Characteristics 1 10
   - 2.2 DC Characteristics 2 12
   - 2.3 AC Characteristics 13
3. Mode Register Definition 20

Pin Descriptions

Pin name	Function
CK_t, CK_c	Clock
CKE	Clock enable
CS_n	Chip select
CA0 to CA9	DDR command/address inputs Address configurations Row:R0 to R13, Column:C0 to C10 (×16 bits), C0 to C9 (×32 bits) Bank:BA0 to BA2
DM0 to DM3	Input data mask ×16: DM0 to DM1 ×32: DM0 to DM3
DQ0 to DQ31	Data input/output ×16: DQ0 to DQ15 ×32: DQ0 to DQ31
DQS0_t to DQS3_t, DQS0_c to DQS3_c	Data strobe ×16: DQS0_t to DQS1_t, DQS0_c to DQS1_c ×32: DQS0_t to DQS3_t, DQS0_c to DQS3_c
ODT	On-die termination
VDD1	Core power supply 1
VDD2	Core power supply 2
VDDCA	Input receiver power supply
VDDQ	I/O power supply
VREFCA	Reference voltage for CA input receiver
VREFDQ	Reference voltage for DQ input receiver
VSS	Ground
VSSCA	Ground for input receivers
VSSQ	I/O ground
ZQ	Reference pin for output drive strength calibration
NU*1	Not usable

Note: 1. Don’t connect.

Pin Capacitance

Parameter	Symbol	Pins	min	max	Unit	Note
Input capacitance	CCK	CK_t, CK_c	0.5	1.2	pF	1, 2
	CI1	All other DDR3 Mobile RAM input only pins	0.5	1.1	pF	1, 2
Data input/output capacitance	CIO	DQ0 to DQ31, DM0 to DM3, DQS0_t to DQS3_t, DQS0_c to DQS3_c	1.0	1.8	pF	1, 2, 3
	CZQ	ZQ	0.0	2.0	pF	1, 2, 3

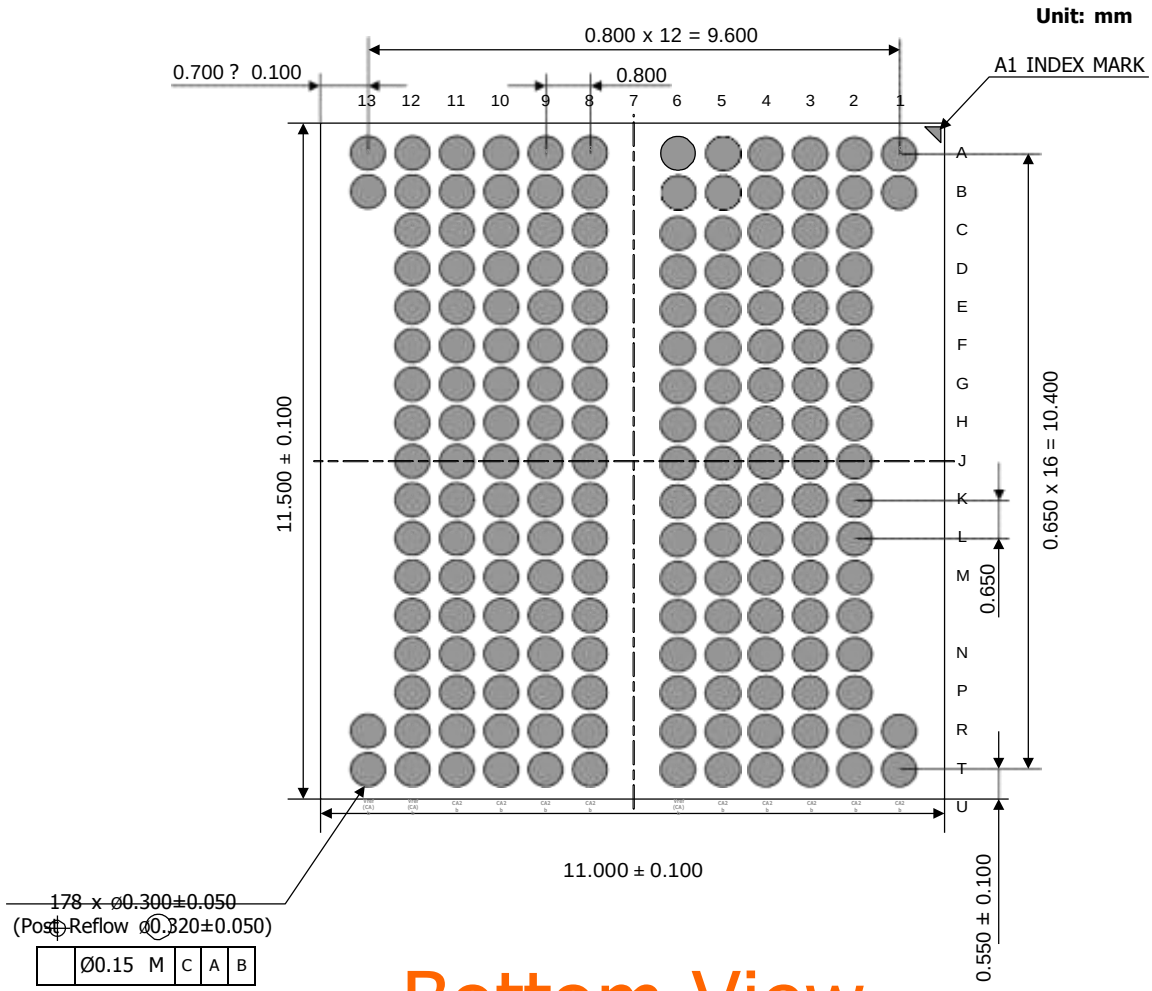
Notes: 1. This parameter is not subject to production test. It is verified by design and characterization.
2. These parameters are measured on f = 100MHz, VOUT = VDDQ/2, TA = +25°C.
3. DOUT circuits are disabled.

Pin Configurations

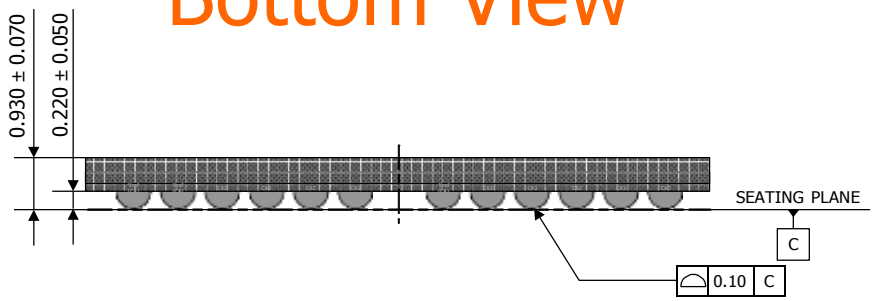
(Top view)

PACKAGE INFORMATION

178 Ball 0.65mm pitch 11.0mm x 11.5mm [t = 1.00mm max] FBGA



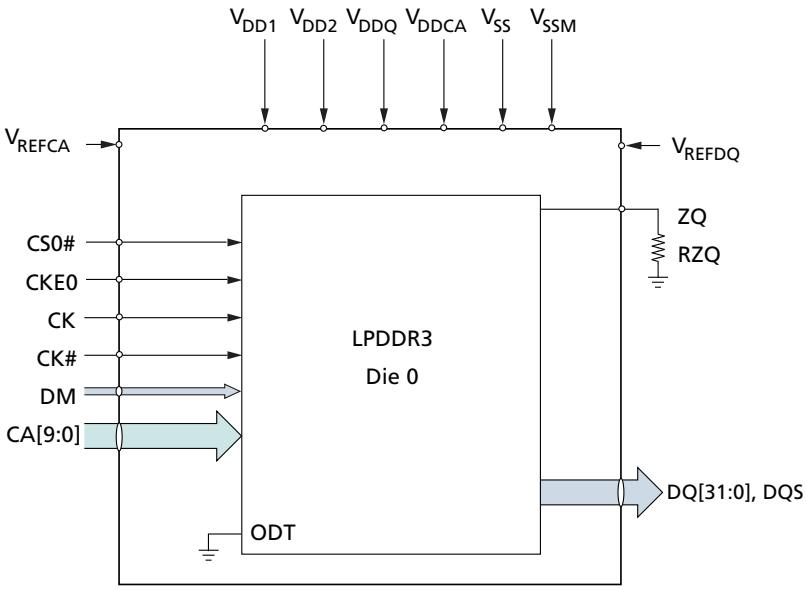
Bottom View



Front View

Package Block Diagrams

Single Rank, Single Channel Package Block Diagram



1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR3 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

1.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	–0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	–0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	–0.4	1.6	V	2, 3
VDDQ supply voltage relative to VSSQ	VDDQ	–0.4	1.6	V	2, 4
Voltage on any ball relative to VSS	VIN, VOUT	–0.4	1.6	V	
Storage Temperature	TSTG	–55	125	°C	5

Notes: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. See Power-Ramp section “Power-up, initialization and Power-Off” in the ”DDR3 Mobile RAM General Functionality and Electrical Condition” specification for relationship between power supplies.
3. VREFCA ≤ 0.6 × VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.
4. VREFDQ ≤ 0.7 × VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.
5. Storage Temperature is the case surface temperature on the center/top side of the DDR3 Mobile RAM Device. For the measurement conditions, please refer to JESD51-2 standard.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2 Recommended DC Operating Conditions

Table 2: Recommended DC Operating Conditions (Tj= –30°C to +85°C)

Parameter	Symbol	min	typ	max	Unit
Core Power1	VDD1	1.70	1.80	1.95	V
Core Power2	VDD2	1.14	1.20	1.30	V
Input Buffer Power	VDDCA	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

2. Electrical Specifications

2.1 DC Characteristics 1

Table 3: IDD Specification Parameters and Operating Conditions
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Symbol	Power Supply	1600 max	1333 max	Unit	Parameter/Condition
IDD0_1	VDD1	6.0	6.0	mA	**Operating one bank active-precharge current**
IDD0_2	VDD2	30	30	mA	**Conditions for operating devices are**
IDD0_IN	VDDCA VDDQ	6.0	6.0	mA	tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
IDD2P_1	VDD1	0.4	0.4	mA	**Idle power-down standby current**
IDD2P_2	VDD2	0.9	0.9	mA	tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
IDD2P_IN	VDDCA VDDQ	0.1	0.1	mA	
IDD2PS_1	VDD1	0.4	0.4	mA	**Idle power-down standby current with clock stop**
IDD2PS_2	VDD2	0.9	0.9	mA	CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
IDD2PS_IN	VDDCA VDDQ	0.1	0.1	mA	
IDD2N_1	VDD1	0.4	0.4	mA	**Idle non power-down standby current**
IDD2N_2	VDD2	11.5	11	mA	tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
IDD2N_IN	VDDCA VDDQ	6.0	6.0	mA	
IDD2NS_1	VDD1	0.4	0.4	mA	**Idle non power-down standby current with clock stop**
IDD2NS_2	VDD2	9.5	9.5	mA	CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
IDD2NS_IN	VDDCA VDDQ	6.0	6.0	mA	
IDD3P_1	VDD1	0.7	0.7	mA	**Active power-down standby current**
IDD3P_2	VDD2	5.0	5.0	mA	tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
IDD3P_IN	VDDCA VDDQ	0.1	0.1	mA	
IDD3PS_1	VDD1	0.7	0.7	mA	**Active power-down standby current with clock stop**
IDD3PS_2	VDD2	5.0	5.0	mA	CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
IDD3PS_IN	VDDCA VDDQ	0.1	0.1	mA	
IDD3N_1	VDD1	1.0	1.0	mA	**Active non power-down standby current**
IDD3N_2	VDD2	12.5	12	mA	tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE; ODT disabled
IDD3N_IN	VDDCA VDDQ	6.0	6.0	mA	

Table 3: IDD Specification Parameters and Operating Conditions
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Symbol	Power Supply	1600 max	1333 max	Unit	Parameter/Condition
IDD3NS_1	VDD1	1.0	1.0	mA	**Active non power-down standby current with clock stop** CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
IDD3NS_2	VDD2	10.5	10.5	mA	
IDD3NS_IN	VDDCA VDDQ	6.0	6.0	mA	
IDD4R_1	VDD1	2.0	2.0	mA	**Operating burst read current** tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank active; BL = 8; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for ×16 bits; ODT disabled
IDD4R_2	VDD2	200	175	mA	
IDD4R_IN	VDDCA	6.0	6.0	mA	
IDD4W_1	VDD1	2.0	2.0	mA	**Operating burst write current** tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank active; BL = 8; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for ×16 bits; ODT disabled
IDD4W_2	VDD2	190	165	mA	
IDD4W_IN	VDDCA VDDQ	6.0	6.0	mA	

IDD5_1	VDD1	20	20	mA	**All bank auto refresh burst current**
					tCK = tCK(avg)min; CKE is HIGH between valid commands;
					tRC = tRFCabmin; Burst refresh;
					CA bus inputs are SWITCHING;
					Data bus inputs are STABLE;
					ODT disabled

IDD5_2	VDD2	100	100	mA	
IDD5_IN	VDDCA VDDQ	6.0	6.0	mA	

IDD5AB_1	VDD1	2.0	2.0	mA	**All bank auto refresh average current**
					tCK = tCK(avg)min; CKE is HIGH between valid commands;
					tRC = tREFI;
					CA bus inputs are SWITCHING;
					Data bus inputs are STABLE;
					ODT disabled

IDD5AB_2	VDD2	12	11.5	mA	
IDD5AB_IN	VDDCA VDDQ	6.0	6.0	mA	

IDD5PB_1	VDD1	2.0	2.0	mA	**Per bank auto refresh average current**
					tCK = tCK(avg)min; CKE is HIGH between valid commands;
					tRC = tREFIpb;
					CA bus inputs are SWITCHING;
					Data bus inputs are STABLE;
					ODT disabled

IDD5PB_2	VDD2	12	11.5	mA	
IDD5PB_IN	VDDCA VDDQ	6.0	6.0	mA	
IDD8_1	VDD1	16	16	µA	**Deep power-down current** CK_t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
IDD8_2	VDD2	6.0	6.0	µA	
IDD8_IN	VDDCA VDDQ	12	12	µA	

Notes: 1. IDD values published are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.

Table 4: IDD6 Full and Partial Array Self-Refresh Current
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Parameter		Symbol	Value	Unit	Condition
Self-Refresh Current +45°C	Full Array	IDD6_1	200	µA	CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; ODT disabled
		IDD6_2	800	µA	
		IDD6_IN	10	µA	
	1/2 Array	IDD6_1	160	µA	
		IDD6_2	500	µA	
		IDD6_IN	10	µA	
	1/4 Array	IDD6_1	130	µA	
		IDD6_2	300	µA	
		IDD6_IN	10	µA	
	1/8 Array	IDD6_1	120	µA	
		IDD6_2	200	µA	
		IDD6_IN	10	µA	
Self-Refresh Current +85°C	Full Array	IDD6_1	900	µA	
		IDD6_2	3200	µA	
		IDD6_IN	12	µA	
	1/2 Array	IDD6_1	650	µA	
		IDD6_2	2200	µA	
		IDD6_IN	12	µA	
	1/4 Array	IDD6_1	550	µA	
		IDD6_2	1700	µA	
		IDD6_IN	12	µA	
	1/8 Array	IDD6_1	500	µA	
		IDD6_2	1400	µA	
		IDD6_IN	12	µA	

Note: 1. IDD6 85°C is the maximum and IDD6 45°C is typical of the distribution of the arithmetic mean.

2.2 DC Characteristics 2

Table 5: Electrical Characteristics and Operating Conditions
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Symbol	min	max	Unit	Parameter/Condition	Note
IL	–2	+2	µA	**Input leakage current:** For CA, CKE, CS_n, CK_t, CK_c Any input 0V ≤ VIN ≤ VDDCA (All other pins not under test = 0V)	2
IVREF	–1	+1	µA	**VREF supply leakage current:** VREFDQ = VDDQ/2 or VREFCA = VDDCA/2 (All other pins not under test = 0V)	1

Notes: 1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t, DQS_c output leakage specification. Please refer to the DDR3 Mobile RAM General Functionality and Electrical Condition data sheet (E1853E) for details.

2.3 AC Characteristics

Table 6: AC Characteristics Table*3 *5 *9
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Max. frequency			—	800	667	MHz
Clock Timing						
Average clock period	tCK(avg)	min	—	1.25	1.50	ns
		max	—	100		ns
Average high pulse width	tCH(avg)	min	—	0.45		tCK(avg)
		max	—	0.55		
Average low pulse width	tCL(avg)	min	—	0.45		tCK(avg)
		max	—	0.55		
Absolute clock period	tCK(abs)	min	—	tCK(avg)min + tJIT(per)min		ns
Absolute clock high pulse width (with allowed jitter)	tCH(abs), allowed	min	—	0.43		tCK(avg)
		max	—	0.57		
Absolute clock low pulse width (with allowed jitter)	tCL(abs), allowed	min	—	0.43		tCK(avg)
		max	—	0.57		
Clock period jitter (with allowed jitter)	tJIT(per), allowed	min	—	–70	–80	ps
		max	—	70	80	
Maximum clock jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max	—	140	160	ps
Duty cycle jitter (with allowed jitter)	tJIT(duty), allowed	min	—	min((tCH(abs)min – tCH(avg)min), (tCL(abs)min – tCL(avg)min)) × tCK(avg)		ps
		max	—	max((tCH(abs)max – tCH(avg)max), (tCL(abs)max – tCL(avg)max)) × tCK(avg)		
Cumulative error across 2 cycles	tERR(2per), allowed	min	—	–103	–118	ps
		max	—	103	118	
Cumulative error across 3 cycles	tERR(3per), allowed	min	—	–122	–140	ps
		max	—	122	140	
Cumulative error across 4 cycles	tERR(4per), allowed	min	—	–136	–155	ps
		max	—	136	155	
Cumulative error across 5 cycles	tERR(5per), allowed	min	—	–147	–168	ps
		max	—	147	168	
Cumulative error across 6 cycles	tERR(6per), allowed	min	—	–155	–177	ps
		max	—	155	177	
Cumulative error across 7 cycles	tERR(7per), allowed	min	—	–163	–186	ps
		max	—	163	186	
Cumulative error across 8 cycles	tERR(8per), allowed	min	—	–169	–193	ps
		max	—	169	193	
Cumulative error across 9 cycles	tERR(9per), allowed	min	—	–175	–200	ps
		max	—	175	200	
Cumulative error across 10 cycles	tERR(10per), allowed	min	—	–180	–205	ps
		max	—	180	205	
Cumulative error across 11 cycles	tERR(11per), allowed	min	—	–184	–210	ps
		max	—	184	210	
Cumulative error across 12 cycles	tERR(12per), allowed	min	—	–188	–215	ps
		max	—	188	215	

Table 6: AC Characteristics Table*3 *5 *9
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Cumulative error across n = 13, 14 . . . 19, 20 cycles	tERR(nper), allowed	min	—	tERR(nper),allowed,min = (1 + 0.68ln(n)) × tJIT(per),allowed,min		ps
		max	—	tERR(nper),allowed,max = (1 + 0.68ln(n)) × tJIT(per),allowed,max		
Read Parameters						
DQS output access time from CK_t, CK_c	tDQSCK	min	—	2500		ps
		max	—	5500		
DQSCK delta short*15	tDQSCKDS	max	—	220	265	ps
DQSCK delta medium*16	tDQSCKDM	max	—	511	593	ps
DQSCK delta long*17	tDQSCKDL	max	—	614	733	ps
DQS – DQ skew	tDQSQ	max	—	135	165	ps
DQS output high pulse width	tQSH	min	—	tCH(abs) – 0.05		tCK(avg)
DQS output low pulse width	tQSL	min	—	tCL(abs) – 0.05		tCK(avg)
DQ output hold time from DQS	tQH	min	—	min (tQSH, tQSL)		ps
Read preamble*11, *12	tRPRE	min	—	0.9		tCK(avg)
Read postamble*11, *13	tRPST	min	—	0.3		tCK(avg)
DQS low-Z from clock*11	tLZ(DQS)	min	—	tDQSCK(min) – 300		ps
DQ low-Z from clock*11	tLZ(DQ)	min	—	tDQSCK(min) – 300		ps
DQS high-Z from clock*11	tHZ(DQS)	max	—	tDQSCK(max) – 100		ps
DQ high-Z from clock*11	tHZ(DQ)	max	—	tDQSCK(max) + (1.4 × tDQSQ(max))		ps
Write Parameters*10						
DQ and DM input hold time (VREF based)	tDH	min	—	150	175	ps
DQ and DM input setup time (VREF based)	tDS	min	—	150	175	ps
DQ and DM input pulse width	tDIPW	min	—	0.35		tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min	—	0.75		tCK(avg)
		max	—	1.25		
DQS input high-level width	tDQSH	min	—	0.4		tCK(avg)
DQS input low-level width	tDQSL	min	—	0.4		tCK(avg)
DQS falling edge to CK setup time	tDSS	min	—	0.2		tCK(avg)
DQS falling edge hold time from CK	tDSH	min	—	0.2		tCK(avg)
Write postamble	tWPST	min	—	0.4		tCK(avg)
Write preamble	tWPRE	min	—	0.8		tCK(avg)
CKE Input Parameters						
CKE min. pulse width (high and low pulse width)	tCKE	min	3	7.5		ns
CKE input setup time	tISCKE*1	min	—	0.25		tCK(avg)
CKE input hold time	tIHCKE*2	min	—	0.25		tCK(avg)
Command path disable delay	tCPDED	min	2	2		tCK(avg)
Command Address Input Parameters*10						
Address and control input setup time	tISCA	min	—	150	175	ps
Address and control input hold time	tIHCA	min	—	150	175	ps
CS_n input setup time	tISCS	min	—	270	290	ps
CS_n input hold time	tIHCS	min	—	270	290	ps
Address and control input pulse width	tIPWCA	min	—	0.35		tCK(avg)
CS_n input pulse width	tIPWCS	min	—	0.7		tCK(avg)

Table 6: AC Characteristics Table*3 *5 *9
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Boot Parameters (10 MHz – 55 MHz)*4, *6, *7						
Clock cycle time	tCKb	max	—	100		ns
		min	—	18		
CKE input setup time	tISCKEb	min	—	2.5		ns
CKE input hold time	tIHCKEb	min	—	2.5		ns
Address & control input setup time	tISb	min	—	1150		ps
Address & control input hold time	tIHb	min	—	1150		ps
DQS output data access time from CK_t, CK_c	tDQSCKb	min	—	2.0		ns
		max	—	10		
Data strobe edge to output data edge	tDQSQb	max	—	1.2		ns
Mode Register Parameters						
Mode register write command period (MRW command to MRW command interval)	tMRW	min	10	10		tCK(avg)
Mode register set command delay (MRW command to non-MRW command interval)	tMRD	min	10	14		ns
Mode register read command period	tMRR	min	4	4		tCK(avg)
Additional time after tXP has expired until MRR command may be issued	tMRRI	min	—	tRCD (min)		ns
DDR3 Mobile RAM Core Parameters						
Read latency	RL	min	3	12	10	tCK(avg)
Write latency (Set A)	WL	min	1	6	6	tCK(avg)
Write latency (Set B)	WL	min	1	9	8	tCK(avg)
ACTIVATE to ACTIVATE command period	tRC	min	—	tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)		ns
CKE min. pulse width during self-refresh (low pulse width during self-refresh)	tCKESR	min	3	15		ns
Self-refresh exit to next valid command delay	tXSR	min	2	tRFCab + 10		ns
Exit power-down to next valid command delay	tXP	min	2	7.5		ns
CAS to CAS delay	tCCD	min	4	4		tCK(avg)
Internal read to precharge command delay	tRTP	min	4	7.5		ns
RAS to CAS delay	tRCD	min	3	18		ns
Row precharge time (single bank)	tRPpb	min	3	18		ns
Row precharge time (all banks)	tRPab	min	3	21		ns
Row active time	tRAS	min	3	42		ns
		max	—	70		µs
Write recovery time	tWR	min	3	15		ns
Internal write to read command delay	tWTR	min	4	7.5		ns
Active bank A to active bank B	tRRD	min	2	10		ns
Four bank activate window	tFAW	min	8	50		ns
Minimum deep power-down time	tDPD	min	—	500		µs

Table 6: AC Characteristics Table*3 *5 *9
(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
Temperature Derating						
DQS output access time from CK_t, CK_c (derated)	tDQSCK	max	—	5620		ps
RAS to CAS delay (derated)	tRCD	min	—	tRCD + 1.875		ns
ACTIVATE to ACTIVATE command period (derated)	tRC	min	—	tRC + 1.875		ns
Row active time (derated)	tRAS	min	—	tRAS + 1.875		ns
Row precharge time (derated)	tRP	min	—	tRP + 1.875		ns
Active bank A to active bank B (derated)	tRRD	min	—	tRRD + 1.875		ns
DDR3 Mobile RAM Refresh Requirement Parameters						
Refresh window	tREFW	max	—	32		ms
Required number of REFRESH commands	R	min	—	8192		
Average time between REFRESH commands (for reference only)	tREFI	max	—	3.9		µs
	tREFIpb	max	—	0.4875		µs
Refresh cycle time	tRFCab	min	—	130		ns
Per bank refresh cycle time	tRFCpb	min	—	60		ns
Burst refresh window = 4 × 8 × tRFCab	tREFBW	min	—	4.16		µs
ZQ Calibration Parameters						
Initialization calibration time	tZQINIT	min	—	1		µs
Long calibration time	tZQCL	min	6	360		ns
Short calibration time	tZQCS	min	6	90		ns
Calibration reset time	tZQRESET	min	3	50		ns
Write Leveling Timings						
First DQS_t, DQS_c edge after write leveling mode is programmed*14	tWLMRD	min	—	40		ns
DQS_t, DQS_c delay after write leveling mode is programmed*14	tWLDQSEN	min	—	25		ns
Write leveling output delay	tWLO	min	—	0		ns
		max	—	20		ns
Write leveling hold time	tWLH	min	—	175	205	ps
Write leveling setup time	tWLS	min	—	175	205	ps
CA Training Timing parameters						
First CA calibration command after CA calibration mode is programmed	tCAMRD	min	—	20		tCK(avg)
First CA calibration command after CKE is low	tCAENT	min	—	10		tCK(avg)
CA calibration exit command after CKE is high	tCAEXT	min	—	10		tCK(avg)
CKE low after CA calibration mode is programmed	tCACKEL	min	—	10		tCK(avg)
CKE high after the last CA calibration results are driven	tCACKEH	min	—	10		tCK(avg)
Data out delay after CA training calibration command is programmed	tADR	max	—	20		ns
MRW CA exit command to DQ tristate	tMRZ	min	—	3		ns
CA calibration command to CA calibration command delay	tCACD	min	—	RU (tADR/tCK) + 2		tCK(avg)

Table 6: AC Characteristics Table*3 *5 *9

(Tj = –30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V) (cont'd)

Parameter	Symbol	min max	min tCK*8	1600	1333	Unit
ODT Parameters						
Asynchronous RTT turn-on delay from ODT input	tODTon	min	—	1.75		ns
		max	—	3.5		ns
Asynchronous RTT turn-off delay from ODT input	tODToff	min	—	1.75		ns
		max	—	3.5		ns
Automatic RTT turn-on delay after READ data	tAODTon	max	—	tDQSCK(max) + 1.4 × tDQSQ(max) + tCK(avg, min)		ps
Automatic RTT turn-off delay prior to READ data	tAODToff	min	—	tDQSCK(min) – 300		ps
RTT disable delay from power-down, self-refresh and deep power-down entry	tODTd	max	—	12		ns
RTT enable delay from power-down and self-refresh exit	tODTe	max	—	12		ns

Notes: 1. CKE input setup time is measured from CKE reaching high/low voltage level to CK_t, CK_c crossing.
2. CKE input hold time is measured from CK_t, CK_c crossing to CKE reaching high/low voltage level.
3. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
4. To guarantee device operation before the DDR3 Mobile RAM Device is configured a number of AC boot timing parameters are defined in the Table 6 on page 10. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
5. Measured with 4V/ns differential CK_t/CK_c slew rate and nominal VIX (differential input cross point voltage).
6. The DDR3 Mobile RAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in Section 3 Mode Register Definition on page 17.
7. The output skew parameters are measured with Ron default settings into the reference load.
8. These parameters should be satisfied with both specification, analog (ns) value and min. tCK.
9. All AC timings assume an input slew rate of 2V/ns.
10. Read, Write, and Input setup and hold values are referenced to VREF.
11. For low-to-high and high-to-low transitions the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 1 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

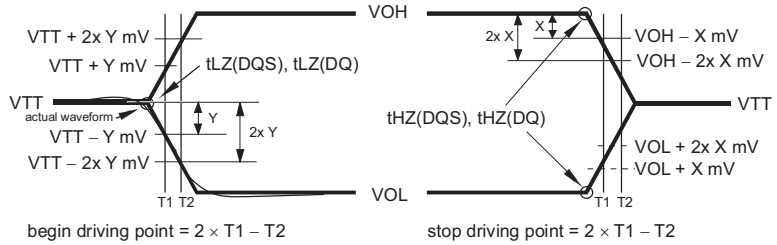


Figure 1: tLZ and tHZ Method for Calculating Transition and Endpoints

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t – DQS_c.

12. Measured from the start driving of DQS_t – DQS_c to the start driving the first rising strobe edge.
13. Measured from the start driving the last falling strobe edge to the stop driving DQS_t – DQS_c.
14. The max values are system dependent.
15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.

2.3.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

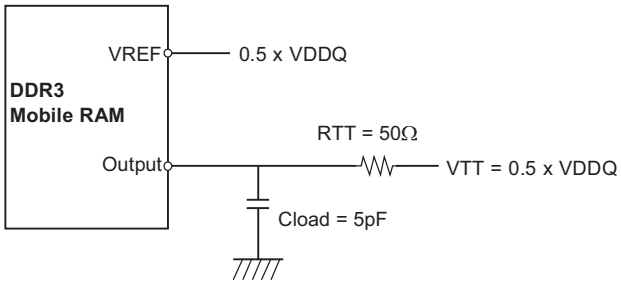


Figure 2: HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Note: 1. All output timing parameter values (like tDQSCK, tDQSQ, tHZ, tRPRE etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

3. Mode Register Definition

Table 7 shows the mode registers for DDR3 Mobile RAM.
Each register is denoted as “R” if it can be read but not written and “W” if it can be written but not read. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 7: Mode Register Assignment

MR#	MA <7:0>	Function	Acce-ss	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	RL3	WL (Set B) Support	(RFU)	RZQI		(RFU)		DAI	MR#0
1	01H	Device Feature 1	W	nWR (for AP)			(RFU)		BL			MR#1
2	02H	Device Feature 2	W	Write Leveling	WL Select	(RFU)	nWRE	RL & WL				MR#2
3	03H	I/O Config-1	W	(RFU)				DS				MR#3
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			MR#4
5	05H	Basic Config-1	R	Manufacturer ID								MR#5
6	06H	Basic Config-2	R	Revision ID1 (Die Revision)								MR#6
7	07H	Basic Config-3	R	Revision ID2 (RFU)								MR#7
8	08H	Basic Config-4	R	I/O width		Density				Type		MR#8
9	09H	Test Mode	W	Vendor-Specific Test Mode								
10	0AH	IO Calibration	W	Calibration Code								MR#10
11	0BH	ODT Feature	W	(RFU)					PD control	DQ ODT		MR#11
12:15	0CH~0FH	(Reserved)		(RFU)								
16	10H	PASR_Bank	W	Bank Mask								MR#16
17	11H	PASR_Seg	W	Segment Mask								MR#17
18:31	12H~1FH	(Reserved)		(RFU)								
32	20H	DQ Calibration Pattern A	R	See “DQ Calibration”.								MR#32
33:39	21H~27H	(Do Not Use)										
40	28H	DQ Calibration Pattern B	R	See “DQ Calibration”.								MR#40
41	29H	CA Training mode 1 entry	W	1	0	1	0	0	1	0	0	
42	2AH	CA Training mode exit	W	1	0	1	0	1	0	0	0	
43:47	2BH~2FH	(Do Not Use)		(RFU)								
48	30H	CA Training mode 2 entry	W	1	1	0	0	0	0	0	0	
49:62	31H~3EH	(Reserved)		(RFU)								
63	3FH	Reset	W	X								MR#63
64:126	40H~7EH	(Reserved)		(RFU)								
127	7FH	(Do Not Use)										
128:190	80H~BEH	(Reserved)		(RFU)								
191	BFH	(Do Not Use)										
192:254	C0H~FEH	(Reserved)		(RFU)								
255	FFH	(Do Not Use)										

Notes: 1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

MR#0_Device Information (MA<7:0> = 00H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI		(RFU)		DAI

OP<0>	DAI (Device Auto-Initialization Status) 0B: DAI complete 1B: DAI still in progress
OP<4:3>	RZQI (Built in Self Test for RZQ Information) 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)
OP<6>	WL (Set B) Support 1B: DRAM supports WL (Set B)
OP<7>	RL3 Support 1B: DRAM supports RL = 3, nWR = 3, WL = 1 for frequencies $\leq$ 166MHz

Notes: 1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.

2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 2), the DDR3 Mobile RAM device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.

4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240$\Omega \pm$ 1%).

MR#1 Device Feature 1 (MA<7:0> = 01H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)		BL		

OP<2:0>	BL 011B: BL8 All others: Reserved
OP<7:5>	If nWRE (in MR#2 OP<4>) = 0 001B: nWR = 3 100B: nWR = 6 110B: nWR = 8 111B: nWR = 9 else (if nWRE (in MR#2 OP<4>) = 1) 000B: nWR = 10 (default) 001B: nWR = 11 010B: nWR = 12 100B: nWR = 14 110B: nWR = 16 All others: Reserved

Notes: 1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

2. The range of nWR is extended using an extra bit (nWRE) in MR#2.

Table 8: Burst Sequence by BL, BT and WC

						Burst Cycle Number and Burst Address Sequence							
C2	**C1**	**C0**	**WC**	**BT**	**BL**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0B	0B	0B	Wrap	Seq	8	0	1	2	3	4	5	6	7
0B	1B	0B				2	3	4	5	6	7	0	1
1B	0B	0B				4	5	6	7	0	1	2	3
1B	1B	0B				6	7	0	1	2	3	4	5
Others			Any	Any		Illegal (Not allowed)							

2. The burst address represents C2...C0.

Notes: 1. C0 input is not present on CA bus. It is implied zero.

-

MR#2 Device Feature 2 (MA<7:0> = 02H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Leveling	WL Select	(RFU)	nWRE	RL & WL			

OP<3:0>	RL & WL If OP<6> = 0 (WL Set A, default) 0001B: RL = 3/ WL = 1 (≤ 166MHz) *1 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 6 (≤ 667MHz, default) 1001B: RL = 11 / WL = 6 (≤ 733MHz) 1010B: RL = 12 / WL = 6 (≤ 800MHz) 1100B: RL = 14 / WL = 8 (≤ 933MHz) 1110B: RL = 16 / WL = 8 (≤ 1066MHz) All others: Reserved If OP<6> = 1(WL Set B *1) 0001B: RL = 3/ WL = 1 (≤ 166MHz) *1 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 8 (≤ 667MHz, default) 1001B: RL = 11 / WL = 9 (≤ 733MHz) 1010B: RL = 12 / WL = 9 (≤ 800MHz) 1100B: RL = 14 / WL = 11 (≤ 933MHz) 1110B: RL = 16 / WL = 13 (≤ 1066MHz) All others: Reserved
OP<4>	nWRE 0B: Enable nWR programming ≤ 9 1B: Enable nWR programming > 9 (default)
OP<6>	WL Select 0B: Select WL Set A (default) 1B: Select WL Set B *2
OP<7>	Write Leveling 0B: Write Leveling Mode disabled (default) 1B: Write Leveling Mode enabled

Notes: 1. See MR#0, OP<7>
2. See MR#0, OP<6>

Table 9: DDR3 Mobile RAM Read and Write Latency

Data Rate [Mbps]	333	800	1066	1200	1333	1466	1600
tCK [ns]	6	2.5	1.875	1.67	1.5	1.36	1.25
RL	3	6	8	9	10	11	12
WL (Set A)	1	3	4	5	6	6	6
WL (Set B)	1	3	4	5	8	9	9

MR#3 I/O Configuration 1 (MA<7:0> = 03H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

OP<3:0>	DS 0001B: 34.3Ω typical pull-down/pull-up 0010B: 40Ω typical pull-down/pull-up (default) 0011B: 48Ω typical pull-down/pull-up 0100B: Reserved 0110B: Reserved 1001B: 34.3Ω typical pull-down, 40Ω typical pull-up 1010B: 40Ω typical pull-down, 48Ω typical pull-up 1011B: 34.3Ω typical pull-down, 48Ω typical pull-up All others: Reserved

MR#4 Device Temperature (MA<7:0> = 04H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		

OP<2:0>	Refresh Rate 000B: Low temperature operating limit exceeded 001B: 4 × tREFI, 4 × tREFIpb, 4 × tREFW 010B: 2 × tREFI, 2 × tREFIpb, 2 × tREFW 011B: 1 × tREFI, 1 × tREFIpb, 1 × tREFW(≤ +85°C) 100B: 0.5 × tREFI, 0.5 × tREFIpb, 0.5 × tREFW 101B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, do not de-rate AC timing 110B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, de-rate AC timing 111B: High temperature operating limit exceeded
OP<7>	TUF(Temperature Update Flag) 0B: OP<2:0> value has not changed since last read of MR#4. 1B: OP<2:0> value has changed since last read of MR#4.

Notes: 1. A Mode Register Read from MR#4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to "1" if OP2:OP0 has changed at any time since the last read of MR#4.
5. DDR3 Mobile RAM will drive OP<6:5> to '0'.
6. Specified operating temperature range and maximum operating temperature are refer to Section 1 Electrical Conditions on page 6. If maximum temperature is 85°C, functionality for over 85°C is not guaranteed.

MR#5 Basic Configuration 1 (MA<7:0> = 05H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

OP<7:0>	Manufacturer ID 00000011B 00000101B

MR#6 Basic Configuration 2 (MA<7:0> = 06H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1 (Die Revision)							

OP<7:0>	Revision ID1 (Die Revision) 00000010B: C-version Revision ID1 (Die Revision) 00000000B: A-version

MR#7 Basic Configuration 3 (MA<7:0> = 07H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2 (RFU)							

OP<7:0>	Revision ID2 (RFU)

MR#8 Basic Configuration 4 (MA<7:0> = 08H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

OP<1:0>	Type 11B: S8
OP<5:2>	Density 0110B: 4G
OP<7:6>	I/O width 00B: × 32 01B: × 16

MR#10 Calibration (MA<7:0> = 0AH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

OP<7:0>	Calibration Code FF: Calibration command after initialization AB: Long calibration 56: Short calibration C3: ZQ Reset others: Reserved

Notes: 1. Host processor shall not write MR#10 with “Reserved” values.
2. DDR3 Mobile RAM Devices shall ignore calibration command when a “Reserved” value is written into MR#10.
3. See AC timing table for the calibration latency.

MR#11 ODT Feature (MA<7:0> = 0BH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)					PD Control	DQ ODT	

OP<1:0>	DQ ODT 00B : Disabled (default) 01B : RZQ/4 10B : RZQ/2 11B : RZQ/1
OP<2>	PD Control (Power-down Control) 0B: ODT disabled by DRAM during power-down (default) 1B: ODT enabled by DRAM during power-down

MR#16 PASR_Bank Mask (MA<7:0> = 10H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

OP<7:0> — Bank Mask
0B: refresh enable to the bank (=unmasked, default)
1B: refresh blocked (=masked)

Bank and OP corresponding table

OP<7:0>	Bank	
	Bank #	Bank Address
OP0	Bank 0	000B
OP1	Bank 1	001B
OP2	Bank 2	010B
OP3	Bank 3	011B
OP4	Bank 4	100B
OP5	Bank 5	101B
OP6	Bank 6	110B
OP7	Bank 7	111B

Note: 1. Each bank can be masked independently by setting each OP value.

MR#17 PASR Segment Mask (MA<7:0> = 11H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

OP<7:0>	Segment Mask 0B: refresh enable to the segment (=unmasked, default) 1B: refresh blocked (=masked) Segment and OP corresponding table

OP<7:0>	Segment	
	Segment #	Row Address (R13:11)
OP0	Segment 0	000B
OP1	Segment 1	001B
OP2	Segment 2	010B
OP3	Segment 3	011B
OP4	Segment 4	100B
OP5	Segment 5	101B
OP6	Segment 6	110B
OP7	Segment 7	111B

Note: 1. Each segment can be masked independently by setting each OP value.

MR#32 DQ Calibration Pattern A (MA<7:0> = 20H):

Reads to MR#32 return DQ Calibration Pattern “A”.

MR#40 DQ Calibration Pattern B (MA<7:0> = 28H):

Reads to MR#40 return DQ Calibration Pattern “B”.

MR#63 Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: 1. For additional information on MRW RESET.