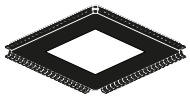
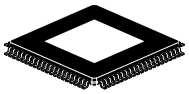
Automotive flexible U-chip for braking and transmission



TQFP80 (Exp. pad down)



TQFP80 (Exp. pad up)

Product status link
L9300

Product summary		
Order code	Package	Packing
L9300TU80T	TQFP80 exp. pad up	Tray
L9300TD80T	TQFP80 exp. pad down	Tray
L9300TD80T-TR		Tape and reel

Features

- AEC-Q100 qualified
- Four voltage regulators
  - One configurable 5 V or 6.5 V buck regulator
  - One configurable 5 V linear/tracking regulator
  - Two linear regulators with selectable output voltage
- Four tracking regulators/wheel speed sensor interfaces
- Six low-side/high-side current control drivers
  - Integrated current sense path
  - Current accuracy (in normal range)
    - ± 8 mA in 0 to 0.5 A range
    - ± 1% in 0.5 A to 1.5 A range
  - Current accuracy (in extended range)
    - ± 20 mA in 0 to 0.075 A range
    - -15 / +12 mA 0.075 A to 0.3 A
    - - 5 / +4% in 0.3 A to 0.5 A range
    - ± 4% in 0.5 A to 2 A range
  - Max driver RDS_{ON} 500 mΩ @ 175 °C
  - 11-bit current set-point resolution
  - Variable and fixed frequency current control algorithm
  - Programmable dither function
  - Selectable driver slew-rate control
- Two high-side NFET pre-drivers
- Integrated charge-pump
- CAN transceiver
- Two watchdogs type
  - Hardware watchdog
  - Software Query and Answer based watchdog
- Wake-up control
- Temperature sensor and monitoring
- Dual band gap reference and oscillator
- 32-bit SPI interface
- TQFP 80 EP (14x14)

Description

The device is an integrated circuit designed for automotive environment and implemented in BCD8s_auto technology.

The device configurability involves both the supplies block and the valve drivers stage and particularly address transmission applications.

1 Main features details

1.1 Supplies

1.1.1 VDD1 regulator

VDD1 is a buck regulator with internal N-ch FET that can provide 6.5 V or 5 V with 3% accuracy.

1.1.2 VDD2 regulator

VDD2 is a configurable internal regulator. It can work as tracking regulator (± 20 mV) or linear 5 V regulator (2% accuracy) and can provide up to 200 mA. VDD2 regulator is short to battery protected

1.1.3 VDD3 regulator

VDD3 is a linear regulator based on an external pass transistor. The output voltage selection is obtained through an external voltage divider. The accuracy of VDD3 is ± 2%.

1.1.4 VDD4 regulator

VDD4 is a linear regulator based on an external pass transistor. The output voltage selection is obtained through an external voltage divider. The accuracy of VDD4 is ± 2%.

1.1.5 TRK 1, 2, 3, 4

TRK1, TRK2, TRK3, TRK4 are 4 additional configurable tracking regulators. The regulators track the TRK_SEL pin voltage with an error of ± 20 mV. The tracking regulator outputs can be configured to be used alternatively as wheel speed interfaces.

1.2 Valve drivers

1.2.1 Current controlled channels

The device provides 6 current controlled channels. Each channel is based on a LS/HS driver structure. The device is able to work as low–side driver (with high–side active freewheeling) or as high–side driver (with low–side active freewheeling).

1.3 Others

1.3.1 High–side pre-driver

The device provides 2 High–side pre-drivers, and one of them is able to work in PWM mode up to roughly 18 kHz.

1.3.2 Watchdog

Watchdog functionality to monitor CPU activity.

1.3.3 CAN

The device includes a CAN interface.

1.3.4 RESET

The device includes two Reset pins. Both of them can be used as output while one of them can be used also as input.

1.3.5 GPO

The device provides a low–side open drain general purpose output. This output can be used as a standard low–side output or as a configurable interrupt generator through dedicated SPI bit in the Service Enable register.

2 Block diagrams

Figure 1. Internal block diagram

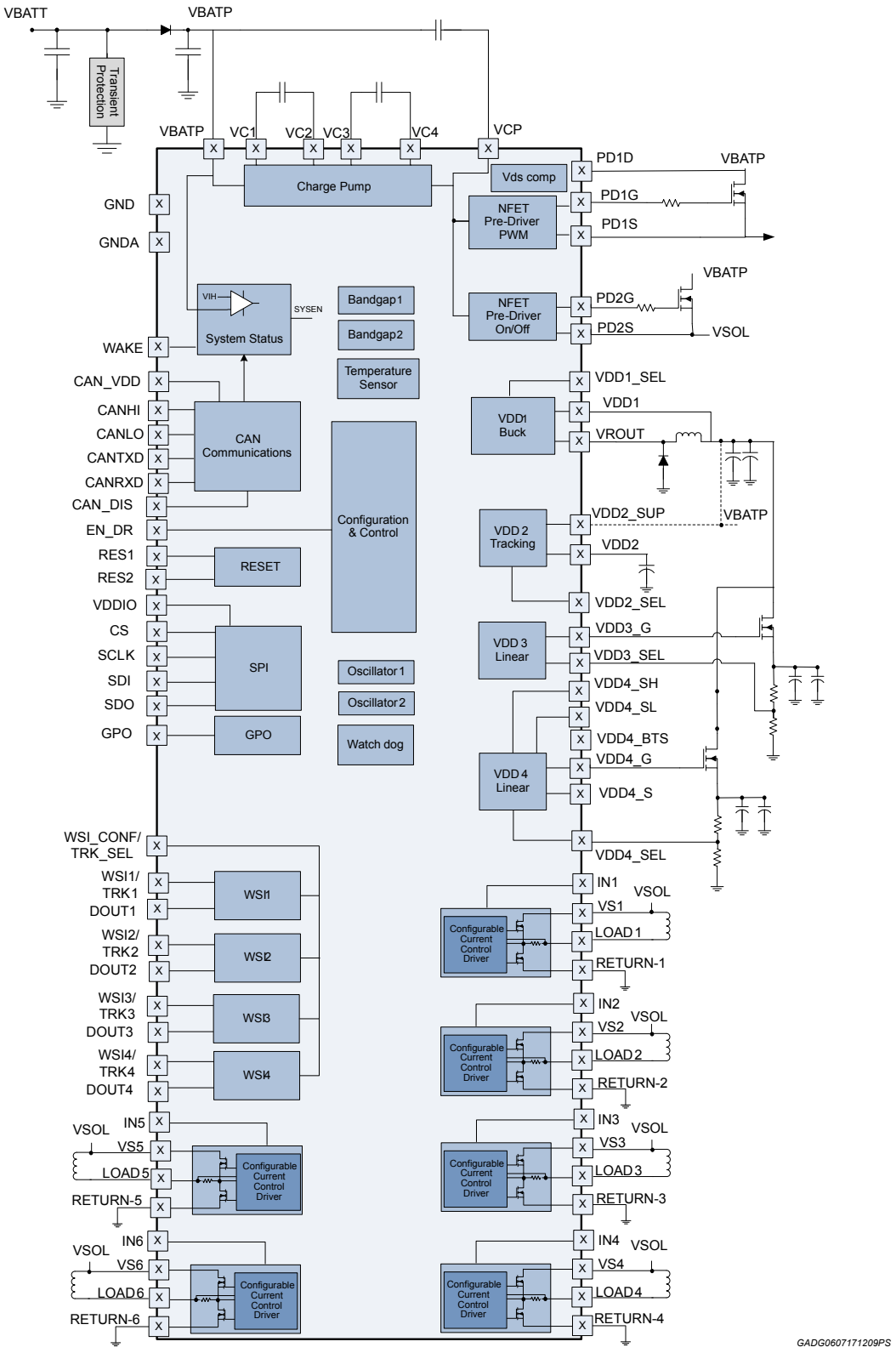
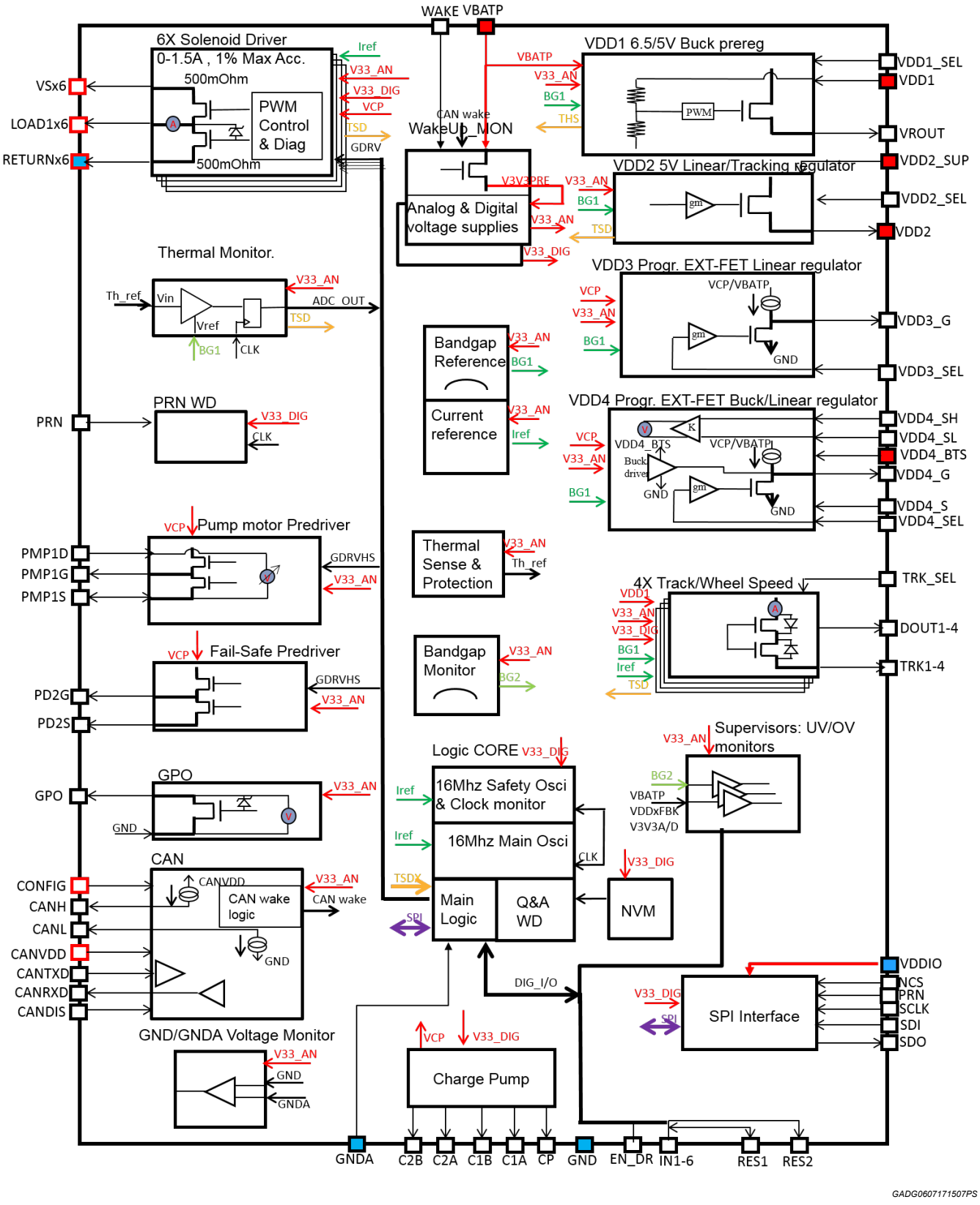
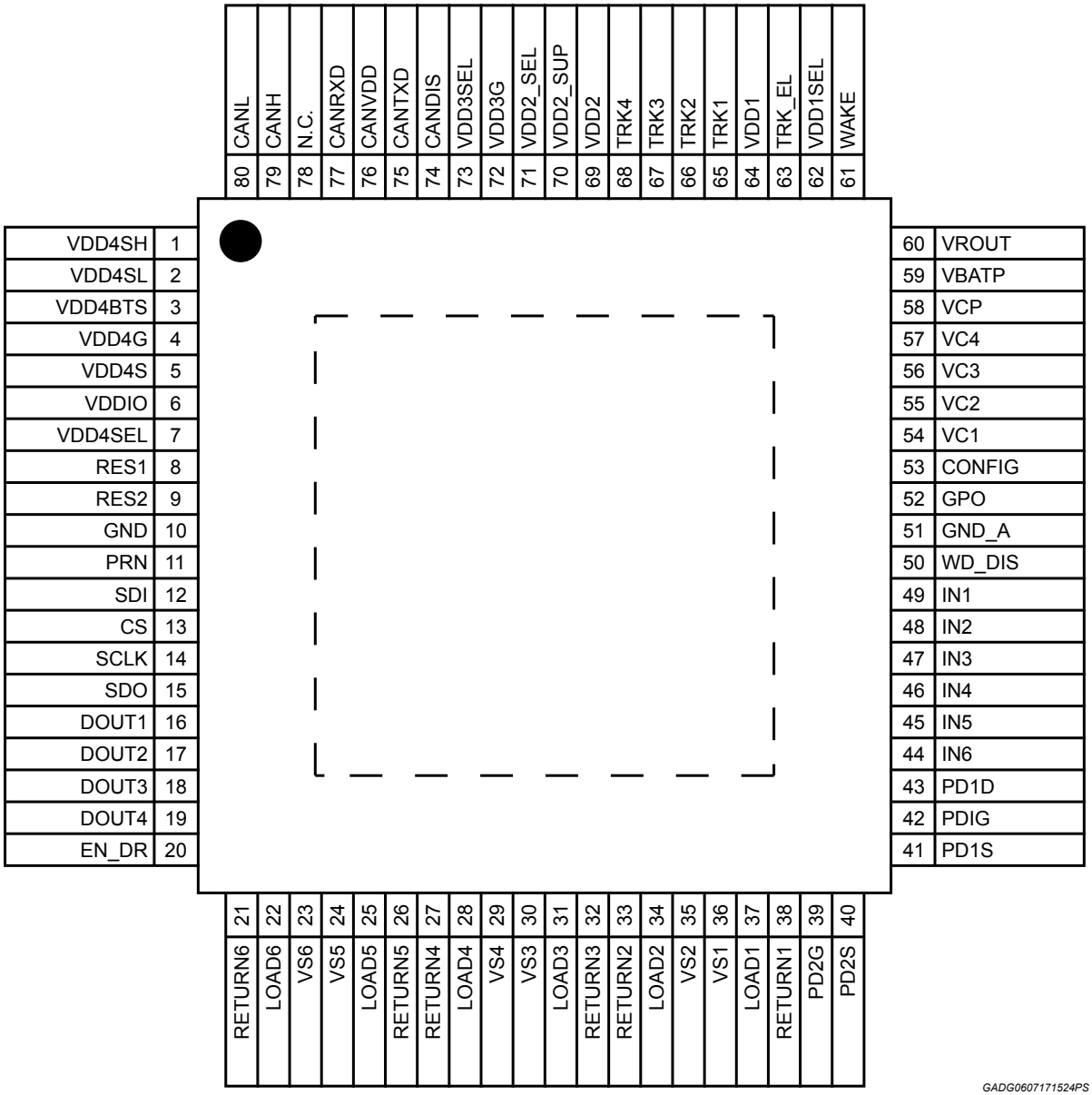


Figure 2. Internal block diagram with internal supply domain partitioning



3 Pin out

Figure 3. **Pin out (exposed pad down top view, exposed pad up bottom view)**



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4 Absolute maximum ratings

The component must withstand all the following stimuli without any damage or latch-up. Exceeding any of these values or sustaining it for extended period (defined in battery voltage range table) may lead to characteristics degradation or component damage. All voltages are related to analog ground pin GND.

Table 1. Absolute maximum ratings (-40 °C ≤ T_j ≤ 175 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin Direction
VBATP	Global		-0.3		40	V	S
VCP	Local	VCP-VBATP < 13 V, VBATP-VCP < 0.3 V	-0.3		50	V	S
VC1, VC3	Local	VCx-VBATP<0.3V	-0.3		40	V	O
VC2, VC4	Local	VCx-VBATP<13V VBATP-VCx<0.3V	-0.3		50	V	O
VSx	Global	In the application condition -1/+40V; no impact on other functions(1)	-0.3		40	V	S
PD1D	Global		-0.3		40	V	I
PD1G	Local	Internally shorted to PD1S (off phase). PD1G-PD1S<13V	-2		50	V	O
PD1S	Global	PD1S-PD1G<0.3V	-2		40	V	O
PD2G	Local	Internally shorted to PD2S (off phase). PD2G-PD2S<13V	-0.3		50	V	O
PD2S	Global	In the application condition: VSx in short condition supplied by PD2S -1/+40V, no impact on other functions.(1) PD2S-PD2G<0.3V	-0.3		40	V	O
GPO	Global	In the application condition -1/+40V; no impact on other functions(1)	-0.3		40	V	O
LOADx	Global	In the application condition -1/+40V; no impact on other functions(1)	-0.3		40	V	O
RETURNx	Local		-0.3		0.3	V	I
VDD1	Local		-0.3		19	V	O
VDD1_SEL	Local		-0.3		40	V	I
VROUT	Local		-2		40	V	O
VDD2_SUP	Global		-0.3		40	V	S
VDD2	Global		-2		40	V	O
VDD2_SEL	Local		-0.3		19	V	I
VDD3_G	Local		-0.3		19	V	O
VDD3_SEL	Local		-0.3		19	V	I
VDD4_SH	Global		-0.3		40	V	I
VDD4_SL	Global		-0.3		40	V	I
VDD4_G	Local	VDD4G-VDD4S<13V, VDD4G-VDD4BTS<0.3V	-0.3		50	V	O
VDD4_S	Local	In the application condition -2/+40V (Schottky diode activation time<0.2us), no impact on other functions.(2) VDD4S-VDD4G<0.3V	-0.3		40	V	O
VDD4_SEL	Local		-0.3		19	V	I
VDD4_BTS	Local	VDD4BTS-VDD4G<13V	-0.3		50	V	S
TRKn	Global		-2		40	V	O

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	Pin Direction
TRL_SEL	Local		-0.3		19	V	I
VDDIO	Local		-0.3		19	V	S
WAKE	Global	(3)	-0.3		40	V	I
CONFIG	Local	(3)	-0.3		40	V	I
CS, SCLK, SDI, EN_DR, VDD1_SEL, CAN_DIS, PRN, WD_DIS	Local		-0.3		19	V	I
SDO, DOUTx	Local		-0.3		19	V	O
RES1, RES2	Local		-0.3		5.5	V	O
INx	Local		-0.3		19	V	I
CAN_VDD	Local		-0.3		19	V	S
CANTXD	Local		-0.3		19	V	I
CANRXD	Local		-0.3		19	V	O
CANH, CANL	Global	CANH-CANL≤40V	-18		40	V	I/O
GND_A	Local	Digital ground reference	-0.3		0.3	V	S
GND	Local	Ground reference		0		V	S

1. *In case ECU pin is shorted to GND and gnd shift is present, the absolute can be exceeded without damage and without impact on other functions provided that the max reverse current on the involved pin is within the max value specified in the electrical characteristic sections;*
2. *During Schottky diode activation time the absolute value can be exceeded without impact on buck functionality.*
3. *Protected with external 1 kΩ series resistor during battery transients*

4.1 Latch-up trials

Latch-up tests performed according to JEDEC 78 class 2 Level A

4.2 ESD

Table 2. ESD requirements

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
ESD HBM Global	HBM global pins	ESD according Human Body Model (HBM), Q100-002 for global pins; (100 pF/1.5 kΩ)	-4		4	kV	Global
ESD HBM	HBM local pins	ESD according Human Body Model (HBM), Q100-002 for all pins; (100 pF/1.5 kΩ)	-2		2	kV	ALL
ESD CDM Corner(1)	CDM corner pins	ESD according Charged Device Model (CDM), Q100-011 Corner pins	-750		750	V	Corner
ESD CDM	CDM all pins	ESD according Charged Device Model (CDM), Q100-011 All pins	-500		500	V	ALL

1. *VDD4_SH, WAKE: -650V, slug-up version only.*

5 Temperature ranges and thermal data

All parameters are guaranteed, and tested, in the temperature range T_j -40÷150 °C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to T_j 175 °C).

Device functionality at high temperature is guaranteed by bench validation, electrical parameters are guaranteed by correlation with ATE tests at reduced temperature and adjusted limits (if needed).

Table 3. Temperature ranges and thermal data

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
T_a	Operating Temperature		-40		135	°C	ALL
T_j	Junction Temperature		-40		175	°C	ALL
T_{str}	Storage Temperature		-50		175	°C	ALL
$R_{THj\text{-}c}$(1)	Thermal Resistance junction to case			0.66	0.9	°C/W	ALL
$R_{THj\text{-}a}$(1)	Thermal Resistance junction to ambient		8.5			°C/W	ALL

1. *With 2s2p PCB thermally enhanced, cold plate as per std Jedec best practice guidelines (JESD51), assuming P_{diss} = 5 W dissipated statically and homogeneously.*

6 Battery voltage range

Table 4. Battery voltage range

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VBATP operative	Normal Operative Voltage Range(1)	T_a = -40 °C	5.5		19	V	VBATP
		T_a = 27 °C	5.55		19	V	
		T_a = 135 °C	5.6		19	V	
VBATP double	Full Operating Voltage Range(2)	$T_a \leq$ 50 °C	19		27	V	VBATP
VBATP high	High Voltage Range(3)	$T_a \leq$ 50 °C	27		40	V	VBATP
VBATP low	Low Voltage Range(4)	T_a = -40 °C	-0.3		5.5	V	VBATP
		T_a = 27 °C	-0.3		5.55	V	
		T_a = 135 °C	-0,3		5.6	V	

1. *The device shall be capable of full functional operation; min value of VBATP pin is considering the drop voltage of its reverse protection diode.*
2. *The device shall be capable of full functional operation at $T_a \leq$ 50 °C There shall be no damage to flexible, no false operation and input pins shall withstand voltage and current defined in Absolute ratings regardless of battery voltage range. Also, linear regulators output shall not exceed the Transient Load Response defined in related section and output voltage of other output signals (i.e., CPU control signal, CAN-RXD, etc) shall not exceed the voltage at normal operation. Full functional operation shall resume without any operator intervention when battery voltage returns to Normal Operating Voltage Range at $T_a \leq$ 50 °C*
3. *There shall be no damage to the device, Solenoid channels will be disabled, together with Fail Safe and Pump pre-drivers, to limit power dissipation; input pins shall withstand voltage and current defined in Absolute ratings regardless of battery voltage range. Regulator outputs shall not exceed the Transient Load Response defined in related section and output voltage of other output signals (i.e., CPU control signal, CAN-RXD, etc.) shall not exceed the voltage at normal operation. Switching regulators may violate Transient Load Response accuracy depending on target regulated voltage, however no reset should be triggered. Full functional operation shall resume without any operator intervention when battery voltage returns to Normal Operating Voltage Range.*
4. *Depending on VBATP input level the device may be in reset condition or operating mode with degraded parameters. Details of VBATP voltage range are described in Functional table, degraded parameters are specified in Electrical Characteristic tables.*

7 Power up and power down

7.1 Device configuration

The device can be configured to work in two different modes through a dedicated pin CONFIG.

As the protected battery is available and internal logic is out of reset (PORn released), the device sense the connection on the CONFIG pin: in case the pin is grounded the device is configured to work with reduced stby current consumption (no CAN activity during stby) and with a subset of functions disabled in ON state. An external 1 kΩ resistor is highly recommended to implement the connection to limit the risk of parasitic effects in case of ground shifts in the board. Once configured in reduced current consumption mode, the following features are kept disabled:

- CAN WAKE-UP
- Q&A WATCHDOG

The status of CONFIG pin is latched at power-up and available as echo on bit15 (Asic Configuration) of TRKFAULT SPI register; the latched configuration can be reset only by a switch-off of the device: in case CONFIG pin connection is lost during device activity the status of the device will not change until new power-up sequence. To avoid additional current consumption from protected battery line when the device is configured in fully functional mode no internal pull-up/down structure is implemented on the pin itself; to latch properly the high configuration on CONFIG pin, CONFIG has to be connected to a power supply available before the ASIC PORn release (example: battery line).

7.2 Power up

As the protected battery is available the device moves to a stand-by state (STBY): at that point a wake up signal on the WAKE pin is required to turn on the device and to start the regulators power up sequence as in figure below.

The device first enables internal charge pump and VDD1 pre-regulator, the following regulator’s enable signals are delayed until VDD1 reaches the VDD1_ST_en threshold to guarantee they have enough supply voltage to perform slope control and minimize overshoot; this delay is applied independently of the chosen supply for configurable regulators. Regulator’s enable is moreover delayed each other to distribute total in-rush current from supply lines: first regulator enabled after VDD1 is VDD4, followed by VDD3 and finally from VDD2 and TRKn outputs. The latest regulators wait for VDD3 and VDD4 to be out from under voltage conditions to ensure proper configuration latch in case either VDD3 or VDD4 is used as tracking reference.

Figure 4. Internal supply power-up timings

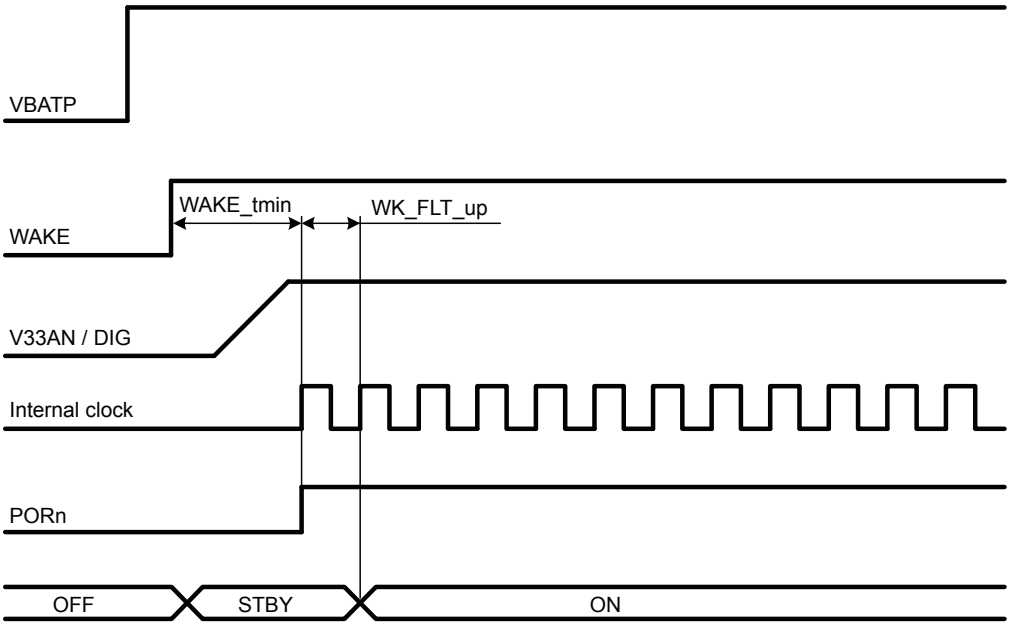
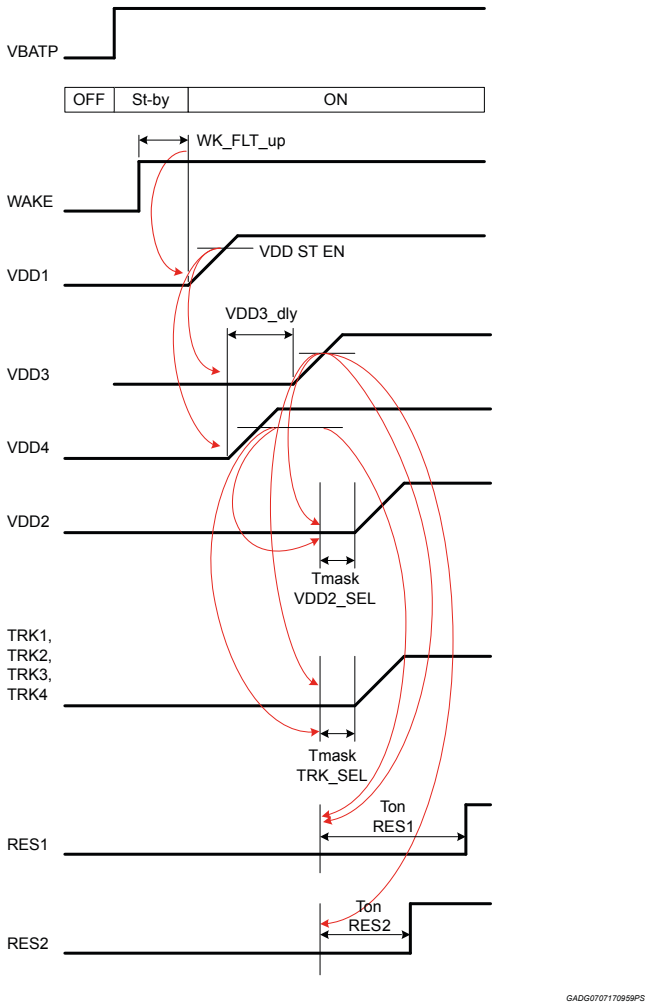


Figure 5. **Wake up through WAKE pin**



7.3 Keep on

The device provides three different possibilities to stay ON.

1. A persistent high signal on WAKE pin
2. The setting of the power hold bit through SPI
3. The refreshing of the keep alive SPI bit within a certain time frame.

At each high to low transition on the WAKE pin the device enters the keep-alive mode for one keep-alive period (KA_period).

If the device receives an SPI command to set the power hold bit within the first keep-alive period, the device remains awake.

If the device receives an SPI command to refresh the keep-alive bit within the first keep-alive period the device remains awake. Once the keep-alive bit is refreshed a new KA_period starts and so forth. To stay on the keep-alive bit should be refreshed at each KA_period; after each refresh of the keep alive counter, the keep alive bit is automatically reset.

Otherwise after the KA_period the device exits the keep-alive mode and enters in power down, unless the WAKE pin remains high.

At each power up by CAN the device enters the keep-alive mode for one keep-alive period (KA_period).

If the device receives an SPI command to set the power hold bit within the first keep-alive period the device remains awake.

If the device receives an SPI command to refresh the keep-alive bit within the first keep-alive period the device remains awake. Once the keep-alive bit is refreshed a new KA_period starts and so forth. To stay on the keep-alive bit should be refreshed at each KA_period.

7.4 Power down

The power down, depending on the keep on condition that is maintaining on the device, can happen in three different ways.

In Figure 6 the power down related to a high low transition on the WAKE pin.

In Figure 7 the power down related to the removal of power hold bit.

In Figure 8 the power down related to the not refreshing keep-alive bit from the microcontroller.

During power down all the regulators are switched off at the same time except VDD4 that is delayed by a fixed timing, provided that ASIC battery is kept supplied. No voltage control is performed during power down; in case relative voltage between regulators is needed it has to be guaranteed through external components.

Figure 6. **Power down from WAKE pin**

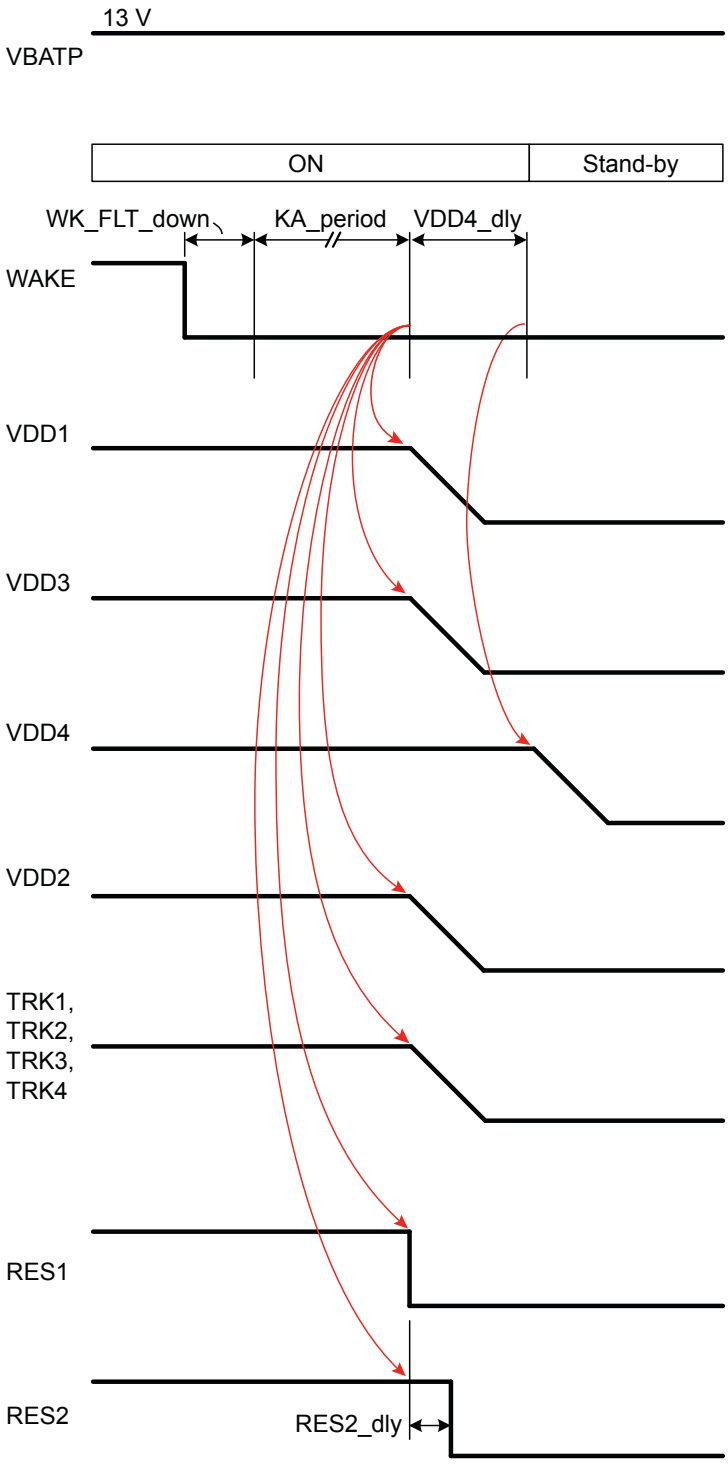


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Figure 7. **Power down from power hold condition**

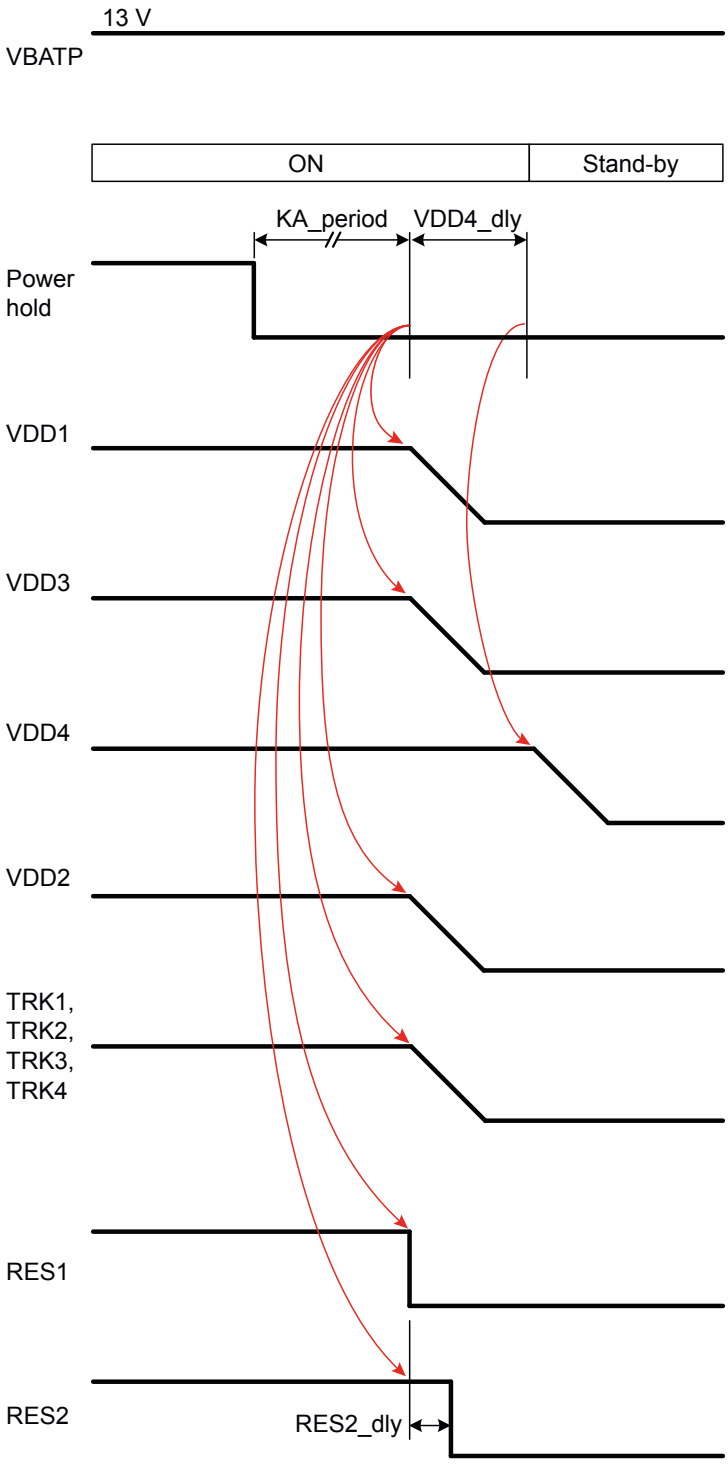

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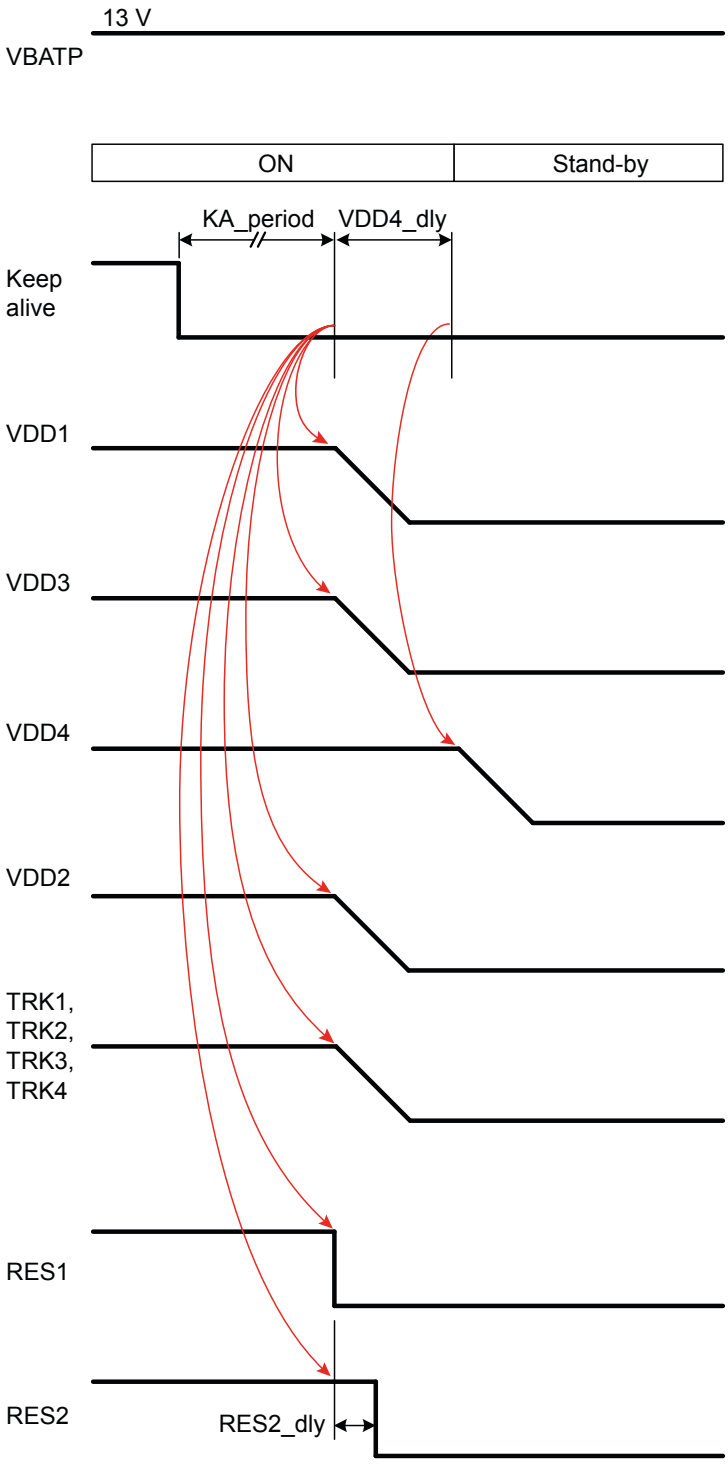
Figure 8. **Power down from not refreshing keep-alive bit**



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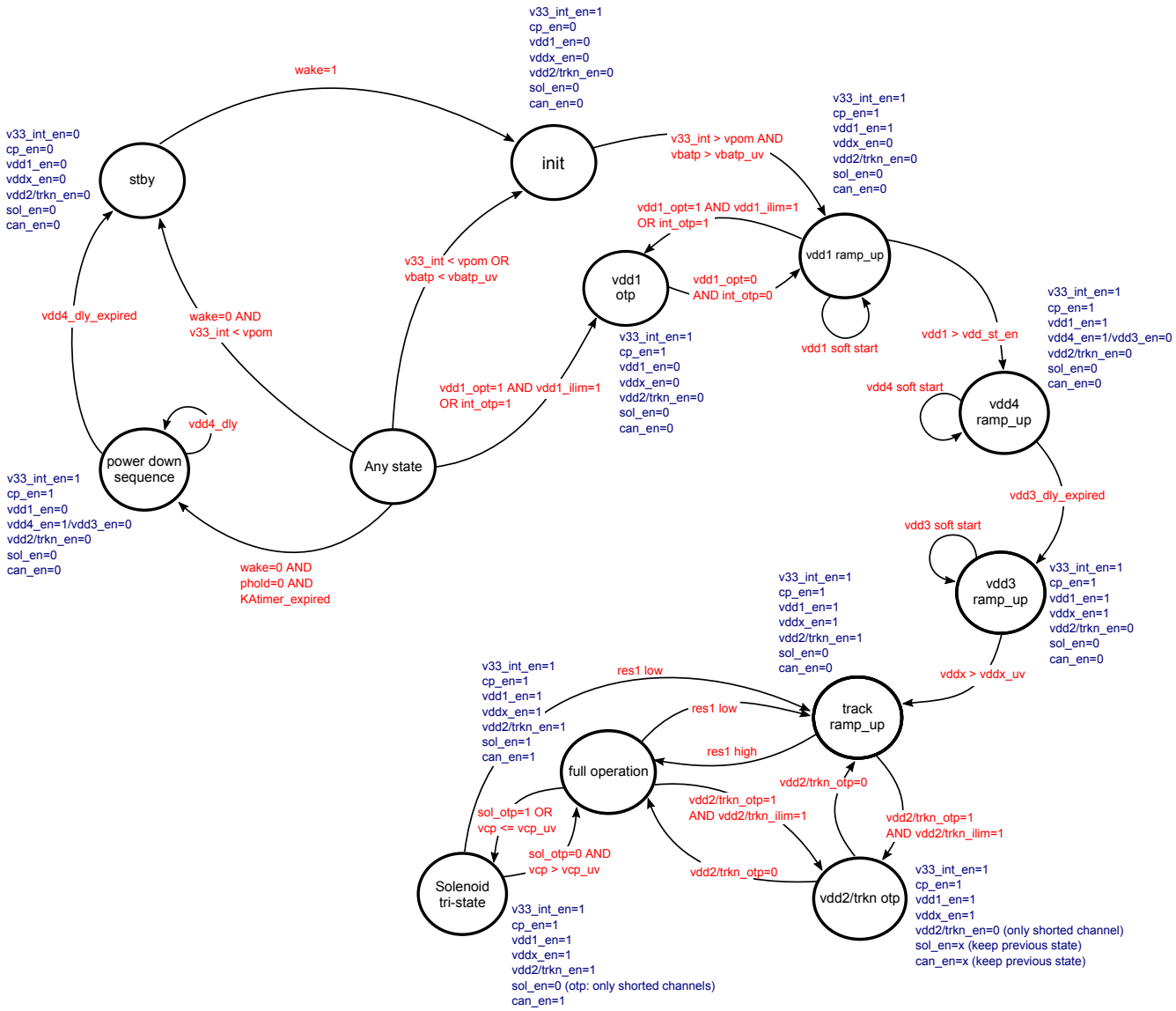
7.5 Functional state block diagram

Figure 9. Device state block diagram



7.6 Power up/down electrical characteristics

5.5V ≤ VBATP ≤ 19V; -40°C ≤ Tj ≤ 175°C unless otherwise noticed. All voltages referred to GND pin.

Table 5. Power up/down electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Current Consumption							
VBATP_stby_cur	VBATP stby current consumption	WAKE=0V, VBATP, PD1D, VDD4_SH, VDD4_SL, VDD2_SUP, VSx=13V CONFIG=0V Tambient <= 70°C	5		45	µA	VBATP
VBATP_stby_cur	VBATP stby current consumption	WAKE=0V, VBATP, PD1D, VDD4_SH, VDD4_SL, VDD2_SUP, VSx=13V, CONFIG=13V	20		90	µA	VBATP
VBATP_cur	VBATP ON current cunsumption	VBATP = 13V, WAKE=HIGH	20	30	75	mA	VBATP
Wake Up							
WAKE_high_th	WAKE high threshold		2.7		3.5	V	WAKE
WAKE_low_th	WAKE low threshold		2		2.7	V	WAKE
WAKE_hys	WAKE hysteresis		0.5			V	WAKE
WAKE_pd	WAKE pull down	WAKE < WAKE_high_th	0.4		2	MΩ	WAKE
CONFIG_low	Low current mode				0.75	V	CONFIG
CONFIG_high	Full functionality mode		1.75			V	CONFIG
VDD_st_en	Supply start enable		4.3	4.5	4.7	V	VDD1
VDD_st_en_deglitch	Digital filter time	Guaranteed by scan	7.5	10	12.5	µs	VDD1
Tmask_VDD2_SEL	Masking of VDD2 enable signal (after VDD3/4_uv release)	Guaranteed by scan	150	200	250	µs	VDD2_SEL
Tdelay_VDD2	Analog delay on soft start ramp		100		700	µs	VDD2
Tmask_TRK_SEL	Masking of TRKn enable signal (after VDD3/4_uv release)	Guaranteed by scan	150	200	250	µs	TRK_SEL
Tdelay_TRKn	Analog delay on soft start ramp		100		700	µs	TRKn
WK_FLT_up	Wake up deglitch	Guaranteed by scan	7.5	10	12.5	µs	WAKE
WK_FLT_down	Wake up deglitch	Guaranteed by scan	7.5	10	12.5	µs	WAKE
WAKE_tmin	Wake high minimum time to power-on internal logic	Design info, guaranteed by design	150			µs	WAKE
Keep On							
KA_period	Keep-alive period	Guaranteed by scan	180	200	220	ms	WAKE
VDD3_dly	Delay VDD3 from VDD4 at power up	Guaranteed by scan	0.8	1	1.2	ms	VDD3/4
Power Down							
VDD4_dly	Delay VDD4 from VDD3 at power down	Guaranteed by scan	23		35	µs	VDD3/4

8 Power supply

8.1 VDD1

8.1.1 VDD1 functional description

VDD1 is a configurable buck regulator with internal high–side MOS and external recirculation diode. The regulator, based, on the status of VDD1_SEL pin, can provide 2 different output voltages. On VDD1_SEL an internal 500 kΩ pull up resistor is present. If VDD1_SEL is left open VDD1 selected output voltage is 6.5 V, while if VDD1_SEL is connected to GND the output selected voltage is 5 V.

The VDD1_SEL pin is latched at power-up after internal PORn release to avoid unwanted changes in VDD1 output voltage during operation: the echo of latched value is available in SPI registers.

The switching frequency of the buck PWM is around 470 kHz.

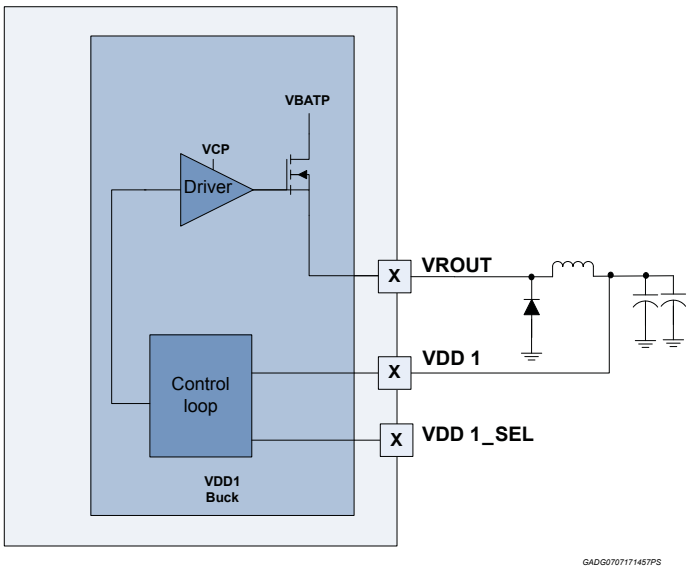
VDD1 has peak current limitation circuitry to be protected in case of shorts on the output voltage. When the output stage sensed current is higher than current limitation value the output, after min duty cycle has expired, is switched off until next PWM rising edge; in case the short condition cannot be removed, the regulator is then forced to work at minimum duty cycle causing a drop in the output voltage.

The status of the current limitation circuit is internally monitored to detect when the regulator is not able to provide the target output voltage: in case the circuit is triggered VDD1 OVER CURRENT flag is set in SPI registers. The fault condition may be triggered at low battery even if load current is within the specified range: due to design implementation the current limitation is triggered to be able to run automatically at 100% duty cycle and minimize dropout. The diagnostic is not masked during power-up phase.

VDD1 has an internal thermal protection with dedicated thermal sensor: in case the temperature shutdown is reached and the OVER CURRENT flag is set, all the regulators are turned off and a dedicated diagnostic bit is set. Once the sensed temperature is decreased below the shutdown threshold plus a thermal hysteresis, power-up sequence is restarted (vdd1_ramp_up state re-triggered).

T_SD_VDD1 is the SPI bit that latches the thermal shutdown and it is cleared on SPI read.

Figure 10. VDD1 regulator circuit



8.1.2 VDD1 electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ T_j ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 6. VDD1 electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{VDD1}	Output load current	Application note	0.01		1.3	A	VDD1
C_{VDD1}	Output capacitor	Application note Temperature and component drift included	-35%	22	+35%	µF	VDD1
C_{VDD1}ESR	Output capacitor ESR	Application note f ≤ 150 kHz			150	mΩ	VDD1
L_{VROUT}	Buck inductor	Application note Component & temperature drift included	-20%	22	+20%	µH	VROUT
L_{VROUT}	Inductor res	Application note			105	mΩ	VROUT
Configuration Input							
V_{IL}	Logic Input Low Voltage		-		0.75	V	VDD1_SEL
V_{IH}	Logic Input High Voltage		1.75			V	VDD1_SEL
$V_{hysteresis}$	Input hysteresis Voltage		0.1		1	V	VDD1_SEL
VDD1_SELPU	VDD1_SEL pull-up to internal logic supply	VDD1_SEL = 0 V	10	30	60	µA	VDD1_SEL
VDD1							
VDD1_Vout1	Regulated output voltage	VDD1_SEL = low VBATP ≥ 6 V, 10 mA ≤ I_{VDD1} ≤ 1.3 A	4.85	5	5.15	V	VDD1
VDD1_Vout2	Regulated output voltage	VDD1_SEL = high VBATP ≥ 7.5 V, 10 mA ≤ I_{VDD1} ≤ 1.3 A	6.305	6.5	6.695	V	VDD1
VDD1_line	Line regulation	VBATP 7.5 V to 19 V, I_{VDD1} = 10 mA, 1.3 A	-10		+10	mV	VDD1
VDD1_load	Load regulation	I_{VDD1} = 10 mA to 1.3 A, VBATP 7.5 V to 19 V	-10		+10	mV	VDD1
VDD1_Vout1_tr 1	Transient output voltage 1	VDD1_SEL = low, VBATP = 13 V, I_{VDD1} = 10 mA to 1.3 A dI/dt = 500 mA/µs, C_{VDD1} = 22 µF, LVROUT = 22 µH, Guaranteed by design	-8		+8	%	VDD1
VDD1_Vout2_tr 1	Transient output voltage 1	VDD1_SEL = high, VBATP = 13 V, I_{VDD1} = 10 mA to 1.3 A dI/dt = 500 mA/µs, C_{VDD1} = 22 µF, LVROUT = 22 µH, Guaranteed by design	-8		+8	%	VDD1
VDD1_Vout1_tr 2	Transient output voltage 2	VDD1_SEL = low, VBATP step 12 V to 18 V; 18 V to 12 V, dVBATP/dt = 3 V/µs, I_{VDD1} = 10 mA,1.3 A, C_{VDD1} = 22 µF, LVROUT = 22 µH, Guaranteed by design	-8		+8	%	VDD1
VDD1_Vout2_tr 2	Transient output voltage 2	VDD1_SEL = high, VBATP step 12 V to 18 V; 18 V to 12 V, dVBATP/dt = 3 V/us, I_{VDD1} = 10 mA, 1.3 A, C_{VDD1} = 22 µF, LVROUT = 22 µH, Guaranteed by design	-8		+8	%	VDD1
VDD1_ripple	Ripple voltage	VBATP = 13 V, I_{VDD1} = 1.3 A Guaranteed by design	-20		+20	mV	VDD1
VDD1_slope	Slope control	VBATP = 13 V	5		25	V/ms	VDD1
VDD1_ovs_1	Overshoot at power on Vout1				5.2	V	VDD1

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD1_ovs_2	Overshoot at power on Vout2				6.7	V	VDD1
VDD1_ovs_1 a	Overshoot VBATP step on Vout1	VBATP step from 5.5 V to 13 V during 10 µS, considering 1 µH wiring harness, Guaranteed by design			5.5	V	VDD1
VDD1_ovs_2 a	Overshoot VBATP step on Vout2	VBATP step from 5.5 V to 13 V during 10 µS, considering 1 µH wiring harness, Guaranteed by design			7.5	V	VDD1
PSRR	PSRR	VBATP = 13 V, I_{VDD1} = 1.3 A, Vnoise = 1 Vpp, fnoise = 100-200 Hz, C_{VDD1} = 22 µF, LVROUT = 22 µH Guaranteed by design	50			dB	VDD1
VROUT_ovc	Ipeak limitation	Open loop, current ramp on VROUT	2.5		3.5	A	VROUT
VROUT_min_duty	VDD1 output stage minimum on time duration	Design info, Guaranteed by design	100		300	ns	VROUT
Sw_fr	Switching frequency			f_{OSCINT}/34		kHz	VROUT
Buck_Rds_ON	High–side Rds_ON	Tj=150 °C			0.35	Ω	VROUT
Buck_Rds_ON	High–side Rds_ON	Tj=175 °C, Guaranteed by design			0.4	Ω	VROUT
Buck_ton	High–side ton	Guaranteed by design	5		40	ns	VROUT
Buck_toff	High–side toff	Guaranteed by design	5		40	ns	VROUT
VDD1 Diagnostic							
T_SD_VDD1	Temperature shut down		175		185	°C	VROUT
T_SD_hy	Temperature shut down hysteresis		5		10	°C	VROUT
T_SD_deglitch	Digital deglitch filter time	Guaranteed by scan	7.5	10	12.5	µs	VROUT

8.1.3 VDD1 error handling

Table 7. VDD1 type of errors

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VDD1 overcurrent	ON state	**VDD1 OVER CURRENT** SPI fault bit (4) latched in **SERVFLT** register	On read	N.A.
VDD1 overtemperature	ON state	If current limitation is not triggered: no action If current limitation is triggered: all outputs except Charge Pump, CAN and GPO disabled, all regulators disabled, power up sequence interrupted and **T_SD_VDD1** SPI fault bit (5) latched in **SERVFLT** register	On read	Automatic restart with re-trigger of power-up sequence after OT fault disappears.

8.2 VDD2

8.2.1 VDD2 functional description

VDD2 is an internal regulator that is configurable through VDD2_SEL pin. If 3.3 V ≤ VDD2_SEL ≤ 5 V, the regulator tracks VDD2_SEL while if VDD2_SEL = 0 V VDD2 works as linear 5 V regulator. VDD_SUP is the supply voltage of VDD2 regulator that can be connected externally to VBATP or, to limit the power dissipation, to VDD1.

Since VDD2 could be used to track either VDD3 or VDD4 voltages, VDD2 enable and configuration pin is sensed and latched at power up only after VDD3 and VDD4 voltages are above their own undervoltage thresholds: this is

intended to avoid wrong configuration latch during VDD3 and VDD4 rising phase. Echo of the latched VDD2 configuration is available in SPI registers.

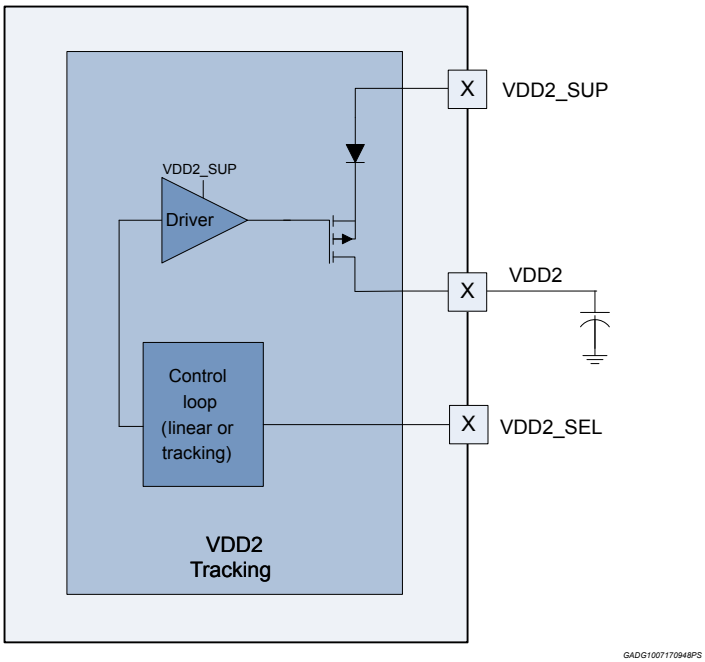
VDD2 output is short to battery protected to avoid reverse current into VDD2_SUP pin: in case the protection is triggered a diagnostic bit is set in the dedicated SPI register.

An out of regulation comparator is implemented: this comparator senses when the internal current limitation circuitry is activated to regulate properly the output voltage due to either a low drop condition or an overcurrent condition. Once out of regulation condition is detected a flag is set in SPI registers and latched until read. The diagnostic is not masked during power-up phase.

VDD2 has a thermal protection with thermal sensors shared with TRKn regulators. In case the temperature shutdown threshold is reached, and the regulator detects an out of regulation fault, it will be turned off and its dedicated diagnostic bit will be set. Once the sensed temperature is decreased below the shutdown threshold plus a thermal hysteresis, the regulator is automatically turned on with soft start function. T_SD_TRK is the bit that latches the thermal shutdown and it is cleared on SPI read.

A dedicated disable SPI bit VDD2_DIS (default condition = 0) is present and it can be used to switch off VDD2 regulator and avoid thermal on/off oscillations in case the short on output pin cannot be removed.

Figure 11. VDD2 linear or tracking regulator



8.2.2 VDD2 electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VDD2_SUP ≤ 19 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin. If VDD2_SUP < 6 V the regulator may enter in Rds ON mode where tracking error and line/load regulation accuracy depend on regulator dropout.

Table 8. VDD2 electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{VDD2}	Output load current	Application note	10		200	mA	VDD2
C_{VDD2}	Output capacitor	Application note Component & temperature drift included	-25%	2.2	+25%	µF	VDD2
C_{VDD2} ESR	Output capacitor maximum ESR	Application note f ≤ 150 kHz	0.01		1	Ω	VDD2
C_{VDD2} EXT	External sensor capacitor	Application note			150	µF	VDD2

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD2_SUP_Ileak_dis	VDD2_SUP leakage current	VDD2_SUP = 13 V, WAKE = 0 V	-1		1	µA	VDD2_SUP
Configuration Input							
VIL	Logic Input Low Voltage		-		0.75	V	VDD2_SEL
VIH	Logic Input High Voltage		1.75		-	V	VDD2_SEL
Vhysteresis	Input hysteresis Voltage		0.1		1	V	VDD2_SEL
VDD2_SELPD	VDD2_SEL pull down	VDD2_SEL = 5 V	10	50	130	µA	VDD2_SEL
Tracking configuration 3.3 V ≤ VDD2_SEL ≤ 5 V							
VDD2_Vout	Regulated output voltage	VDD2_SUP ≥ 6 V, 10 mA ≤ I_{VDD2} ≤ 200 mA	VDD2_SEL -20 mV	VDD2_SEL	VDD2_SEL +20 mV	V	VDD2
VDD2_error	Matching error	VDD2_SEL – VDD2, VDD2_SUP ≥ 6 V, 10 mA ≤ I_{VDD2} ≤ 200 mA	-20 m		+20 m	V	VDD2
VDD2_line	Line regulation	VDD2_SUP 6 V to 19 V, I_{VDD2} = 10 mA, 200 mA	-10		+10	mV	VDD2
VDD2_load	Load regulation	I_{VDD2} = 10 mA to 200 mA, VDD2_SUP 6 V to 19 V	-10		+10	mV	VDD2
VDD2_Vout_tr1	Transient output voltage 1	VBATP = 13 V, I_{VDD2} = 10 mA to 200 mA dI/dt = 200 mA/µs, C_{VDD2} = 2.2 µF, Guaranteed by design	-5		+5	%	VDD2
VDD2_Vout_tr2	Transient output voltage 2	VDD2_SUP step 12 V to 18 V; 18 V to 12 V dVDD2_SUP/dt = 3 V/ µs, I_{VDD2} = 10 mA, 200 mA, C_{VDD2} = 2.2 µF, Guaranteed by design	-5		+5	%	VDD2
VDD2_RdsON	RdsON	Tj =150 °C, VDD2_SUP = VDD2_SEL, I_{VDD2} = 200 mA			3.6	Ω	VDD2
VDD2_RdsON	RdsON	Tj = 175 °C, VDD2_SUP = VDD2_SEL, I_{VDD2} = 200 mA, Guaranteed by design			4	Ω	VDD2
VDD2_PSSR	PSSR	VDD2_SUP = 6.5 V, I_{VDD2} = 200 mA, Vnoise = 1 Vpp, fnoise = 465 kHz, C_{VDD2} = 2.2 µF Guaranteed by design	20			dB	VDD2
VDD2_cur lim	Current limitation	VDD2 = -2 V	250		390	mA	VDD2
VDD2_rev cur	Reverse current in off condition	VDD2 = VDD2_SUP + 2 V, VDD2 disabled	0.2		2	mA	VDD2
VDD2_rev cur	Reverse current in on condition	VDD2 = VDD2_SUP + 2 V, VDD2 enabled	0.2		2	mA	VDD2
VDD2_ovs_a	Overshoot at power on	I_{VDD2} = 10 mA, C_{VDD2} = 2.2 µF			5.5	V	VDD2
VDD2_ovs_b	Overshoot at VBATP step	VBATP step from 5.5 to 13 V during 10 µS, considering 1 µH wiring harness, I_{VDD2} = 200 mA, C_{VDD2} = 2.2 µF, Guaranteed by design			5.7	V	VDD2
VDD2_off	Off state voltage				1	V	VDD2
VDD2_soft	Slope control	VDD2_SUP=VBATP = 13 V I_{VDD2} = 10 mA, C_{VDD2} = 2.2 µF	5		30	V/ms	VDD2
Linear configuration VDD2_SEL=0 V							

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD2_Vout	Regulated output voltage	VDD2_SUP ≥ 6 V, 10 mA ≤ I_{VDD2} ≤ 200 mA	4.9	5	5.1	V	VDD2
VDD2_line	Line regulation	VDD2_SUP 6 V to 19 V, I_{VDD2} = 10 mA, 200 mA	-10		+10	mV	VDD2
VDD2_load	Load regulation	I_{VDD2} = 10 mA to 200 mA, VBATP 6 V to 19 V	-10		+10	mV	VDD2
VDD2_Vout_tr1	Transient output voltage 1	VDD2_SUP = 13 V, I_{VDD2} = 10 mA to 200 mA dI/dt = 200 mA/µs, C_{VDD2} = 2.2 µF, Guaranteed by design	-5		+5	%	VDD2
VDD2_Vout_tr2	Transient output voltage 2	VDD2_SUP step 12 V to 18 V; 18 V to 12 V, dVDD2_SUP/dt = 3 V/µs, I_{VDD2} = 10 mA, 200 mA, C_{VDD2} = 2.2 µF, Guaranteed by design	-5		+5	%	VDD2
VDD2_RdsON	RdsON	Tj = 150 °C, VDD2_SUP = VDD2_SEL, I_{VDD2} = 200 mA			3.6	Ω	VDD2
VDD2_RdsON	RdsON	Tj = 175 °C, VDD2_SUP = VDD2_SEL, I_{VDD2} = 200 mA, Guaranteed by design			4	Ω	VDD2
VDD2_PSSR	PSSR	VDD2_SUP = 6.5 V, I_{VDD2} = 200 mA, Vnoise = 1 Vpp, fnoise = 465 kHz, C_{VDD2} = 2.2 µF Guaranteed by design	20			dB	VDD2
VDD2_cur lim	Current limitation	VDD2 = -2 V	250		375	mA	VDD2
VDD2_rev cur	Reverse current in off condition	VDD2 = 20 V VDD2_SUP from 0 V to 19 V, VDD2 disabled	0.2		2	mA	VDD2
VDD2_rev cur	Reverse current in on condition	VDD2 = 20 V VDD2_SUP from 0 V to 19 V VDD2 enabled	0.2		2	mA	VDD2
VDD2_ovs_a	Overshoot at power on	I_{VDD2} = 10 mA, C_{VDD2} = 2.2 µF			5.5	V	VDD2
VDD2_ovs_b	Overshoot at VBATP step	VBATP step from 5.5 V to 13 V during 10 µs, considering 1 µH wiring harness, I_{VDD2} = 200 mA, C_{VDD2} = 2.2 µF			5.7	V	VDD2
VDD2_off	Off state voltage				1	V	VDD2
VDD2_soft	Soft start	I_{VDD2} = 10 mA, C_{VDD2} = 2.2 µF	5		25	V/ms	VDD2
Diagnostic							
VDD2_rev_cur_det	Reverse current detection voltage		VDD2_SUP		VDD2_SUP +0.2	V	VDD2
T_SD_TRK	Temperature shut down		175		185	°C	VDD2
T_SD_hy	Temperature shut down hysteresis		5		10	°C	VDD2
T_SD_deglitch	Digital deglitch filter time	Guaranteed by scan	7.5	10	12.5	µs	VDD2

8.2.3 VDD2 error handling

Table 9. **VDD2 type of errors**

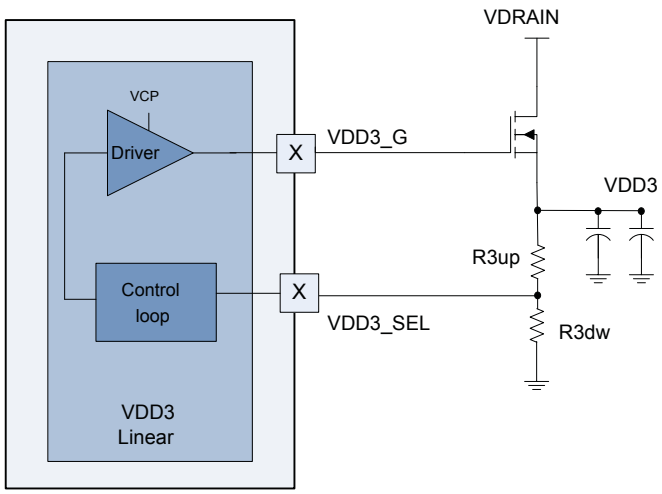
Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VDD2 out of regulation	ON state	Set **VDD2_OUT_OF_REGULATION** SPI flag (4) in **TRK-CAN FAULT** register	On read	N.A
VDD2 reverse current	ON state	VDD2 internal path to VDD2_SUP open, **VDD2_REVERSE_CURRENT** SPI flag (6) latched in **TRK-CANFAULT** register	On read	Automatic restart when fault disappears.
VDD2 overtemperature	ON state	No action if out of regulation is not triggered; output disabled, and **T_SD_TRK** (5)SPI fault bit latched otherwise in **TRK-CAN FAULT** register	On read	Automatic restart with slope control after OT fault disappears.

8.3 VDD3

8.3.1 VDD3 functional description

VDD3 is a linear regulator using external N-channel transistor as output stage to deliver current to the load and reduce ASIC power dissipation. The regulated voltage is configurable through the external feedback resistors. Dedicated monitors are present on VDD3_SEL pin to detect VDD3 undervoltage and overvoltage conditions; voltage monitors are not masked during power-up phase.

Figure 12. **VDD3 linear regulator with external N-ch FET**



VDRAIN can be connected to either VBATP or, in order to limit power consumption, to a pre-regulated voltage.

8.3.2 VDD3 electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VDRAIN ≤ 19 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin. STD20NF06L used as test reference for external MOS.

Table 10. **VDD3 electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Ciss	External FET input capacitor	Application note: FET selection max input capacitance to guarantee stability			900	pF	
Gm	External FET transconductance	Application note: FET selection		20		mho	
Vth	External FET threshold	Application note: FET selection threshold voltage			3	V	
VDD3_Vout	Output voltage	Application note	0.8		5	V	VDD3
I_{VDD3}	Output load current	Application note	0.01		1	A	VDD3
C_{VDD3}	Output capacitor	Application note	5	22	40	µF	VDD3
C_{VDD3_OPT}	Optional output capacitor(1)	Application note max drivable cap in parallel with C_{VDD3}			220	µF	VDD3
C_{VDD3} ESR	Output capacitor ESR	Application note f ≤ 150 kHz	0.01		0,1	Ω	VDD3
C_{DRAIN3} EMI	Drain Output capacitor	Application note, VDRAIN=VBATP Capacitor required on the drain of external N-channel FET to prevent self-mode oscillations and to improve EMI robustness	1			µF	
C_{DRAIN3} EMI	Drain Output capacitor	Application note, VDRAIN=VDD1 Capacitor required on the drain of external N-channel FET to prevent self-mode oscillations and to improve EMI robustness	0.1			µF	
R3up	Feedback resistor range		5		15	kΩ	VDD3_SEL
VDD3 Regulator							
VDD3_SEL	Regulated feedback voltage	0.01 A ≤ I_{VDD3} ≤ 1 A	0.8–2%	0.8	0.8+2%	V	VDD3_SEL
VDD3_SEL line	Line regulation	VDRAIN 6 V to 19 V, I_{VDD3} = 0.01 A, 1 A	-5		+5	mV	VDD3_SEL
VDD3_SEL load	Load regulation	I_{VDD3} = 0.01 A to 1 A, VDRAIN 6 V to 19 V	-5		+5	mV	VDD3_SEL
VDD3_SEL _tr1	Transient output voltage 1	VDRAIN = 13 V, VDD3 ≥ 3.3 V, ΔI_{VDD3} =300 mA; dI/dt = 0.5 A/µs, C_{VDD3} = 5 µF, Guaranteed by design	-5		+5	%	VDD3_SEL
VDD3_SEL _tr1	Transient output voltage 1 (No Reset Asserted)	VDRAIN = 13 V, VDD3 < 3.3 V, ΔI_{VDD3} =300 mA; dI/dt = 0.5 A/µs, C_{VDD3} = 5 µF, Guaranteed by design	-8		+8	%	VDD3_SEL
VDD3_SEL _tr2	Transient output voltage 2 (No Reset Asserted)	VDRAIN step 12 V to 18 V; 18 V to 12 V, dVDRAIN/dt = 3 V/µs, I_{VDD3} = 0.01 A, 1 A, C_{VDD3} = 5 µF, Guaranteed by design	-7		+7	%	VDD3_SEL
VDD3_G out	Gate output voltage	VBATP = 5.5 V, Open loop condition, VDD3_SEL = 0.7 V	12		16	V	VDD3_G
VDD3_G pd	Gate internal pull down		100		1000	kΩ	VDD3_G
VDD3_PSSR	PSSR	VDRAIN = 6.5 V, I_{VDD3} = 500 mA, Vnoise = 1 Vpp, fnoise = 465 kHz, C_{VDD3} = 5 µF Guaranteed by design	20			dB	VDD3
VDD3_SEL ovs_a	Overshoot at power on	I_{VDD3} = 10 mA, C_{VDD3} = 5 µF			4%	V	VDD3_SEL

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD3_SEL ovs_b	Overshoot at VBATP step	VBATP step from 5.5 V to 13 V during 10 µs, I_{VDD3} = 500 mA, C_{VDD3} = 5 µF, Guaranteed by design			10%	V	VDD3_SEL
VDD3_SEL soft	Slope control	VDRAIN=VBATP = 13 V I_{VDD3} = 10 mA, C_{VDD3} = 4.7 µF	1		5	V/ms	VDD3_SEL
Diagnostic							
VDD3_UV	VDD3_SEL undervoltage		VDD3_SEL typ * (9.1/10)		VDD3_SEL typ * (9.6/10)	V	VDD3_SEL
VDD3_UV_ft	VDD3_SEL undervoltage filter time	Guaranteed by scan	8		16	µs	VDD3_SEL
VDD3_OV	VDD3_SEL overvoltage		VDD3_SEL typ * (11/10)		VDD3_SEL typ * (11.8/10)	V	VDD3_SEL
VDD3_OV_ft	VDD3_SEL overvoltage filter time	Guaranteed by scan	16		32	µs	VDD3_SEL

1. *If VDRAIN is supplied by VDD1, the value of the optional filtering capacitor must be chosen taking into account VDD1 current limitation value vs in-rush current during regulator power-up and supply transients.*

8.3.3 VDD3 error handling

Table 11. VDD3 type errors

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VDD3 under voltage	ON state	RES1, RES2 driven low. **VDD3 UNDER VOLTAGE** SPI flag (6) latched in **SERVFLT** register	On read	Automatic after fault disappears
VDD3 over voltage	ON state	RES1, RES2 driven low. **VDD3 OVER VOLTAGE** SPI flag (8) latched in **SERVFLT** register	On read	Automatic after fault disappears

8.4 VDD4

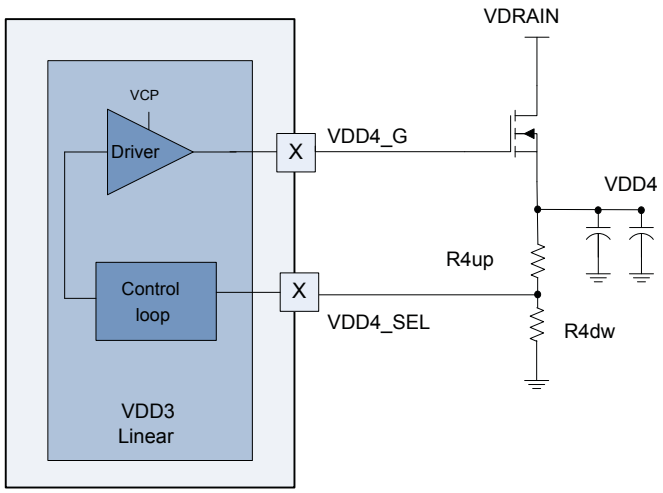
8.4.1 VDD4 functional description

VDD4 is a linear regulator that can work with an external N-channel FET. An external feedback resistor sets the output voltage of the regulator.

To configure VDD4 to work as a linear regulator VDD4_SH pin has to be left floating; the configuration (VDD4_SH connected to supply line or open) is latched after VDD1 has reached. VDD_st_en threshold to avoid wrong configuration detection during battery ramp-up. When used in linear configuration the unused pins can be left floating (alternatively VDD4_BTS can be shorted with VDD4S to the source of external FET). Echo of the latched configuration is available in SPI registers.

Dedicated monitors are present on VDD4_SEL pin to detect VDD4 undervoltage and overvoltage conditions; voltage monitors are not masked during power-up phase.

Figure 13. **VDD4 regulator linear configuration**



VDRAIN can be connected to either VBATP or, in order to limit power consumption, to a preregulated voltage.

8.4.2 VDD4 electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VDRAIN ≤ 19 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin. STD20NF06L used as test reference for external MOS.

Table 12. **VDD4 electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Configuration Input							
V_{IL}	Logic Input Low Voltage		-		0.75	V	VDD4_SH
V_{IH}	Logic Input High Voltage		1.75		-	V	VDD4_SH
$V_{hysteresis}$	Input hysteresis Voltage		0.1		1	V	VDD4_SH
$I_{leak\_VDD4\_SH}$	Leakage current	VDD4_SH = 13 V, WAKE=0 V	-1		1	µA	VDD4_SH
$I_{leak\_VDD4\_SL}$	Leakage current	VDD4_SL = 13 V, WAKE=0 V	-1		1	µA	VDD4_SL
VDD4_SHPD	VDD4_SH pull down	VDD4_SH = 5 V	10	50	100	µA	VDD4_SH
Linear Configuration							
Ciss	External FET input capacitor	Application note: FET selection max input capacitance to guarantee stability			900	pF	
Gm	External FET transconductance	Application note: FET selection		20		mho	
Vth	External FET threshold	Application note: FET selection threshold voltage			3	V	
VDD4_Vout	Output voltage	Application note	0.8		5	V	VDD4
I_{VDD4}	Output load current	Application note	0.01		1	A	VDD4
C_{VDD4}	Output capacitor	Application note	5		40	µF	VDD4
CVDD4_OPT	Optional output capacitor(1)	Application note: max drivable cap in parallel with C_{VDD4}			200	µF	VDD4
C_{VDD4} ESR	Output capacitor ESR	Application note f <= 150 kHz	0.01		0,1	Ω	VDD4

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
CDRAIN3 EMI	Drain Output capacitor	Application note, VDRAIN=VBATP, capacitor required on the drain of external N-ch FET to prevent selfmode oscillations and to improve EMI robustness	1			µF	
CDRAIN3 EMI	Drain Output capacitor	Application note, VDRAIN=VDD1, capacitor required on the drain of external N-ch FET to prevent selfmode oscillations and to improve EMI robustness	0.1			µF	
R4up	Feedback resistor range	Application note	5		15	kΩ	VDD4_SEL
VDD4_SEL	Regulated feedback voltage	0.01 A ≤ I_{VDD3} ≤ 1 A	0.8 – 2%	0.8	0.8 + 2%	V	VDD4_SEL
VDD4_SEL line	Line regulation	VDRAIN 6 V to 19 V, I_{VDD4} = 0.01 A, 1 A	-5		+5	mV	VDD4_SEL
VDD4_SEL load	Load regulation	I_{VDD4} = 0.01 A to 1 A, VDRAIN 6 V to 19 V	-5		+5	mV	VDD4_SEL
VDD4_SEL _tr1	Transient output voltage 1	VDRAIN = 13 V, VDD4 ≥ 3.3 V, ΔI_{VDD4} =300 mA; dI/dt = 0.5 A/µs, C_{VDD4} = 5 µF, Guaranteed by design	-5		+5	%	VDD4_SEL
VDD4_SEL _tr1	Transient output voltage 1 (No Reset Asserted)	VDRAIN = 13 V, VDD4 < 3.3 V, ΔI_{VDD4} =300 mA; dI/dt = 0.5 A/µs, C_{VDD4} = 5 µF, Guaranteed by design	-8		+8	%	VDD4_SEL
VDD4_SEL _tr2	Transient output voltage 2 (No Reset Asserted)	VDRAIN step 12 V to 18 V; 18 V to 12 V, dVDRAIN/dt = 3 V/µs, I_{VDD4} = 0.01 A, 1 A, C_{VDD4} = 5 µF, Guaranteed by design	-7		+7	%	VDD4_SEL
VDD4_G out	Gate output voltage	VBATP = 5.5 V, Open loop condition, VDD4_SEL = 0.7 V	12		16	V	VDD4_G
VDD4_G pd	Gate internal pull down		100		1000	kΩ	VDD4_G
VDD4_PSSR	PSSR	VDRAIN = 6.5 V, I_{VDD3} = 500 mA, Vnoise = 1 Vpp, fnoise = 465 kHz, C_{VDD4} = 5 µF Guaranteed by design	20			dB	VDD4
VDD4_SEL ovs_a	Overshoot at power on	I_{VDD4} = 10 mA, C_{VDD4} = 5 µF			+4%	V	VDD4_SEL
VDD4_SEL ovs_b	Overshoot at VBATP step	VBATP step from 5.5 V to 13 V during 10 µs, I_{VDD4} = 500 mA, C_{VDD4} = 5 µF, Guaranteed by design			+10%	V	VDD4_SEL
VDD4_SEL soft	Slope control	VDRAIN=VBATP = 13 V I_{VDD4} = 10 mA, C_{VDD4} = 4.7 µF	1		5	V/ms	VDD4_SEL
Diagnostic							
VDD4_UV	VDD4_SEL undervoltage		VDD4_SEL typ * (9.1/10)		VDD4_SEL typ * (9.6/10)	V	VDD4_SEL
VDD4_UV_ft	VDD4_SEL undervoltage filter time	Guaranteed by scan	8		16	µs	VDD4_SEL
VDD4_OV	VDD4_SEL overvoltage		VDD4_SEL typ * (11/10)		VDD4_SEL typ * (11.8/10)	V	VDD4_SEL
VDD4_OV_ft	VDD4_SEL overvoltage filter time	Guaranteed by scan	16		32	µs	VDD4_SEL

1. *If VDRAIN is supplied by VDD1, the value of the optional filtering capacitor must be chosen taking into account VDD1 current limitation value vs in-rush current during regulator power-up and supply transients.*

8.4.3 VDD4 error handling

Table 13. **VDD4 type errors**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VDD4 under voltage	ON state	RES1 driven low. **VDD4 UNDER VOLTAGE** SPI flag (7) latched in **SERVFLT** register	On read	Automatic after fault disappears
VDD4 over voltage	ON state	RES1 driven low. **VDD4 OVER VOLTAGE** SPI flag (9) latched in **SERVFLT** register	On read	Automatic after fault disappears

8.5 TRK 1, 2, 3, 4

TRK1, TRK2, TRK3, TRK4 are four tracking regulators that can be configured to work also as wheel speed interface depending on the voltage applied on TRK_SEL pin. All four regulators act as wheel speed interface in case the TRL_SEL pin is grounded, otherwise each regulator tracks independently the voltage provided at TRK_SEL pin (3.3 ≤ TRK_SEL ≤ 5) with a matching error of ± 20 mV. Since TRK outputs can be used to track VDD3 or VDD4 voltages, their configuration is masked and they are kept disabled until both VDDx voltages are above their undervoltage threshold to avoid wrong configuration detection during power-up. Once triggered the configuration is latched and the echo of the configuration is provided in SPI registers.

8.5.1 Tracking regulator configuration

Functional description

Connecting TRK_SEL to either VDD3 or VDD4 output voltage or an external voltage reference the TRKn outputs are configured as tracking regulators and start providing an output voltage in track with the desired reference. The four TRKn outputs are however able to track only voltages starting from 3.3V.

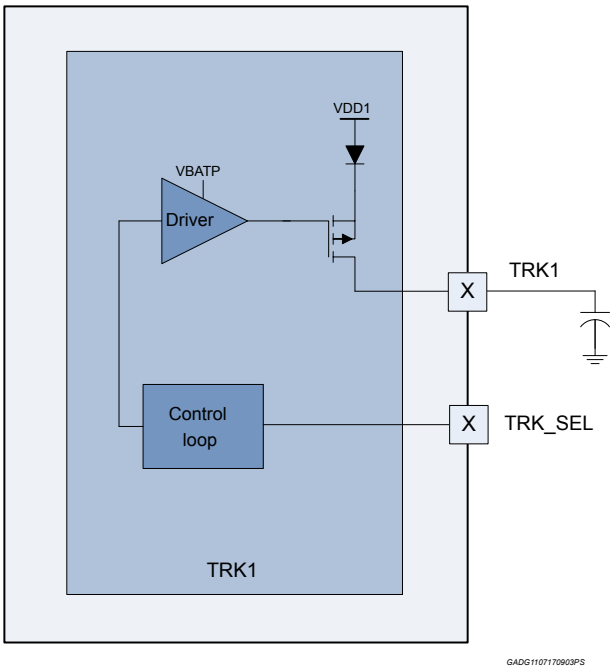
TRK outputs are short to battery protected to avoid reverse current into VDD1 pin: in case the protection is triggered a diagnostic bit is set in the dedicated SPI register.

An out of regulation comparator is implemented: this comparator senses when the internal current limitation circuitry is activated to regulate properly the output voltage due to either a low drop condition or an overcurrent condition. Once out of regulation condition is detected a flag is set in SPI registers and latched until read. The diagnostic is not masked during power-up phase.

TRK regulators have a thermal protection with thermal sensors shared with VDD2 regulator. In case the temperature threshold is reached and the out of regulation flag is set, only the regulator in fault condition is turned off and a dedicated diagnostic bit is set. Once the sensed temperature is decreased below the shutdown threshold plus a thermal hysteresis, the regulator is automatically turned on with soft start function. T_SD_TRK is the bit that latches the thermal shutdown and it is cleared on SPI read.

A dedicated disable SPI bit TRKn_DIS (default condition: track enabled) is present and it can be used to avoid thermal on/off oscillations in case the short on output pin cannot be removed.

Figure 14. **TRK regulators**



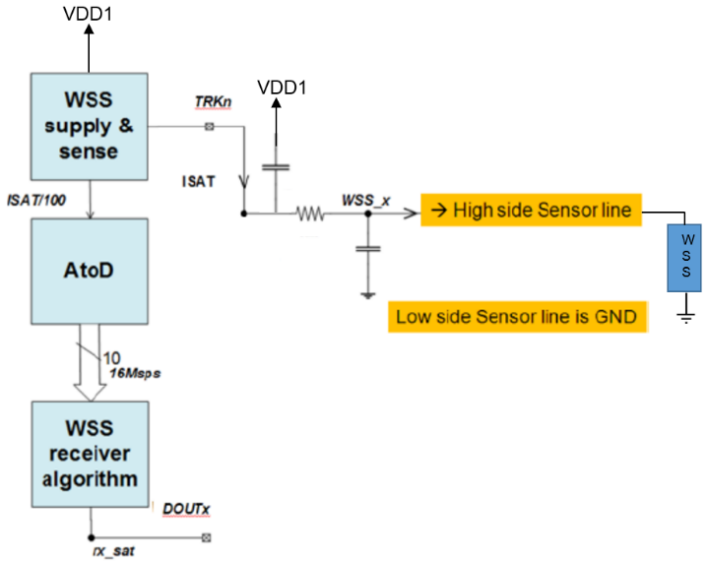
8.5.2 WSI configuration

Functional description

If TRK_SEL pin is grounded, the device provides 4 wheel speed sensor interfaces on TRKn pins: the status of each sensor is reported to the microcontroller via the SPI. The input signal of an active sensor is a rectangular signal with variable pulse width and output currents of 2 level (7/14 mA) or 3 levels (7/14/28 mA) depending on the sensor itself. The sensor types are standard active 2-level wheel speed sensors (7/14 mA).

A simplified block diagram of the interface is shown below. The interface supply is given on the VDD1 pin. The circuitry consists of a power interface that mirrors current flowing in the external sensor and transmits this current information to the decoder, which produces a digital value for each remote sensor channel. Decoded data are then output through the Remote Sensor Data Registers (WSIRSDRx). Received signals can be processed to the corresponding discrete logic output pin DOUT1-DOUT4. The power interface also contains error detection circuitry; when a fault is detected, the error code is stored in a global SPI data buffer in the Remote Sensor Data Registers (WSIRSDRx).

Figure 15. **WSI control blocks**



Remote sensor configuration can be addressed via the Remote Sensor Configuration Registers (WSIRSCRx). The Remote Sensor Control Register (WSICTRL) allows for digital algorithm and DOUTx output buffer of each channel to be switched on and off; sensor supply interface is indeed automatically enabled during power-up sequence of the device.

Each TRKn interface is kept independent from each other with dedicated logic and protected against faults on TRKn pins (short to battery or to ground).

In the VDA sensor communication, data bit D0 in the WSIRSDRx register might be used by the sensor as a fault bit. Therefore, this bit is latched as D0_L in order to detect whether a fault has occurred: the data bits are instead updated every speed pulse so intermittent fault conditions could be lost. This bit is cleared-upon-read.

If the device detects an error on the sensor interface, the FLTBIT in WSIRSDRx will be set to ‘1’ and the following bits will be used to report the detected errors. Otherwise, the register will contain only data information. Detailed information on data and fault reporting are explained in the following sections.

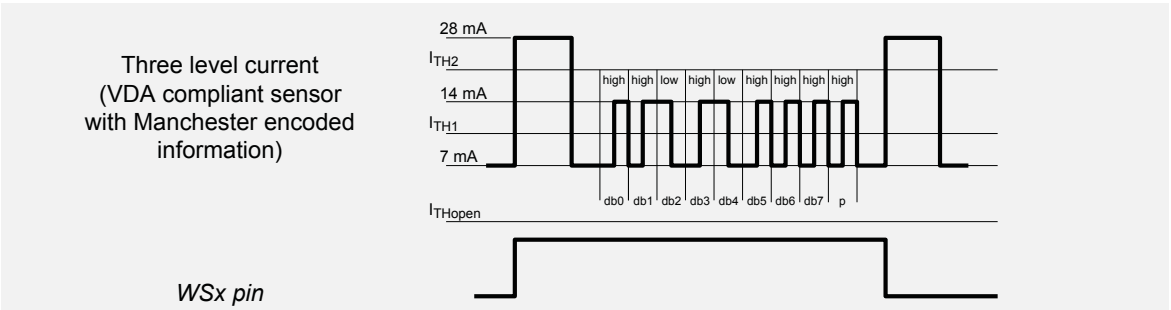
Active wheel speed sensor

The remote sensor interface senses circuit conditions and decodes active wheel speed sensor signals with various pulse widths and output currents. The following sensor types are supported and selected through the Remote Sensor Configuration Register (WSIRSCR).

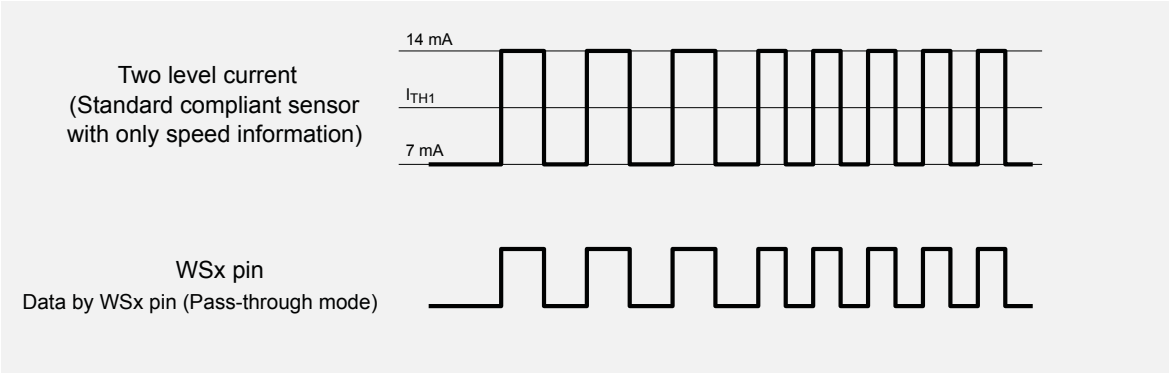
- Standard active 2-level wheel speed sensors (7/14mA similar to ATS682LSHTN)
- Three level (7/14/28 mA similar to KMI22) VDA compliant sensor with direction and air gap information (“Requirement Specification for Standardized Interface for Wheel Speed Sensor with Additional Information”, Version 2.0)
- PWM encoded 2-level sensors with 2 edges per tooth (similar to TLE4942/BOSCH DF11)
- PWM encoded 2-level sensors with 1 edge per tooth (similar to ATS651LSH/BOSCH DF11)

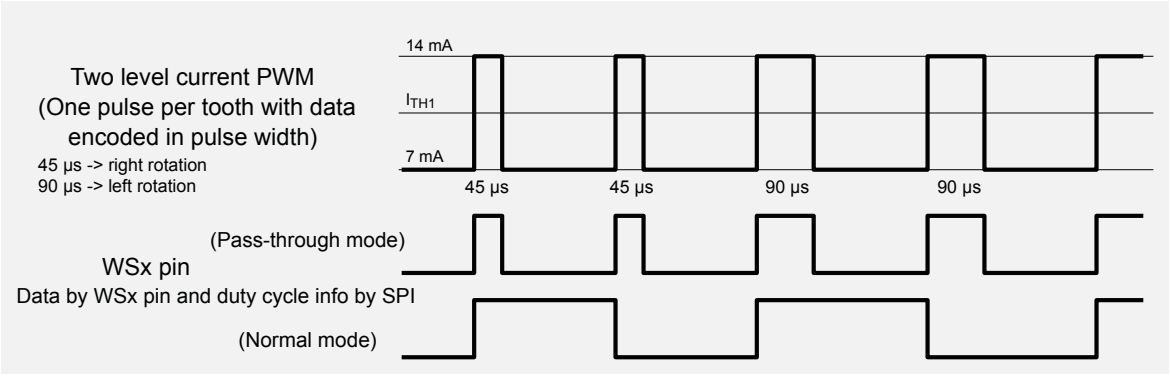
Received wheel speed frames from all the above sensors are decoded into signals suitable for the microcontroller through the four independent DOUTx output pins.

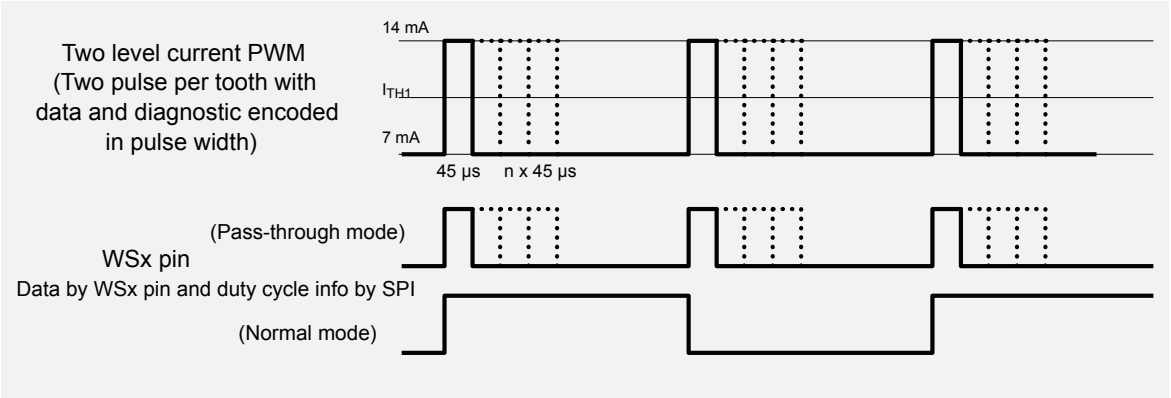
Figure 16. WS compatibility



Data and diagnostic by SPI: Three level sensors have eight data bits and a parity bit which are written into the register upon receiving. At higher speeds not all bits can be transmitted The data register for each wheel contains the number of data bits received between two speed pulses





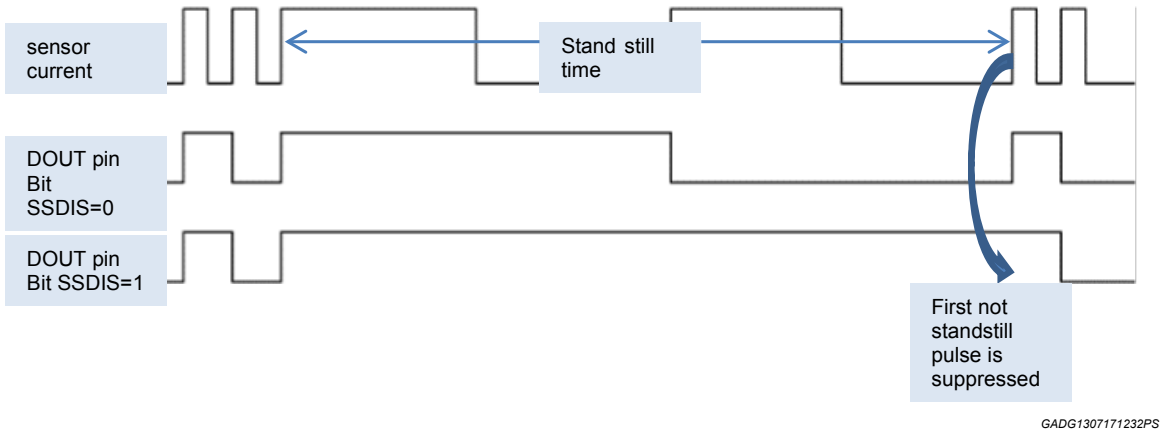


For all sensors, other than the standard active 2-level sensor, additional sensor data (diagnostics, etc.) are decoded and available within the Remote Sensor Data Registers (WSIRSDR0, WSIRSDR1, WSIRSDR2, and WSIRSDR3). Only for 2nd level PWM encoded sensors the user may choose to have all data processed through the microcontroller by selecting pass through mode, WSIPTEN, within the Remote Sensor Configuration Register (WSIRSCR). In pass-through mode, the remote sensor interface simply conditions the incoming sensor current pulses to digital pulses, no decoding is performed. When STD sensor is selected, the IC automatically forces the pass-through mode.

The sensor input filter time, deglitch filter, (delay until a threshold crossing is detected) can be configured in 15 steps. Filters can be selected individually for each channel, through the Remote Sensor Configuration Register, WSFILT bits.

For PWM encoded sensors with two edges per tooth not in pass-through mode, the standstill signal can be processed directly to the DOUTx output pins. This is done in the Remote Sensor Configuration Register, SSDIS bit. Since the decoder has to measure the pulses in order to determine whether they are stand-still pulses or not, the first standstill pulse will always be seen on the DOUTx output pins and the first not stand-still pulse after a stand-still period will be suppressed.

Figure 17. Standstill operation when PWM two edges per tooth is selected



Data from the sensor are not latched: last incoming frame overwrites the previous one once validated. Faults coming from diagnostic (i.e. over current, short to ground or battery) are latched until the microcontroller reads them.

Two different digital algorithms can be selected:

- Auto-adjusting current trip points. With this option, the ASIC is able to find sensor DC current value (named IB0) in the range from 2.5 mA to 21 mA (default is 7 mA). The ASIC is also able to detect the current value of the data pulse and compute the first threshold (named Ith1): Ith1 = IB0 + ΔIth1/2 where ΔIth1 is in the range from 5 mA to 9.3 mA (default is 7 mA).

  Besides, in case of VDA selected, the ASIC is also able to recognize the current value of the speed pulse by computing a second threshold (named Ith2): Ith2 = IB0 + ΔIth1 + ΔIth2/2 where ΔIth2 in the range from 10 mA to 18.6 mA (default is 14 mA).

  ΔIth1 can be read on WSIRSDR[4:7] and can assume values in the range form 54 to 100; ΔIth2 can be read on WSIRSDR[8:11] and can assume values in the range form 108 to 200. When one of delta is saturated it is possible for the user to select whether this information should be flagged in WSIRSDR[0:3]; this can be done through Disable Delta Error bit on WSICTRL register.

- Fixed current trip points where the thresholds are settled by SPI. To avoid the risk of wrong settings (inverted thresholds, thresholds outside WSI limits and similar) only first threshold can be directly specified while, to determine the second one, offset current information must be provided. Both values, threshold and offset, can be specified through 8-bit word (range 0x00 → 0xFF): default values are 10 mA for first threshold and 10 mA for offset (i.e. 20 mA default for second threshold). A fixed offset of 54 is added to SPI value to prevent settings out of range. Complete formulas for threshold computation are the following (ref_cur = I_{TH1}/106):
  - First threshold = [ref_cur] * (54 + WSI_FIRST_TH)

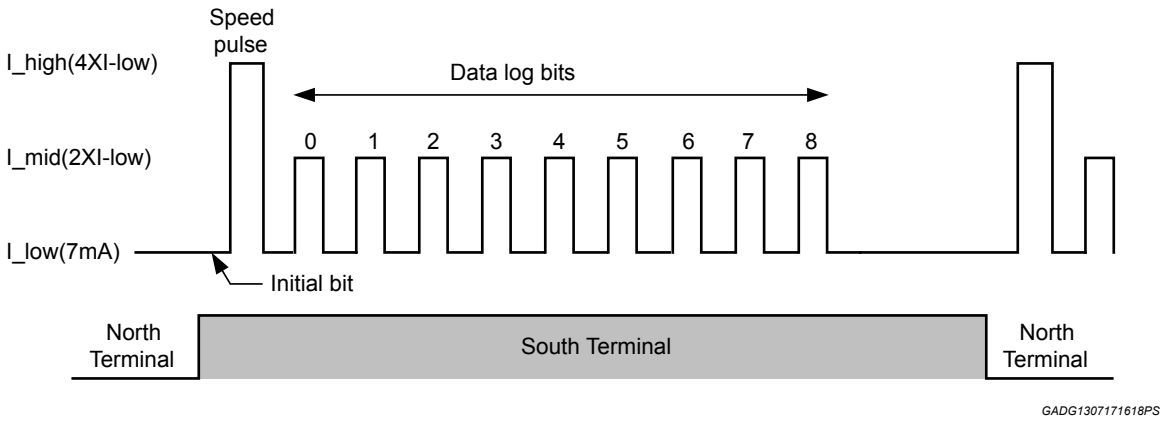
– Second threshold = [ref_cur] * (108 + WSI_FIRST_TH + WSI_OFFS_TH)

VDA sensor decoding

For the three level wheel speed sensor, additional information is Manchester encoded between two consecutive speed pulses.

The device measures each speed pulse duration and its value is used as time base for Manchester decoder which provides decoding for the bit [0:8] shown in the figure below. The number of the data log bit depends on the speed so that the device is able to inform the microcontroller about the number of bit effectively received.

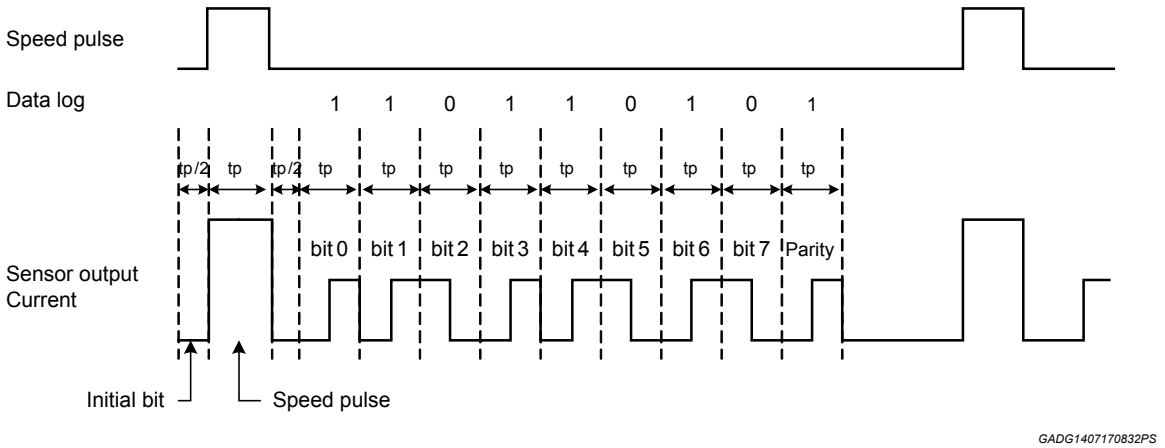
Figure 18. Definition of speed pulse and data log bits



Normal sensor operation

Normal operation frames are composed as shown in the figure below.

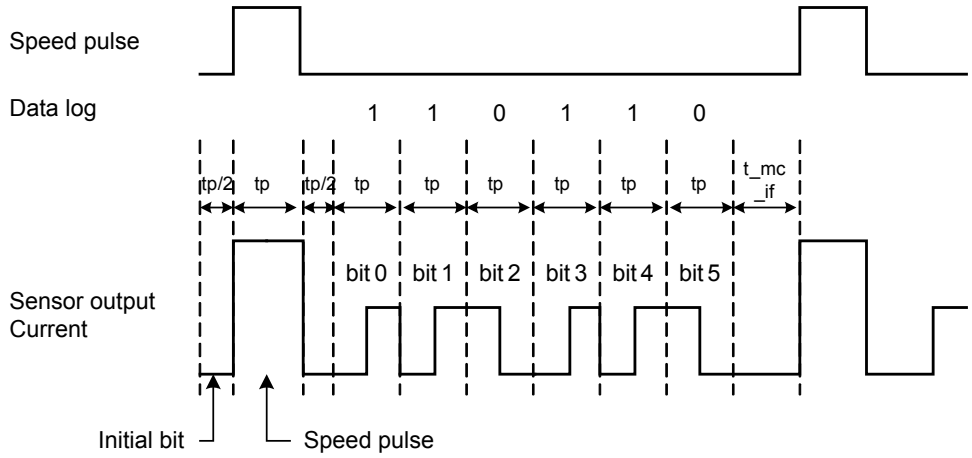
Figure 19. Signal monitoring: normal speed



High-speed operation

The number of datalog bit is reduced at high-speed operations (see next figure). There are four dedicated bit on the SPI WSIRSDRx register which show how many valid bit are coming from the VDA sensor.

Figure 20. **Signal monitoring: high Speed**

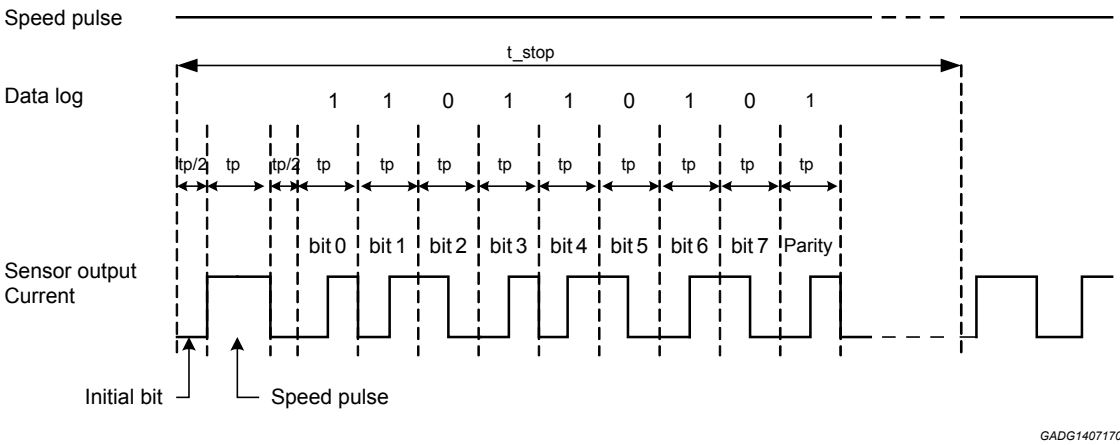


Standstill operation

The ASIC is able to understand whether the VDA sensor is in standstill mode. Stanstill operation frames are composed as shown in the next figure. In this case the speed pulse is not modulated at current level I_high but a level I_mid is used.

The expected number of transmitted datalog bit is equal to 9 but no automatic check is performed.

Figure 21. **Signal monitoring: standstill**



Start & stop condition for data decoding

According to the sensor status, the starting and the end point for decoding the VDA data can slightly vary. The different behaviors are summarized by the table below.

Table 14. **Decoding start/stop behaviour**

Sensor condition	Decoding start	Decoding stop
Normal speed	28 mA pulse with tp	Rising edge of 28 mA pulse or no modulation is performed for 5/4*tp
High speed	28 mA pulse with tp	Rising edge of 28 mA pulse
Stand still	14 mA pulse with tp	No modulation is performed for 5/4*tp

Wheel Speed data register formats

In the wheel speed sensor interface, four data registers are used (Remote Sensor Data Register WSIRSDR0-WSIRSDR3).

Independent data registers are defined for each wheel speed channel and their contents are determined by sensor type. Three level VDA sensors have eight data bit (stored in WSIRSDRx registers) and parity check performed at device level, in case parity check fails an error flag is set in WSIRSDRx register. At fast speed, the sensor may not transmit all bit: the ASIC is able both to process normal or either truncated frames by providing together with data, a 4 bit counter to inform the microcontroller about the number of received valid bit. For PWM encoded sensors, each pulse length is written to the sensor data register with a typical resolution of 5 µs per bit. In case of pulse width duration equal or higher than 1.045 ms and less or equal than 2.55 ms, the standstill condition will be recognized. The register is updated when a PWM falling edge is detected; in case of stuck-at 1 of the PWM signal the register is updated when the counter reaches the overflow value (0x1FF): in this case the standstill bit not set and the counter in overflow will signal a fault to the microcontroller in WSIRSDR register. No data are available for STD sensors.

Sensor data integrity: LCID and CRC

WSIRSDR[3:0] data register contain a Logical Channel ID which is a 2-bit field for remote sensors used to link the received data to the corresponding logical channel number. WSIRSDR[3:0] register contain also a 3 bit CRC field computed on the data packet for data integrity check. To satisfy functional safety requirements LCID, DATA and CRC bit fields propagate through the same data path as a single item to the SPI output. The CRC checksum can also be evaluated using a polynomial approach with the following parameters for the algorithm:

- Polynomial $G_3(x) = x^3+x+1$, whose hexadecimal equivalent code is “0xB”;
- Number of CRC bit: 3;
- Initial seed: all ones;
- Input word length: 17 bit;
- LSB first;
- Additional left shift number: 3.

Test mode

In order to test the connection between IC and microcontroller, the device features a wheel speed test mode that allows test patterns to be applied on the four wheel speed outputs DOUTx. The test mode can be entered via SPI and the test patterns can also be controlled via SPI commands. Test patterns can be composed only of static high or low signals, which can be selected via SPI. For safety reasons only one channel at a time can be switched into test mode.

Remote sensor interface fault protection

Short to GND, current limit

Each output is short circuit protected by an independent current limit and a thermal detection circuit. In case the output current level reaches or exceed the I_{LIMTH} for a time period greater than TILIMTH and meanwhile the remote sensor interface thermal protection is triggered the output stage is disabled. In case the thermal warning level would not be reached, the current limitation circuitry will prevent damages on the channel, still while operating the output. An internal up-down counter will count in 25 µs increment up to T_{ILIMTH}. The filter time is chosen in order to avoid false current limit detection for in-rush current that may happen at interface switch-on. When the output is turned off due to current limit, the appropriate fault code is set in the Remote Sensor Fault Bits (FLTBIT). The fault timer latch is cleared when the satellite channel is switched off then re-enabled through the Remote Sensor Configuration Register (WSIRSCR). This fault condition does not interfere with the normal operation of the IC, nor with the operation of the other channels.

Short to Battery

All outputs are independently protected against a short to battery condition. Short to battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The short-to-battery detection circuit has input offset voltage (10 mV, minimum) to prevent disconnecting of the output under an open circuit condition.

In order to prevent back feeding, a reverse protection diode is integrated. A short to battery is detected when the output TRKn pin voltage increases above the supply pin voltage for a TSTBTH time. An internal up-counter will

count in 1.5 µs increment up to T_{STBTH}. The counter will be cleared if the short condition is not present for at least 1.5 µs. Other channels are not affected in case of short of one output pin. Output in short resumes normal operation once the fault condition is removed. As in the case previously described, the fault code can be read from fault bits.

Leakage to Battery, Open condition

The sensor interface offers also an open condition detection. The auto-adjusting counter for satellite current sensing will drop in case the current flowing through TRKn pin is lower than 1mA. The fault code can be read from fault bits. The channel in this condition is not shutdown.

Leakage to Ground

The sensor interface offers as well the detection of a leakage to ground condition that will possibly raise the sensor current higher than operating range, but still lower than the overcurrent detection threshold. The CURRENT_HI fault flag is asserted when the fault condition lasts for longer than deglitch filter time. This fault flag can be read from WSIRSDRx registers. The channel in this condition is not shutdown. Two leakage to ground thresholds are implemented depending on the configured sensor: for standard 2 levels sensors, an instantaneous threshold is set, while for other sensors a lowest threshold on evaluated base current can be used. Selection of the proper threshold is automatically done configuring the sensor via SPI registers.

Thermal shutdown

Each output is protected by an over-temperature detection circuit: in case the remote sensor interface thermal protection is triggered, only the output stage that provides a current limitation flag is disabled and a corresponding thermal fault is latched (WSITEMP) and reported in the Remote Sensor Data Register (WSIRSDRx). The thermal fault flag is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Configuration Register (WSIRSCRx). The digital channel stays off until the register fault is set while the wheel speed supply automatically recovers as soon as the fault condition disappears.

8.5.3 WSI electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 15. WSI electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Configuration Input							
VIL	Logic Input Low Voltage		-		0.75	V	TRK_SEL
VIH	Logic Input High Voltage		1.75		-	V	TRK_SEL
$V_{hysteresis}$	Input hysteresis Voltage		0.1		1	V	TRK_SEL
TRK_SELPD	TRK_SEL pull down	TRK_SEL = 5 V	10	50	100	µA	TRK_SEL
Tracking Regulator Configuration							
I_{TRKn}	Output load current	Application note	10		100	mA	TRKn
C_{TRKn}	Output capacitor	Application note	-25%	2.2	+25%	µF	TRKn
C_{TRKn} ESR	Output capacitor ESR	Application note f ≤ 150 kHz	0.01		1	Ω	TRKn
C_{TRKn} EXT	External sensor capacitor	Application note max drivable cap in parallel with CTRKn			150	µF	TRKn
TRK_SEL vol	TRK_SEL range	Application note	3		5	V	TRK_SEL
TRKn_Vout	Regulated output voltage	3.3 V ≤ TRK_SEL ≤ 5 V VDD1 ≥ 6 V, 10 mA ≤ ITRKn ≤ 100 mA	TRK_SEL – 20 mV	TRK_SEL	TRK_SEL + 20 mV	V	TRKn
TRKn_error	Matching error	TRK_SEL – TRKn VDD1 ≥ 6 V, 10 mA ≤ ITRKn ≤ 100 mA	-20 m		+20 m	V	TRKn
TRKn_line	Line regulation	VDD1 6 V to 19 V, I_{TRKn} = 10 mA, 100 mA	-10		+10	mV	TRKn
TRKn_load	Load regulation	I_{TRKn} = 10 mA to 100 mA, VBATP 6 V, 19 V	-10		+10	mV	TRKn

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
TRKn_Vout_tr1	Transient output voltage 1	VBATP = 13 V I_{TRKn} = 10 mA to 100 mA dI/dt = 100 mA/µs CTRKn = 2.2 µF Guaranteed by design	-5		+5	%	TRKn
TRKn_Vout_tr2	Transient output voltage 2	VDD1 ≥ 6 V dVDD1/dt = 3 V/µS I_{TRKn} = 10 mA, 100 mA CTRKn = 2.2 µF Guaranteed by design	-5		+5	%	TRKn
TRKn_RdsON	RdsON	T_j =150 °C			8	Ω	TRKn
TRKn_RdsON	RdsON	T_j =175 °C Guaranteed by design			9	Ω	TRKn
TRKn_PSSR	PSSR	VDD1 = 6.5 V, I_{TRKn} = 100 mA, Vnoise = 1 Vpp, fnoise = 465 kHz, C_{VDD2} = 2.2 µF Guaranteed by design	20			dB	TRKn
TRKn_cur lim	Current limitation	TRKn = -2 V	150		350	mA	TRKn
TRKn_rev cur	Reverse current in off condition	TRKn = VBATP + 2 V TRKn disabled	0.2		2	mA	TRKn
TRKn_rev cur	Reverse current in on condition	TRKn = VBATP + 2 V TRKn enabled	0.2		2	mA	TRKn
TRKn_ovs_a	Overshoot at power on	ITRKn = 10 mA CTRKn = 2.2 µF			5.5	V	TRKn
TRKn_ovs_b	Overshoot at VBATP step	VBATP step from 5.5 V to 13 V during 10 µs, considering ITRKn = 100 mA CTRKn = 2.2 µF Guaranteed by design			5.7	V	TRKn
TRKn_off	Off state voltage				1	V	TRKn
Diagnostic							
TRKn_rev_cur_det	Reverse current detection voltage		VDD1		VDD1+0.2	V	TRKn
T_SD_TRK	Temperature shut down		175		185	°C	TRKn
T_SD_hy	Temperature shut down hysteresis		5		10	°C	TRKn
T_SD_deglitch	Digital deglitch filter time	Guaranteed by scan	7.5	10	12.5	µs	TRKn
Wheel Speed Sensor Configuration							
C_{TRK}	TRK load capacitance	Application note	6			nF	TRKn
$V_{TRKnmax}$	Max. output voltage				VDD1	V	TRKn
TRKn_RdsON	RdsON	Tj=150 °C Up to ILIMTH			8	Ω	VDD2
R_{TRKn}	Output resistance	Tj=175 °C Up to ILIMTH, Guaranteed by design			9	Ω	TRKn
I_{BO}	Base Current	Auto-adjusting option (default value)	+9%	-7	-9%	mA	TRKn
I_{TH1}	7-14 mA detection		-9%	-9.8	+9%	mA	TRKn
I_{TH2}	14-28 mA detection		-9%	-19.6	+9%	mA	TRKn
I_{LIMTH}	Output Current Limit	VTRKn=GND	-80		-40	mA	TRKn
I_{STBTH}	Static reverse current into TRKn	VTRKn > VDD1 + VTRKnSTB	0.0		10	mA	TRKn
Diagnostic							
I_{LKGB}	Open sensor detection	VTRKn=OPEN	-4		-1	mA	TRKn

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
t_{FLT_OPEN}	Open detection filter time	Guaranteed by scan	10		20	µs	TRKn
I_{LKGG}	Leakage to GND threshold	Guaranteed by scan	+9%	-15.3	-9%	mA	TRKn
I_{LKGG}	Leakage to GND threshold	2 level std sensor only	+9%	-23	-9%	mA	TRKn
t_{FLT_LKG}	Leakage deglitch filter time	Guaranteed by scan	88	104	120	µs	TRKn
T_{MSK_ILIMTH}	Current limit blanking time at power-on	Guaranteed by scan	250	300	350	µs	TRKn
$t_{ILIMITH}$	Current limit filter time	Guaranteed by scan	500		600	µs	TRKn
$V_{TRKnSTB}$	Output Short to Battery Threshold		VDD1		VDD1+0.2	V	TRKn
t_{STBTH}	Short to battery deglitch time	Guaranteed by scan	10		20	µs	TRKn
T_SD_TRK	Temperature shut down		175		185	°C	TRKn
T_SD_hy	Temperature shut down hysteresis		5		10	°C	TRKn
T_SD_deglitch	Digital deglitch filter time	Guaranteed by scan	7.5	10	12.5	µs	TRKn
Digital Output							
VOL	Logic Output Low Voltage	Isource = 1 mA			0.4	V	DOUTx
VOH	Logic Output High Voltage	Isink = 1 mA	VDDIO-0.4			V	DOUTx
t_{rise}	Rise time	From 20% to 80% output voltage, LOAD=20pF	0.05		2	µs	DOUTx
t_{fall}	Fall time	From 80% to 20% output voltage, LOAD=20pF	0.05		2	µs	DOUTx
I_{leak}	Tristate leakage current	TRK_SEL=VDD4 0<DOUTx<VDDIO	-0.5		0.5	µA	DOUTx
$t_{deglitch}$	DOUT deglitch filter time	Configurable by SPI (4bits) Guaranteed by scan	7.5		15.6	µs	DOUTx
$t_{latency}$	Latency time between receiving sensor data @TRKn pin and reaching VOH on WSx pin	Trigger point 80% of TRKn modulated current) Guaranteed by scan	0.5		5	µs	DOUTx
t_{jitter}	Jitter on Latency time	Design info, not tested	0.1		125	ns	DOUTx

8.5.4 WSI error handling

Table 16. WSI type of error

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
Tracking Configuration				
TRK out of regulation	ON state	Set **TRK_OUT_OF_REGULATION** SPI flag (3:0) in **TRK-CAN FAULT** register	On read	N.A.

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
TRK reverse current	ON state	TRK internal path to VDD1 open, **TRK_REVERSE_CURRENT** SPI flag (10:7) latched in **TRK-CAN FAULT** register	On read	Automatic restart when fault disappears.
TRK overtemperature	ON state	No action if out of regulation is not triggered; output disabled, and **T_SD_TRK** SPI fault bit (5) latched otherwise in **TRK-CAN FAULT** register	On read	Automatic restart with slope control after OT fault disappears.
Wheel Speed Sensor Configuration				
Short to ground, current limitation	ON state	**STG** SPI fault (9) latched in **WSIRSDRx** register.	On read	N.A.
Short to battery	ON state	**STB** SPI fault (8) latched in **WSIRSDRx** register. Sensor supply disconnected to avoid reverse current flow	On read	Automatic restart after fault disappears.
Leakage to battery	ON state channel enabled	**OPENDET** SPI fault (6) latched in **WSIRSDRx** register	On read	N.A.
Leakage to GND	ON state channel enabled	**CURRENT HI** SPI fault (7) latched in **WSIRSDRx** register	On read	N.A.
Parity error, invalid data	ON state channel enabled, VDA sensor only	**INVALID** SPI fault (4) latched in **WSIRSDRx** register	On read	N.A.
No decoding data	ON state channel enabled, VDA sensor only	**NODATA SPI fault (3) latched** in **WSIRSDRx** register	On read	N.A.
Pulse duration counter overflow	ON state channel enabled, PWM sensor only	**PULSE OVERFLOW SPI fault (2) latched** in **WSIRSDRx** register	On read	N.A.
OT	ON state	**WSITEMP** fault (5) latched in **WSIRSDRx** register and output disabled if STG fault is triggered; no action otherwise	On read	Wheel Speed supply automatic restart after fault disappears. Clear **STG** and **WSITEMP** faults and re-enable the faulted channel to enable algorithm and digital outputs.

9 Reset

9.1 Resets outputs

9.1.1 Reset outputs functional description

The device provides two different reset signals RES1 and RES2: RES1 is the logic OR of VDD3 undervoltage/ overvoltage, VDD4 undervoltage/overvoltage and watchdog fault (details on watch dog reset conditioning is reported in the watchdog section).

RES2 is triggered only by an undervoltage or overvoltage on VDD3.

Both RES1 and RES2 are open drain circuits. RES1 is bidirectional. When the RES1 is driven low (by internal or external command) automatically all the drivers are disabled. An echo of reset signal driven low from external condition is detected and latched into Service Fault SPI register to let the microcontroller understand the fault generation mechanism after the reset signal disappears. Both the reset signals are active low.

Figure 22. Reset generation

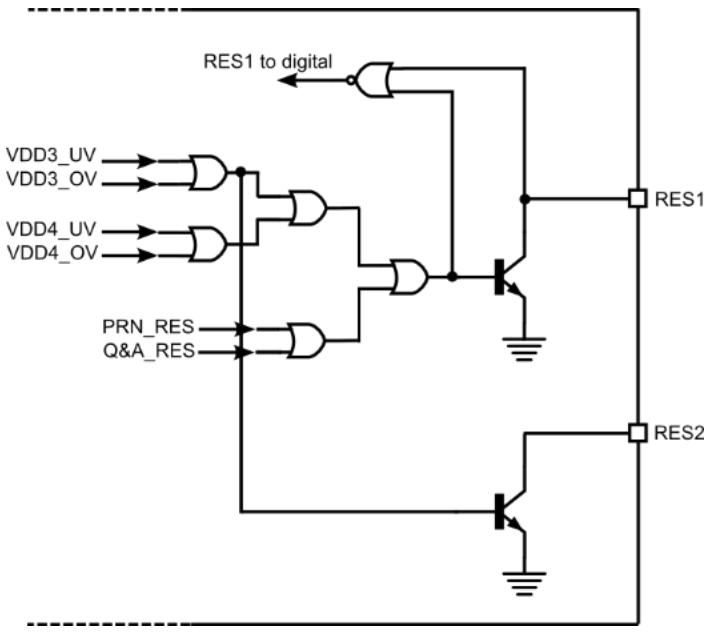


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Figure 23. **Reset power up/down**

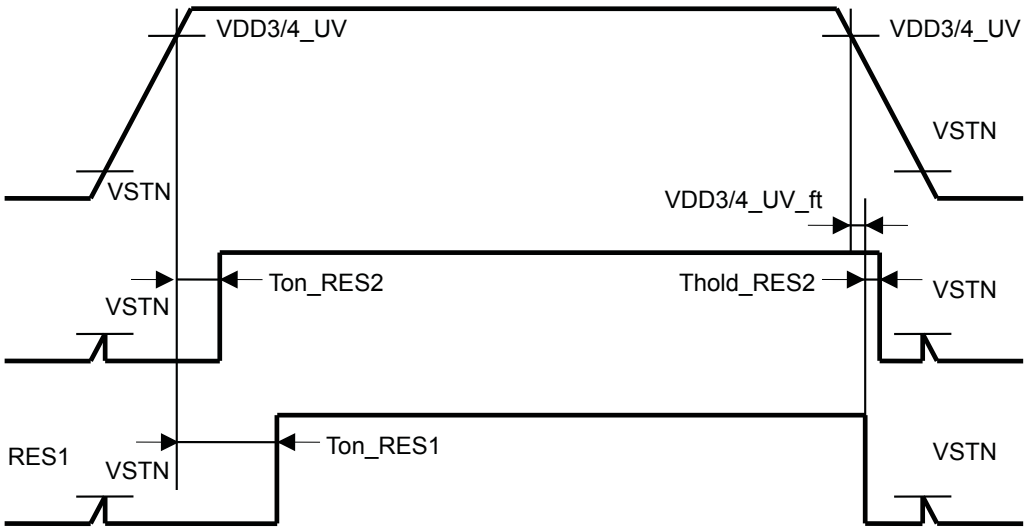


Figure 24. **VDD3 reset conditioning**

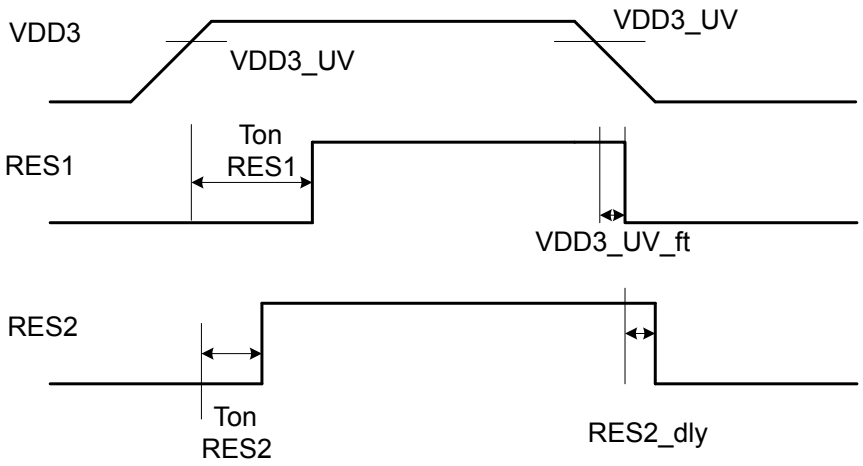
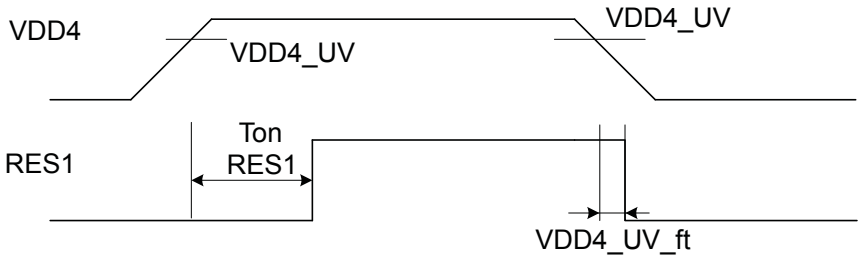


Figure 25. **VDD4 reset conditioning**



9.1.2 Reset outputs electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 3.1 V ≤ VDDIO ≤ 5.2 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin.

Table 17. Reset outputs electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RES1 Input							
RES1_L_IN	RES1 low input voltage				0.75	V	RES1
RES1_H_IN	RES1 high input voltage		1.75			V	RES1
RES1_IN_tdeglitch	RES1 to digital, digital deglitch filter	Guaranteed by scan	4.75	5	6.25	µs	RES1
RES1 Output							
VSTN	RES1 activation voltage (minimum VDDIO voltage to activate reset output)	Guaranteed by design			1	V	
RES1_L	RES1 low level	VDDIO ≥ 1 V ext 1 kΩ pull up to VDDIO			0.4	V	RES1
IRES1_L	RES1 current capability	VDDIO = 4.5 V, RES1 in reset condition VRES1 = 0.4 V	5		30	mA	RES1
RES1_H	RES1 high level	No reset condition 1 kΩ pull up to VDDIO	VDDIO -50 mV		VDDIO	V	RES1
Ileak_RES1	Leakage current in off condition	RES1 = 5 V			10	µA	RES1
Vclamp	RES1 clamp voltage	Isource = 10 mA	5.5		7	V	RES1
RES1_RT	RES1 rise time	Cload = 100 pF, Rpull up = 1 kΩ	0.1		1.5	µs	RES1
RES1_FT	RES1 fall time	Cload 100 pF, Rpull up = 1 kΩ	0.1		0.8	µs	RES1
RES2 Output							
VSTN	RES2 activation voltage (minimum VDDIO voltage to activate reset output)	Guaranteed by design			1	V	
RES2_L	RES2 low level	VDDIO ≥ 1 V ext 1 kΩ pull up to VDDIO			0.4	V	RES2
IRES2_L	RES2 current capability	VDDIO = 4.5 V, RES2 in reset condition VRES2 = 0.4 V	5		30	mA	RES2
RES2_H	RES2 high level	No reset condition 1 kΩ pull up to VDDIO	VDDIO -50 mV		VDDIO	V	RES2
Ileak_RES2	Leakage current in off condition	/RES2 = 5 V	-	-	10	µA	RES2
Vclamp	RES2 clamp voltage	Isource = 10 mA	5.5		7	V	RES2
RES2_RT	RES2 rise time	Cload 100pF, Rpull up = 1 kΩ	0.1		0.8	µs	RES2
RES2_FT	RES2 fall time	Cload 100pF, Rpull up = 1 kΩ	0.1		0.8	µs	RES2
RES Timings							
Ton_RES1	Reset filter	Guaranteed by scan	10	12	14	ms	RES1
Ton_RES2	Reset filter	Guaranteed by scan	1.2	1.6	2	ms	RES2
RES2_dly	Reset 2 delay	Guaranteed by scan	2	3	4	µs	RES2

9.1.3 Reset outputs error handling

Table 18. Reset outputs type of error

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
RES1 output low	ON state	SPI register reset, as described in **SPI register map**	N.D.	Automatic after fault disappears, SPI configuration to be reinitialized
RES1 input low	ON state	SPI register reset, as described in **SPI register map**, set **RES1 to digital** SPI bit (16) in **SERVFLT** register	On read	Automatic after fault disappears, SPI configuration to be reinitialized
RES2 output low	ON state	No action	N.D.	N.A.

9.2 Ground Loss

9.2.1 Ground Loss Functional Description

The device provides the ground loss detection for GND and GND_A ground pins.

At device start-up, once internal logic is out of PORn state, two dedicated comparators monitor the voltage of each ground pin using the other ground pin as 0V reference. If the voltage of at least one of the two ground pins is higher than Ground Loss threshold for a time longer than Ground Loss filter time then Ground Loss fault is detected.

In case of Ground Loss detection the logic takes the following actions:

- Bit19 (Ground Loss) in Service Fault register is set “high”
- All the device outputs (see Functional Table) are turned off

The device is forced in this condition until the ground loss fault is present. If the fault is removed and both the voltages on GND and GND_A pins become lower than Ground Loss threshold then all the outputs are automatically restarted by the logic.

9.2.2 Ground Loss electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ T_j ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin.

Table 19. Ground Loss electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
GND Monitors							
GND_loss_th	Ground Loss threshold		100	200	350	mV	GND
GND_A_loss_th	Digital Ground Loss threshold		100	200	350	mV	GND_A
GND_loss_filt	Ground Loss filter time		8	16	24	µs	GND, GND_A

9.2.3 Ground Loss error handling

Table 20. Ground Loss type of error

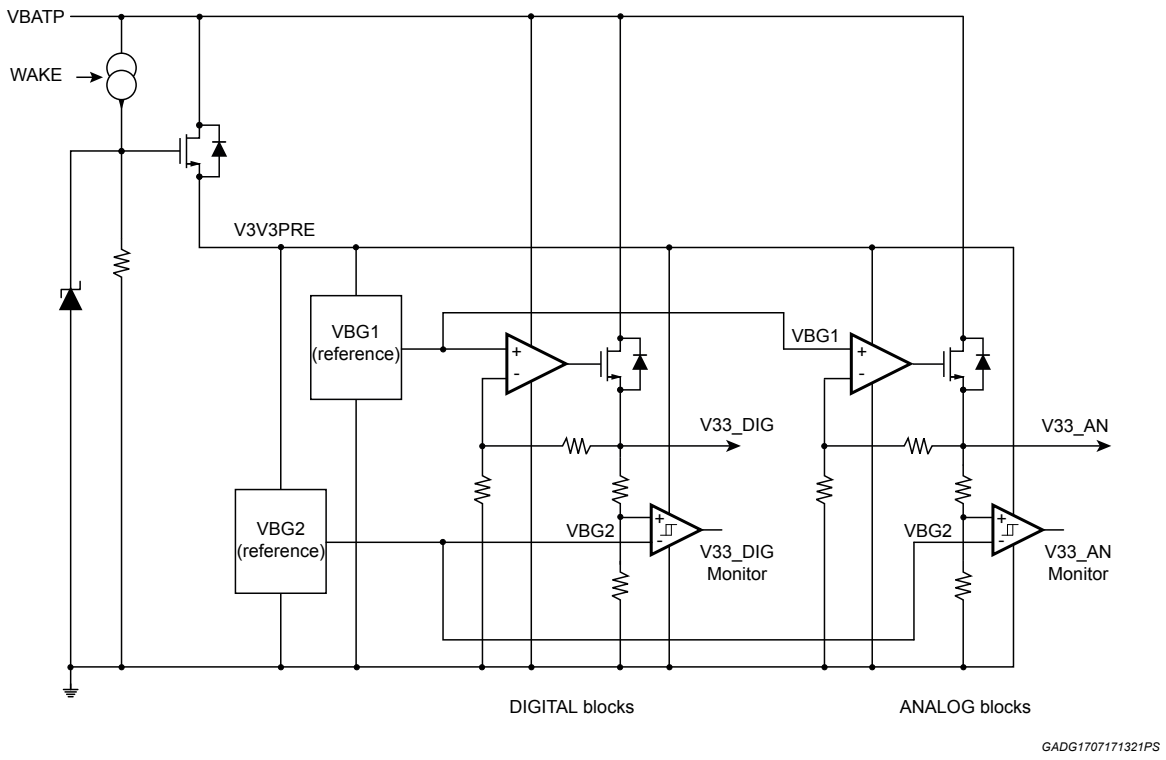
Type of error	Detection condition	Action	Clear SPI flag	Restart condition
GND_loss	ON state	Outputs OFF as in Functional Table, set **Ground Loss** bit (19) in SPI **SERVFLT** register	On read	Automatic after fault disappears
GND_A_loss	ON state	Outputs OFF as in Functional Table, set **Ground Loss** bit (19) in SPI **SERVFLT** register	On read	Automatic after fault disappears

9.3 Internal Supply

9.3.1 Internal supply functional description

The internal supply partitioning consists of two different supply domains: one includes the digital core and the other is used for the analog functions. Both the supply domains are achieved directly from protected battery line and are monitored using independent references to always ensure proper functionality of the device. In case a fault happens on either the analog or digital supply a power on reset (PORn) is generated both forcing the device in reset state with all the outputs disabled and causing RES1, RES2 assertion.

Figure 26. Internal supply concept



9.3.2 Internal supply electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages referred to GND pin.

Table 21. Internal supply electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Internal Supply						
VBG1	Internal band-gap reference	Design info, not tested		1.214		V
VBG2	Internal band-gap reference for monitor circuits	Design info, not tested		1.214		V
V33_AN	Internal 3v3 reference for analog	Design info, not tested	3	3.3	3.6	V
V33_DIG	Internal 3v3 reference for digital	Design info, not tested	3	3.3	3.6	V
Diagnostic						
V33_AN_uv	V33_AN Power On Reset threshold		2.6		3	V
V33_DIG_uv	V33_DIG Power On Reset threshold	Guaranteed by design	1.5		2.6	V
PORn_flt	Power On Reset analog deglitch		2		15	µs

9.3.3 Internal supply error handling

Table 22. **Internal supply error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
V33_AN_uv	ON state	All Outputs OFF, SPI registers reset as described in **SPI register map**	N.D.	Automatic with retrigger of power-up sequence after fault disappears
V33_DIG_uv	ON state	All Outputs OFF, SPI registers reset as described in **SPI register map**	N.D.	Automatic with retrigger of power-up sequence after fault disappears

9.4 Reference oscillator

9.4.1 Reference voltage functional description

The device uses an internal 16 MHz oscillator, trimmed for 7% accuracy, as system clock for digital circuits and as time base for digital timings and filters. Since a loss of the reference frequency would cause a stuck in the logic core, this oscillator is duplicated and redundancy is used to guarantee the correct functionality.

To reduce emissions of the main logic core and of the switching circuits in general, spread spectrum is operating on the main oscillator. A Synchronous Digital Modulator generates 64 total steps to the spread spectrum input. Half of them modulate the oscillator with a frequency higher than 16 MHz, half of them modulate the oscillator with a frequency lower than 16 MHz. The frequency deviation is about: ±32 (steps) x 0.1% (spread spectrum resolution) = ±3%.The 64 different levels at 16 MHz average rate result in a modulation frequency of 16 MHz / 128 = 125 KHz. The central 16 MHz frequency is varied by a triangular modulation at 125 kHz with 3% of modulation index. Spread spectrum is always active and can be disabled setting the proper bit in the SERVICE ENABLE register.

9.4.2 Reference oscillator electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 23. **Reference oscillator electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Internal Oscillator						
fOSCINT	Internal Oscillator main frequency		-7%	16	+7%	MHz
fOSCINT_mod_freq	Spread spectrum modulation frequency	Guaranteed by scan		125		kHz
fOSCINT_mod_id_min	Spread spectrum minimum modulation index		-5	-3		%
fOSCINT_mod_id_max	Spread spectrum miaximum modulation index			3	5	%

9.5 Thermal monitor

9.5.1 Thermal monitor functional description

To guarantee current control accuracy and real time calibration, the temperature of the die is continuously monitored through a sigma-delta temperature sensor; temperature information is coded in digital domain in a 8bit word stored into a dedicated SPI register. If the die overheats above T_SD_int threshold, solenoid driver and regulators are disabled until die temperature decreases below turn-off threshold. Die temperature can be calculated with the following formula:

$$T = \left(\frac{SPICODE}{255} \times 305\right) - 85\ [°C]$$

9.5.2 Thermal monitor electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 24. **Thermal monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Thermal Monitor						
T_INT_acc	Thermal sensor accuracy	Guaranteed by design	-10		10	°C
T_SD_INT	Thermal shutdown threshold		175		185	°C
T_SD_flt	Thermal shutdown filter time	Guaranteed by scan	7.5	10	12.5	µs

9.5.3 Thermal monitor error handling

Table 25. **Thermal monitor error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
CORE OT	ON state	All ASIC functions except Charge Pump disabled, **T_SD_int** fault bit (8) set in SPI **Temperature sensor** register	On read	Automatic with retrigger of power-up sequence after fault disappears

9.6 Battery monitor

9.6.1 Battery monitor functional description

The device includes a voltage monitor that detects the under voltage and over voltage condition on VBATP pin. In case of under voltage (VB_UV1) or over voltage (VB_OV) the device reacts as indicated in the Functional table chapter and in case of over voltage the proper diagnostic bit is set and latched in the SPI register.

9.6.2 Battery monitor electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 26. **Battery monitor electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Battery Monitor							
VBATP_UV	VBATP under voltage		3		3.8	V	VBATP
VBATP_UV_HYS	VBATP under voltage hysteresis			200		mV	VBATP
VBATP_UV_FLT	VBATP under voltage filter time	Guaranteed by scan	7.5	10	12.5	µs	VBATP
VBATP_OV	VBATP over voltage		27		31	V	VBATP
VBATP_OV_HYS	VBATP over voltage hysteresis			2		V	VBATP
VBATP_OV_FLT	VBATP over voltage filter time	Guaranteed by scan	75	100	125	µs	VBATP

9.6.3 Battery monitor error handling

Table 27. **Battery monitor error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VBATP_uv	ON state	Outputs OFF as in Functional Table, set **VBATP UNDER VOLTAGE** bit (2) in SPI **SERVFLT**. register, reset according to **SPI map table**	On read	Power up sequence retriggered after fault disappears, configuration to be renewed

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VBATP_ov	ON state	Solenoid drivers and pre-drivers disabled, LS clamp of solenoid outputs disabled; set **VBATP OVER VOLTAGE** bit (1) in SPI **SERVFLT** register	On read	After fault disappear, set **ENCHx, Fail Safe Pre-Driver Enable**, **Pump Pre-Driver Enable**in **SERVENA** register, **DRVENAx** bit in **SolEnDRV**register,

10 Valve drivers

10.1 Solenoid driver

10.1.1 Solenoid driver functional description

The device provides 6 current control channels. Each channel includes the driving transistor, the recirculation transistor and the current sensing structure and can work in low–side driving mode with high–side recirculation or in high–side driving mode with low–side recirculation, as reported in Figure 27.

The LS or HS mode is configured through an SPI bit.

If HS_config_x = 0 (default) low–side mode is enabled (the load is connected to VS), if HS_config_x = 1, high–side mode is activated (the load is connected to ground).

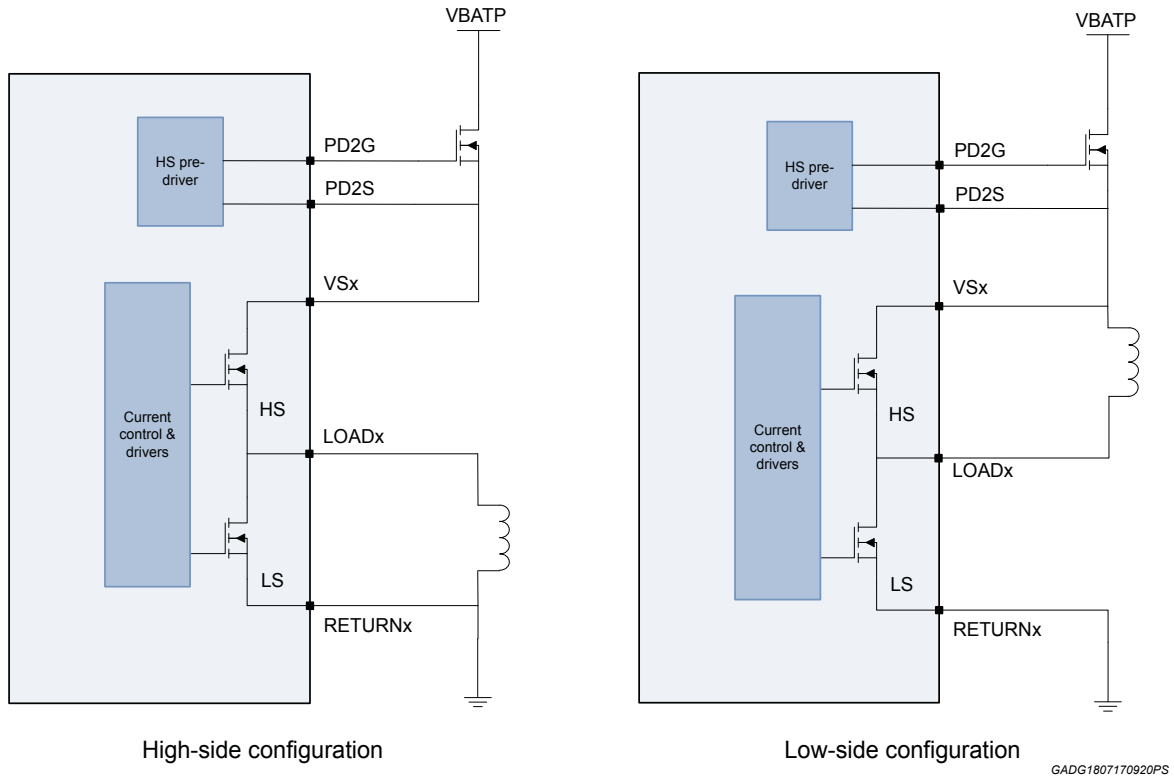
Channels can be configured independently as high–side or low–side, however channel configuration is managed by channel pairs and on a single pair not all the configurations are possible: in case HS/LS configuration is needed the first channel must be LS and the second channel HS.

Table 28. First and second channel configurations

First channel configuration	Second channel configuration	
HS	HS	Allowed
LS	HS	Allowed
HS	LS	Forbidden
LS	LS	Allowed

The microcontroller can inhibit solenoid activation by means of the EN_DR input pin: if this pin is kept low the solenoid are kept in disable condition; to avoid spurious event on EN_DR input pin, a de-glitch filter is present.

Figure 27. **High–side and low–side configuration**



If CONFIG pin is set to high, solenoid activation depends also on the Q&A WD status as described in section Section 14.1.2 Watchdog states evolution

The solenoid drivers can work in two different configurations selectable by SW_cntr_x bit (default =0): hardware mode when the current flowing in the load is controlled by internal control loop or software mode where the loop is closed by external microcontroller and the driver is actuated through INx pins.

The following parameters can be configured only when the solenoid driver is not active:

- HS-LS configuration
- Software/Hardware Current Control Feedback
- Operating Current Range
- Overcurrent Threshold

The following parameters can be modified during channel operation:

- Current Set Point (HW mode only)
- Switching Period (HW mode only)
- Dither (HW mode only)
- Control Loop parameters (HW mode only)
- Full on mode (HW mode only)
- Slew Rate Control

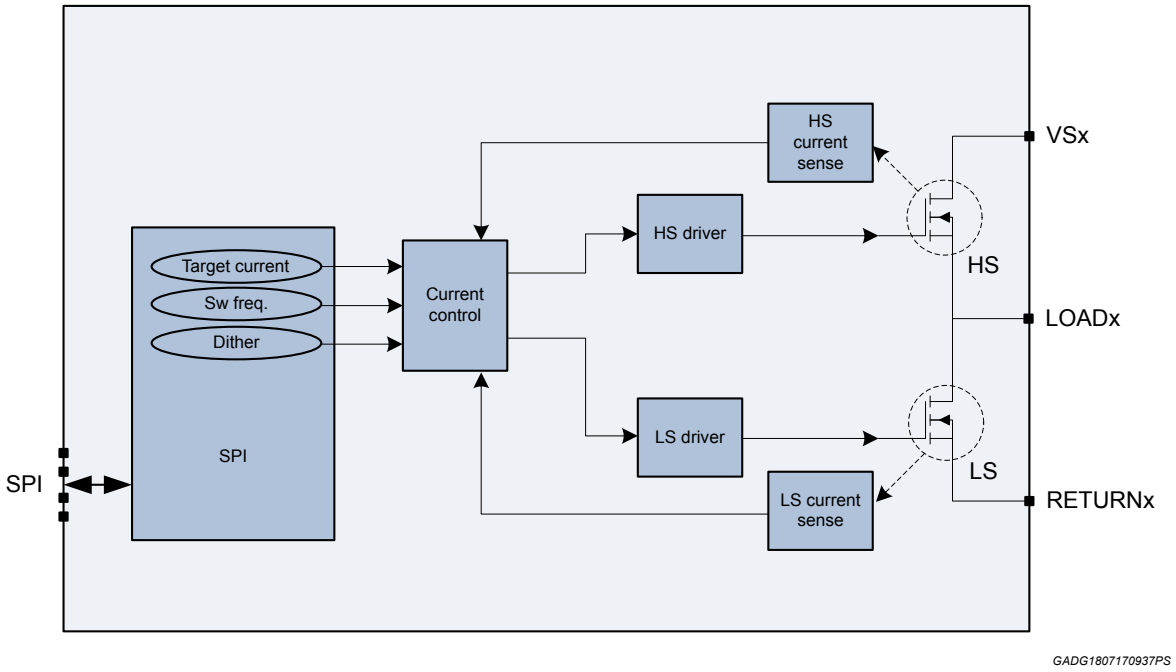
10.1.1.1 *Hardware current control*

In this case, SW_cntr_x = 0, the device needs to receive the target of the load current from the microcontroller through SPI together with the target switching frequency. Once the channel is enabled the device starts to drive in PWM mode the drivers (HS & LS) adjusting consequently the duty cycle to reach the target load current.

The switching frequency and the regulated current can be programmed separately for each channel.

The device offers the possibility to synchronize the turning on of all the channels by writing to 1 all the corresponding bits in the enable register.

Figure 28. **Hardware control configuration**



Current Set Point

The load current set point can be programmed independently for each driver using the dedicated SETPOINT_x 11bit register. Formula used to evaluate set point varies depending on HILOAD bit setting in CONFIGURATION register and it is summarized in the table below.

Table 29. **Setpoint configuration**

SETPOINT	Load target current HILOAD = 0 [bit resolution = 1500/2047 = 0.733 mA]	Load target current HILOAD = 1 [bit resolution = 2000/2047 = 0.9770 mA]
0	0 [mA]	0 [mA]
1	1 * 0,733 [mA]	1 * 0,977 [mA]
2	2 * 0,733 [mA]	2 * 0,977 [mA]
…	…	…
2046	2046 * 0,733 [mA]	2046 * 0,977 [mA]
2047	1500 [mA]	2000 [mA]

Note: All the values written inside the SETPOINT_x 11-bit register are considered current set point to be reached by the algorithm. For this reason, if a 0x0 value is programmed, it is not guaranteed that the driver will be completely switched off and a current equal to 0mA + Ireg_acc_L is allowed to flow on the connected load.

Switching Period Programming

HW current control feedback can work both at variable or fixed frequency, the operating mode can be selected through a dedicated configuration bit in the CTRLCFG register; in case variable frequency is chosen the digital control loop may vary the PWM period during transients in order to improve the settling time; in such a configuration the programmed PWM period becomes a target for the inner period control loop. In HW mode the PWM switching period of each solenoid driver can be programmed through a dedicated 11bit SPI register (CTRLCFG), the period can be programmed to:

- (N*64+1)*Tref_PWM where Tref_PWM = 125 ns in fixed frequency mode and N is the programmed value in the register
- (N*64+2)*Tref_PWM where Tref_PWM = 125 ns in variable frequency mode and N is the programmed value in the register; the switching period control loop reaches stable point of operation when the effective frequency is between the SPI register target value and (N*64+2 + (1/Kfi – 1))*Tref_PWM with an average value over time equal to (N*64+2+(1/Kfi – 1)/2)*Tref_PWM) so it is affected by PI period control loop settings.

In both HW modes (fixed and variable frequency) the minimum operating period is clamped by setting N = 12 for N ≤ 12 values.

Table 30. Fixed and variable period programming

PWM_CTRLCFG	Period when in Fixed Frequency	Period when in variable Frequency
0	769*125n [s]	770*125n [s]
1	769*125n [s]	770*125n [s]
2	769*125n [s]	770*125n [s]
…	…	…
12	769*125n [s]	770*125n [s]
13	833*125n [s]	834*125n [s]
…	…	…
2046	130945*125n [s]	130946*125n [s]
2047	131009*125n [s]	131010*125n [s]

The resulting PWM period of solenoid drivers is internally checked and feedback in the PWMSENSE SPI register: the period is checked against reference Tmin and Tmax values, outside these limits a flag TMOUT is set in the SPI register PWMSENSE to inform that the control loop is working at unusual value.

The Tmin is fixed at 800*Tref_PWM while the Tmax value is set at 133334*Tref_PWM. Tmax limit only applies for variable frequency mode. Both in variable and fixed frequency mode, in case no PWM signal is generated after Tmax value, the period meter is reset at 196609*Tref_PWM and the average current is calculated.

Dither Programming

On the target current a dither modulation can be superimposed (this functionality can be disabled).

Dither modulation can be configured through SPI registers setting the number of steps to be implemented, their amplitude and their duration Tstep: once the previous parameters are defined the achieved dither waveform is similar to the one shown in the next figure.

Dither step duration can be computed using the formula:

$Tstep= (1+ (M+1)*2^N)*tref\_dth$

where tref_dth=128*125ns;

the mantissa value (M) can be programmed through 5 bit , from 0 to 31, of dedicated register DITHPGM, while the exponent value (N) value can vary from 0 to 7 (3 bit programming) in the same register.

Amplitude of the single step can be calculated multiplying the value set by Dither current step amplitude bits in the DITHPGM SPI register times the dither resolution Dth_res (equal to 1LSB of current set-point resolution); total dither step number in a period is four times the value written in the Dither current step bits of DITHPGM register.

Total amplitude of the dither waveform is clamped between -1024 and 1023 LSB.

One particular condition is implemented in case number of dither step is set to 0: a single positive and negative pulse is generated with amplitude provided by amplitude parameter.

Through a dedicated bit in the CONFIGURATION register it is possible to enable dither synchronization feature: once this bit is set the dither waveform is changed to start the new dither step synchronously to solenoid PWM signal. Synchronization can be implemented in two ways depending on the settings of SYNC_TYPE bit in

CONFIGURATION register: if the SYNC_TYPE is set to 0 the dither step synchronization is done at each change in the step value itself otherwise the synchronization is performed at the start of each dither period.

In case of dither step synchronization at each dither step is selected (SYNC_TYPE = 0) the dither step duration is increased with respect to the programmed value to include an integer number of PWM periods; the exact formula is given by:

$Tstep\_sync = ceil\ (((1 + (M+1)*2^N)*tref\_dth)/T_{pwm})*T_{pwm}$

The resulting dither period is 4 times the programmed Dither current step number bits of DITHPGM register multiplied by T_step_sync.

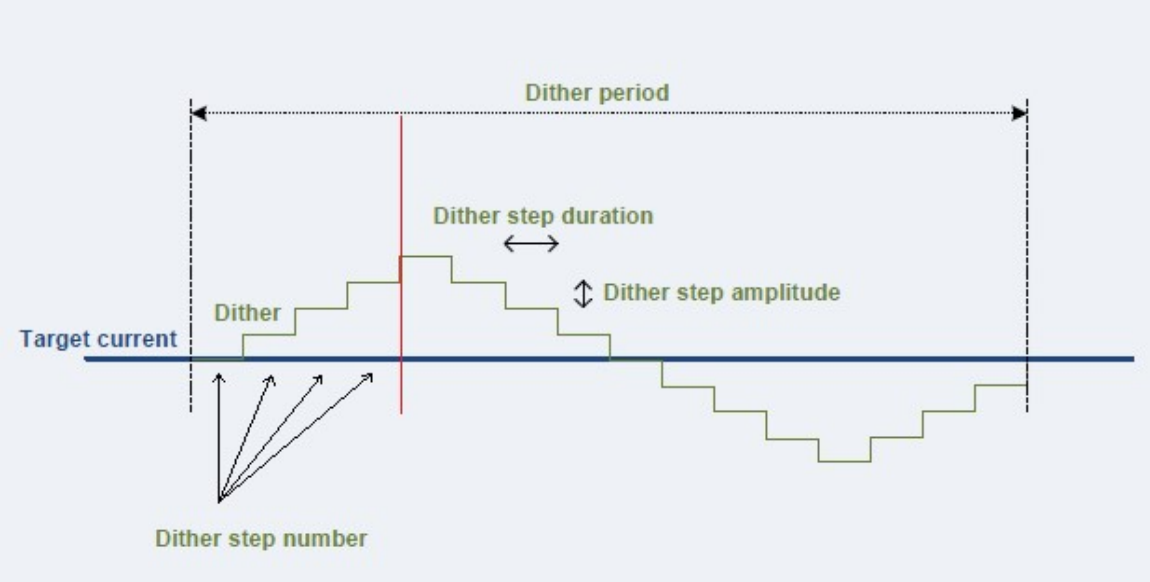
$Dither\ Period = 4 * N_{step} * Tstep\_sync$

In case of dither period synchronization at each dither period is selected (SYNC_TYPE = 1) only the first dither step duration is increased with respect to the programmed value in order to have a resulting dither period including an integer number of PWM periods; the Tstep_duration formula is unchanged with respect to the the condition of synchronization disabled, while the resulting dither period is given by:

$Dither\ Period = ceil\ (4*N_{step}*T_{step}/T_{PWM})*T_{PWM}$

Where N_{step} is the programmed Dither current step number in DITHPGM register.

Figure 29. Dither functionality



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HW Current Control Loop Configuration

When HW current feedback mode is selected, the solenoid current is controlled through a PI algorithm. In order to tune the transient response and settling time of the loop that may vary changing the load configuration, a sub set of control loop parameters are available through SPI registers.

For both variable and fixed frequency control the following parameters can be changed.

- KI Integral portion of the loopgain:
  - In variable frequency mode it is based on the formula $KI = 2^{-(N+3)}$
  - In fixed frequency mode it is based on the formula $KI = 2^{-(N+5)}$

where N is the decimal value stored in the 3 bits of the KGAINS register.

- KP Proportional portion of the loop gain:
  - $KP = 2^{N+1}$

where N is the decimal value stored in the 3 bits of the KGAINS register.

Note: Default values in KGAINS register are set in order to operate properly with typical load values in fixed frequency mode.

For variable frequency mode only the following parameters can be used to control integrator saturation of PI loop. In fixed frequency mode integrator saturation limits are internally computed and the above parameters are not used.

- INTLIMVAL Integrator Saturation Limit. Its value is:
  - 2^{N+7} if N≤13, where N is the decimal value stored in the 4 bits
  - 2^{20} if N>13

where N is the decimal value stored in the 4 bits of the INTGLIM register.

- TRINTLIMVAL Transient Integrator Saturation Limit: it is the integrator saturation limit during set point change transient response; transient response is defined as the time needed from set point change to reach zero error in the sensed current.
  - 0xxx → *TRINTLIMVAL* = 2^{-N} * *INTLIMVAL*
  - 1xxx → *TRINTLIMVAL* = *1*

where N is the decimal value stored in the 3 less significant bits of the INTGLIM register.

In variable frequency mode additional parameters can be configured through the Frequency Control Register to tune the PI coefficients of the frequency control loop:

- KFI Integral portion of the frequency control loop gain: it is available through 3 bits as 2^{-N}
- KFP Proportional portion of the frequency control loop gain: it is available through 3 bits as 2^{-N}
- FCIL: Frequency Control Integrator Limit: it enables saturation of the integrator in the frequency control loop. Saturation limit is internally computed and cannot be programmed.

Full On Mode

Each driver can be programmed to work in full on mode. If the bit FULL_ON_x is set to 1 (default is 0) the driver is kept on continuously, until the bit is programmed to 0 or a fault occurs.

10.1.1.2 Software current control

In this configuration, SW_cntr_x = 1, the device works as simple driver and provides the load current measurement to the microcontroller by SPI. In that way the microcontroller can close the current control loop acting directly on the parallel input of the channels.

In software mode a toggling of INx longer than INx_in_ft is used to trigger the measurement of the mean current flowing in the load; average current is calculated and updated into the dedicated AVGCUR SPI register at the end of a valid PWM input signal (see Figure 32 / Figure 33). To properly turn on the driver a command duration longer than LOADx_Ton_res has to be provided. (the same for the turning-off phase).

In case the INx input command is stucked, the average is evaluated till timeout set to 133334*tref_PWM, where tref_PWM = 125 ns, and a warning flag TMOUT is set in PWMSENSE register. At TMOUT the average current and PWM code calculations are restarted automatically.

Figure 30. **Software mode filter time**

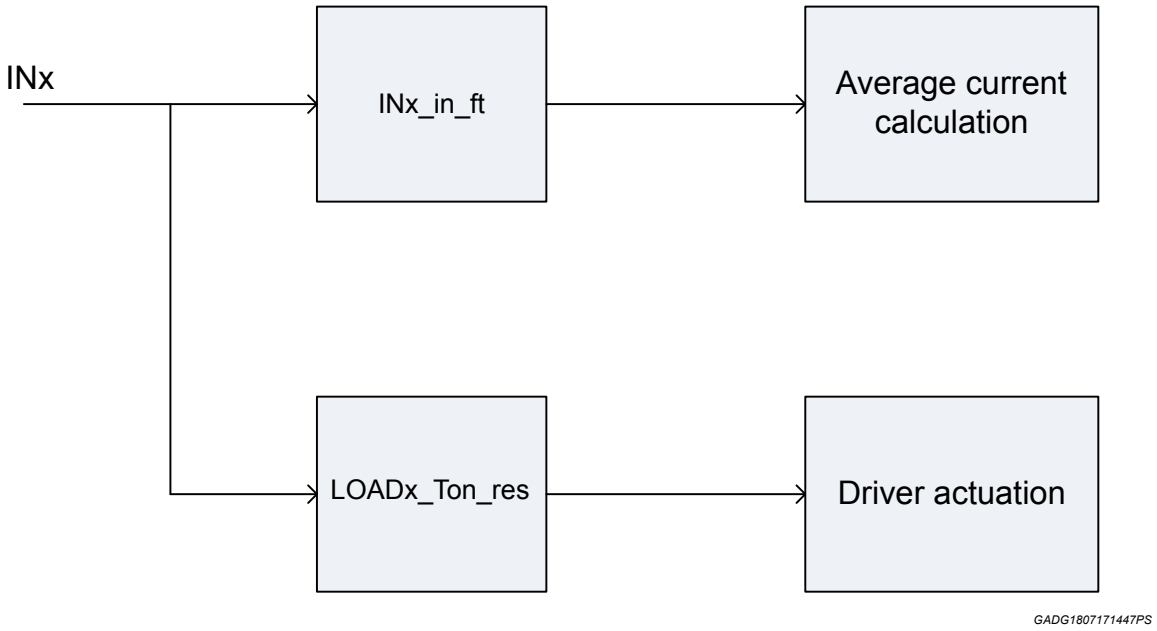
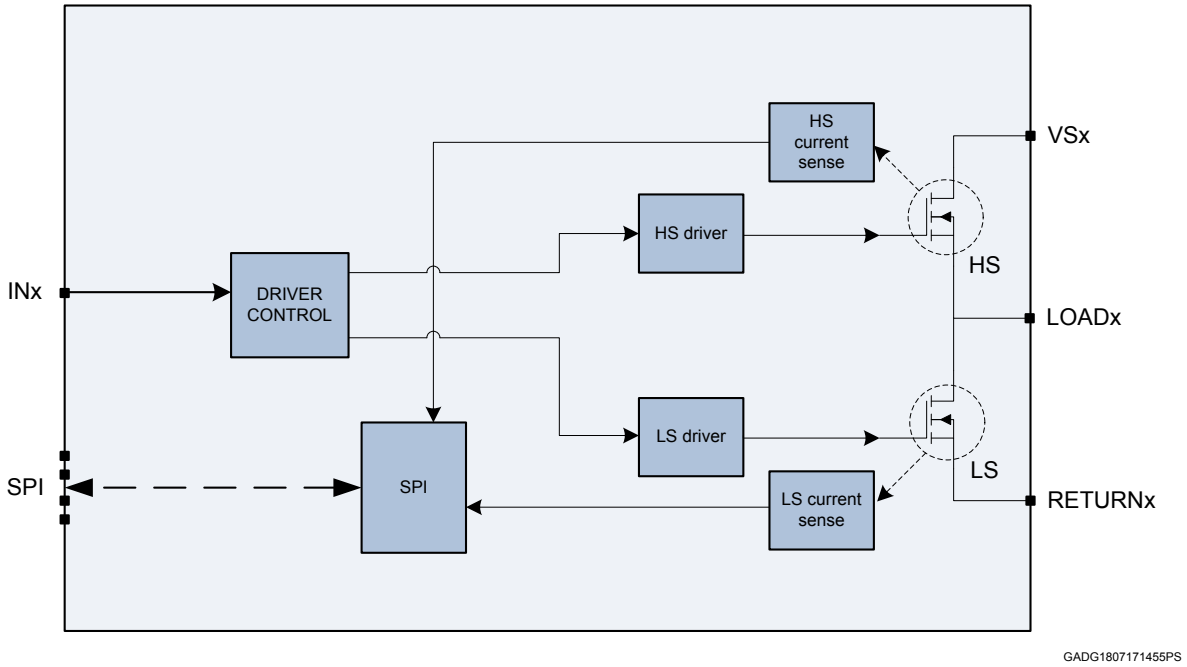


Figure 31. **Software control loop configuration**



Depending on the chosen configuration (HS or LS mode), INx polarity is as following:

Table 31. **Configuration HS and LS mode**

INx pin	Low–side Configuration		High–side Configuration	
	LS	HS	LS	HS
High	ON	OFF	OFF	ON
Low	OFF	ON	ON	OFF

Figure 32. **Driver timing chart HS_config=0, SW_cntr=1**

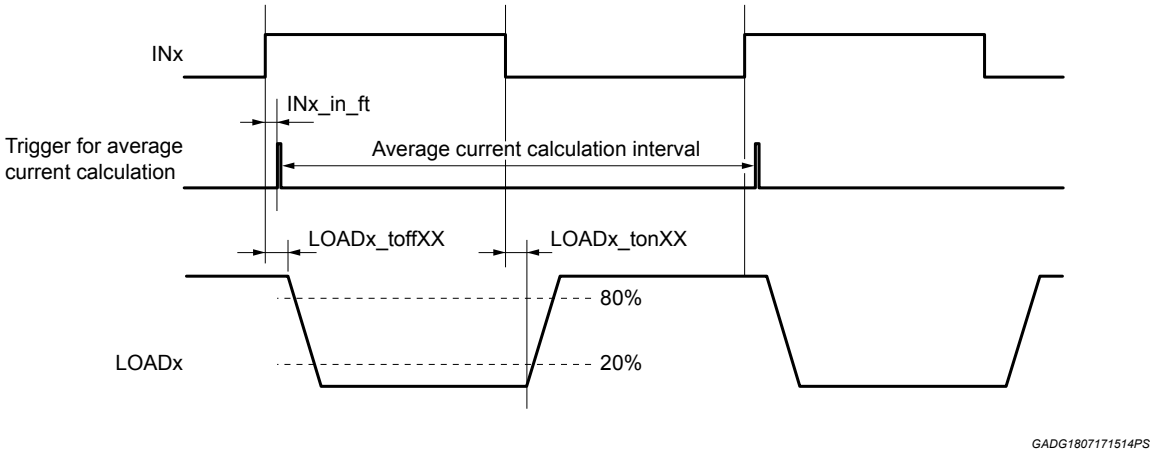
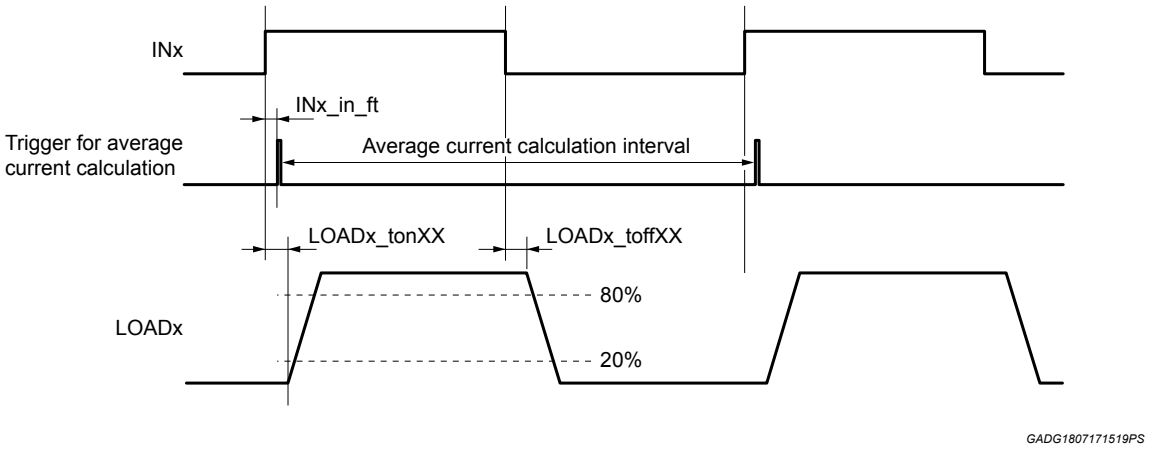


Figure 33. **Driver timing chart HS_config=1, SW_cntr=1**



10.1.1.3 *Solenoid current feedback*

Solenoid computed average current, sensed through internal current sense amplifier, is available for SPI reading in the AVGCUR register; the current information is stored in 11 bits.

AVGCUR is the average current post processed by the control algorithm over an entire PWM period. The Average current is updated every PWM cycle. The calculation starts when PWM raises and stops when a new PWM raises.

Table 32. Average current configuration

AVGCURR	Load target current HILOAD = 0 [bit resolution = 1500/2047 = 0.733 mA]	Load target current HILOAD = 1 [bit resolution = 2000/2047 = 0.9770 mA]
0	0 [mA]	0 [mA]
1	1 * 0,733 [mA]	1 * 0,977 [mA]
2	2 * 0,733 [mA]	2 * 0,977 [mA]
…	…	…
2046	2046 * 0,733 [mA]	2046 * 0,977 [mA]
2047	1500 [mA]	2000 [mA]

INSTCUR is the instantaneous current in the solenoid valve as it is read by the PI control loop input after offset compensation and calibration; the data is stored in the INSTCURR register with 12 bit signed (2's complement) format where the LSB is the ADC full scale (peak current regulation value, 2.25 A or 3 A depending on HILOAD bit settings) divided by 2047. This data can be used for example in SW mode to verify solenoid current flow depending on PWM level on INx inputs.

Table 33. Instantaneous current configuration

INSTCURR	Load target current HILOAD = 0 [bit resolution = 2250/2047 = 1.099 mA]	Load target current HILOAD = 1 [bit resolution = 3000/2047 = 1.465 mA]
0	0 [mA]	0 [mA]
± 1	± 1 * 1,099 [mA]	± 1 * 1,465 [mA]
± 2	± 2 * 1,099 [mA]	± 2 * 1,465 [mA]
…	…	…
± 2046	± 2046 1,099 [mA]	± 2046 * 1,465 [mA]
± 2047	± 2250 [mA]	± 3000 [mA]

The current sense amplifier input offset is cancelled through the choppering function; the following chopper parameters can be set through Frequency Control Register:

- Chopper time sets the toggling time of the chopper function (chopper period is twice this value)
  - If TOFSCHOP = 0 → *Offset Toggling Chopper Time* = 2^6 * 125ns
  - If TOFSCHOP = 1 → *Offset Toggling Chopper Time* = 2^7 * 125ns
- Offset Integrator time: sets the integrator time constant used to estimate the recovered high–side/low–side offsets of current sense circuit. The estimated offset values are available on read in the CSA Offset Compensation SPI register: the values are stored in the register using 9 bit signed (2's complement) for both HS and LS where the LSB weight is
  - Case 1.5 A full scale: 1.5 A * 1.5/213 = 275 µA/LSB
  - Case 2 A full scale: 2 A * 1.5/213 = 367 µA/LSB
  - If TOFSINT = 0 → *Offset IntegratorTime* = 2^{14} * 125 ns
  - If TOFSINT = 1 → *Offset IntegratorTime* = 2^{15} * 125 ns
- Offset Filter time sets the cut off frequency of the hi-pass filter used to extract offset choppered signal superimposed on the output current.
  - Offset Filter Time = 2^{N+3} * 125 ns where N is the decimal value stored in the 3 bits.

10.1.1.4 *Solenoid PWM period feedback*

The driver PWM period, generated by internal logic, is internally measured at each PWM rising edge and provided to the MCU for comparison with the programmed one in the PWMSENSE SPI register. The PWM period is provided over 18 bits in order to feedback also periods exceeding TMOUT values; the period value is equal to *N*Tref_PWM* where N is the value in the PWMSENSE register and Tref_PWM is 125 ns.

Table 34. **Solenoid PWM period feedback**

PWM_SENSE	Period when in Fixed Frequency
0	0 [s]
1	1 * 125 [ns]
2	2 * 125 [ns]
…	…
133333	133333 * 125 [ns]
133334	133334 * 125 [ns]
…	…
262143	262143 * 125 [ns]

10.1.1.5 *Driver diagnostic*

Thermal Protection

Each solenoid channel has a dedicated temperature sensor that continuously monitors the temperature of the low–side and of the high–side power FET. In case the temperature warning is reached a dedicated diagnostic bit is set and latched (T_WARN_x, where x indicates the channel where the thermal warning occurs). The latch is automatically cleared on SPI read if thermal warning condition is no longer present.

In case the temperature shut down is reached the related channel is put in tristate (setting the target current and the enable bit to zero); the GPO, if configured as IRQ, is triggered and a dedicated diagnostic bit is set. T_SD_x is the bit that latches the thermal shut down and it is cleared on SPI read. Channel activation is prevented if thermal shut down condition is still present on SPI read, GPO, if configured ad IRQ, follows T_SD_x bit (if not masked).

Overcurrent Protection

An overcurrent protection is present for each HS and LS of each solenoid channel. The overcurrent threshold is selectable through OVC_thres_x (where x indicates the channel).

Hardware mode: In case of overcurrent (on HS or on LS) the solenoid channel is put in tristate (setting the target current and the enable bit to zero), the GPO, if configured as IRQ, is triggered down and a dedicated diagnostic bit is set (OVC_LS_x or OVC_HS_x, where x indicates the channel and LS/HS the power MOS where the fault occurred). To restart the channel the microcontroller has to clear the fault bit (reading the fault register), to give the target current and the enable bit.

Software mode: The overcurrent protection in software mode is configurable by SPI (OVC_R bit). If OVC_R = 0 (default condition) in case of overcurrent (on HS or on LS) the solenoid channel is put in tristate (setting the enable bit to zero), the GPO, if configured as IRQ, is triggered down and a dedicated diagnostic bit is set (OVC_LS_x or OVC_HS_x, where x indicates the channel and LS/HS the power MOS where the fault occurred). To restart the channel the microcontroller has to clear the fault bit (reading the fault register) and to enable the channel. If OVC_R = 1 the restart function is activated: in this condition, when an overcurrent occurs, the failed power MOS is turned off, the GPO, if configured as IRQ, is triggered down, a dedicated diagnostic bit is set (OVC_LS_x or OVC_HS_x, where x indicates the channel and LS/HS the power MOS where the fault occurred) and the slew rate of the power in fault condition is automatically set to 11 (higher value to limit dissipation issue). The diagnostic bit can be cleared only by reading the register by SPI, however the channel can be restarted at the following rising edge of the parallel command.

Figure 34. **Driver behavior in short to GND condition: HS_config=1, SW_cntr=1, OVC_R=1**

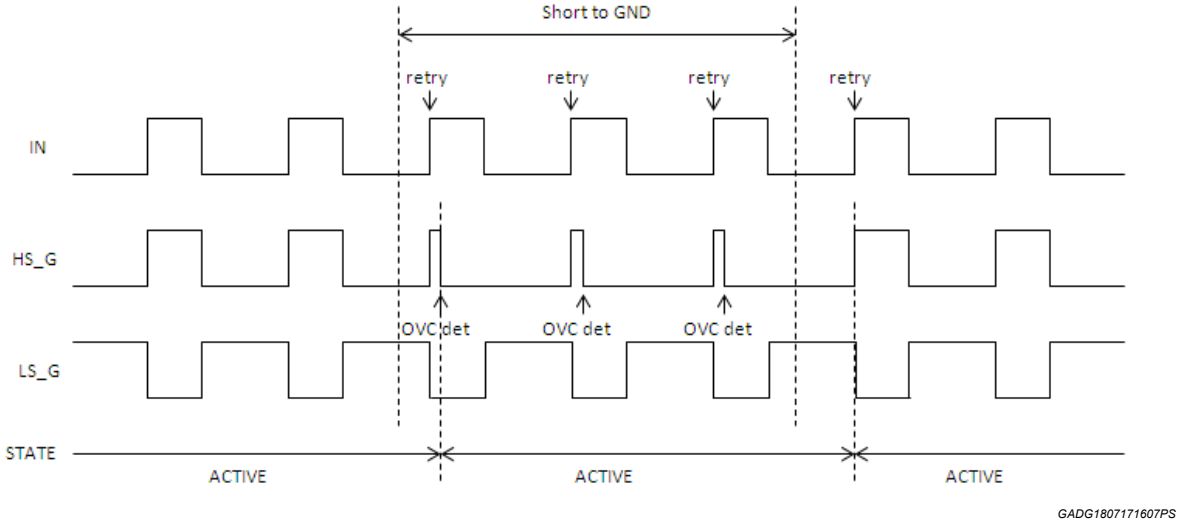
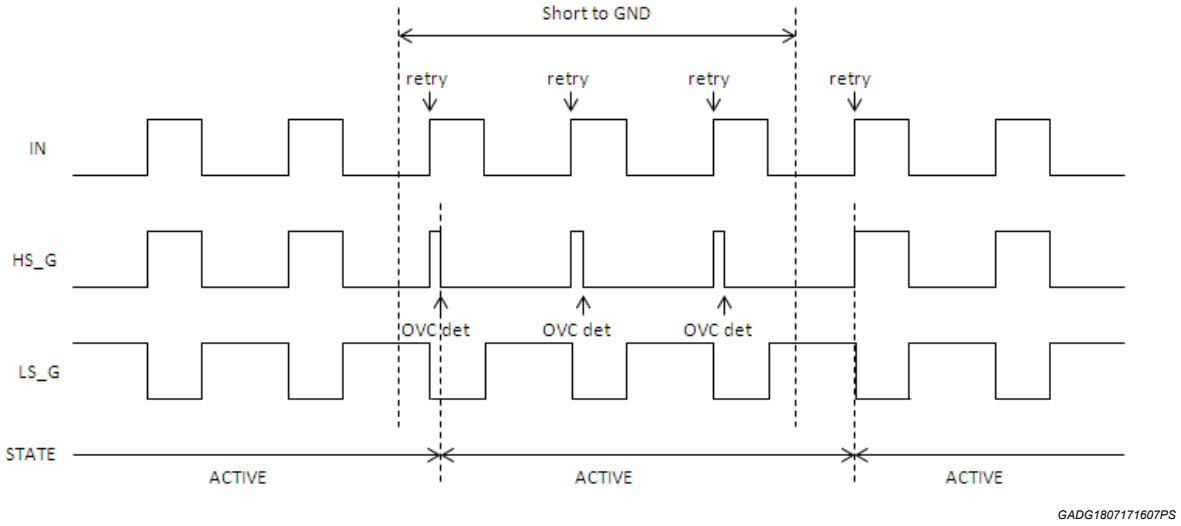


Figure 35. **Driver behavior in short to battery condition: HS_config=1, SW_cntr=1, OVC_R=1**



Solenoid supply disconnection

When solenoid driver is configured in LS configuration recirculation happens through the internal HS FET. If the supply of HS power stage is lost, due to the inductive nature of the load, voltage at LOADx pin could rise above absolute ratings damaging the device; to prevent such a condition a clamping structure is integrated in the LS driver. If the clamping structure is activated in normal operation it means a disconnection of HS supply happened: as a consequence the solenoid channel is put in tristate and a dedicated diagnostic bit is set. To restart the channel the microcontroller has to clear the fault bit (reading the fault register) and to enable the channel again. LS clamp circuitry is automatically disabled when VBATP over voltage is detected to avoid unwanted clamp activation during load dump event.

OFF State Diagnostic

The device provides off-state diagnostic for each channel; simplified schematic of implemented diagnostic is shown in Figure 36 and Figure 37 depending on the chosen configuration.

By default diagnostic pull up/down currents are disabled and comparator outputs are masked by internal logic, to enable OFF state diagnostic the channel must be put first in tristate condition and then (if not already done with previous SPI frames) diagnostic must be enabled. Once the desired channel is put in tristate a false diagnostic can be sensed due to the time needed to discharge output voltage through the load. To avoid unwanted fault

detection a blanking time is implemented: during this time diagnostic comparators are masked. The diagnostic blanking time is programmable through SPI to choose the proper value depending on external load value and ESD capacitor connected to the output pin. Fault conditions are latched and cleared on SPI read, however they do not prevent enabling of the solenoid channels.

OFF state diagnostic comparators are the same for both HS and LS configuration and their output is decoded from internal logic to set SPI fault bits according to the following tables:

Figure 36. LS configuration diagnostic

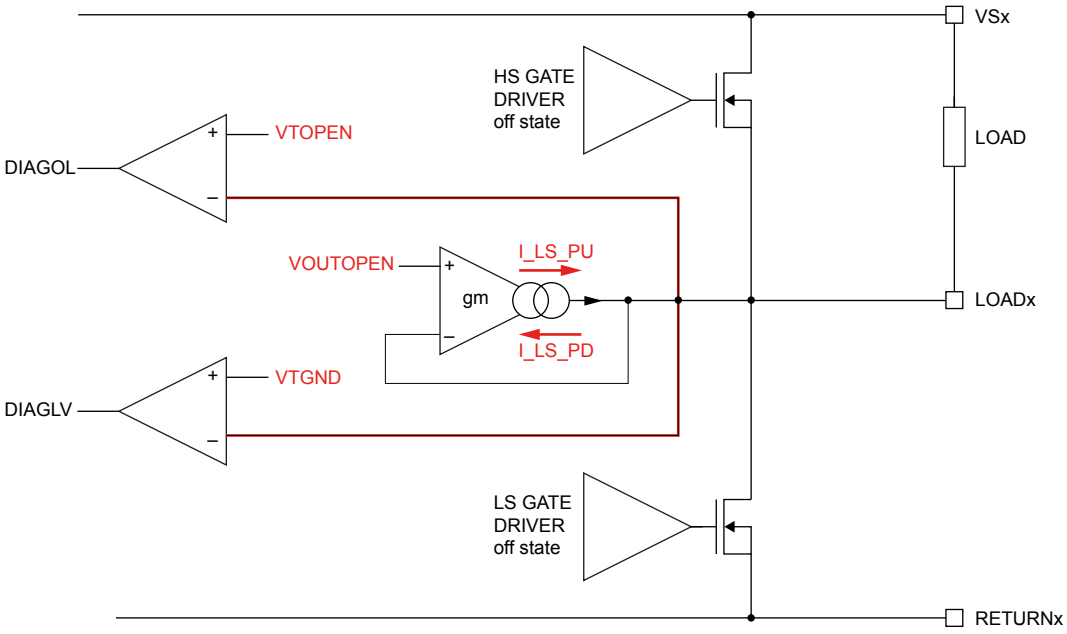


Table 35. LS diagnostic truth table

Comparator Output		FAULT DETECTION	Exception Registers [6:5]	
DIAGOL	DIAGLV		OPEN LOAD	SHORT
0	0	Normal operation – no fault-	0	0
0	1	Not possible	0	0
1	0	Open load	1	0
1	1	Short to ground	0	

Figure 37. **HS configuration diagnostic**

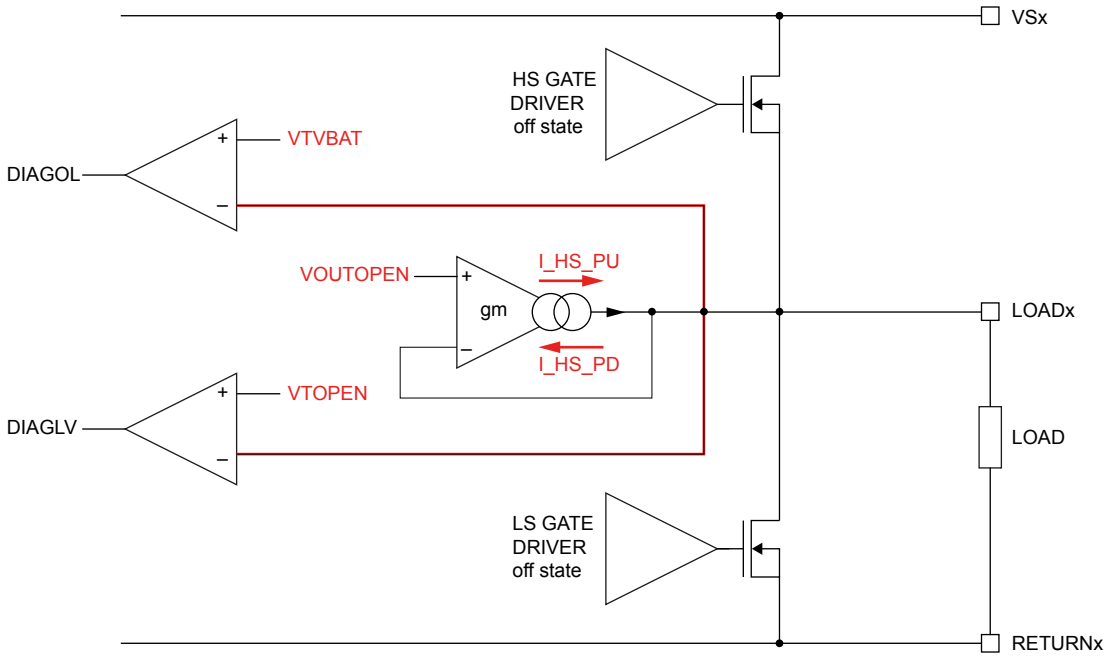


Table 36. **HS diagnostic truth table**

Comparator Output		FAULT DETECTION	Exception Registers [6:5]	
DIAGOL	DIAGLV		OPEN LOAD	SHORT
0	0	Short to Battery	0	0
0	1	Not possible	0	0
1	0	Open load	1	0
1	1	Normal operation – no fault-	0	0

10.1.2 Solenoid driver electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VSx ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 37. **Solenoid driver electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Enable Input							
VIL	Logic Input Low Voltage				0.75	V	EN_DR
VIH	Logic Input High Voltage		1.75			V	EN_DR
Vhysteresis	Input hysteresis Voltage		0.1		1	V	EN_DR
EN_DRPD	EN_DR pull-down	INx = 5 V	10	50	100	µA	EN_DR
EN_DR_deglitch	EN_DR deglitch filter time	Guaranteed by scan	1		2	µs	EN_DR
VIL	Logic Input Low Voltage				0.75	V	INx
VIH	Logic Input High Voltage		1.75			V	INx
Vhysteresis	Input hysteresis Voltage		0.1		1	V	INx
INxPD	INx pull-down	INx = 5 V	10	50	100	µA	INx

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
INx_in_ft	INx input filter time	Software mode Guaranteed by scan	1		2	µs	INx
INx_delay_AVG	Delay time from INx_in_ft to average current update	Software mode Guaranteed by scan	1		5.5	µs	INx
Power Stage							
Irev_VSx	VSx reverse current	Application note: in the application condition, no impact on other functions, no reset generation(1)	-3			A	VSx
Irev_LOADx	LOADx reverse current	Application note: in the application condition, no impact on other functions, no leakage from nearby pins, no reset generation(2)	-3			A	LOADx
VSx_lkg	VSx current leakage stby	Output disabled, WAKE = 0 V, VS = 13 V	-1		1	µA	VSx
LOADx_lkg	LOADx current leakage tristate	Output disabled, WAKE = VS = 13 V, LOADx = VS or GND	-130		+140	µA	LOADx
HS_RdsON	High–side RdsON	T_j = 150 °C, I_{LOAD} = 1 A			0.44	Ω	LOADx
HS_RdsON	High–side RdsON	T_j = 175 °C, I_{LOAD} = 1 A			0.5	Ω	LOADx
LS_RdsON	Low–side RdsON	T_j = 150 °C, I_{LOAD} = 1 A			0.44	Ω	LOADx
LS_RdsON	Low–side RdsON	T_j = 175 °C, I_{LOAD} = 1 A			0.5	Ω	LOADx
Driver Parameters							
LOADx_ton_res	ton filter time	Software mode, Guaranteed by scan	3		4	µs	LOADx
LOADx_toff_res	toff filter time	Software mode, Guaranteed by scan	3		4	µs	LOADx
LOADx_SR00	Voltage slew rate SR00	20% to 80% & 80% to 20%, VBATP=13 V, Rload = 6 Ω, Cload = 10 nF	0.1	0.3	0.5	V/µs	LOADx
LOADx_SR01	Voltage slew rate SR01	20% to 80% & 80% to 20%, VBATP=13 V, Rload = 6 Ω, Cload = 10 nF	0.5	1	1.8	V/µs	LOADx
LOADx_SR10	Voltage slew rate SR10	20% to 80% & 80% to 20%, VBATP=13 V, Rload = 6 Ω, Cload = 10 nF	1.8	4	6	V/µs	LOADx
LOADx_SR11	Voltage slew rate SR11	20% to 80% & 80% to 20%, VBATP=13 V, Rload = 6 Ω, Cload = 10 nF	4	8	12	V/µs	LOADx
LOADx_ton00	ton 00	SW mode from INx to 20% in HS, from INx to 80% in LS	1		27	µs	LOADx
LOADx_ton01	ton 01	SW mode, from INx to 20% in HS,from INx to 80% in LS	1		18	µs	LOADx
LOADx_ton10	ton 10	SW mode, from INx to 20% in HS,from INx to 80% in LS	1		14	µs	LOADx
LOADx_ton11	ton 11	SW mode, from INx to 20% in HS,from INx to 80% in LS	1		13	µs	LOADx
LOADx_toff00	toff 00	SW mode, from INx to 80% in HS, from INx to 20% in LS	1		50	µs	LOADx
LOADx_toff01	toff 01	SW mode, from INx to 80% in HS, from INx to 20% in LS	1		23	µs	LOADx
LOADx_toff10	toff 10	SW mode, from INx to 80% in HS, from INx to 20% in LS	1		19	µs	LOADx
LOADx_toff11	toff 11	SW mode, from INx to 80% in HS, from INx to 20% in LS	1		18	µs	LOADx
Current Control							
Ireg_range	Current regulation range	HILOAD_x = 0	0		1.5	A	LOADx
Ipeak_range	Peak Current regulation range	HILOAD_x = 0	0		2.25	A	LOADx
Ireg_acc_L	Current regulation accuracy	HILOAD_x = 0, 0 A ≤ Ireg ≤ 0.5 A (3)	-8		8	mA	LOADx

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Ireg_acc	Current regulation accuracy	HILOAD_x = 0, 0.5 A < Ireg ≤ 1.5 A [3]	-1		+1	%	LOADx
Ireg_res	Current regulation resolution	HILOAD_x = 0		0.733		mA	LOADx
Ireg_res	Current regulation resolution	HILOAD_x = 1		0.977		mA	LOADx
Ireg_range	Current regulation range	HILOAD_x = 1	0		2	A	LOADx
Ipeak_range	Peak Current regulation range	HILOAD_x = 1	0		3	A	LOADx
Ireg_acc_L	Current regulation accuracy	HILOAD_x = 1, 0 A ≤ Ireg ≤ 0.075 A[4]	-20		+15	mA	LOADx
Ireg_acc_L	Current regulation accuracy	HILOAD_x = 1, 0.075 A < Ireg ≤ 0.3 A[4]	-15		+12	%	LOADx
Ireg_acc_L	Current regulation accuracy	HILOAD_x = 1, 0.3 A < Ireg ≤ 0.5 A[4]	-5		+4	%	LOADx
Ireg_acc	Current regulation accuracy	HILOAD_x = 1, 0.5 A < Ireg ≤ 2 A[4]	-4		+4	%	LOADx
Ireg_res	Current regulation resolution	HILOAD_x = 1		1		LSB	LOADx
Dth_ampl	Dither Tstep amplitude	HILOAD_x = 0	0		93	mA	LOADx
Dth_ampl	Dither Tstep amplitude	HILOAD_x = 1	0		124	mA	LOADx
Dth_res	Dither Tstep resolution	HILOAD_x = 0		0.733		mA	LOADx
Dth_res	Dither Tstep resolution	HILOAD_x = 1		0.977		mA	LOADx
Dth_num	Dither Tstep number	Guaranteed by scan	0		31	step	LOADx
Dth_dur	Dither Tstep duration	Guaranteed by scan			65.5	ms	LOADx
On State Diagnostic							
I_HS_ovc0	HS overcurrent	OVC_thres_x=0	-5	-4	-3	A	LOADx
I_HS_ovc1	HS overcurrent	OVC_thres_x=1, 25 °C ≤ T_j ≤ 175 °C	-6.5		-4.5	A	LOADx
		OVC_thres_x=1, -40 °C ≤ T_j ≤ 25 °C	-7		-4.5	A	LOADx
I_LS_ovc0	LS overcurrent	OVC_thres_x=0	3	4	5	A	LOADx
I_LS_ovc1	LS overcurrent	OVC_thres_x=1, 25 °C ≤ T_j ≤ 175 °C	4.5		6.5	A	LOADx
		OVC_thres_x=1, -40 °C ≤ T_j ≤ 25 °C	4.5		7	A	LOADx
I_HS_ocv_flt	HS overcurrent filter time	Guaranteed by scan	3		5	µs	LOADx
I_LS_ocv_flt	LS overcurrent filter time	Guaranteed by scan	3		5	µs	LOADx
T_WARN	Temperature warning		175		185	°C	LOADx
T_SD	Temperature shut down		185		200	°C	LOADx
T_SD_hy	Temperature shut down hysteresis		5		10	°C	LOADx
T_SD_deglitch	Digital deglitch filter time	Guaranteed by scan	7.5	10	12.5	µs	LOADx
Vclamp	LOADx clamp voltage	VBATP < 27 V	32	35	38	V	LOADx
Vclamp_dly	LOADx clamp activation detection delay	Design info, not tested	0.5		2	µs	LOADx
Vclamp_flt	LOADx clamp detection filter time	Guaranteed by scan	2.5	5	7.5	µs	LOADx
Eclamp	Energy clamp single pulse	Iload=2 A, Tj=100 °C			25	mJ	LOADx
Eclamp	Energy clamp single pulse	Iload=2 A, Tj=175 °C			18	mJ	LOADx
Off State Diagnostic – LS Configuration							
VTGND	Short to GND threshold voltage	LS mode, driver tristate, diagnostic on	1.9	2.1	2.3	V	LOADx
VTOPEN	Open load threshold voltage	LS mode, driver tristate, diagnostic on	2.7	2.9	3.1	V	LOADx
VOUTOPEN	Open load voltage	LS mode, driver tristate, diagnostic on	2.3	2.5	2.7	V	LOADx
I_LS_THOPEN	Open load threshold current		30	60	90	µA	LOADx

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_LS_PD	Diagnostic pull down current		40	70	120	µA	LOADx
I_LS_PU	Diagnostic pull up current		50	75	100	µA	LOADx
td_blank_0	Blank time 0	Bit_blank_x = 0, Guaranteed by scan	5.06		7.44	ms	LOADx
td_blank_1	Blank time 1	Bit_blank_x = 1, Guaranteed by scan	2.53		3.75	ms	LOADx
tflt_diagoff	Filter time	Guaranteed by scan	55		80	µs	LOADx
	Minimum OFF time for correct diagnostic (Blank time 0)	Application note (esd cap < 12nF, Bit_blank = 0)	7.52			ms	LOADx
	Minimum OFF time for correct diagnostic (Blank time 1)	Application note (esd cap < 6nF, Bit_blank = 1)	3.83			ms	LOADx
Off State Diagnostic – HS Configuration							
VTVBAT	Short to battery threshold voltage	HS mode, driver tristate, diagnostic on	2.7	2.9	3.1	V	LOADx
VTOPEN	Open load threshold voltage	HS mode, driver tristate, diagnostic on	1.9	2.1	2.3	V	LOADx
VOUTOPEN	Open load voltage	HS mode, driver tristate, diagnostic on	2.3	2.5	2.7	V	LOADx
I_HS_THOPEN	Open load threshold current		30	60	90	µA	LOADx
I_HS_PU	Diagnostic pull up current		40	70	100	µA	LOADx
I_HS_PD	Diagnostic pull down current		210	245	320	µA	LOADx
td_blank_0	Blank time 0	Bit_blank_x = 0, Guaranteed by scan	1		1.5	ms	LOADx
td_blank_1	Blank time 1	Bit_blank_x = 1, Guaranteed by scan	500		750	µs	LOADx
tflt_diagoff	Filter time	Guaranteed by scan	55		80	µs	LOADx
	Minimum OFF time for correct diagnostic (Blank time 0)	Application note (esd cap < 12nF, Bit_blank = 0)	1580			µs	LOADx
	Minimum OFF time for correct diagnostic (Blank time 1)	Application note (esd cap < 6nF, Bit_blank = 1)	830			µs	LOADx

1. *Parallel reverse current on multiple channels not considered: max negative total pulsed current, assuming VSx shorted at Ta = 135, is -14 A.*
2. *Parallel reverse current on multiple channels not considered.*
3. *Provided configuration parameters and current control settings are able to allow proper regulation*
4. *Provided configuration parameters and current control settings are able to allow proper regulation, assuming constant HILOAD setting over life time*

10.1.3 Solenoid driver error handling

Table 38. Solenoid driver error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
HS Overcurrent	Solenoid in PWM mode or full on mode, HS on	HW mode: Solenoid channel set in tristate, current set-point set to 0. **HS over current** bit (2) set in **Exceptions** register. SW mode: same as HW mode if OVC_R bit is set to 0, otherwise only the fault is latched and the channel is kept enabled and reactivated at next PWM edge	On read	Clear the fault via SPI and set **DRVENAx** bit in **SolEnDRV**register
LS Overcurrent	Solenoid in PWM mode or full on mode, HS on	HW mode: Solenoid channel set in tristate, current set-point set to 0. **LS over current** bit (1) set in **Exceptions** register. SW mode: same as HW mode if OVC_R bit is set to 0, otherwise only the fault is latched and the channel is kept enabled and reactivated at next PWM edge	On read	Clear the fault via SPI and set **DRVENAx** bit in **SolEnDRV**register

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
Overvoltage, clamp activation	On state	Driver set to tristate mode, **LS_CLAMP_ACT** SPI fault (3) latched in **Exceptions** register	On read	Clear the fault via SPI and set **DRVENAx** bit in **SolEnDRV**register
Short to ground (LVT)	Solenoid in tristate mode, diagnostic enabled	**Short Detection** fault bit (5) latched in **Exceptions** register	On read	N. D.
Open load (OPL)	Solenoid in tristate mode, diagnostic enabled	**Open Load** fault bit (6) latched in **Exceptions** register	On read	N. D.
Overtemperature Warning	On state	**T_WARN** SPI fault (15) latched in **Exceptions** register	On read	N. D.
Overtemperature Shutdown	On state	**Solenoid channel set in tristate, current set-point set to 0. T_SD** SPI fault (0) latched in **Exceptions** register	On read	Clear the fault via SPI and set **DRVENAx** bit in **SolEnDRV**register

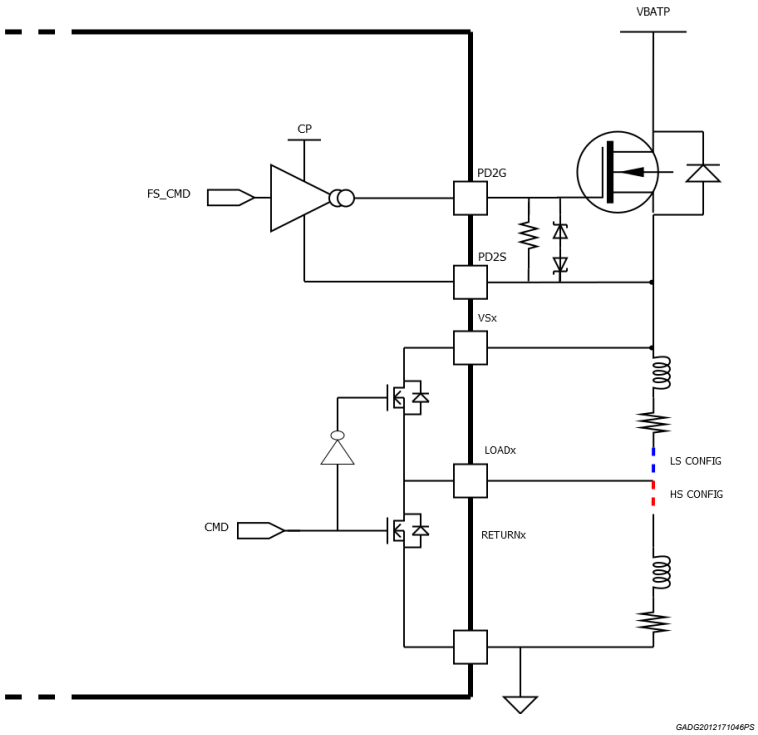
10.2 Fail-safe pre-driver

10.2.1 Fail-safe pre-driver functional description

For safety purpose the solenoid loads may be connected to battery line through an external fail-safe switch driven by the device: in case of fault the device should be able to switch-off external fail-safe switch to avoid unwanted energization of solenoid loads.

The turning ON and OFF command has to be delivered through SPI communication.

Figure 38. Failsafe concept



10.2.2 Fail–safe pre–driver electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ PD1D ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 39. Fail-safe Pre-driver electrical characteristics

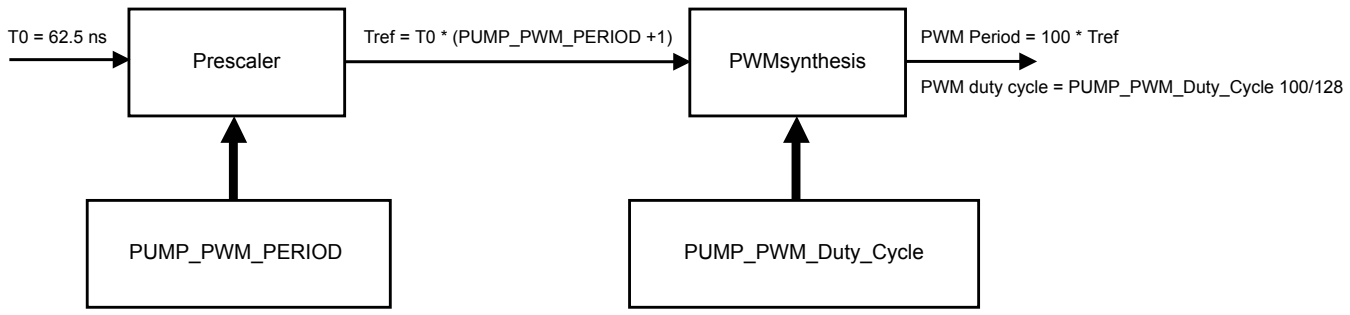
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Failsafe Pre-driver							
PD2_ON	PD2 ON voltage	PD2G – PD2S	7		10	V	PD2G, PD2S
PD2_OFF	PD2 OFF voltage	PD2G – PD2S	0		1	V	PD2G, PD2S
PD2_Isource	PD2 current source		0.5	1	1.5	mA	PD2G
PD2_Isink	PD2 current sink		2.5	5	7.5	mA	PD2G
PD2S_Ibias_OFF	PD2S bias current from CP supply	Failsafe Pre-driver disabled, WAKE = VBATP = 13V	-350	-250	-150	µA	PD2S
PD2S_Ibias_ON	PD2S bias current from CP supply	FailSafe Pre-driver enabled, WAKE = VBATP = 13V	-250	-160	-100	µA	PD2S

10.3 Pump pre-driver

10.3.1 Pump pre-driver functional description

The device provides a pump motor pre-driver channel that can operate in PWM mode. The value of switching frequency and value of the duty cycle of the pre-driver have to be programmed by SPI using PUMP_TCK_PGM (8bit) and PUMP_DTY_PGM (8bit) registers. The picture below shows the architecture of the PWM generation.

Figure 39. Pump PWM programming



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The PUMP_PWM_PERIOD register can be programmed from 8 to 255, with the following relation:

- If PUMP_PWM_PERIOD < 8 → Tref = 9 * T0
- If PUMP_PWM_PERIOD ≥ 8 → Tref = (PUMP_TCK_PGM + 1) * T0

The table below shows the PUMP_T_PWM relation.

Table 40. Pump PWM frequency decoding

PUMP_PWM_PERIOD	PWM Period [µs]	PWM Frequency [kHz]
0	56,25	17,777
1	56,25	17,777

PUMP_PWM_PERIOD	PWM Period [µs]	PWM Frequency [kHz]
…	…	…
7	56,25	17,777
8	56,25	17,777
9	62,50	16,000
10	68,75	14,545
…	…	…
255	1600,00	0,625

The PUMP_PWM_Duty_Cycle register can be programmed from 0 to 255, with the following relation:

- If PUMP_PWM_DUTY_CYCLE < 128 → PWM duty cycle = PUMP_PWM_DUTY_CYCLE * 100/128 [%]
- If PUMP_PWM_DUTY_CYCLE ≥ 128 → PWM duty cycle = 100 [%]

The following table explains the duty cycle programming.

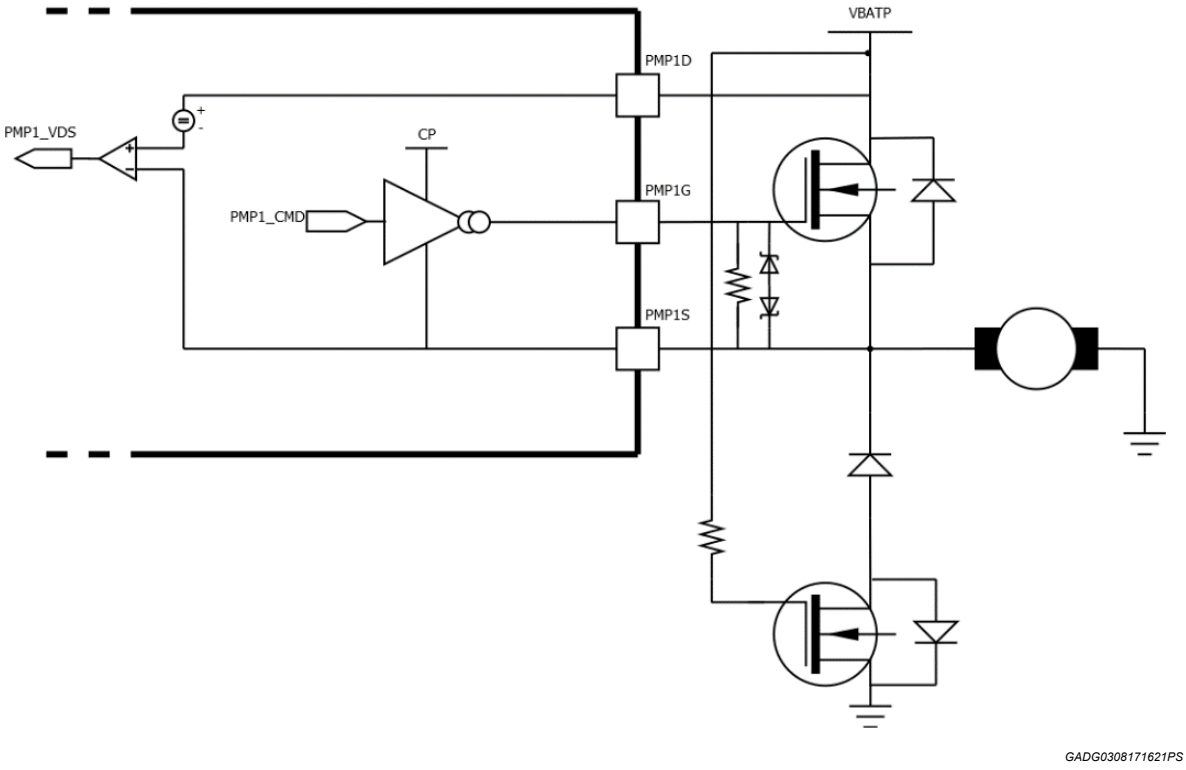
Table 41. Pump PWM duty cycle decoding

PUMP_PWM_Duty_Cycle	Duty cycle
0	0,000 %
1	0,781 %
2	1,562 %
…	…
20	15,625 %
…	…
60	46,875 %
…	…
127	99,219 %
128	100 %
…	…
255	100 %

The pump pre–driver has a VDS monitoring that is used to protect the external FET in case of short circuit to ground. Through PUMP_VDS_PGM1 and PUMP_VDS_PGM2 SPI configuration bits four different VDS thresholds are programmable.

In case of short circuit detection the pump pre-driver is switched off, a dedicated diagnostic bit is set and, if programmed, the GPO is triggered. The fault configuration is latched and it is cleared on SPI read, once the fault is cleared the pump pre-driver is automatically turned on keeping duty cycle and frequency information.

Figure 40. **Pump motor concept**



10.3.2 Pump pre-driver electrical characteristics

5.5V ≤ VBATP ≤ 19V; 5.5V ≤ PD1D ≤ 19V; -40°C ≤ Tj ≤ 175°C unless otherwise noticed. All voltages refer to GND pin.

Table 42. **Pump pre-driver electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Pump Pre-driver							
	PWM frequency	Application note	0.5		19	kHz	
	Ext. N-ch gate charge	Application note			30	nC	
PD1_ON	PD1 ON voltage	PD1G – PD1S	7		10	V	PD1G, PD1S
PD1_OFF	PD1 OFF voltage	PD1G – PD1S		0	0.5	V	PD1G, PD1S
PD1_Isource	PD1 current source		10	25	35	mA	PD1G
PD1_Isink	PD1 current sink		10	25	35	mA	PD1G
PD1D_Ileak_dis	PD1D leakage current	Pump Pre-driver disabled, PD1D = VBATP = 13V, WAKE = 0V	-1		1	µA	PD1D
PD1D_Ileak_dis	PD1D leakage current	Pump Pre-driver disabled PD1D = VBATP = WAKE = 13V	40	90	150	µA	PD1D
PD1D_Ileak_en_on	PD1D leak current	Pump Pre-driver enabled, PWM on, PD1D = VBATP = WAKE = 13V	200	270	400	µA	PD1D
PD1D_Ileak_en_off	PD1D leak current	Pump Pre-driver enabled, PWM off, PD1D = VBATP = WAKE = 13V	200	360	500	µA	PD1D
PD1S_Ibias_dis	PD1S bias current from CP supply	Pump Pre-driver disabled PD1D = VBATP = WAKE = 13V	-650	-485	-350	µA	PD1S

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
PD1S_Ibias_en_on	PD1S bias current from CP supply	Pump Pre-driver enabled, PWM on, PD1D = VBATP = WAKE = 13V	-300	-185	-100	µA	PD1S
PD1S_Ibias_en_off	PD1S bias current from CP supply	Pump Pre-driver enabled, PWM off, PD1D = VBATP = WAKE = 13V	-600	-485	-200	µA	PD1S
On State Diagnostic							
PD1_VDS	VDS th	PUMP_PREDRIVER_TH = 00	0.35	0.5	0.65	V	PD1S, PD1D
PD1_VDS	VDS th	PUMP_PREDRIVER_TH = 01	0.8	1	1.2	V	PD1S, PD1D
PD1_VDS	VDS th	PUMP_PREDRIVER_TH = 10	1.3	1.5	1.7	V	PD1S, PD1D
PD1_VDS	VDS th	PUMP_PREDRIVER_TH = 11	1.75	2	2.25	V	PD1S, PD1D
T_PD1_VDS_blank	VDS blank time	Guaranteed by scan	7	10	13	µs	PD1S, PD1D
T_PD1_VDS_flt	VDS filter time	EMI filter Guaranteed by deisgn	200	600	1000	ns	PD1S, PD1D

10.3.3 Pump pre-driver error handling

Table 43. Pump pre-driver error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VDS fault	PUMP enabled in PWM mode	Mask PUMP pre-driver PWM to keep the PUMP FET off and set **VDS Pump Pre Driver Fault** bit (11) in **SERVFLT** register	On read	Automatic on SPI read

11 Charge pump

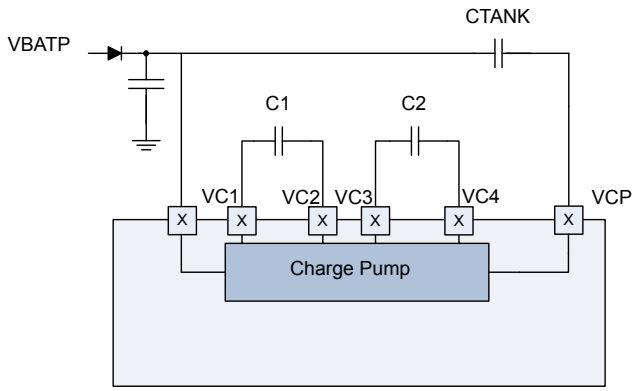
11.1 Charge pump functional description

The device uses a two stage charge pump circuit with external capacitors to ensure external MOSFET pre–drivers, valve drivers and VDD3/4 low drop performances are guaranteed during low battery cranking.

An internal control loop monitors the output voltage and controls charge the pump efficiency in order to reduce charge pump activity at light loads to reduce emissions during normal activity; when the battery input is low the charge pump is able to work at full power to guarantee relevant parameters.

The device provides an under voltage monitor on charge pump voltage. In case of fault the device behaves as reported in the Functional table chapter and a dedicated SPI bit is set and latched. The diagnostic is not masked during power-up phase.

Figure 41. Charge pump



11.2 Charge pump electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C, unless otherwise noticed. All voltages refer to GND pin.

Table 44. Charge Pump electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Charge pump							
C1, C2	External capacitor	Application note		68		nF	VCx
CTANK	Tank capacitor	Application note		220		nF	VCP
VCP_freq	Charge pump frequency			fOSCINT[MG1] /34		kHz	VCx
VCP_out	Target CP output	Design info, not tested		VBATP+9		V	VCP
VCP_out	Minimum charge pump output voltage	Iload=10 mA VBATP min=5.5 V	VBATP+7			V	VCP
Diagnostic							
VCP_UV	VCP under voltage		VBATP+5 V		VBATP+6 V	V	VCP
VCP_UV_FLT	VCP digital under voltage filter time	Guaranteed by scan	7.5	10	12.5	µs	VCP

11.3 Charge pump error handling

Table 45. **Charge Pump error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VCP_uv	ON state	Solenoid outputs and PUMP pre-driver disabled, set **CP UNDER VOLTAGE** bit (3) in SPI **Service Fault register**	On read	After fault disappears, set **ENCHx**, **Pump Pre-Driver Enable** in **SERVENA** register and **DRVENAx** bit in **SolEnDRV** register for PUMP and solenoids

12 General purpose output (GPO)

12.1 GPO functional description

The device provides a low–side open drain general purpose output. This output can be used as a standard low–side output or as a configurable interrupt generator through dedicated SPI bit in the Service Enable register.

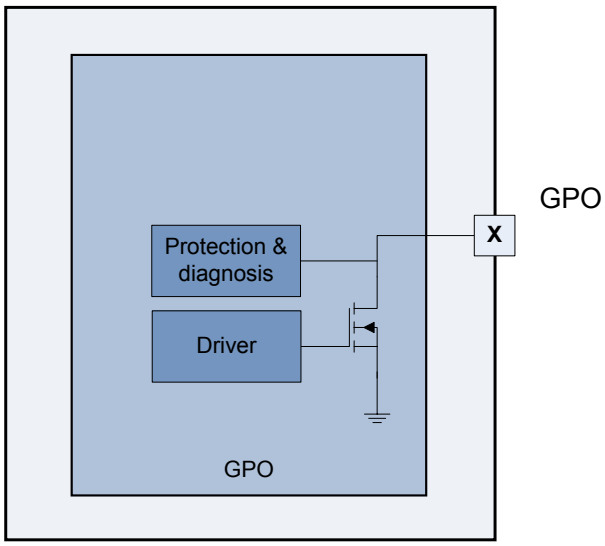
Default configuration at device power on reset is IRQ functionality (GPO Configuration = 0): driver works as General Purpose Output and it can be used to generate an interrupt to the microcontroller whenever a fault is detected by the device. In case of interrupt generation GPO pin is driven low. The second functionality (GPO Configuration = 1) is as low–side led driver (50 mA current capability): in this case the GPO output is directly driven by the microcontroller through SPI command bit.

When used as LS driver GPO is equipped with on state and off state diagnostic. The off state diagnostic is made of open load and short to GND checks; open load diagnostic can be disabled by SPI bit together with its diagnosis bias current to use GPO output for LED mode operation; the short to GND off state diagnostic remains active and behaves as usual.

During on state of the GPO output the driver (both in IRQ or LS configuration) is protected against short to battery event through over current diagnostic: when an over current fault occurs the driver switches immediately off to reduce the power dissipation, the fault is latched and is cleared by SPI read; the GPO driver is kept off until the fault is cleared, then it is restarted automatically.

The turn on/off time is fixed; during turn-off the slope is controlled by external RC load.

Figure 42. GPO driver



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The table below lists the fault that can trigger an interrupt in IRQ mode; the trigger generation by these faults can be masked through Service Fault Mask and Driver Fault Mask SPI registers.

Table 46. **Service and Driver Fault Mask registers**

Name	Description	Value	SPI bit
Service Fault Mask register			
WD_LOAD_DIS_GPO	When WD_CNT counter becomes lower than WD_th_low threshold and solenoid drivers are disabled	E_WD_LOAD_DIS_GPO=0 the fault affects GPO E_WD_LOAD_DIS_GPO =1 the fault does not affect GPO	E_WD_LOAD_DIS_GPO
EN_DR - EN_DR pin is in low state	When EN_DR pin input is in low state	E_EN_GPO=0 the ENABLE pin affects GPO E_SOL_GPO =1 the ENABLE pin does not affect GPO	E_EN_GPO
SPI FAULT - SPI fault	SPI CLOCK number is not 32	E_FSPI_GPO=0 the fault affects GPO E_FSPI_GPO =1 the fault does not affect GPO	E_FSPI_GPO
VBATP_OV - VBATP overvoltage	When battery supply pin voltage reaches overvoltage threshold	E_FVBO_GPO=0 the fault affects GPO E_FVBO_GPO =1 the fault does not affects GPO	E_FVBO_GPO
OT_VDD2/TRKx - overtemperature VDD2/TRKx regulator	When the temperature for VDD2 or TRKx regulator reaches overtemperature threshold	E_VDD2/TRK_TH_GPO=0 the fault affects GPO E_VDD2/TRK_TH_GPO =1 the fault does not affects GPO	E_VDD2/TRK_TH_GPO
VDS_FAULT - VDS fault on pump pre-driver	When the VDS comparator of pump pre-driver detects an overvoltage	E_PVDS_GPO=0 the fault affects GPO E_PVDS_GPO=1 the fault does not affect GPO	E_PVDS_GPO
Driver Fault Mask register			
TW – Solenoid thermal warning	When the temperature for each channel reaches warning threshold	E_SOL_TW_GPO=0 the fault affects GPO E_SOL_TW_GPO=1 the fault does not affect GPO	E_SOL_TW_GPO (z from 1 to 6)
COMP_TEST – Solenoid comparators self test	When the PWM check on open load comparator fails	E_SOL_COMP_GPO=0 the fault affects GPO E_SOL_COMP_GPO=1 the fault does not affect GPO	E_SOL_COMP_GPO[12]
COMP_TEST – Solenoid comparators self test	When the PWM check on lvt comparator fails	E_SOL_COMP_GPO=0 the fault affects GPO E_SOL_COMP_GPO=1 the fault does not affect GPO	E_SOL_COMP_GPO[11]
LOGIC BIST – Solenoid logic BIST	When the logic BIST ends	E_SOL_BIST_GPO=0 the fault affects GPO E_SOL_BIST_GPO=1 the fault does not affect GPO	E_SOL_BIST_GPO[10]
LOGIC BIST – Solenoid logic BIST	When the logic BIST starts or fails	E_SOL_BIST_GPO=0 the fault affects GPO E_SOL_BIST_GPO=1 the fault does not affect GPO	E_SOL_BIST_GPO[9]
ANALOG BIST – Solenoid analog BIST	When the analog self test of open load comparator fails	E_SOL_ABIST_GPO=0 the fault affects GPO E_SOL_ABIST_GPO=1 the fault does not affect GPO	E_SOL_ABIST_GPO[8]
ANALOG BIST – Solenoid analog BIST	When the analog self test of lvt comparator fails	E_SOL_ABIST_GPO=0 the fault affects GPO E_SOL_ABIST_GPO=1 the fault does not affect GPO	E_SOL_ABIST_GPO[7]
OL - Solenoid open load	When the open load is detected	E_SOL_OL_GPO_x=0 the fault affects GPO E_SOL_OL_GPOx=1 the fault does not affect GPO	E_SOL_OL_GPO
SHORT - Solenoid short to battery in HS configuration/ short to GND in LS configuration	When the short is detected	E_SOL_SHORT_GPO=0 the fault affects GPO E_SOL_SHORT_GPO=1 the fault does not affect GPO	E_SOL_SHORT_GPO
LS CLAMP	When solenoid LS active clamp is triggered	E_LSCLAMP_GPO=0 the fault affects GPO E_LSCLAMP_GPO=1 the fault does not affect GPO	E_LSCLAMP_GPO

Name	Description	Value	SPI bit
HS OVC - Solenoid overcurrent	When the HS current reaches overcurrent threshold in being turned on	E_SOL_HSOVC_GPO the fault affects GPO E_SOL_HSOVC_GPO=1 the fault does not affect GPO	E_SOL_HSOVC_GPO
LS OVC - Solenoid overcurrent	When the LS current reaches overcurrent threshold in being turned on	E_SOL_LSOVC_GPO the fault affects GPO E_SOL_LSOVC_GPO=1 the fault does not affect GPO	E_SOL_LSOVC_GPO
OT - Solenoid overtemperature	When the temperature for each channel reaches overtemperature threshold	E_SOL_OT_GPO=0 the fault affects GPO E_SOL_OT_GPO=1 the fault does not affect GPO	E_SOL_OT_GPO

12.2 GPO electrical characteristics

5.5V ≤ VBATP ≤ 19V; -40°C ≤ Tj ≤ 175°C unless otherwise noticed. All voltages refer to GND pin.

Table 47. GPO electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Power Stage							
Irev_GPO	GPO reverse current	Application note: in the application condition, no impact on other functions, no leakage from nearby pins, no reset generation	-50			mA	GPO
$R_{DS\text{-}on\ GPO}$	Low–side rdson	Tj=150°C, Iload = 50mA			17.8	Ω	GPO
$R_{DS\text{-}on\ GPO}$	Low–side rdson	Tj=175°C, Iload = 50mA			20	Ω	GPO
OUT_{lk}	Output leakage current	WAKE = VBATP= 0V, GPO = 13V			10	µA	GPO
Driver Parameters							
$t_{Turn\text{-}On\_\ GPO}$	Turn-on delay time	From command to 90% GPO pin. Load: 250Ω, 10nF			5	µs	GPO
$t_{Turn\text{-}Off\_\ GPO}$	Turn-off delay time	From command to 10% GPO pin. Load: 250Ω, 10nF			5	µs	GPO
On State Diagnostic							
IOVC	Over current threshold		70		120	mA	GPO
TFILTEROVC	Over current filtering time	Guaranteed by scan	4	6	8	µs	GPO
TFILTERdiagoff	Filtering open load and short to gnd diag. off	Guaranteed by scan	30	50	70	µs	GPO
Off State Diagnostic							
td_mask	Diagnosis mask delay after switch-off	Guaranteed by scan	300		500	µs	GPO
VHVT	Open load threshold voltage	Off state, diagnosis enabled	VOUTOPEN +160 mV		3	V	GPO
VOUTOPEN	Output open load voltage	Off state, diagnosis enabled	2.3		2.7	V	GPO
VLVT	Short-circuit to gnd threshold voltage	Off state, diagnosis enabled	1.9		VOUTOPEN -200 mV	V	GPO
IOUT_PD	Output diagnostic pull down current	Off state, diagnosis enabled, GPO = 5V	50		110	µA	GPO
IOUT_PU	Output diagnostic pull up current	Off state, diagnosis enabled, GPO = 1.5V	110	160	210	µA	GPO
Itopen	Open load threshold current		30		100	µA	GPO

12.3 GPO error handling

Table 48. **GPO error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
GPO Overcurrent	On state, LS on	GPO output switched-off and SPI **GPO OVC** fault bit (13) latched in **SERVFLT** register	On read	Automatic on SPI read
Open load (OPL)	On state, LS configuration, LS off, diagnostic enabled	Set SPI **GPO OL** (14) fault bit in **SERVFLT** register	On read	N.A.
Short to GND (STG)	On state, LS configuration, LS off	Set SPI **GPO STG** (12) fault bit in **SERVFLT** register	On read	N.A.

13 PRUN watchdog

13.1 PRUN watchdog functional description

The device integrates a window watchdog monitoring the status of PRN input signal to check micro controller activity; when the microcontroller is able to provide at PRN input pin a square wave in range of certain frequency, the watchdog fault is not triggered and RES1 signal stays high by external pull-up resistance. The WDT logic detects the only rising edge of PRN signal in PRN pin.

Figure 43. PRUN WD block diagram

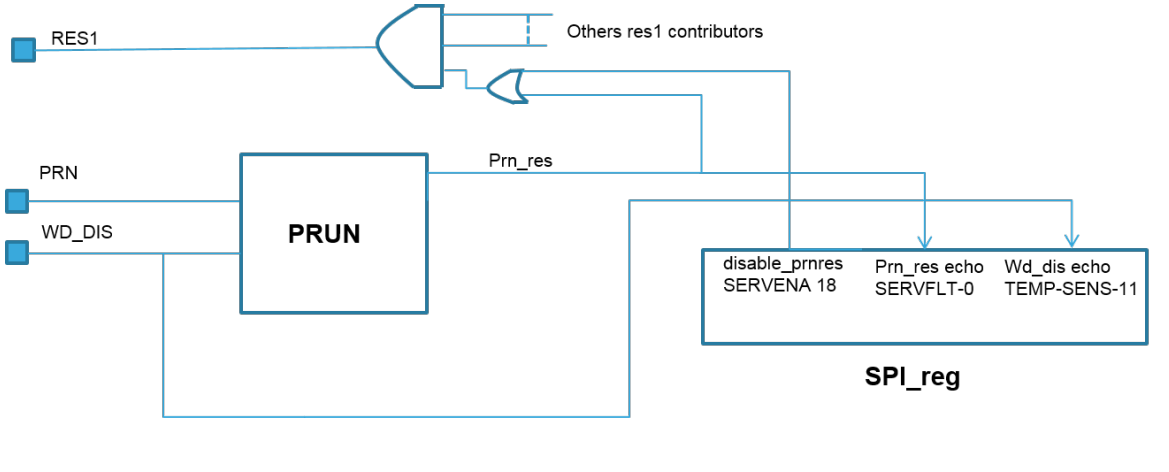
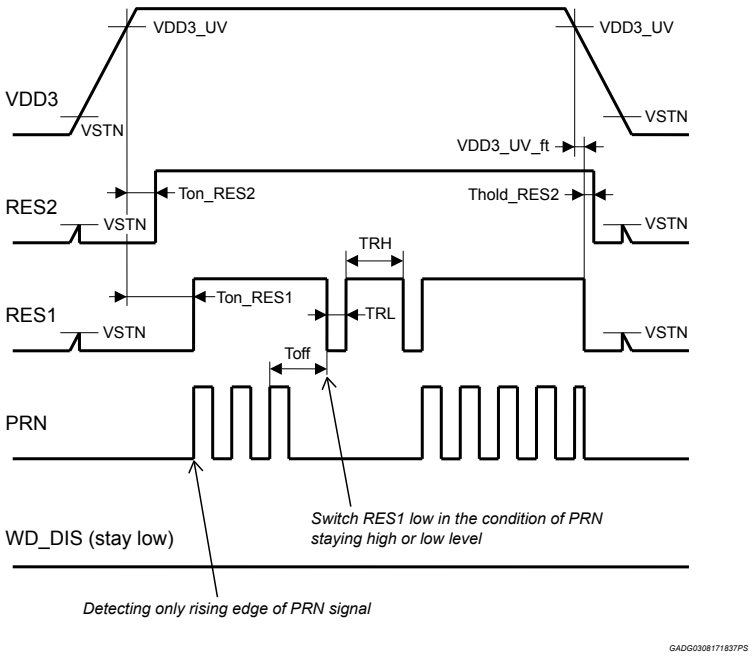
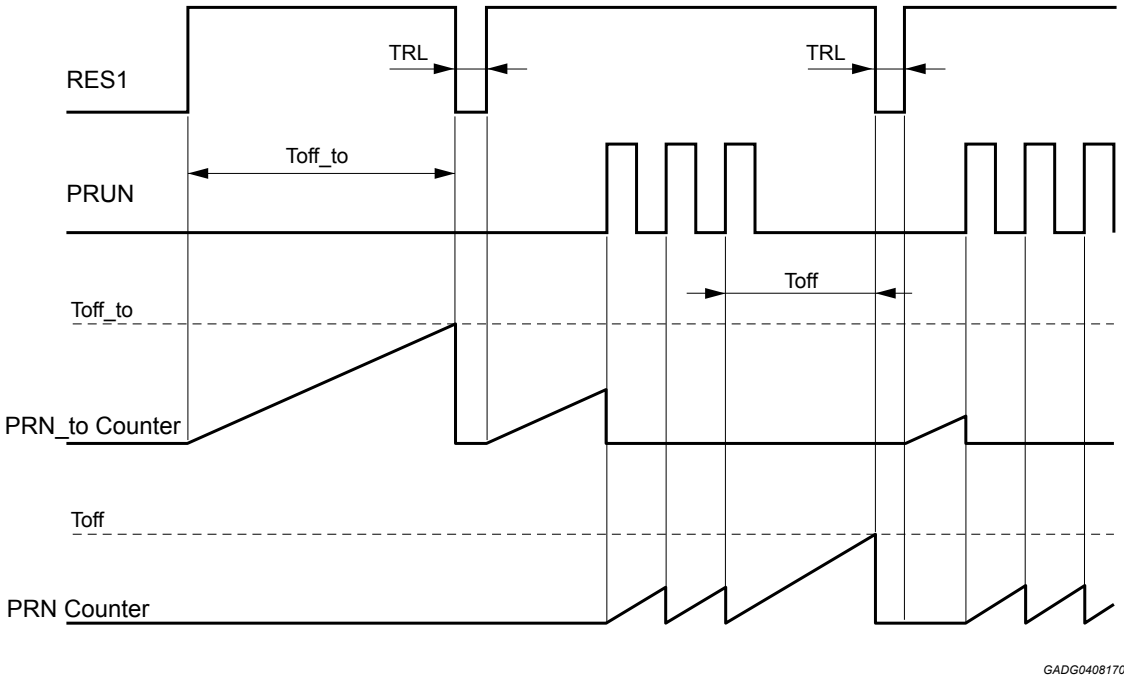


Figure 44. PRUN WD initialization



When PRN signal, on PRN pin, is missing for a timeout duration (Toff_to or Toff), a low level signal will be present on RES1 pin and a Time_out diagnostic flag is latched on Service Fault SPI register. After TRL period of time, high level signal will be present again on RES1 pin. If PRN signal continues to be missing, even after the RES1 signal returns to high, or in case a discontinuous PRN signal is provided on PRN pin, the RES1 pin is repetitively driven to low and high the above operation of turning low/high repeats frequently. RES1 generation can be masked through SPI bit in the Service Enable register to let MCU test the watchdog functionality: microcontroller may stop serving PRN pin causing watchdog fault generation without being reset in order to check the PRN functionality. At power-up of the device, after RES1 has been released, the watchdog is initialized. At start-up, in order to allow microcontroller to finish its boot sequence and starting to serve PRN pin continuously, the watchdog waits for a valid PRN pulse (Figure 47) until a time out time Toff_to; as soon as a valid PRN pulse is provided the Toff_to timing is stopped and the watchdog timer switches to nominal Toff timings. Toff_to is triggered at each RES1 rising edge, Toff is triggered at each PRN rising edge.

Figure 45. WD time-out timings at power up



PRN Watchdog can be enabled or disabled through the WD_DIS pin, internally pulled down.

In case disable mode is selected (WD_DIS = HIGH), a RES1 won't be generated even if PRN signal, on PRN pin, is missing.

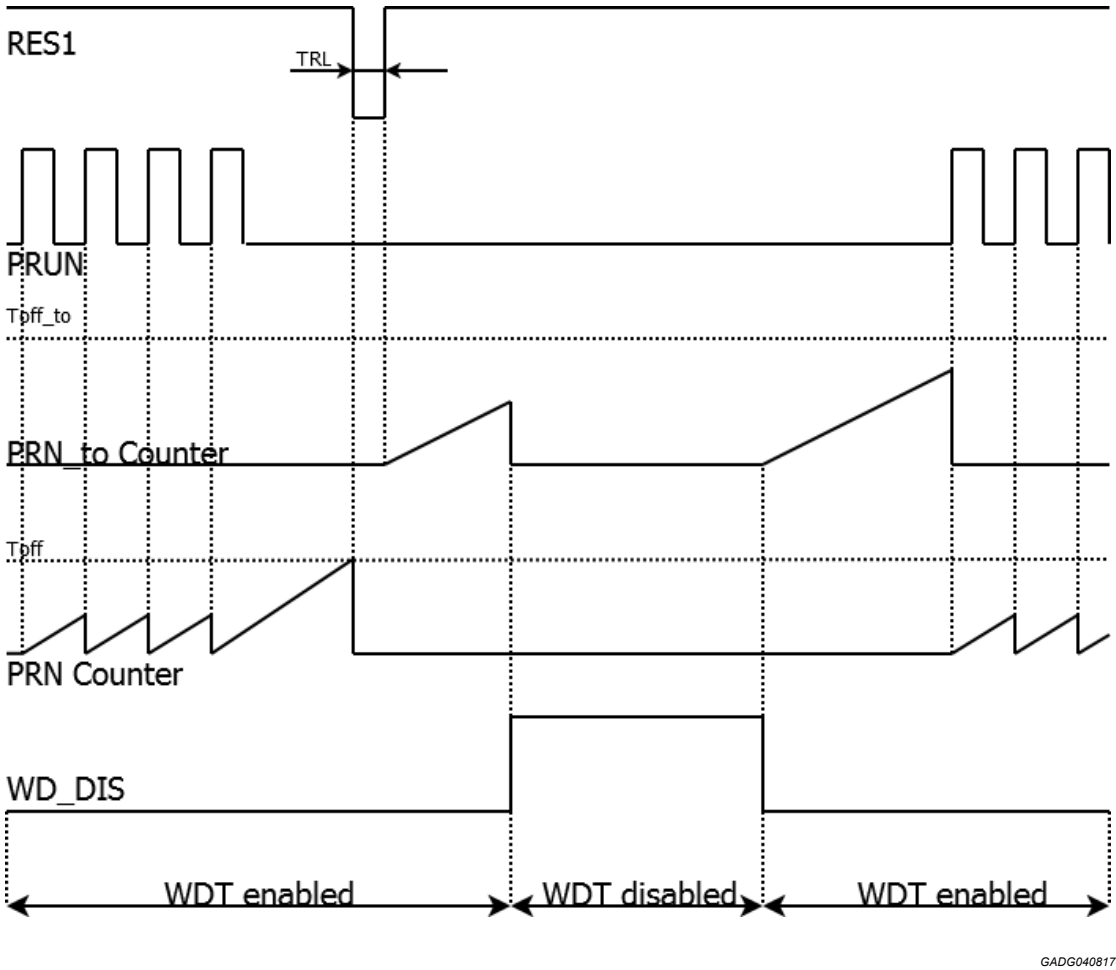
If WD_DIS pin is left open or it is pulled down to ground, PRN Watchdog is enabled.

In case disable mode is selected (WD_DIS = high), the above operation never appears even in case of no PRN signal.

An echo of WD_DIS signal is present into SPI registers to validate pin status from external.

In case no PRN signal is present at WD_DIS falling edge the watchdog starts with timeout counter as in case of RES1 release; timeout is stopped at first PRN rising edge signal.

Figure 46. **WD enable/disable function**



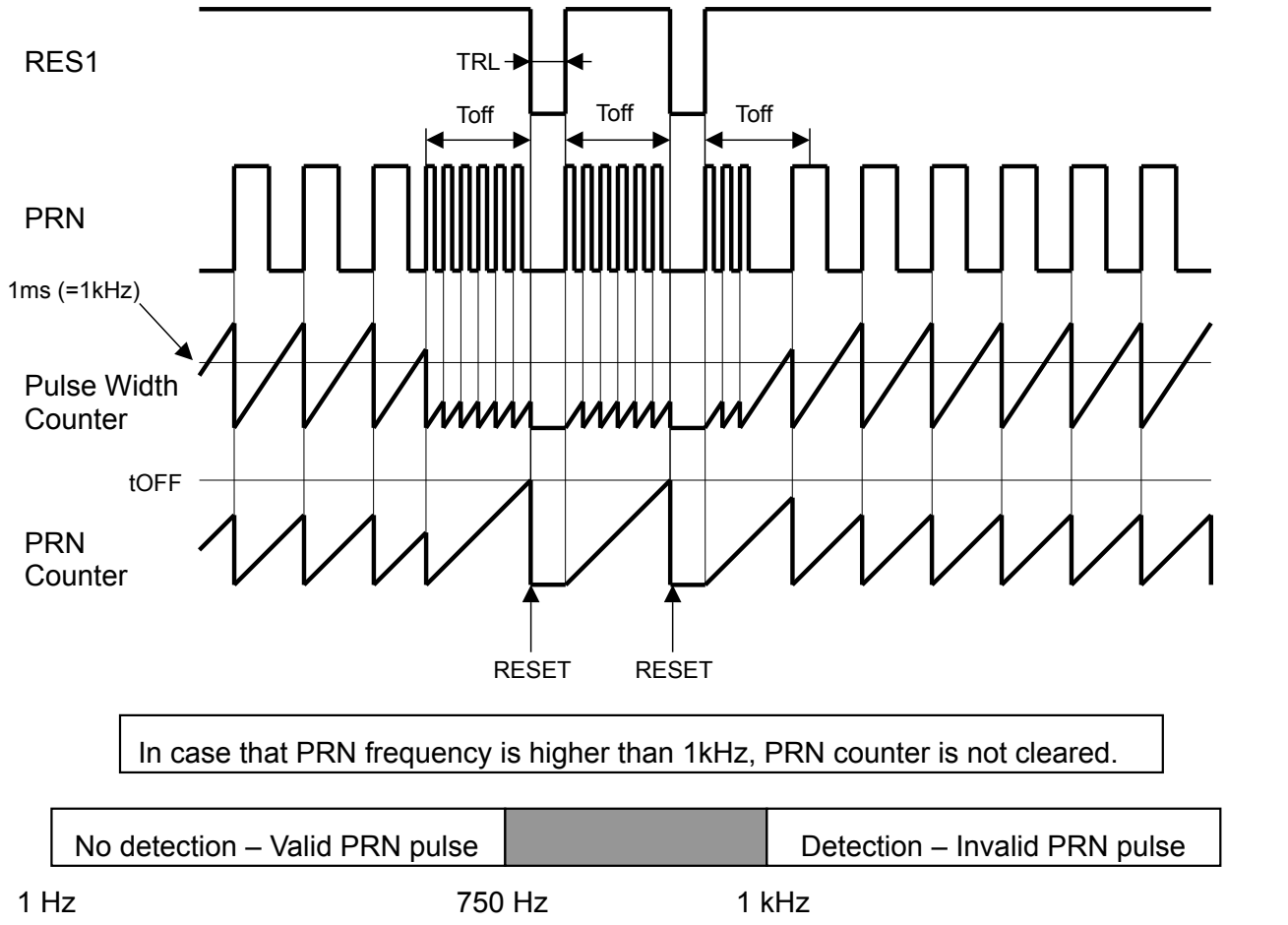
13.1.1 PRUN over frequency detection

PRUN Over Frequency Detection PRN frequency error is detected if the frequency is higher than 1 kHz and is not detected if the frequency is lower than 750 Hz. In other words, when the interval between PRN rising edges is less than 1ms, watchdog detects PRUN over frequency and not clear WDT counter. In addition, if this condition continues during Toff, RES1 pin drives low.

Table 49. **How PRN frequency effects PRUN**

PRN frequency	Effect on PRUN logic
from 0 Hz to 750 Hz	PRN width counter surely reset. No RES1 generated
from 750 Hz to 1 kHz	Gray area. No action guaranteed
from 1 kHz	PRN width counter not reset. RES1 generated

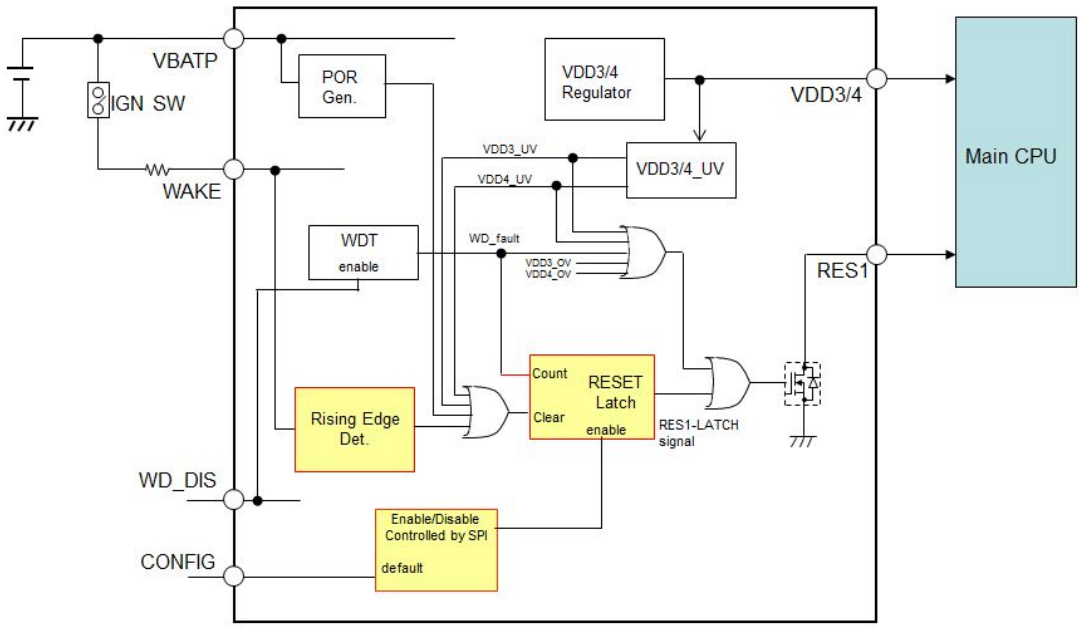
Figure 47. **WD PRUN over frequency detection**



13.1.2 Reset-Latch function

The device provides the Reset-Latch function to keep the RES1 signal at low level once 4 PRN reset event has been detected.

Figure 48. Reset latch block diagram



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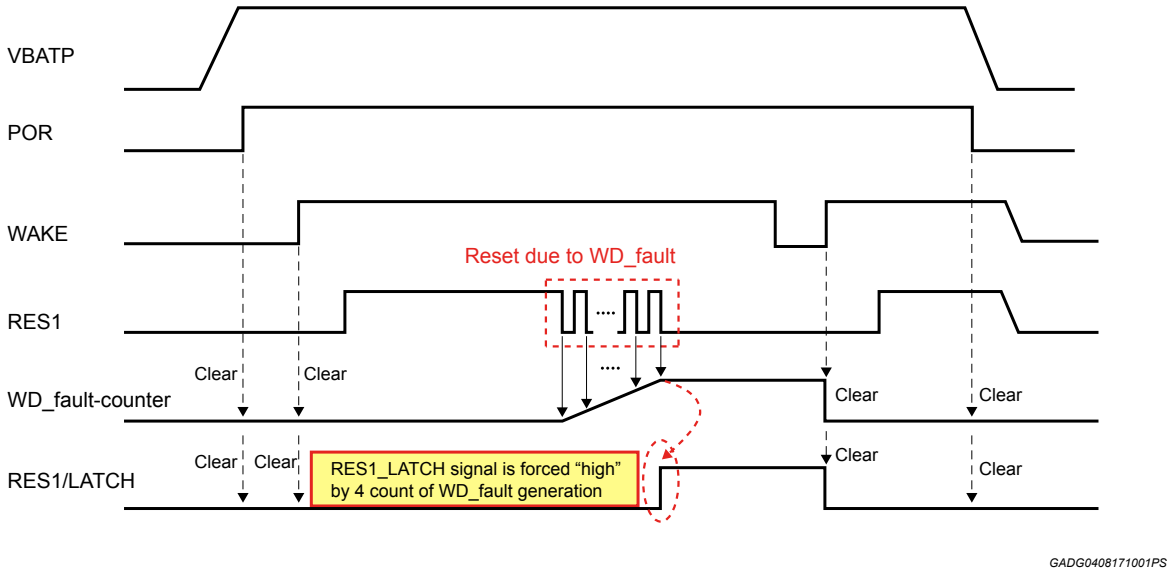
Reset-Latch function can be enabled or disabled setting bit17 (Enable Reset-Latch) in Service Enable register. Default value for bit17 after power depends on ASIC configuration pin: it is 0 (function disabled) in case CONFIG pin is high and 1 (function enabled) in case CONFIG pin is low.

If Reset-Latch function is enabled then RES1 is latched in “low” state condition after 4 counts of WD_fault generation. Watchdog fault counter can be cleared by the following events:

- PORn
- rising edge on WAKE pin
- VDD3 undervoltage
- VDD4 undervoltage.

Figure 49. **Reset-Latch timing diagram**



13.2 PRUN watchdog electrical characteristics

5.5V ≤ VBATP ≤ 19V; -40°C ≤ Tj ≤ 175°C unless otherwise noticed. All voltages refer to GND pin.

Table 50. **PRUN WD electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Input Pin							
Vil(PRN)	Low Input Voltage		-		0.75	V	PRN
Vih(PRN)	High Input Voltage		1.75			V	PRN
Ipd(PRN)	Pull-down Input Current	PRN = 5 V	10	50	100	µA	PRN
Vil(WD_DIS)	Low Input Voltage				0.75	V	WD_DIS
Vih(WD_DIS)	High Input Voltage		1.75			V	WD_DIS
Ipd(WD_DIS)	Pull-down Input Current	WD_DIS = 5 V	10	50	100	µA	WD_DIS
PRUN Timings							
Toff_to	Timeout at power up	Guaranteed by scan	230	300	370	ms	PRN
Toff	Clock off reset time	Guaranteed by scan	11		16	ms	PRN
TRL	Reset pulse low time	Guaranteed by scan	1		1.25	ms	RES1
TRH	Reset pulse high time	Guaranteed by scan	230	300	370	ms	RES1
FreqH	PRUN Over Frequency Detection	Guaranteed by scan	1			kHz	PRN

13.3 PRUN watchdog error handling

Table 51. **PRUN WD error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
PRUN Toff violation	On state	RES1 driven low for TRL if Reset-Latch disabled, stucked low otherwise, SPI register reset as described in **SPI register map**. **PRUN Watchdod Time-Out** SPI flag (0) set in **SERVFLT** register	On read	Automatic at RES1 release, SPI configuration to be reinitialized
PRUN over frequency detection	On state	Watchdog counter not reset	N.D.	N.A.

14 Q&A Watchdog

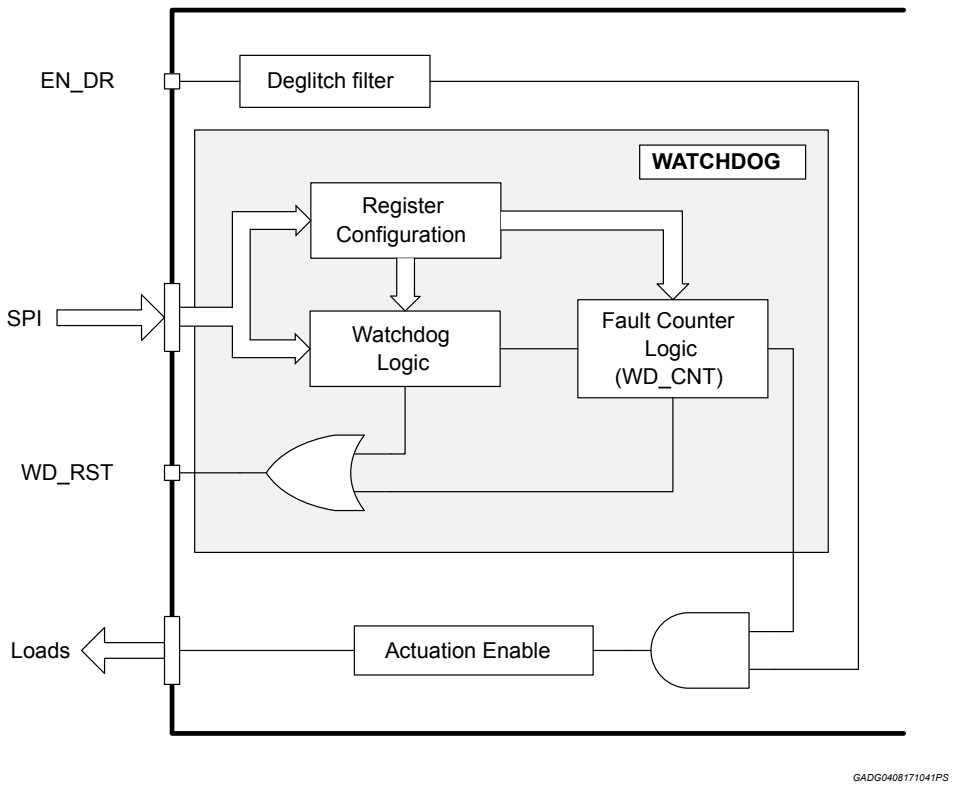
14.1 Q&A watchdog functional description

ASIC and Microcontroller exchange Queries and Answers on a defined timing base.

An internal Watchdog logic is implemented to inhibit load actuation such as to send Reset signal.

A second switch-off path, as shown in Figure 52. Bidirectional Timing check evolution, is provided to allow the Micro to force the switch off the actuation channels.

Figure 50. WD block diagram



14.1.1 Timing

Two modes of timing checks are provided:

- Monodirectional: Timing check based only on Answers. Microcontroller must send answers on a defined time window
- Bidirectional: Timings are bidirectionally checked. ASIC must receive queries on a defined time window. Microcontroller must send answers on a define time window

The selection between Mono and Bidirectional mode is possible through WD_REQ_CHECK_EN SPI register. Default configuration is Monodirectional mode. Both the Mono and Bidirectional modes require the same Q/A procedure to be controlled by the µC but:

- in Monodirectional mode the Query can be sent in the whole timing windows between 2 Answers. Only the timings between 2 consecutive answers must respect the defined timing window
- in Bidirectional mode both the Request and the Answer must be sent on a predefined timing interval.

In case time windows are not respected an error is generated.

Figure 51. Monodirectional Timing check evolution

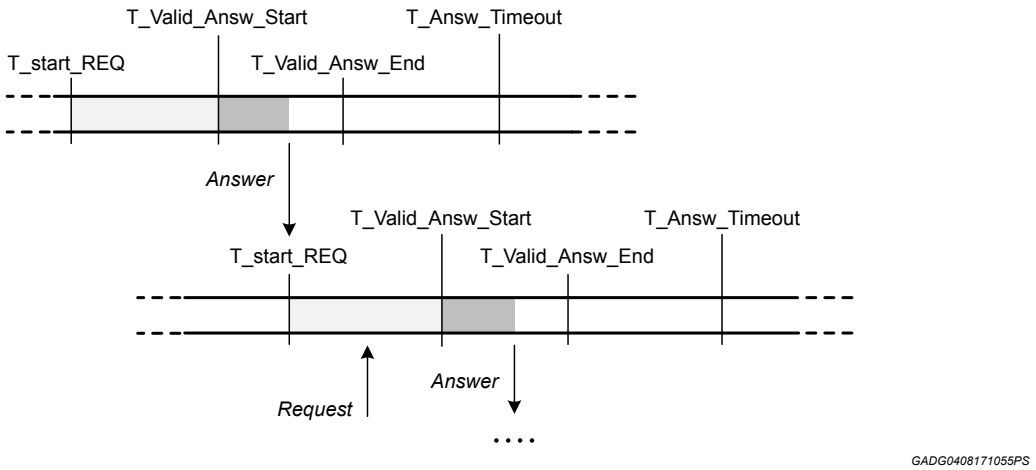


Figure 52. Bidirectional Timing check evolution

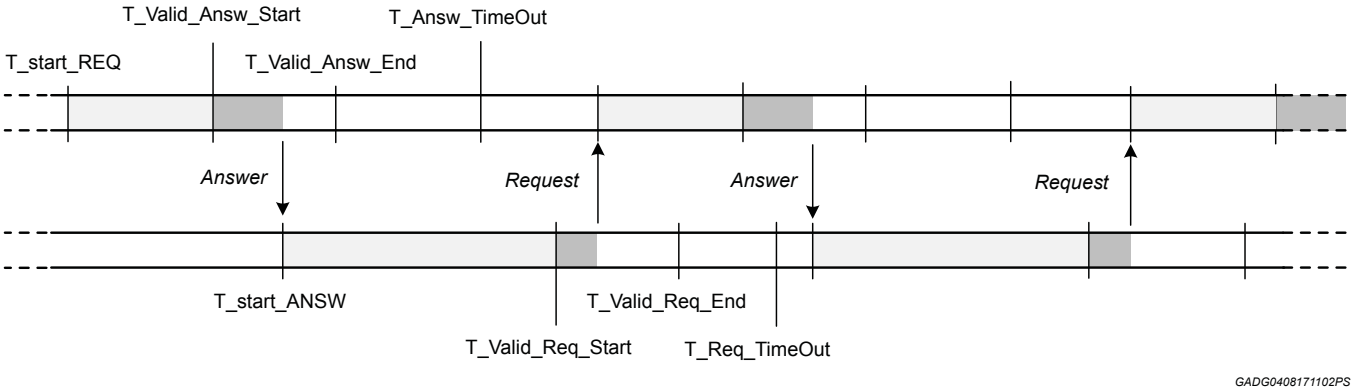


Table 52. Timing parameter legenda

Timing parameter	Description
T_start_REQ	Micro reads, through SPI register seed to elaborated
T_Valid_Answ_Start	Starting time interval for Valid answers
T_Valid_Answ_End	Ending time interval for Valid answers
T_Answ_TimeOut	Time out for answer
T_start_ANSW	Micro sends, through SPI register answer to the ASIC
T_Valid_Req_Start	Starting time interval for next following request
T_Valid_Req_End	Ending time interval for next following request
T_Req_TimeOut	Time out for request

When the Micro finishes its boot procedures, it sends the first Seed request to the device. From this moment all the timing counters start and cannot be stopped.

The Watchdog Time base is based on the WD frequency of about 250 kHz (clk_4us = SYS_CLK/64). Because of the resynchronization of the internal signals, the latency between the Answer received and the update of the WD_Cnt_value is up to 4* clk_4 µs.

The clock used for the timing windows is a divided version of clk_4us in order to obtain a timing resolution of **WD_CLK** equal to 64 µs or 256 µs depending on the **WD_CLK_DIV** settings.

Bidirectional mode

Micro must send a valid Answer inside the timing interval defined by the two SPI programmable parameters ***T_Valid_Answ_Start*** and ***T_Valid_Answ_End***. The timing window restarts after each Query received.

In case the Micro sends an Answer before ***T_Valid_Answ_Start*** or after ***T_Valid_Answ_End*** an error will be generated.

In case the **WD_TO_RST_EN** is set:

If there is no Answer before ***T_Answ_TimeOut*** elapses a WD_RST is generated, the internal **WD_RST_Cnt_Value** is incremented and the flag **WD_RST_TO_Answ** is set.

In case the **WD_TO_RST_EN** is not set:

If there is no Answer before ***T_Answ_TimeOut*** elapses, the error event counter **WD_Cnt_Value** is decreased and the device starts to wait again for the Answer with the same timing procedure. The WD_FSM is on the “Wait for answer after an Error” state, the status register **WD_FSM_Status** = “11”. When the Micro sends the answer to the device (T_start_ANSW) the WD_REQ_TMR timer starts to count.

Micro must send a new seed request inside the timing interval defined by the two SPI programmable parameters ***T_Valid_Req_Start*** and ***T_Valid_Req_End***. The timing window restarts at each Answer received.

In case the Micro sends the request before ***T_Valid_Req_Start*** or after ***T_Valid_Req_End*** an error is generated.

In case the **WD_TO_RST_EN** is set:

If there is no request before ***T_Req_TimeOut*** elapses a WD_RST is generated, the internal **WD_RST_Cnt_Value** is incremented and the flag **WD_RST_TO_Req** is set.

In case the **WD_TO_RST_EN** is not set:

If there is no request before ***T_ Req _TimeOut*** elapses, the error event counter **WD_Cnt_Value** is decreased and the device starts to wait again for the request with the same timing procedure. The WD_FSM is on the “Wait for query after an Error” state, the status register **WD_FSM_Status** = “11”. When the Micro sends the request to the device, the WD_ANSW_TMR timer starts to count.

Monodirectional mode

Micro must send a valid Answer inside the timing interval defined by the two SPI programmable parameters ***T_Valid_Answ_Start*** and ***T_Valid_Answ_End***. The first timing window starts after the first Query received. The timing window restarts at each Answer received.

In case the Micro sends an answer before ***T_Valid_Answ_Start*** or after ***T_Valid_Answ_End*** an error will be generated.

If there is no Answer before ***T_Answ_TimeOut*** elapses the same procedure as for bidirectional mode (reset/”Wait for answer after an Error” depending on the **WD_TO_RST_EN setting**)is performed.

Micro must send a new seed request inside the timing window between two answers.

If there is no request before ***T_Answ_TimeOut*** elapses the same procedure as for the bidirectional mode (reset/”Wait for query after an Error” depending on the **WD_TO_RST_EN setting**) is performed.

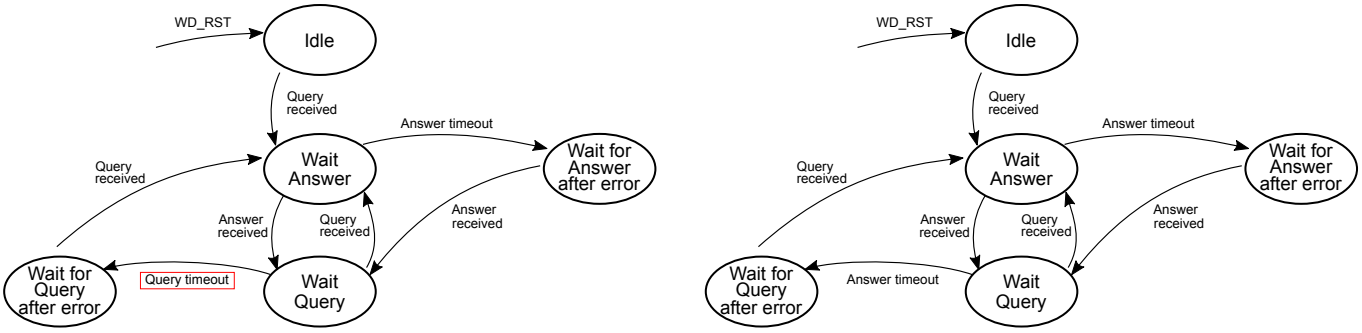
14.1.2 Watchdog states evolution

ASIC starts the WD evolution state machine (WD_FSM) in IDLE mode where it is waiting for the first seed request from micro through SPI.

In this way the starting period is completely under the control of the Micro allowing to safely concluding boot procedure before starting the WD seed request/answer mechanism. During this period WD configuration registers can be programmed. The first seed request acts as a WD state machine start. After this event the WD never stops and WD configuration registers become locked. A safety mechanism based on a “un-lock 20 bits key” prevents to modify the configuration registers while the Q/A algorithm is running. The unlock procedure is described in the SPI register paragraph.

WD_CNT is a 4 bit counter used to collect Good and Bad answer furnished by the Micro as reaction of Seeds sent.

Figure 53. **WD FSM evolution. WD_TO_RST_EN =0**



Bidirectional mode

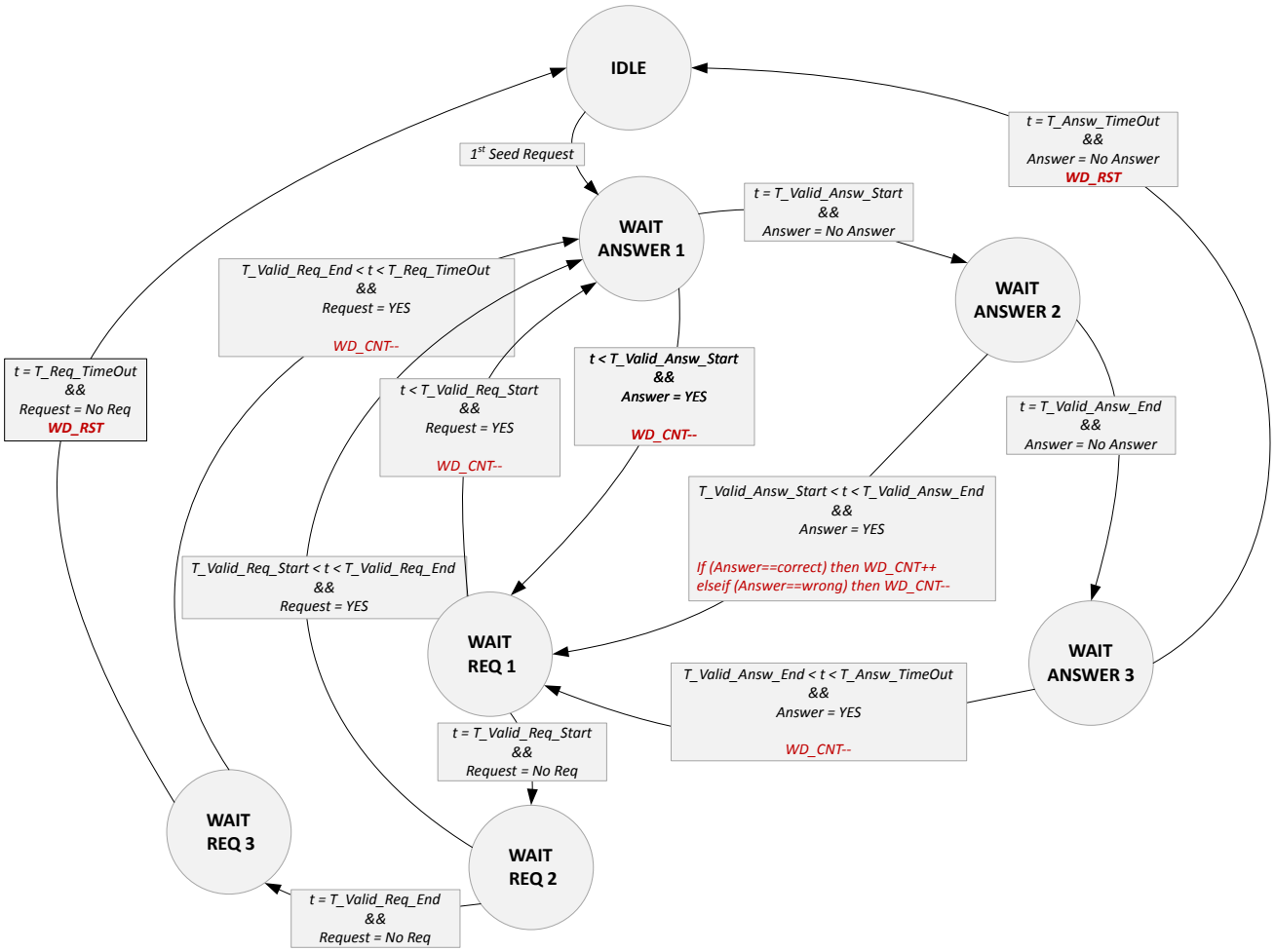
Monodirectional mode

Figure 54. **WD FSM evolution. WD_TO_RST_EN = 1**

Bidirectional mode

Monodirectional mode

Figure 55. State evolution in case of WD_TO_RST_EN=1



Depending on the value of the WD_CNT counter the ASIC stops the actuation, sends the WD_RST or performs the actuation.

The WD_CNT is incremented, by a number of steps as defined through the SPI configurable parameter ***WD_cnt_good_step***, when a correct answer is given in the right time interval.

In all the other cases, as defined in the WD state machine (Figure 56), the WD_CNT is decremented by a number of steps as defined through the SPI configurable parameter ***WD_cnt_bad_step***.

If WD_CNT reaches the value of zero:

- An internal WD_RST is generated, the ***WD_RST_Cnt_Value*** is updated and the ***WD_Cnt_Flag*** is set.
- the WD FSM stops and moves to its initial state (IDLE) waiting for a new Query for restarting
- the freeze on the configuration registers is removed
- the drivers are disabled, to have the device in a safe condition
- If ***WD_RST_EN*** is set to 1 then a WD_RST will be sent by the ASIC

Two different thresholds are defined (both programmable through SPI): ***WD_th_low*** and ***WD_th_high.***

If WD_CNT value is lower than ***WD_th_low***, but greater than zero, there will be no actuation (Solenoid Channels, Motor Pump, Fail Safe and GPO are impacted) such as any WD_RST.

If WD_CNT is greater than ***WD_th_low*** and lower than ***WD_th_high*** the load actuation is managed in hysteresis mode:

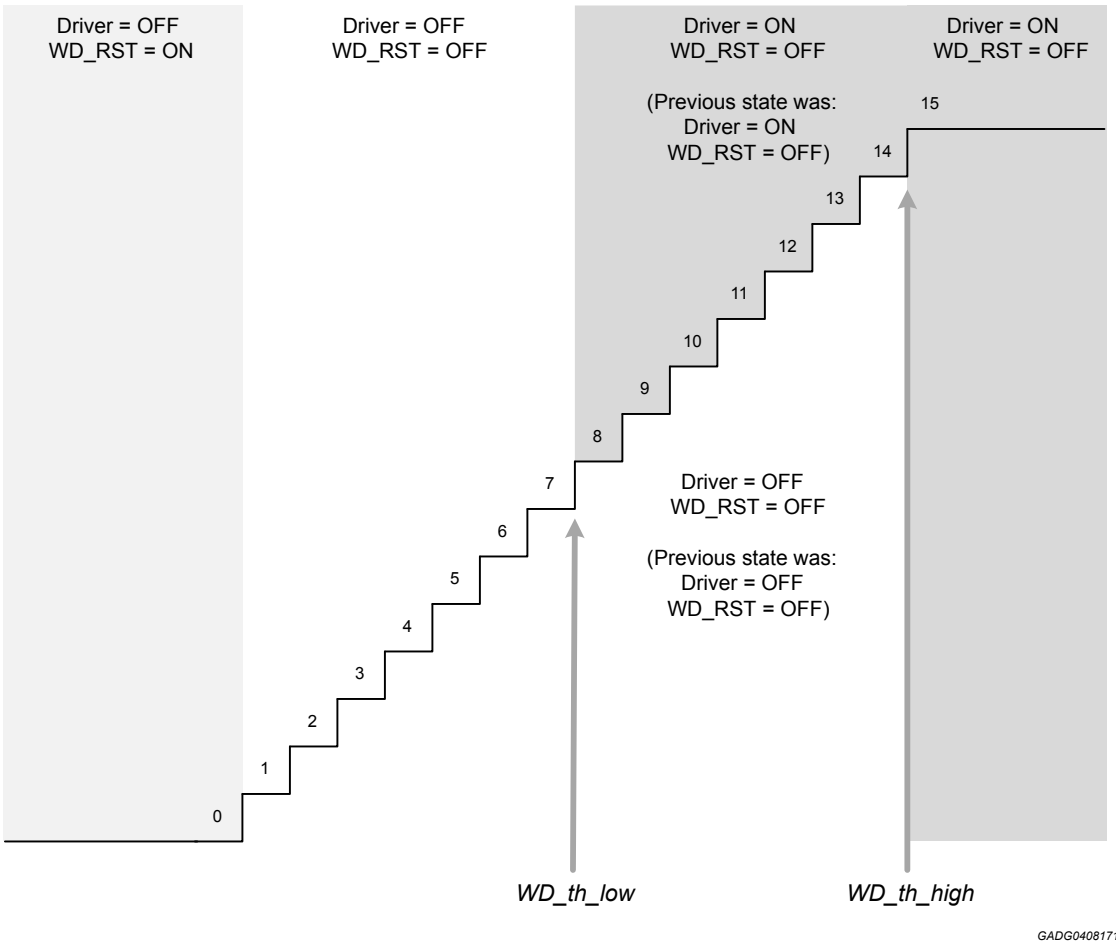
If actuation is ON (Solenoid Channels, Motor Pump, Fail Safe and GPO are impacted) it will be stopped only when WD_CNT becomes lower than ***WD_th_low***, while if actuation was OFF it will be performed only when WD_CNT becomes equal to ***WD_th_high*** and only when WD_CNT exceeds this threshold loads are actuated.

In this way, actuation of loads can be performed only if the WD has been started and a certain number of good Request/Answer has been exchanged.

In any case, WD_CNT will be saturated when WD_CNT = ***"1111"***.

When the WD algorithm is not active (FSM is in IDLE) the WD_CNT = WD_th_low.

Figure 56. Driver actuation and WD_RTS versus WD_CNT value



All the status information is stored onto the ***WD_Status_reg***, readable through SPI. This register will be cleaned as consequence of each read operation.

In case a WD_RST is generated, the ASIC restarts the WD evolution state machine in IDLE mode waiting for the seed request from micro through SPI. WD configuration registers are preserved but can be modified by the micro before starting the WD mechanism.

In the same way, also the status register, ***WD_Status_reg***, is preserved and can be read through SPI.

14.1.3 Out Of Sequence error cases

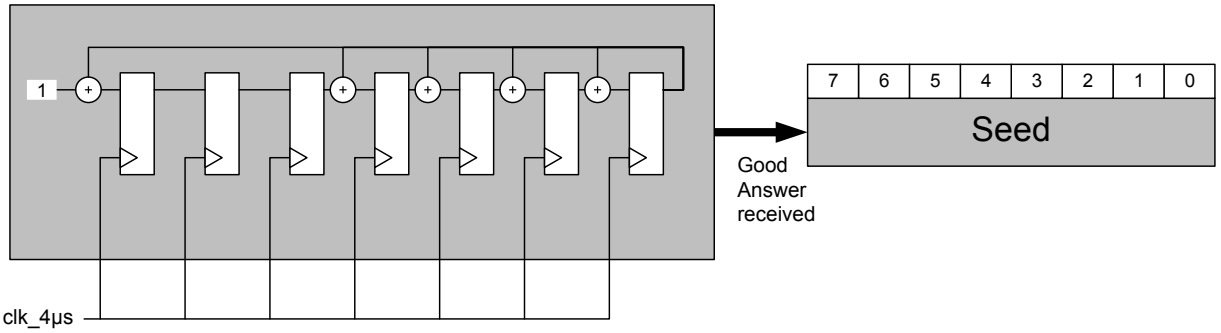
Two cases of unexpected errors have been identified:

- If a request of a new seed arrives to the ASIC before the previous answer received, the ASIC serves the new request, sending the old Seed decreasing the value of WD_CNT by the amount ***WD_cnt_bad_step***.
- If an answer arrives to the ASIC before a new request and after another answer, the ASIC ignores this answer but it decreases the value of WD_CNT by the amount ***WD_cnt_bad_step***.

14.1.4 Seed generation and answer check

Seeds are 8-bits wide word generated an LSFR pseudo-random algorithm. A new seed is generated and sent onto an SPI word, ***WD_Seed***, each time a new Seed request, T_start_REQ, is sent to the ASIC.

Figure 57. Seed generation algorithm block diagram



Seed is generated by freezing the 8-bits wide free running LSFR, running at a WD_clk clock period, each T_start_REQ event.

As described in Figure 57, seed is generated by the LSFR algorithm. At each clock period (4 µs clock) the new seed is generated According to the LSFR algorithm. A new seed is stored onto the WD_Seed only in case of a correct answer received. In case of an error, the same seed is available onto the WD_Seed until a correct answer is received.

Figure 58. Seed selection and elaboration flow

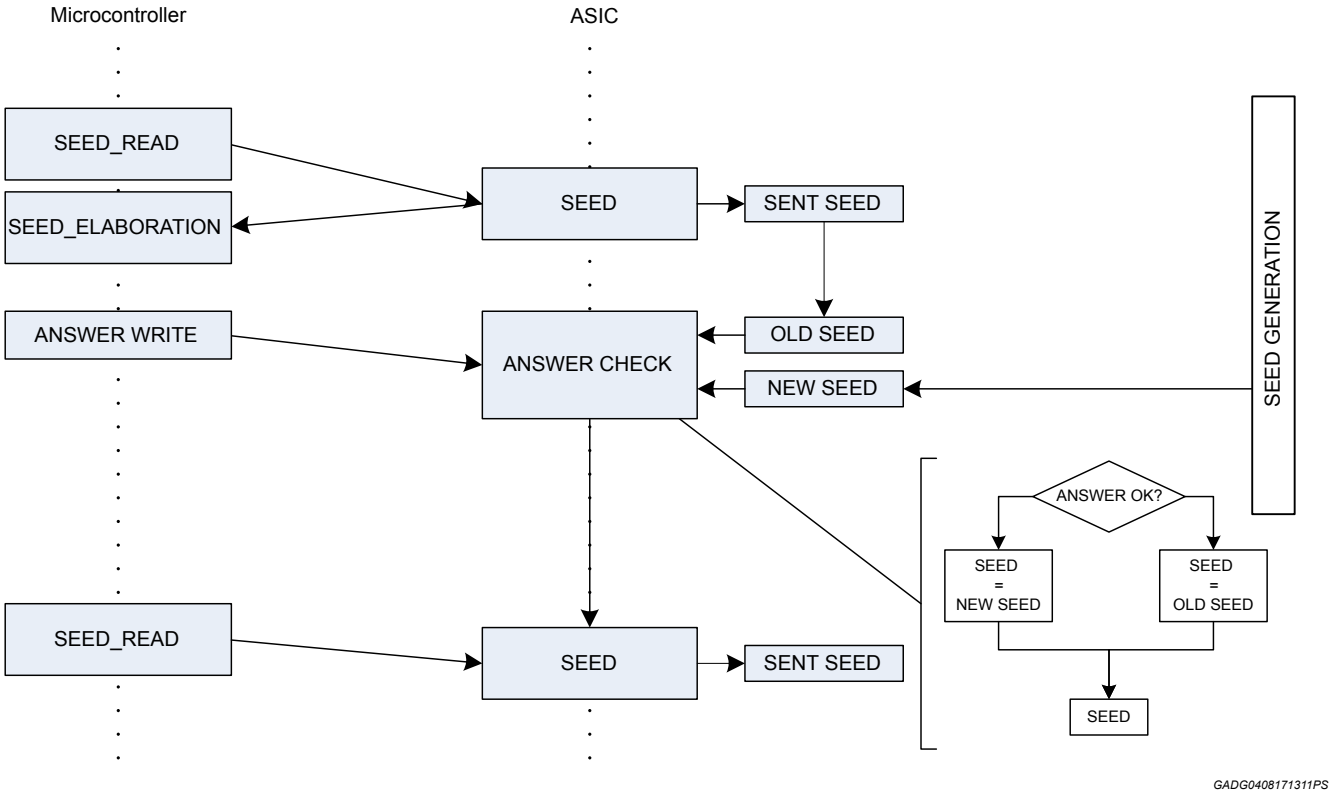
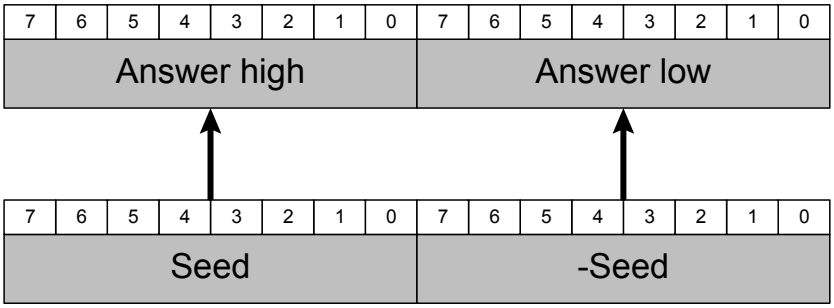


Figure 59. **Answer check generation algorithms block diagram**



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The answer is a 16-bits wide word checked against a 16-bits word composed by two bytes, Answer_Low and Answer_High, generated from the seed sent.

Answer_Low is the logical 2's complement of the seed while Answer_High is a replica of the seed sent.

14.2 Q&A watchdog SPI registers

When a Read operation is performed, a new seed is sent and the read is treated as a new Seed request. When an Answer write is not treated as a new Seed request and the seed related to that answer is sent back.

14.2.1 Register unlock procedure

All the SPI parameters can be programmed before the WD mechanism starts. After the first seed request, the registers are locked to prevent from unexpected modification by the µC.

To modify the register, µC must send an unlock key. After the key is received a register can be modified. After the first SPI write access (to any address) received after the Unlock key, registers are automatically locked.

Unlock_Cmd = 20'h0f0f0

Example of unlock usage: To change the WD Req Timings and Answ Timing while WD is working

WD is running → All the WD config registers are locked
Unlock_Cmd is received → Lock is removed
Write Access to WD Req Timing register → WD Req Timing updated
→ All the WD config registers are automatically locked
Unlock_Cmd is received → Lock is removed
Write Access to WD Answ Timing register → WD Ans Timing updated
→ WD config registers are automatically locked

15 CAN Interface

15.1 CAN interface functional description

The CAN interface main features are the following:

- Compatible to the ISO 11898-2 standard
- Communication speed up to 1 Mbit/s
- Function range from -18 V to +40 V DC at CAN pins
- GND disconnection fail safe at module level
- GND shift operation at system level
- Microcontroller interface with CMOS compatible I/O Pins.
- Matched output slopes and propagation delay
- Receive-only mode available

In order to further reduce the current consumption in standby mode, the integrated CAN bus interface offers an ultra low current consumption.

15.1.1 CAN error handling

At V33_DIG > PORn threshold (internal power on reset), the CAN transceiver is enabled. CAN transmitter is supplied by a dedicated pin (CANVDD) to avoid disturbances of CAN activity on main supply lines. The CAN transmitter is disabled only in case of the following errors:

- Dominant TxDC timeout
- CAN permanent recessive
- RxDC permanent recessive
- Thermal shutdown TSD_VDD1
- WD reset

The CAN receiver is not disabled in case of any failure condition.The device provides the following 4 error handling features; the CAN error handling function can be disabled by setting a proper SPI bit.

Dominant TxDC Timeout

If TXDC is in dominant state (low) for t > $t_{TXDC\_DOM\_TO}$ the transmitter is disabled, status bit is latched and cleared by SPI read. The transmitter remains disabled until the status register is cleared.

CAN Permanent Recessive

If TXDC changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter is disabled, status bit is latched and cleared by SPI read. The transmitter remains disabled until the status register is cleared.

CAN Permanent Dominant

If the bus state is dominant (low) for t > $t_{CAN\_DOM\_TO}$ a permanent dominant status is detected. The status bit is latched and cleared by SPI read. The transmitter is not disabled.

RXDC Permanent Recessive

If RXDC Pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXDC does not follow TXDC for 4 times the transmitter is disabled. The status bit is latched and can be cleared by SPI read. The transmitter remains disabled until the status register is cleared.

15.1.2 Wakeup (from CAN)

When the device is in standby mode, with CAN wake up option enabled, the CAN bus traffic is detected. For the wake up feature the device logic differentiates different conditions. When the device is in standby mode, with CAN wake up option enabled, the CAN bus traffic is detected. For the wake up feature the device logic differentiates between the following conditions.

Normal pattern wakeup

Normal pattern wakeup can occur when CAN pattern wakeup option is enabled and the CAN transceiver was set in standby mode while CAN bus was in recessive (high) state or dominant (low) state. In order to wake up the device, the following criteria must be fulfilled:

- The CAN interface wakeup receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than 2 µs
- The distance between 2 pulses must be longer than 2 µs.
- The two pulses must occur within a time frame of 1.0 ms

Wake up from short to GND condition

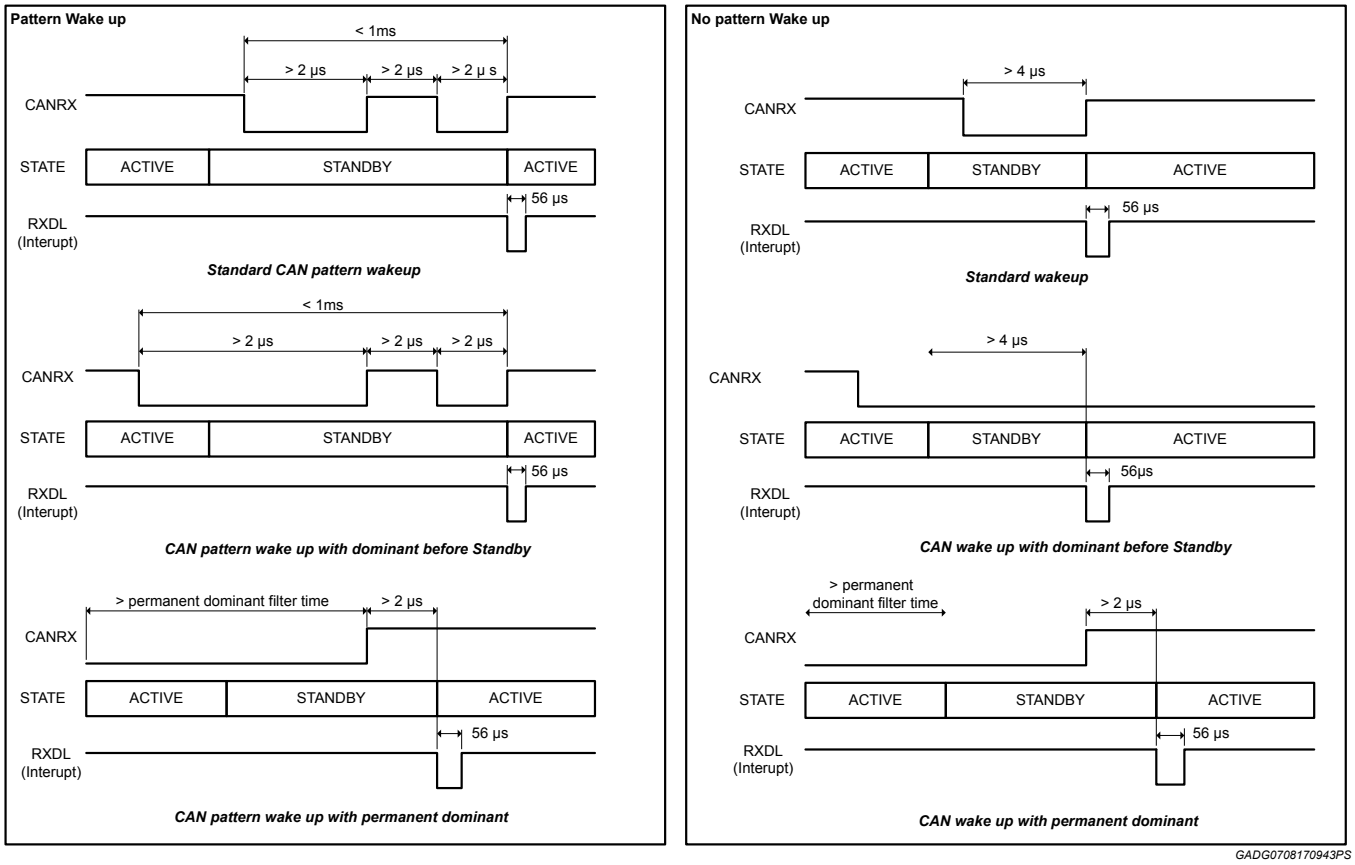
Even if CAN pattern wake up option is enabled, but the CAN transceiver was set in standby mode after a qualified permanent dominant state, recessive level at CAN switches the device to active mode.

No pattern wakeup

If the CAN pattern wakeup option is disabled, any transition either dominant (low) state to recessive (high) state or recessive (high) state to dominant (low) state switch the device to active mode (after a filtering time of tWUF).

Note: A wakeup caused by a message on the bus starts the voltage regulator and the microcontroller switches the application back to normal operation mode.

Figure 60. CAN wake up capabilities



15.1.3 CAN Sleep Mode

During active mode it is possible to deactivate the CAN transceiver with a dedicated SPI command. The CAN transceiver remains deactivated until it is activated again. With a deactivated CAN the receiver input termination network is disconnected from the bus and the CANH, CANL bus lines are driven to GND.

15.1.4 CAN receive-only mode

With a configuration bit in control register it is possible to disable the CAN transmitter in active mode. In this mode it is possible to listen to the bus but not sending to it. The receiver termination network is still activated in this mode. The same effect can be obtained driving high the CAN_DIS pin.

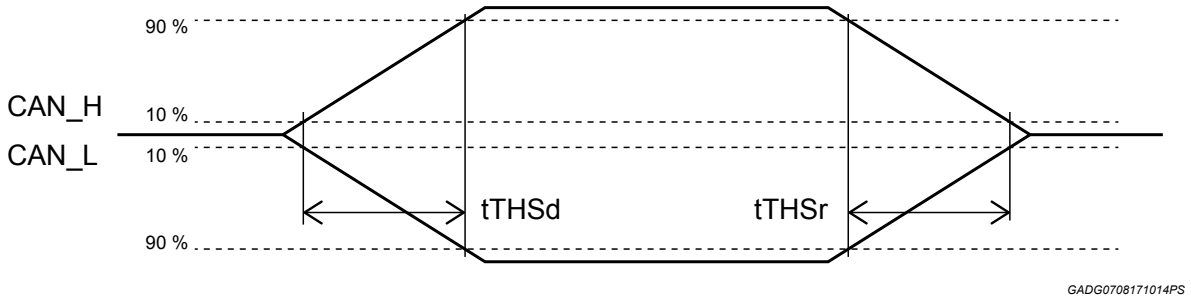
15.1.5 CAN looping mode

If the proper configuration bit in control register is set the TxDC input is mapped directly to the RxDC Pin. This mode can be used in combination with the CAN receive-only mode, to run diagnosis for the CAN protocol handler of the microcontroller.

15.1.6 CAN disable

CAN transmitter can be disabled through a dedicated pin active high. In this mode it is possible to listen to the bus, but not sending to it. The receiver termination network is still activated in this mode (same as CAN Receive-only Mode)

Figure 61. CAN transition time



15.2 CAN electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 4.8 V ≤ CANVDD ≤ 5.2 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin.

Table 53. CAN electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Input Pin							
VTXDCLOW	Input voltage dominant threshold	Active mode			0.75	V	TXD
VTXDCHIGH	Input voltage recessive threshold	Active mode	1.75			V	TXD
VTXDCHYS	VTXDCHIGH-VTXDCLOW	Active mode	0.2	0.4		V	TXD
RTXDCPU	TXDC pull up resistor	Active Mode, Pull-up to internal logic supply	10		60	µA	TXD
Vil(CAN_DIS)	Low Input Voltage				0.75	V	CAN_DIS
Vih(CAN_DIS)	High Input Voltage		1.75			V	CAN_DIS
Ipd(CAN_DIS)	CAN_DIS pull-down	CAN_DIS = 5V	10	50	100	µA	CAN_DIS

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Output Buffer							
VRXDCLOW	Output voltage dominant level	Active mode, ILOAD = 1 mA		0.2	0.5	V	RXD
VRXDCHIGH	Output voltage recessive level	Active mode, ILOAD = 1 mA	VDDIO - 0.5	VDDIO - 0.2		V	RXD
CAN Transmitter And Receiver Parameters							
VCANHDOM	CANH voltage level in dominant state	Active mode; VTXDC=VTXDCLOW; RL = 60 Ω, RL = 50 Ω	2.75		4.5	V	CANH
VCANLDOM	CANL voltage level in dominant state	Active mode; VTXDC=VTXDCLOW; RL=60 Ω, RL=50 Ω	0.5		2.25	V	CANL
VDIFFODOM	Differential output voltage in dominant state: VCANHDOM - VCANLDOM	Active mode; VTXDC=VTXDCLOW; RL=60 Ω , RL=50 Ω	1.5		3	V	CANH, CANL
VCM	Driver symmetry: VCANHDOM + VCANLDOM	Active mode; VTXDC=VTXDCLOW; RL=60 Ω ;	0.9* CANVDD	CANVDD	1.1* CANVDD	V	CANH, CANL
VCANHREC	CANH voltage level in recessive state	Active mode; VTXDC=VTXDCHIGH; No Load	2	2.5	3	V	CANH
VCANLREC	CANL voltage level in recessive state	Active mode; VTXDC=VTXDCHIGH; No Load	2	2.5	3	V	CANL
VCANHRECLP	CANH voltage level in recessive state (Low Power mode)	Stby mode, CONFIG=16 V; VTXDC=VTXDCHIGH; No Load	-0.1	0	0.1	V	CANH
VCANLRECLP	CANL voltage level in recessive state (Low Power mode)	Stby mode, CONFIG=16 V; VTXDC=VTXDCHIGH; No Load	-0.1	0	0.1	V	CANL
VDIFFOREC	Differential output voltage in recessive state: VCANHREC - VCANLREC	Active mode; VTXDC=VTXDCHIGH; No Load	-50		50	mV	CANH, CANL
VDIFFORECLP	Differential output voltage in recessive state (Low Power mode): VCANHREC - VCANLREC	Stand-by mode, CONFIG=16V; VTXDC=VTXDCHIGH; No Load	-50		50	mV	CANH, CANL
VCANHLCM	Common mode bus voltage	Measured with respect to the ground of each CAN node, design info	-12		12	V	CANH, CANL
IOCANHDOM	CANH output current in dominant state	Active mode; VTXDC=VTXDCLOW; VCANH=0V	-100	-75	-45	mA	CANH
IOCANLDOM	CANL output current in dominant state	Active mode; VTXDC=VTXDCLOW; VCANL=5 V	45	75	100	mA	CANL
ILEAK	Input leakage current	Unpowered device; VBUS=5 V			250	µA	CANH, CANL
RIN	Internal resistance	Active mode & Stby mode, CONFIG=16 V; VTXDC=VTXDCHIGH; No Load	20	34	50	kΩ	CANH, CANL

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
RIN_MATCH	Internal resistor matching CANH,CANL	Active mode & Stand-by mode, CONFIG=16V; VTXDC=VTXDCHIGH; No Load RIN(CANH) – RIN(CANL)			3	%	CANH, CANL
RIN_DIFF	Differential internal resistance	Active mode & Stand-by mode, CONFIG=16 V; VTXDC=VTXDCHIGH; No Load	40	68	100	kΩ	CANH, CANL
CIN	Internal capacitance	Guaranteed by design		20	50	pF	CANH, CANL
CIN_DIF	Differential internal capacitance	Guaranteed by design		10		pF	CANH, CANL
VTHDOM	Differential receiver threshold voltage recessive to dominant state	Active mode			0.9	V	CANH, CANL
VTHDOMLP	Differential receiver threshold voltage recessive to dominant state (low power mode)	Stby mode, CONFIG = 16 V			1.15	V	CANH, CANL
VTHREC	Differential receiver threshold voltage dominant to recessive state	Active mode	0.5			V	CANH, CANL
VTHRECLP	Differential receiver threshold voltage dominant to recessive state (low power mode)	Stby mode, CONFIG=16 V	0.2			V	CANH, CANL
CAN Transmitter Timings							
tTxPD_HL	Propagation delay TXDC to RXDC (High to Low)	Active mode; 50%VTXDC to 50% VRXDC; CRXDC=100 pF; RL = 60 Ω	0		255	ns	CANH, CANL
tTxPD_LH	Propagation delay TXDC to RXDC (Low to High)	Active mode; 50%VTXDC to 50% VRXDC; CRXDC = 100 pF; RL = 60 Ω	0		255	ns	CANH, CANL
tWUF	Wake up filter time	Guaranteed by scan	0.5		5	µs	CANH, CANL
tTXDC_DOM_TO	TXDC dominant time-out	Guaranteed by scan	800		1280	µs	CANH, CANL
tCAN_DOM_TO	CAN permanent dominant time-out	Guaranteed by scan	800		1280	µs	CANH, CANL
tTHSd	State transition time	Measured between 10% to 90%	10	64	80	ns	CANH, CANL
tTHSr	State transition time	Measured between 10% to 90%	10	16	80	ns	CANH, CANL

15.3 CAN error handling

Table 54. **CAN error handling**

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
TX permanent dominant	On state, Error Handling enabled	Transmitter disabled and error flag **CAN DOMINANT TX TO** (16) set in **TRKFAULT** register	On read	Automatic after fault is cleared
CAN permanent recessive	On state, Error Handling enabled	Transmitter disabled and error flag **CAN PERMANENT REC** (17) set in **TRKFAULT** register	On read	Automatic after fault is cleared
CAN permanent dominant	On state, Error Handling enabled	Error flag **CAN PERMANENT DOM** (18) set in **TRKFAULT** register	On read	N.A.
RX permanent recessive	On state, Error Handling enabled	Transmitter disabled and error flag **CAN RX PERMANENT REC** (19) set in **TRKFAULT** register	On read	Automatic after fault is cleared

16 SPI interface and register mapping

16.1 SPI functional description

The SPI interface is used to configure the device, control the outputs and read the diagnostic and status registers.
The SPI interface comprises of:

- Supply: VDDIO
- Inputs: SCLK, SDI, CS
- Output: SDO

The SPI Frame is hereafter described:

Figure 62. SPI Frame

SDI Frame (from Master SPI)				SDO Frame (to Master SPI)			
31	Wr/Rdn	15	Data Bit[12:0]	31	Short Frame Error	15	Data Bit[12:0]
30	Add[6:0]	14		30	Long Frame Error	14	
29		13		29	CRC Error	13	
28		12		28	Channel Exceptions[5:0]	12	
27		11		27		11	
26		10		26		10	
25		9		25		9	
24		8		24		8	
23	Reserved = 0	7		23		7	
22	Data[19:13]	6		22	Data[19:13]	6	
21		5		21		5	
20		4		20		4	
19		3		19		3	
18		2	CRC[2:0]	18		2	CRC[2:0]
17		1		17		1	
16		0		16		0	

CRC error and frame length error are reported on SDO of the frame following the corrupted one.

16.1.1 SPI protocol

The SPI protocol is defined by frames of 32bits with 3 bits of CRC (Cyclic Redundancy Check) both input and output directions. SDI frame includes 7 bit address and 20 bit data, SDO frame includes channel exception field for diagnostic status immediate capture. SPI implements In-Frame protocol for data out management.

16.1.2 CRC field

UAL3 SPI frame (upstream/downstream) include a 3 bit CRC field. CRC field is evaluated/checked by using 3° degree poly $G_3(x) = x^3+x+1$. In case CRC error is detected the fault is output in the following SPI frame, if the CRC fault is flagged it means the previous frame is considered invalid and no write operation or clear operation is performed.

16.1.3 Channel exception field details

SDO frame has 6 bits reserved for solenoid channel exceptions, each bit is dedicated to the corresponding channel and it is the OR of all the recorded exceptions.

In this way, it is always possible to detect a failure happening on each solenoid channel during every SPI communication; details and clearing of the channel exception can be retrieved reading the dedicated SPI registers. In case a fault happens during reading operation of its own fault register it is not latched, however if the fault is permanent it is latched as soon as the reading operation has ended.

16.2 SPI electrical characteristics

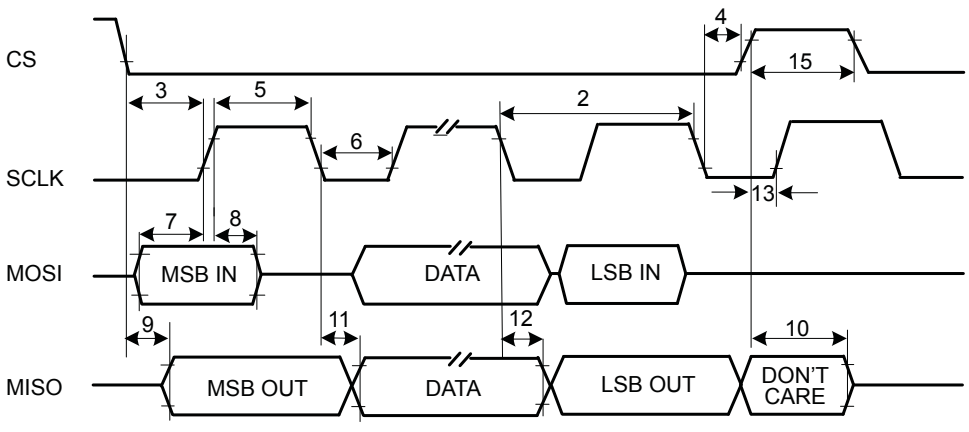
5.5 V ≤ VBATP ≤ 19 V; 3.1 V < VDDIO < 5.2 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin.

Table 55. SPI electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
DC Parameters							
VDDIO	SPI Dedicated Power Supply	Application note	3.0		5.5	V	VDDIO
V_{IL}	Logic Input Low Voltage		-		0.75	V	SCLK
V_{IH}	Logic Input High Voltage		1.75		-	V	SCLK
$V_{hysteresis}$	Input hysteresis Voltage		0.1		1	V	SCLK
SCLKPD	SCLK pull-down	SCLK = 5V	10	50	100	µA	SCLK
V_{IL}	Logic Input Low Voltage		-		0.75	V	SDI
V_{IH}	Logic Input High Voltage		1.75		-	V	SDI
$V_{hysteresis}$	Input hysteresis Voltage		0.1		1	V	SDI
SDIPD	SDI pull-down	SDI = 5V	10	50	100	µA	SDI
V_{IL}	Logic Input Low Voltage		-		0.75	V	CS
V_{IH}	Logic Input High Voltage		1.75		-	V	CS
$V_{hysteresis}$	Input hysteresis Voltage		0.1		1	V	CS
CSPU	CS pull-up to internal logic supply	CS = 0V	10	30	60	µA	CS
V_{OL}	Logic Output Low Voltage	Isource = 1mA			0.4	V	SDO
V_{OH}	Logic Output High Voltage	Isink = 1mA	VDDIO-0.4			V	SDO
Ileak	Tristate leakage current	CS high 0<SDO<VDDIO	-0.5		0.5	µA	SDO
AC Parameters							

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
fop	Transfer Frequency	Design Information			6	MHz	SCLK
tsclk	SCLK Period (2)	Design Information	167			ns	SCLK
tlead	Enable Lead Time (3)	Design Information	750			ns	SCLK
tlag	Enable Lag Time (4)	Design Information	100			ns	SCLK, CS
tsclkhs	SCLK High Time (5)	Design Information	75			ns	SCLK
tsclkls	SCLK Low Time (6)	Design Information	75			ns	SCLK
tsus	MOSI Input Setup Time (7)	Design Information	30			ns	SDI
ths	MOSI Input Hold Time (8)	Design Information	30			ns	SDI
ta	MISO Access Time (9)	Design Information 50pF load			100	ns	SDO
tdis	MISO Disable Time (10)	Design Information 50pF load			100	ns	SDO
tvs	MISO Output Valid Time (11)	Design Information 50pF load			70	ns	SDO
tho	MISO Output Hold Time (12)	Design Information 50pF load	10			ns	SDO
tr	MISO Rise Time (13)	Design Information 50pF load			50	ns	SDO
tf	MISO Fall Time (14)	Design Information 50pF load			50	ns	SDO
tcsn	CS Negated Time (15)	Design Information	750			ns	CS
tsh	SCLK Hold Time (16)	Design Information	100			ns	SCLK
teof	End of frame time	Time from CS rising edge to internal registers update Design Information		1/ fOSCINT	2/fOSCINT	ns	CS

Figure 63. SPI timing



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16.3 SPI registers map table

SPI frame has 7 bits address field and 20 bit data field, then the available address space consists of maximum 128 different registers. Taking account of the logical and physical partition of the functions configurable/monitored by SPI interface, address space has been splitted in pages, each of 16 addresses.

Table below shows the SPI page vs. macro function distribution.

Table 56. SPI register addresses

Page ID [binary]	Macro Function	Address Space Name	SPI Base Address	
			[hex]	[binary]
000	Solenoid Channel 1	Channel_1_BaseAddress	0x00	000 0000
001	Solenoid Channel 2	Channel_2_BaseAddress	0x10	001 0000
010	Solenoid Channel 3	Channel_3_BaseAddress	0x20	010 0000
011	Solenoid Channel 4	Channel_4_BaseAddress	0x30	011 0000
100	Solenoid Channel 5	Channel_5_BaseAddress	0x40	100 0000
101	Solenoid Channel 6	Channel_6_BaseAddress	0x50	101 0000
11x	Global	GLOBAL_BaseAddress	0x60	11x 0000

Note: Assumptions on solenoid channel status.

Solenoid Channel State: (DISABLED, TRISTATED, ACTIVE);

DISABLED: Channel inactive, Driver Hi impedance, no diagnosis available.

TRISTATED: Channel enabled, Driver Hi impedance, Thermal/OFF diagnosis available.

ACTIVE: Channel enabled, Driver operating according PWM, Thermal/ON diagnosis available.

During power on sequence, all solenoid channels are in DISABLED state. At the end of power on sequence, channel status is controlled by EN_DR pin status (0 => DISABLED) and SPI registers (SERVENA and SOLENDRV).

In the following tables RES1 reset event has to be intended as the combination of internal events triggering reset pin low and RES1 trigger from external command; unused bits for SDO data fields are reported as 0 in the data out frame.

Table 57. Register summary table

Register description	Register name
Service enable	SERVENA
Service Fault	SERVFLT
Service Fault Mask	SERVFLTMSK
Temperature sensor	TEMPSENS
WSI Registers	WSITEST
WSI CONFIGURATION CH_1_2	WSIRSCR0
WSI CONFIGURATION CH_3_4	WSIRSCR3
WSI CONTROL	WSICTRL
WSI AUXILIARY CONFIGURATION	WSIAUXCONF
WSI REMOTE SENSOR DATA/FAULT REGISTER 0 to 3	WSIRSDR[0:3]
WSI REMOTE SENSOR DATA REGISTER 4 to 7	WSIRSDR[4:7]
WSI REMOTE SENSOR DATA REGISTER 8 to 11	WSIRSDR[8:11]
TRK-CAN DISABLE	TRKDISABLE
TRK-CAN FAULT	TRKFAULT
Pump Configuration	PUMPCFG
Q&A Seed/Answer	WDG2SEEDANS

Register description	Register name
Q&A Status	WDG2STATUS
Q&A Answer Timing	WDG2ANSTMG
Q&A Request Timing	WDG2RQTMG
Q&A Configuration	WDG2PGM
Q&A Write Unlock	WDG2UNLOCK
Solenoid Driver	SOLENDRV
Exceptions	EXCEPTIONS
CONFIGURATION	CONFIGURATION
DITHPGM	DITHPGM
SetPoint	SETPOINT
CTRLCFG	CTRLCFG
Frequency Control	KFREQCTRL
KGAINS	KGAINS
INTGLIM	INTGLIM
AVGCUR	AVGCUR
INSTCUR	INSTCUR
PWM sense	PWMSENSE
Driver Fault Mask	DRVFLTMSK

16.3.1 Global page registers

Global page contains general control/monitor registers.

Table 58. SPI global page register address mapping

Register description	Register name
Service enable	SERVENA
Service Fault	SERVFLT
Service Fault Mask	SERVFLTMSK
Temperature sensor	TEMPSENS
WSI Registers	WSITEST
WSI CONFIGURATION CH_1_2	WSIRSCR0
WSI CONFIGURATION CH_3_4	WSIRSCR3
WSI CONTROL	WSICTRL
WSI AUXILIARY CONFIGURATION	WSIAUXCONF
WSI REMOTE SENSOR DATA/FAULT REGISTER 0 to 3	WSIRSDR[0:3]
WSI REMOTE SENSOR DATA REGISTER 4 to 7	WSIRSDR[4:7]
WSI REMOTE SENSOR DATA REGISTER 8 to 11	WSIRSDR[8:11]

SERVENA

Service enable

19	18	17	16	15	14	13	12	11	10	9	8	7 6	5	4	3	2	1	0
unused	Disable PRUN Reset	Enable reset Latch	VDDx UV/OV Self Test Enable	Spread Spectrum Disable	PHOLD	KEEP_ALIVE	GPO Diagnostic Disable	GPO CMD	GPO Configuration	Fail Safe Pre-Driver Enable	Pump Pre-Driver Enable	PUMP_PREDRIVER_TH	Solenoid Channel enable_5	Solenoid Channel enable_4	Solenoid Channel enable_3	Solenoid Channel enable_2	Solenoid Channel enable_1	Solenoid Channel enable_0
R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: GLOBAL_BaseAddress + 0x00

Type: RW

Reset: 0b00X0 0000 0000 0011 1111

Description: SERVENA register stores SERVICE Enable bits

[19] **unused**

[18] **Disable PRUN Reset:**

0: PRUN reset generation enabled.

1: PRUN reset generation disabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[17] **Enable reset Latch:**

0: Disable reset Latch feature.

1: Enable reset Latch feature

Reset events: VB_UV, GND_LOSS, PORn

[16] **VDDx UV/OV Self Test Enable:**

0: Self TestDisabled

1: Self Test Enabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[15] **Spread Spectrum Disable:**

0: Spread Spectrum Enabled on 16MHz Main Clock

1: Spread Spectrum Disabled on 16MHz Main Clock

Reset events: VB_UV, GND_LOSS, PORn, RES1

[14] **PHOLD:**

0: PHOLD inactive

1: PHOLD active

Reset events: VB_UV, GND_LOSS, PORn, RES1

[13] **KEEP ALIVE:**

0: no action

1: KA counter refresh

Reset events: VB_UV, GND_LOSS, PORn, RES1

[12] **GPO Diagnostic Disable:**

0: GPO Diag Enabled

1: GPO Diag Disabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[11] **GPO CMD:**

0: GPO LS OFF

1: GPO LS ON

Reset events: VB_UV, GND_LOSS, PORn, T_SD_int

[10] **GPO Configuration:**

0: IRQ

1: LED driver

Reset events: PORn

[9] **Fail Safe Pre-Driver Enable:**

0: DISABLE

1: ENABLE

Reset events: VB_UV, VB_OV, PORn, RES1

[8] **Pump Pre-Driver Enable:**

0: DISABLE

1: ENABLE

Reset events: VB_UV, VB_OV, GND_LOSS, PORn, RES1, CP_UV

[7:6] **PUMP_PREDRIVER_TH:**

00: 0.5V threshold

01: 1V threshold

10: 1.5V threshold

11: 2V threshold

Reset events: VB_UV, GND_LOSS, PORn, RES1

[5:0] **Solenoid Channel Enable[6]:** 6 time repeated single bit field, one for each channel.

ENCH:

0: DISABLE

1: ENABLE

Reset events: VB_UV, VB_OV, GND_LOSS, PORn, RES1, CP_UV

SERVFLT

Service Fault

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ground Loss	unused	EEPROM Trimming (unmasked)	RES1 to digital	Main Oscillator Self check	GPO OL	GPO OVC	GPO STG	VDS Pump Pre Driver Fault	VDDx OV/UV Self Test	VDD4 OVER VOLTAGE	VDD3 OVER VOLTAGE	VDD4 UNDER VOLTAGE	VDD3 UNDER VOLTAGE	T_SD_VDD1	VDD1 OVER CURRENT	CP UNDER VOLTAGE	VBATP UNDER VOLTAGE	VBATP OVER VOLTAGE	PRUN Watchdog Time-Out

Address: GLOBAL_BaseAddress + 0xB

Type: R

Reset: 0b0000 0000 0000 0000 0000

Description: Service Fault register stores Diagnostic flags of enabled services

NOTE: As monitors are working also during startup phases, when voltage levels cannot be stable, it can happen that some fault bit are set to “1” after PORn. To avoid false diagnosis when the device is fully functional, it is suggested to read this register once after the startup in order to clean it.

[19] **Ground Loss:**

0: No Fault

1: GND loss *or* GND_A loss

Reset events: PORn, DATA READ

[18] **unused**

[17] **EEPROM Trimming data CRC error status:**

(Unmasked)

0: no CRC error

1: CRC error

Reset events: VB_UV, GND_LOSS, PORn,

[16] **RES1 to digital:**

0: No Reset request from external

1: Reset request from external

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[15] **Main Oscillator Self check:**

0: Pass

1: Failed

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[14] **GPO OL (Off state diag):**

0: No Fault

1: GPO Open Load

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[13] **GPO OVC (On state diag):**

0: No Fault

1: GPO Over Current

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[12] **GPO STG (Off state diag):**

0: No Fault

1: GPO Short To Ground

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[11] **VDS Pump Pre Driver Fault:**

0: Pump Normal Load

1: Pump Overload

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[10] **VDDx OV/UV Self Test:**

0: Pass

1: Failed

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[9] **VDD4 OVER VOLTAGE:**

0: No Over Voltage

1: Over Voltage

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[8] **VDD3 OVER VOLTAGE:**

0: No Over Voltage

1: Over Voltage

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[7] **VDD4 UNDER VOLTAGE:**

0: Vdd4 Nominal

1: Vdd4 UV

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[6] **VDD3 UNDER VOLTAGE:**

0: Vdd3 Nominal

1: Vdd3 UV

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[5] **T_SD_VDD1:**

0: No Overtemp

1: Overtemp

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[4] **VDD1 OVER CURRENT:**

0: Vdd1 Normal Load

1: Vdd1 Overload

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[3] **CP UNDER VOLTAGE:**

0: CP Nominal

1: CP UV

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[2] **VBATP UNDER VOLTAGE:**

0: Vbatp Nominal

1: Vbatp UV

Reset events: PORn, DATA READ

[1] **VBATP OVER VOLTAGE:**

0: VBATP NOMINAL

1: VBATP OV

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[0] **PRUN Watchdog Time-Out:**

0: No Time-Out

1: Time-Out

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

SERVFLTMSK

Service Fault Mask

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused													E_WD_LOAD_DIS_GPO	Mask CRC error on Trimming data	E_EN_GPO	E_FSPI_GPO	E_FVBO_GPO	E_VDD2/TRK_TH_GPO	E_PVDS_GPO
R													RW	RW	RW	RW	RW	RW	RW

Address: GLOBAL_BaseAddress + 0xC

Type: RW

Reset: 0b0000 0000 0000 0101 1111

Description: Service Fault Mask register is an active Hi Mask register for Service Faults

Setting mask bit disables corresponding service from generating interrupt on GPO (when enabled).

[19:7] **unused**

[6] **E_WD_LOAD_DIS_GPO:**

0: Fault generates interrupt on GPO

1: Fault does not generates interrupt on GPO

Reset events: VB_UV, GND_LOSS, PORn, RES1

[5] **Mask CRC error on trimming data**: (Service Fault[17]).

0: Unmask.

1: Mask

Reset events: VB_UV, GND_LOSS, PORn, RES1

[4] **E_EN_GPO:**

0: Fault generates interrupt on GPO

1: Fault does not generates interrupt on GPO

Reset events: VB_UV, GND_LOSS, PORn, RES1

[3] **E_FSPI_GPO:**

0: Fault generates interrupt on GPO

1: Fault does not generates interrupt on GPO

Reset events: VB_UV, GND_LOSS, PORn, RES1

[2] **E_FVBO_GPO:**

0: Fault generates interrupt on GPO

1: Fault does not generates interrupt on GPO

Reset events: VB_UV, GND_LOSS, PORn, RES1

[1] **E_VDD2/TRK_TH_GPO:**

0: Fault generates interrupt on GPO

1: Fault does not generates interrupt on GPO

Reset events: VB_UV, GND_LOSS, PORn, RES1

[0] **E_PVDS_GPO:**

0: Fault generates interrupt on GPO

1: Fault does not generates interrupt on GPO

Reset events: VB_UV, GND_LOSS, PORn, RES1

TEMPSENS

Temperature sensor

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused		Silicon ID_HW_rev			Silicon ID_Metal_rev			WD_DIS_echo	GND Loss Selftest	GND_A Loss Selftest	T_SD_int	Die Temperature Monitor							

Address: GLOBAL_BaseAddress + 0xD

Type: R

Reset: 0b00XX XXXX X000 0000 0000

Description: Register provides thermal sensor temperature code and overtemperature flag of the analog references

[19:18] **unused**

[17:15] **Silicon ID_HW_rev:** Tracks major silicon revision starting from revision C = 000.
At each silicon revision counter is incremented.
Reset events: PORn

[14:12] **Silicon ID_Metal_rev:** Tracks minor silicon revision starting from revision A = 000.
At each silicon revision counter is incremented
Reset events: PORn

[11] **WD_DIS_echo:**
Reset events: PORn

[10] **GND Loss Selftest:**
0: Pass
1: Failed
Reset events: VB_UV, GND_LOSS, PORn, DATA_READ

[9] **GND_A Loss Selftest:**
0: Pass
1: Failed
Reset events: VB_UV, GND_LOSS, PORn, DATA_READ

[8] **T_SD_int:**
Reset events: VB_UV, GND_LOSS, PORn, DATA_READ

[7:0] **Die Temperature Monitor**:
((N/255)*305)-85 °C
Reset events: PORn

WSITEST

WSI Registers

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused											Config Range							unused	WSSTP: DOUTx Output Test Value
R											RW							R	RW

Address: GLOBAL_BaseAddress + 0x02

Type: RW

Reset: 0b0000 0000 0000 0000

Description: WSISTEST register stores static test configurator bit-field.

This register configures a static test for WSI interface. Test consists in transferring TestBit value on a selected (by Config range) WSI output.

[19:9] **unused**

[8:2] **Config range:** selects one WSI output according to the following range:

1010011: DOUT4 output;

1010101: DOUT3 output;

1011001: DOUT2 output;

1010110: DOUT1 output;

all others: test mode disable

Reset events: VB_UV, GND_LOSS, PORn

[1] **unused**

[0] **WSSTP:** DOUTx Output Test Value:

0: Output for selected DOUTx set ‘high’

1: Output for selected DOUTx set ‘low’

Reset events: VB_UV, GND_LOSS, PORn

WSIRSCR0

WSI CONFIGURATION CH_1_2

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSFILT_2				WSIPTEN_2	SSDIS_2	WSI_FIX_THRESH_2	unused	STS_2		WSFILT_1				WSIPTEN_1	SSDIS_1	WSI_FIX_THRESH_1	unused	STS_1	
RW				RW	RW	RW	R	RW		RW				RW	RW	RW	R	RW	

Address: GLOBAL_BaseAddress + 0x03

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: Any WSI interface is configured by a 10 bit field according to the following format

[19:16] **WSFILT[3:0]:** Wheel Speed filter time selection.

Initial offset = 8 µs;

Bit resolution: 500 ns

0000: 8.0 µs

0001: 8.5 µs

…

1111: 15.5 µs

Reset events: VB_UV, GND_LOSS, PORn

[15] **WSIPTEN:** Pass Through mode enable (valid for PWM encoded sensors)

0: Off

1: On

Reset events: VB_UV, GND_LOSS, PORn

[14] **SSDIS:** DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor)

0: DOUTx enabled during standstill

1: DOUTx disabled during standstill

Reset events: VB_UV, GND_LOSS, PORn

[13] **WSI_FIX_THRESH**: WSI selection of fixed or auto adaptive thresholds

0: auto adaptive thresholds

1: fixed thresholds

Reset events: VB_UV, GND_LOSS, PORn

[12] **unused**

[11:10] **STS:** Sensor Type Selection

00: Two level, Standard

01: Three level, VDA

10: PWM Encoded, 2 level, 2 edges/tooth

11: PWM Encoded, 2 level, 1 edge/tooth

Reset events: VB_UV, GND_LOSS, PORn

[9:6] **WSFILT[3:0]:** Wheel Speed filter time selection.

Initial offset = 8 µs;

Bit resolution: 500 ns

0000: 8.0 µsec

0001: 8.5 µsec

…

1111: 15.5 µsec

Reset events: VB_UV, GND_LOSS, PORn

[5] **WSIPTEN:** Pass Through mode enable (valid for PWM encoded sensors)

0: Off

1: On

Reset events: VB_UV, GND_LOSS, PORn

[4] **SSDIS:** DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor)

0: DOUTx enabled during standstill

1: DOUTx disabled during standstill

Reset events: VB_UV, GND_LOSS, PORn

[3] **WSI_FIX_THRESH**: WSI selection of fixed or auto adaptive thresholds

0: auto adaptive thresholds

1: fixed thresholds

Reset events: VB_UV, GND_LOSS, PORn

[2] **unused**

[1:0] **STS:** Sensor Type Selection

00: Two level, Standard

01: Three level, VDA

10: PWM Encoded, 2 level, 2 edges/tooth

11: PWM Encoded, 2 level, 1 edge/tooth

Reset events: VB_UV, GND_LOSS, PORn

WSIRSCR3

WSI CONFIGURATION CH_3_4

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WSFILT_4				WSIPTEN_4	SSDIS_4	WSI_FIX_THRESH_4	unused	STS_4		WSFILT_3				WSIPTEN_3	SSDIS_3	WSI_FIX_THRESH_3	unused	STS_3	
RW				RW	RW	RW	R	RW		RW				RW	RW	RW	R	RW	

Address: GLOBAL_BaseAddress + 0x04

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: Any WSI interface is configured by a 10 bit field according to the following format

[19:16] **WSFILT[3:0]:** Wheel Speed filter time selection.

Initial offset = 8µs;

Bit resolution: 500ns

0000: 8.0 µsec

0001: 8.5 µsec

…

1111: 15.5 µsec

Reset events: VB_UV, GND_LOSS, PORn

[15] **WSIPTEN:** Pass Through mode enable (valid for PWM encoded sensors)

0: Off

1: On

Reset events: VB_UV, GND_LOSS, PORn

[14] **SSDIS:** DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor)

0: DOUTx enabled during standstill

1: DOUTx disabled during standstill

Reset events: VB_UV, GND_LOSS, PORn

[13] **WSI_FIX_THRESH**: WSI selection of fixed or auto adaptive thresholds

0: auto adaptive thresholds

1: fixed thresholds

Reset events: VB_UV, GND_LOSS, PORn

[12] **unused**

[11:10] **STS:** Sensor Type Selection

00: Two level, Standard

01: Three level, VDA

10: PWM Encoded, 2 level, 2 edges/tooth

11: PWM Encoded, 2 level, 1 edge/tooth

Reset events: VB_UV, GND_LOSS, PORn

[9:6] **WSFILT[3:0]:** Wheel Speed filter time selection.

Initial offset = 8µs;

Bit resolution: 500ns

0000: 8.0 µs

0001: 8.5 µs

…

1111: 15.5 µs

Reset events: VB_UV, GND_LOSS, PORn

[5] **WSIPTEN:** Pass Through mode enable (valid for PWM encoded sensors)

0: Off

1: On

Reset events: VB_UV, GND_LOSS, PORn

[4] **SSDIS:** DOUTx output disabled in case of Standstill condition (valid only for PWM encoded 2 edges sensor)

0: DOUTx enabled during standstill

1: DOUTx disabled during standstill

Reset events: VB_UV, GND_LOSS, PORn

[3] **WSI_FIX_THRESH**: WSI selection of fixed or auto adaptive thresholds

0: auto adaptive thresholds

1: fixed thresholds

Reset events: VB_UV, GND_LOSS, PORn

[2] **unused**

[1:0] **STS:** Sensor Type Selection

00: Two level, Standard

01: Three level, VDA

10: PWM Encoded, 2 level, 2 edges/tooth

11: PWM Encoded, 2 level, 1 edge/tooth

Reset events: VB_UV, GND_LOSS, PORn

WSICTRL

WSI CONTROL

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused										DISABLE DELTA ERR	unused			INIT	DIAG	CHEN_3	CHEN_2	CHEN_1	CHEN_0
R										RW	R			RW	RW	RW	RW	RW	RW

Address: GLOBAL_BaseAddress + 0x05

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: WSICTRL register stores Remote sensor control field

[19:10] **unused**

[9] **Disable Delta Error:** Disable Delta saturation flag inside WSIRSDR[3:0]

0: Flags Enabled

1: Flags Disabled

Reset events: VB_UV, GND_LOSS, PORn

[8:6] **unused**

[5] **INIT:** Allow access to WSI CONFIGURATION CH_x registers

0: Disabled

1: Enabled

Reset events: VB_UV, GND_LOSS, PORn

[4] **DIAG:** Allow access to WSS test reg

0: Disabled

1: Enabled

Reset events: VB_UV, GND_LOSS, PORn

[3:0] **CHEN[3:0]**: Channel x Output enable

0: Disabled

1: Enabled

Reset events: VB_UV, GND_LOSS, PORn

WSIAUXCONF

WSI AUXILIARY CONFIGURATION

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused		WSI_OFFS_TH								unused		WSI_FIRST_TH							
R		RW								R		RW							

Address: GLOBAL_BaseAddress + 0x06

Type: RW

Reset: 0b0000 1101 0000 0011 0011

Description: WSIAUXCONF register stores WSI Thresholds for fixed current trip-point method

[19:18] **unused**

[17:10] **WSI_OFFS_TH[7:0]:**

Offset from first threshold setting in case of fixed threshold algorithm selected

Reset events: VB_UV, GND_LOSS, PORn

[9:8] **unused**

[7:0] **WSI_FIRST_TH[7:0]:**

Low threshold setting in case of fixed threshold algorithm selected Channel x

Reset events: VB_UV, GND_LOSS, PORn

WSIRSDR[0:3]

WSI REMOTE SENSOR DATA/FAULT REGISTER 0 to 3

If Bit 15 = 0

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC			STDSTL	FLT	Latch_D0	LCID		WSS DATA											

If Bit 15 = 1

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC			STDSTL	FLT	On/Off	LCID		ΔIth2 Saturated	ΔIth1 Saturated	STG	STB	CURRENT HI	OPENDET	WSITEMP	INVALID	NODATA	PULSE OVERFLOW	unused	

Address: GLOBAL_BaseAddress + 0x13 + n (where n = 0 to 3)

Type: R

Reset: if bit 15 = 0 then 0bXXX0 X0XX0000 0000 0000 — if bit 15 = 1 then 0bXXX0 X0XX0000 0000 1000

Description: WSIRSDRx register stores status bits of WSS interface. Output format depends on the status of bit 15.

NOTE:

If (CONFIG pin LOW) or (CONFIG pin HIGH and TRKSEL pin HIGH)

≥ TRK MODE start with FAULT bit at 0

If (CONFIG pin HIGH and TRKSEL pin LOW)

≥ WSS MODE start with FAULT bit at 1

FAULT bit is set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA, INVALID, SLOT ERROR, PULSE OVERFLOW ERROR

[19:17] **CRC [2:0]:** CRC based on bits [16:0]

Reset events: VB_UV, GND_LOSS, PORn

[16] **STDSTL:** Standstill indication (only for VDA sensor or PWM 2 edges)

0: Standstill not detected

1: Standstill detected

Reset events: VB_UV, GND_LOSS, PORn

[15] **FLT:** Fault Status, depending on fault status the DATA bits are defined differently. Cleared when all the fault bits are 0, set when one of the fault bits is 1

0: No fault

1: Fault

Value at reset:

0: If (CONFIG pin LOW) or (CONFIG pin HIGH and TRKSEL pin HIGH)

1: If (CONFIG pin HIGH and TRKSEL pin LOW)

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

If Bit 15 = 0 ==> No Fault Condition

[14] **Latch_D0:** Latched D0, set when bit0 has been decoded high in any of previous messages (only for VDA sensor), cleared on read

0: no prior bit0 faults

1: prior message(s) contained bit0 fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[13:12] **LCID[1:0]:** Logical Channel ID

00: ch1

01: ch2

10: ch3

11: ch4

Reset events: VB_UV, GND_LOSS, PORn

[11:0] **WSS DATA:** 12-bit data from wheel speed decoder

VDA data format:

DATA[7:0] Data bits

DATA[11:8] Counter bits

PWD data format:

DATA[8:0] Pulse Data bits

Reset events: VB_UV, GND_LOSS, PORn

If Bit 15 = 1 ==> Fault Condition

[14] **On/Off:** Channel on/off status, cleared by Reset Event or when the channel is commanded OFF via SPI WSICTRL or when the STG bit is set with WSITEMP bit

0: Off

1: On

Reset events: VB_UV, GND_LOSS, PORn

[13:12] **LCID[1:0]:** Logical Channel ID

00: ch1

01: ch2

10: ch3

11: ch4

Reset events: VB_UV, GND_LOSS, PORn

[11] **∆Ith2 Saturated:** Delta Error bit (Enabled only if WSICTRL[9] = 0)

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[10] **ΔIth1 Saturated:** Delta Error bit (Enabled only if WSICTRL[9] = 0)

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[9] **STG:** Short to ground (in current limit condition)

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[8] **STB:** Short to battery

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[7] **CURRENT HI:** Set when channel current exceeds ILKGG for a time determined by an up/down counter

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[6] **OPENDET:** Open Sensor detected. Set when channel current exceeds ILKGB for a time determined by an up/down counter

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[5] **WSITEMP:** Overtemperature detected

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[4] **INVALID:** Invalid data, set when parity error is detected (when this check is feasible), valid only for VDA sensor.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[3] **NODATA:** No data in buffer

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[2] **PULSE OVERFLOW:** Pulse duration counter overflow (only for PWM sensors 1 or 2 edges per tooth)

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn, DATA READ

[1:0] **Unused**

Reset events: VB_UV, GND_LOSS, PORn

WSIRSDR[4:7]

WSI REMOTE SENSOR DATA REGISTER 4 to 7

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Δlth1 current										Base current									

Address: GLOBAL_BaseAddress + 0x13 + n (where n = 4 to 7)

Type: R

Reset: 0b0001 0011 0000 0100 1100

Description: --

[19:10] **Dlth1 current**

Reset events: VB_UV, GND_LOSS, PORn

[9:0] **Base current**

Reset events: VB_UV, GND_LOSS, PORn

WSIRSDR[8:11]

WSI REMOTE SENSOR DATA REGISTER 8 to 11

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused										Δlth2 current									

Address: GLOBAL_BaseAddress + 0x13 + n (where n = 8 to 11)

Type: R

Reset: 0b0000 0000 0000 1001 0111

Description: --

[19:10] **unused**

[9:0] **Dlth2 current**

Reset events: VB_UV, GND_LOSS, PORn

16.3.2 TRACK-CAN registers

Table 59. **TRACK-CAN registers address mapping**

Register description	Register name
TRK-CAN DISABLE	TRKDISABLE
TRK-CAN FAULT	TRKFAULT

TRKDISABLE

TRK-CAN DISABLE

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused									CAN WAKE-UP	CAN PATTERN WAKE-UP	CAN SLEEP MODE	CAN REC-ONLY	CAN LOOP	CAN ERROR HANDLING DIS	VDD2 Regulator Disable	TRK DISABLE_3	TRK DISABLE_2	TRK DISABLE_1	TRK DISABLE_0
R									RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: GLOBAL_BaseAddress + 0x8

Type: RW

Reset: 0b0000 0000 0110 0000 0000

Description: TRK-CAN DISABLE register stores Tracking regulator and CAN interface Disable configuration

[19:11] **unused**

Reset events: -

[10] **CAN WAKE-UP:**

0: CAN Wake-up disabled

1: CAN Wake-up enabled

Reset events: VB_UV, GND_LOSS, PORn

[9] **CAN PATTERN WAKE-UP:**

0: CAN WAKE-UP by any transition

1: CAN WAKE-UP by normal pattern

Reset events: VB_UV, GND_LOSS, PORn

[8] **CAN SLEEP MODE:**

0: Normal mode

1: CAN transceiver disabled and error cleaned

Reset events: VB_UV, GND_LOSS, PORn

[7] **CAN REC-ONLY:**

0: Receiver-Only mode disabled

1: Receiver-Only mode enabled

Reset events: VB_UV, GND_LOSS, PORn

[6] **CAN LOOP:**

0: Can Looping mode disabled

1: Can Looping mode disabled enabled

Reset events: VB_UV, GND_LOSS, PORn

[5] **CAN ERROR HANDLING DIS:**

0: CAN error handling enabled

1: CAN error handling disabled

Reset events: VB_UV, GND_LOSS, PORn

[4] **VDD2 Regulator Disable:**

1: DISABLE

0: ENABLE

Reset events: VB_UV, GND_LOSS, PORn, RES1

[3:0] **TRK DISABLE[3:0]:**

0: ENABLE

1: DISABLE

Reset events: VB_UV, GND_LOSS, PORn, RES1

TRKFAULT

TRK-CAN FAULT

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAN RX PERMANENT REC	CAN PERMANENT DOM	CAN PERMANENT REC	CAN DOMINANT TX TO	ASIC configuration	VDD1_SEL echo	VDD4_SEL echo	TRK_SEL echo	VDD2_SEL echo	TRK REVERSE CURRENT_3	TRK REVERSE CURRENT_2	TRK REVERSE CURRENT_1	TRK REVERSE CURRENT_0	VDD2 REVERSE CURRENT	T_SD_TRK	VDD2_OUT_OF_REGULATION	TRK_OUT_OF_REGULATION_3	TRK_OUT_OF_REGULATION_2	TRK_OUT_OF_REGULATION_1	TRK_OUT_OF_REGULATION_0

Address: GLOBAL_BaseAddress + 0x9

Type: R

Reset: 0b00000000000000

Description: TRK-CAN FAULT stores Tracking regulator and CAN interface faults plus echo of CAN and regulators configuration pins

NOTE: As monitors are working also during startup phases, when voltage levels cannot be stable, it can happen that some fault bit are set to “1” after PORn. To avoid false diagnosis when the device is fully functional, it is suggested to read this register once after the startup in order to clean it.

[19] **CAN RX PERMANENT REC:**

0: No fault

1: CAN RX permanent recessive

Reset events: PORn, DATA READ, CAN ERROR HANDLING DIS

[18] **CAN PERMANENT DOM:**

0: No fault

1: CAN BUS permanent dominant

Reset events: PORn, DATA READ, CAN ERROR HANDLING DIS

[17] **CAN PERMANENT REC:**

0: No fault

1: CAN BUS permanent recessive

Reset events: PORn, DATA READ, CAN ERROR HANDLING DIS

[16] **CAN DOMINANT TX TO:**

0: No fault

1: TO exceed

Reset events: PORn, DATA READ, CAN ERROR HANDLING DIS

[15] **ASIC configuration:**

0: Full operation

1: Reduced stby consumption

Reset events: PORn

[14] **VDD1_SEL echo:**

0: 5V output voltage

1: 6.5V output voltage

Reset events: PORn

[13] **VDD4_SEL echo:**

0: Linear configuration selected

Reset events: PORn

[12] **TRK_SEL echo:**

0: WSSI selected

1: Tracking configuration selected

Reset events: PORn

[11] **VDD2_SEL echo:**

0: Linear configuration selected

1: Tracking configuration selected

Reset events: PORn

[10:7] **TRK REVERSE CURRENT[3:0]:**

0: no reverse current

1: reverse current

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[6] **VDD2 REVERSE CURRENT:**

0: no reverse current

1: reverse current

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[5] **T_SD_TRK:**

0: no vdd2/trk overtemperature detected

1: vdd2/trk overtemperature detected

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[4] **VDD2_OUT_OF_REGULATION**

0: vdd2 nominal load

1: vdd2 overload or low drop

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

[3:0] **TRK_OUT_OF_REGULATION[3:0]**

0: TRK nominal load

1: TRK overload or low drop

Reset events: VB_UV, GND_LOSS, PORn, RES1, DATA READ

16.3.3 Pump registers

PUMPCFG

Pump Configuration

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused				PUMP PWM period								PUMP PWM duty cycle							
R				RW								RW							

Address: GLOBAL_BaseAddress + 0xA

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: PUMPCFG register stores PUMP PWM Period, PUMP PWM Duty cycle

[19:16] **unused**

[15:8] **PUMP PWM Period:** (see Section 10.3.1 Pump pre-driver functional description)
Reset events: VB_UV, GND_LOSS, PORn, RES1

[7:0] **PUMP PWM Duty Cycle:** (see Section 10.3.1 Pump pre-driver functional description)
Reset events: VB_UV, GND_LOSS, PORn, RES1

16.3.4 Q&A watchdog registers

Table 60. Q&A watchdog registers address mapping

Register description	Register name
Q&A Seed/Answer	WDG2SEEDANS
Q&A Status	WDG2STATUS
Q&A Answer Timing	WDG2ANSTMG
Q&A Request Timing	WDG2RQTMG
Q&A Configuration	WDG2PGM
Q&A Write Unlock	WDG2UNLOCK

WDG2SEEDANS

Q&A Seed/Answer

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused				Unused [read mode] Answer high [write mode]								Seed [read mode] Answer low [write mode]							
R				RW								RW							

Address: GLOBAL_BaseAddress + 0xE

Type: RW

Reset: 0b0000 0000 0000 0000 0000 0000

Register behaves differently when read or written.

Description: It contains seed value sent to the micro to be used for Answer elaboration in read mode.

It contains Answer word in write mode

[19:16] **unused**

If Bit 31 = 0 ==> Read operation

[15:8] **unused**

[7:0] **Seed:** Current value of the seed sent to the microcontroller to be used for the Answer elaboration

Reset events: VB_UV, GND_LOSS, PORn

If Bit 31 = 1 ==> Write operation

[15:8] **Answer HIGH:** Higher part of the answer obtained as described on Section 14 Q&A Watchdog

Reset events: VB_UV, GND_LOSS, PORn

[7:0] **Answer LOW:** Lower part of the answer obtained as described on Section 14 Q&A Watchdog

Reset events: VB_UV, GND_LOSS, PORn

WDG2STATUS

Q&A Status

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused		WD_FSM_Status		WD_RST_Cnt_Value				WD_RST_cnt_Flag	WD_RST_TO_Req	WD_RST_TO_Answ	WD_Late_Req	WD_Early_Req	WD_Bad_Answ	WD_Late_Answ	WD_Early_Answ	WD_Cnt_Value			

Address: GLOBAL_BaseAddress + 0xF

Type: R

Reset: 0b0000 0000 0000 0000 0000

Description: Register contains WD status values

[19:18] **unused**

[17:16] **WD_FSM_Status:**

00: Idle

01: Wait For Answer

10: Wait For Query

11: Wait For Query/Wait For Answer after an error

Reset events: VB_UV, GND_LOSS, PORn

[15:12] **WD_RST_Event_Value** Current value of the WD_RST counter event already sent.

Reset events: VB_UV, GND_LOSS, PORn

[11] **WD_RST_Cnt_Flag:** Flag set if the WD_RST signal has been sent because error counter reached zero.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[10] **WD_RST_TO_Req:** Flag set if the WD_RST signal has been sent because Request time out elapsed.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[9] **WD_RST_TO_Answ:** Flag set if the WD_RST signal has been sent because Answer time out elapsed.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[8] **WD_Late_Req:** Flag set if the last request has been sent too late related to the programmed timing parameters.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[7] **WD_Early_Req:** Flag set if the last request has been sent too early related to the programmed timing parameters.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[6] **WD_Bad_Answ:** Flag set if the last answer has been sent inside the right timing window but it isn't the expected answer

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[5] **WD_Late_Answ:** Flag set if the last answer has been sent too late related to the programmed timing parameters.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[4] **WD_Early_Answ:** Flag set if the last answer has been sent too early related to the programmed timing parameters.

0: no fault

1: fault

Reset events: VB_UV, GND_LOSS, PORn

[3:0] **WD_Cnt_Value** Current value of the WD counter

Reset events: VB_UV, GND_LOSS, PORn

WDG2ANSTMG

Q&A Answer Timing

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Answer Time-out Delta						Answer Time-out Delta						Valid Answer Start							

Address: GLOBAL_BaseAddress + 0x10

Type: RW

Reset: 0b0000 0011 0000 1111 1111

Description: Register contains answer timings parameters

[19:14] **Answer Time-out Delta:** End of the period for answers acceptance.

Once reached the WD_RST signal will be sent independently on the Error status (WD_CNT). The value specified is an incremental time starting from T_Valid_Answ_Start and T_Valid_Answ_End_Delta.

Time = (T_Valid_Answ_Start + T_Valid_Answ_End_Delta + T_Answ_TimeOut_Delta) * WD_clk

Reset events: VB_UV, GND_LOSS, PORn

[13:8] **Valid Answer End Delta:** End of the timing window inside which answers must be received.

The value specified is an incremental time starting from T_Valid_Answ_Start.

Time = (T_Valid_Answ_Start + T_Valid_Answ_End_Delta) * WD_clk

Reset events: VB_UV, GND_LOSS, PORn

[7:0] **Valid Answer Start:** Start of the timing window inside which answers must be received. Absolute value.

Time = T_Valid_Answ_Start * WD_clk

Reset events: VB_UV, GND_LOSS, PORn

WDG2RQTMG

Q&A Request Timing

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Request Time-out Delta						Request Time-out Delta						Valid Request Start							

Address: GLOBAL_BaseAddress + 0x11

Type: RW

Reset: 0b0000 0011 0000 1111 1111

Description: Register contains request timings parameters

[19:14] **Request Time-out Delta:** End of the period for requests acceptance.

Once reached the WD_RST signal will be sent independently on the Error status (WD_CNT). The value specified is an incremental time starting from T_Valid_Req_Start and T_Valid_Req_End_Delta.

Time = (T_Valid_Req_Start + T_Valid_Req_End_Delta + T_Req_TimeOut_Delta) * WD_clk

Reset events: VB_UV, GND_LOSS, PORn

[13:8] **Valid Request End Delta:** End of the timing window inside which requests must be received.

The value specified is an incremental time starting from T_Valid_Req_Start.

Time = (T_Valid_Req_Start + T_Valid_Req_End_Delta) * WD_clk

Reset events: VB_UV, GND_LOSS, PORn

[7:0] **Valid Request Start:** Start of the timing window inside which requests must be received. Absolute value.

Time = T_Valid_Req_Start * WD_clk

Reset events: VB_UV, GND_LOSS, PORn

WDG2PGM

Q&A Configuration

19 18	17	16	15	14	13 12 11 10	9 8 7 6	5 4 3	2 1 0
unused	Watchdog reset enable	Watchdog request check enable	Time-out reset enable	Clock division	Low threshold	High threshold	Number of incremental (good) steps	Number of decremental (bad) steps
R	RW	RW	RW	RW	RW	RW	RW	RW

Address: GLOBAL_BaseAddress + 0x12

Type: RW

Reset: 0b0010 0001 1111 1100 1011

Description: Register contains unlock frame

[19:18] **unused**

[17] **Watchdog reset enable:** Enable for the WD_RST signal.

0: WD_RST signal not sent

1: WD_RST signal sent in case of failure

Reset events: VB_UV, GND_LOSS, PORn

[16] **Watchdog request check enable:** Enable for the Request timing checking.

0: Request timing check not performed (monodirectional mode)

1: Request timing check performed

(bidirectional mode)

Reset events: VB_UV, GND_LOSS, PORn

[15] **Time-out reset enable:** Enable for the RST after Timeout generation.

0: RST not generated after a TO event

1: RST generated after a TO event

Reset events: VB_UV, GND_LOSS, PORn

[14] **Clock division:** Frequency Clock division setup.

0: clock not divided (64us)

1: clock divided by (256us)

Reset events: VB_UV, GND_LOSS, PORn

[13:10] **Low threshold:** Threshold level to inhibit the actuation. If WD_CNT is lower than the threshold no actuation will be performed.

Reset events: VB_UV, GND_LOSS, PORn

[9:6] **High threshold:** Threshold level to start the actuation. If WD_CNT is lower than the threshold actuation will be performed depending on the previous state as described on Section 14 Q&A Watchdog

Reset events: VB_UV, GND_LOSS, PORn

[5:3] **Number of incremental (good) steps:** Number of incremental steps for WD_CNT as consequence of a good answer.

Reset events: VB_UV, GND_LOSS, PORn

[2:0] **Number of decremental (bad) steps:** Number of decrement steps for WD_CNT as consequence of an error.

Reset events: VB_UV, GND_LOSS, PORn

WDG2UNLOCK

Q&A Write Unlock

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Watchdog Unlock Frame																			

Address: GLOBAL_BaseAddress + 0x07

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: Register contains unlock frame

[19:0] **Watchdog Unlock Frame** Unlock key as described on Section 14.2.1 Register unlock procedure

Reset events: VB_UV, GND_LOSS, PORn

16.3.5 Solenoid channel registers

Table 61. **Solenoid channel registers address mapping**

Register description	Register name
Solenoid Driver	SOLENDRV
Exceptions	EXCEPTIONS
CONFIGURATION	CONFIGURATION
DITHPGM	DITHPGM
SetPoint	SETPOINT
CTRLCFG	CTRLCFG
Frequency Control	KFREQCTRL
KGAINS	KGAINS
INTGLIM	INTGLIM
AVGCUR	AVGCUR
INSTCUR	INSTCUR
PWM sense	PWMSENSE
Driver Fault Mask	DRVFLTMSK

SOLENDRV

Solenoid Driver

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused								Solenoid Driver Status_5		Solenoid Driver Status_4		Solenoid Driver Status_3		Solenoid Driver Status_2		Solenoid Driver Status_1		Solenoid Driver Status_0	
R								RW		RW		RW		RW		RW		RW	

Address: GLOBAL_BaseAddress + 0x01

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: SOLENDRV packs solenoid driver enable configuration

Solenoid DriverStatus_x configuration is effective when the related channel is activated (SERVENA.Solenoid Channel Enable_x = 1).

[19:12] **unused**

[11:0] **Solenoid DriverStatus [5:0]:** 6 time repeated two bit field, two bits for each channel.

[0]: FULL_ON

0: PWM Mode

1: Full On Mode

[1]: DRVENA

0: Tristate

1: Active

Reset events: VB_UV, GND_LOSS, VB_OV, PORn, RES1, HS/LS_OVC (SW_cntr=0 or SW_cntr=1 and OVC_R=0), T_SD, CP_UV, LS clamp active

EXCEPTIONS

Exceptions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused				T_WARN	CRC error on CSA Compensation data:	CRC error on A2D trimming bits	Comparators Self Test (Active) status		Solenoid Logic BIST Status		Solenoid Diag Self Test(OFF State)		Open Load (OFF State)	Short Detection (OFF State)	Solenoid A/D self check	LS clamp active	HS over current (ON State)	LS over current (ON State)	T_SD

Address: Channel_X_BaseAddress + 0x00

Type: R

Reset: 0b0000 0000 0000 0000 0000

Description: Exceptions Register packs information related to the driver status

The “behavior on exception” is conceived to avoid “automatic” driver restart after exception removal.

Action on exception consists in “TRISTATING” driver.

The driver operation can only be recovered by explicitly write DRVENA = 1.

GPOExc[5:0] and SPIExc[5:0] signals are generated by ORing exception bits.

NOTE: As monitors are working also during startup phases, when voltage levels can not be stable, it can happen that some fault bit are set to “1” after PORn. To avoid false diagnosis when the device is fully functional, it is suggested to read this register once after the startup in order to clean it.

[19:16] **unused**

[15] **T_WARN:** Thermal Warning - Active high - Channel thermal sensor has exceeded “thermal warning threshold”.

0: no fault

1: Thermal warning

Reset events: PORn, DATA READ

Actions on set: No actions related to this bit.

Behavior: Read operation would reset bit status if channel temperature is below “thermal warning threshold”.

[14] **CRC error on CSA Compensation data:**

0: No CRC Error.

1: CRC Error

Reset events: PORn

[13] **CRC error on A2D trimming bits:**

0: No CRC Error

1: CRC Error

Reset events: PORn

[12:11] **Comparators Self Test (Active) status**:

00: No Fault

01: Lo Cmp Test Fail

10: Hi Cmp Test Fail

11: Both Cmps Test fail

Reset events: PORn, DATA READ

[10:9] **Solenoid Logic BIST Status:**

00: Idle

01: BIST running

10: BIST passed

11: BIST failed

Reset events: PORn

[8:7] **Solenoid Diag Self Test(OFF State):** OFF State Diagnostic comparators have failed self-test.

Failure may be linked to wrong internal reference, stuck condition of the comparator or real fault happened on LOADx pin (to be cross-checked with OFF state diagnostic).

Actions on set: No actions related to this bit.

Behavior: Read operation would reset bit status

00: Self Test pass

01: DIAG_LV comparator fail

10: DIAG OL comparator fail

11: Self Test fail

Reset events: PORn, DATA READ

[6] **Open Load (OFF State):**

0: no fault

1: Open load

Reset events: PORn, DATA READ

[5] **Short Detection (OFF State):**

0: no fault

1: Short detected

Reset events: PORn, DATA READ

[4] **Solenoid A/D self check:**

0: pass

1: failed

Reset events: PORn, DATA READ

[3] **LS clamp active:**

0: no fault

1: LS clamp activated

Reset events: PORn, DATA READ

[2] **HS over current (ON State)**

0: no fault:

1: HS over current

Reset events: PORn, DATA READ

[1] **LS over current (ON State)**

0: no fault

1: LS over current

Reset events: PORn, DATA READ

[0] **T_SD:**

0: no fault

1: thermal shut-down

Reset events: PORn, DATA READ

CONFIGURATION

CONFIGURATION

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused				SYNC TYPE	OFS_CMP_DIS	CALIBRATION_DIS	DITHER_SYNC_EN	Solenoid Current Feedback A/D Self Test	Solenoid Logic BIST	Td_Blank	HILOAD	OVC_R (Over Current Retry function)	Overcurrent threshold selection	Enable OFF Diagnosis	Dither Enable	Solenoid Load Configuration	SW_cntr: Current Feedback Control Mode	Output Slew Rate	
R				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	

Address: Channel_X_BaseAddress + 0x01

Type: RW

Reset: 0b0000 0000 0000 0000 0011

Description: Configuration Register packs information related to the channel configuration.

Configuration register can be written only when channel is disabled (ENCHx = 0) or TRISTATED (DRVENAx = 0).

[19:16] **unused**

[15] **SYNC TYPE:**

0: Dither synchronization done at each dither step

1: Dither synchronization done at each dither period

Reset events: VB_UV, GND_LOSS, PORn, RES1

[14] **OFS_CMP_DIS:**

0: Current Sense Offset Compensation active

1: Current Sense Offset Compensation disabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[13] **CALIBRATION_DIS:**

0: Digital current sense calibration active

1: Digital current sense calibration disabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[12] **DITHER_SYNC_EN:**

0: Dither PWM synchronization disabled

1: Dither PWM synchronization enabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[11] **Solenoid Current Feedback A/D Self Test:**

0: Self Test disabled

1: Self Test enabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[10] **Solenoid Logic BIST:**

0: Logic BIST reset

1: Logic BIST enabled

Reset events: VB_UV, GND_LOSS, PORn, RES1

[9] **Td_Blank:**

0: long blank time selected

1: short blank time selected

Reset events: VB_UV, GND_LOSS, PORn, RES1

[8] **HILOAD:**

Current Sense Scale

0: 1.5A max current

1: 2A max current

Reset events: VB_UV, GND_LOSS, PORn, RES1

[7] **OVC_R (Over Current Retry function):**

0: Retry function disabled

1: Retry function enabled

Reset events: VB_UV , GND_LOSS, PORn, RES1

[6] **Overcurrent threshold selection:**

0: 4A thehsold

1: 5A threshold

Reset events: VB_UV , GND_LOSS, PORn, RES1

[5] **Enable OFF Diagnosis:**

0: disable

1: enable

Reset events: VB_UV , GND_LOSS, PORn, RES1

[4] **Dither Enable:**

0: disable

1: enable

Reset events: VB_UV , GND_LOSS, PORn, RES1

[3] **Solenoid Load Configuration:**

0: low–side

1: high–side

Reset events: VB_UV , GND_LOSS, PORn, RES1

[2] **SW_cntr: Current Feedback Control Mode**

0: HW feedback

1: SW feedback

Reset events: VB_UV , GND_LOSS, PORn, RES1

[1:0] **Output Slew Rate:**

00: 0.4 V/µs

01: 1.0 V/µs

10: 4.0 V/µs

11: 8.0 V/µs

Reset events: VB_UV , GND_LOSS, PORn, RES1, OVC detection

DITHPGM

DITHPGM

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dither Tstep mantissa M					Dither Tstep base 2 exponent N			Dither current step amplitude							Dither current step number				

Address: Channel_X_BaseAddress + 0x03

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: Register packs information related to the dither generator configuration.
Each channel driver has a dedicated programmable dither generator. (see Hardware current control)

[19:15] **Dither Tstep mantissa M**
Reset events: VB_UV , GND_LOSS, PORn, RES1

[14:12] **Dither Tstep base 2 exponent N**
Reset events: VB_UV , GND_LOSS, PORn, RES1

[11:5] **Dither current step amplitude**
Reset events: VB_UV , GND_LOSS, PORn, RES1

[4:0] **Dither current step number**
Reset events: VB_UV , GND_LOSS, PORn, RES1

SETPOINT

SetPoint

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused									Current set-point code										
R									RW										

Address: Channel_X_BaseAddress + 0x04

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: Register store current setpoint code (HW mode current control).

Current Control SETPOINT is coded into 11 bits. Current value depends on HILOAD bit).

[19:11] **unused**

[10:0] **Current set-point code:** see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1, OVC detection, T_SD

CTRLCFG

CTRLCFG

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused							Solenoid Diag Self Test	HW feedback Frequency Mode	Target PWM period code										
R							RW	RW	RW										

Address: Channel_X_BaseAddress + 0x05

Type: RW

Reset: 0b0000 0000 0000 0000 0000

Description: Register store current setpoint code (HW mode current control).

[19:13] **unused**

[12] **Solenoid Diag Self Test:**

0: Self Test disabled

1: Self Test enabled

Reset events: VB_UV , GND_LOSS, PORn, RES1

[11] **HW feedback Frequency Mode**

0: fixed

1: variable

Reset events: VB_UV , GND_LOSS, PORn, RES1

[10:0] **Target PWM period code** see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

KFREQCTRL

Frequency Control

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused								FCIL	TOFSCHOP	TOFSINT	TOFSFLT			KFI			KFP		
R								RW	RW	RW	RW			RW			RW		

Address: Channel_X_BaseAddress + 0x06

Type: RW

Reset: 0b0000 0000 1000 1101 0001

Description: Register stores KF, FCIL (Variable frequency forward gain: HW mode current control) and current sense chopper parameters.

[19:12] **unused**

[11] **FCIL:**

0: Disabled

1: Enabled

Reset events: VB_UV , GND_LOSS, PORn, RES1

[10] **TOFSCHOP:** see Hardware current control

Reset events: VB_UV , GND_LOSS, PORn, RES1

[9] **TOFSINT** see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

[8:6] **TOFSFLT:** Chopper Offset Hi-pass Filter Time Cut-off see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

[5:3] **KFI:** Integral Gain of Frequency Control Loop see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

[2:0] **KFP**: Proportional Gain of Frequency Control Loop see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

KGAINS

KGAINS

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused														KI			KP		
R														RW			RW		

Address: Channel_X_BaseAddress + 0x07

Type: RW

Reset: 0b0000 0000 0000 0001 1100

Description: Register stores KI (Integral error gain: HW mode current control) and KP (Proportional error gain: HW mode current control).

[19:6] **unused**

[5:3] **KI:** Integral Gain of HW current control loop see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

[2:0] **KP:** Proportional Gain of HW current control loop see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

INTGLIM

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused												INTLIMVAL				TRINTLIMVAL			
R												RW				RW			

Address: Channel_X_BaseAddress + 0x08

Type: RW

Reset: 0b0000 0000 0000 1001 0001

Description: -

[19:8] **unused**

[7:4] **INTLIMVAL:** Steady state integral absolute limit HW feedback see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

[3:0] **TRINTLIMVAL:**
Transient integral absolute limit HW feedback see Hardware current control

Reset events: VB_UV, GND_LOSS, PORn, RES1

AVGCUR

AVGCUR

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused									AVGCUR										

Address: Channel_X_BaseAddress + 0x09

Type: R

Reset: 0b0000 0000 0000 0000 0000

Description: Register stores Average Current Code in 1 PWM period

[19:11] **unused**

[10:0] **AVGCUR:** Average current code in 1 PWM period (see Hardware current control)

Reset events: PORn

INSTCUR

INSTCUR

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused								INSTCUR											

Address: Channel_X_BaseAddress + 0x0A

Type: R

Reset: 0b0000 0000 0000 0000 0000

Description: Register stores value of sensed current for diagnostic (2's complement value)

[19:12] **unused**

[11:0] **INSTCUR:** Instantaneous current value (2's complement) (see Hardware current control)

Reset events: PORn

PWMSENSE

PWM sense

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused	TMOUT	PWM code																	

Address: Channel_X_BaseAddress + 0x0B

Type: R

Reset: 0b0100 0000 0000 0000 0000

Description: Register stores:

PWM period out of range flag (TMOUT).

PWM code: measured effective PWM period normalized to 125 ns

[19] **unused**

[18] **TMOUT:**

0: no fault

1: fault

Reset events: PORn

[17:0] **PWM code:** see Hardware current control

Reset events: PORn

DRVFLTMSK

Driver Fault Mask

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
unused				E_SOL_TW_GPO	CRC Error on CSA	CRC Error on A2D	E_SOL_COMP_GPO	E_SOL_COMP_GPO	E_SOL_BIST_GPO	E_SOL_BIST_GPO	E_SOL_ABIST_GPO	E_SOL_ABIST_GPO	E_SOL_OL_GPO	E_SOL_SHORT_GPO	E_SOL_A2D_GPO	E_LSCLAMP_GPO	E_SOL_HSOVC_GPO	E_SOL_LSOVC_GPO	E_SOL_LSOVC_GPO
R				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Address: Channel_X_BaseAddress + 0x0C

Type: RW

Reset: 0b0000 1001 1111 1111 1111

Description: Driver Fault Mask register is an active Hi Mask register for Driver Faults.

Setting mask bit disables corresponding fault from generating interrupt on GPO (when enabled).

[19:16] **unused**

[15] **E_SOL_TW_GPO:**

0: No Mask (TW triggers GPO)

1: Mask (TW does not trigger GPO)

Reset events: VB_UV, GND_LOSS, PORn, RES1

[14] **CRC Error on CSA Compensation Parameters Mask:**

0: No Mask (calibration disabled if CRC Error detected).

1: CRC error on Calibration Data Masked.

Reset events: VB_UV , GND_LOSS, PORn, RES1

[13] **CRC Error on A2D Trimming Data Mask:**

0: No Mask (no trimming available if CRC error detected).

1: CRC error Masked (Trimming is applied anyway).

Reset events: VB_UV , GND_LOSS, PORn, RES1

[12] **E_SOL_COMP_GPO (OL - Active mode):** PWM check on open load comparator.

0: No Mask (PWM check failure triggers GPO)

1: Mask (PWM check failure does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[11] **E_SOL_COMP_GPO (LVT - Active mode):** PWM check on lvt comparator.

0: No Mask (PWM check failure triggers GPO)

1: Mask (PWM check failure does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[10] **E_SOL_BIST_GPO (end):**

0: No Mask (logic BIST end triggers GPO)

1: Mask (logic BIST end does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[9] **E_SOL_BIST_GPO (start):**

0: No Mask (logic BIST start or fail triggers GPO)

1: Mask (logic BIST start or fail does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[8] **E_SOL_ABIST_GPO (OL):**

0: No Mask (open load self test failure triggers GPO)

1: Mask (open load self test failure does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[7] **E_SOL_ABIST_GPO (LVT):**

0: No Mask (lvt self test failure triggers GPO)

1: Mask (lvt self test failure does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[6] **E_SOL_OL_GPO:**

0: No Mask (open load triggers GPO)

1: Mask (open load does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[5] **E_SOL_SHORT_GPO:**

0: No Mask (lvt triggers GPO)

1: Mask (lvt does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[4] **E_SOL_A2D_GPO:**

0: No Mask (A2D self test failure triggers GPO)

1: Mask (A2D self test failure does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[3] **E_LSCLAMP_GPO:**

0: No Mask (LS clamp active triggers GPO)

1: Mask (LS clamp active does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[2] **E_SOL_HSOVC_GPO:**

0: No Mask (HS OVC triggers GPO)

1: Mask (HS OVC does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[1] **E_SOL_LSOVC_GPO:**

0: No Mask (LS OVC triggers GPO)

1: Mask (LS OVC does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

[0] **E_SOL_OT_GPO:**

0: No Mask (OT triggers GPO)

1: Mask (OT does not trigger GPO)

Reset events: VB_UV , GND_LOSS, PORn, RES1

17 Functional safety

17.1 Power supply

17.1.1 VDD3(4) Regulator

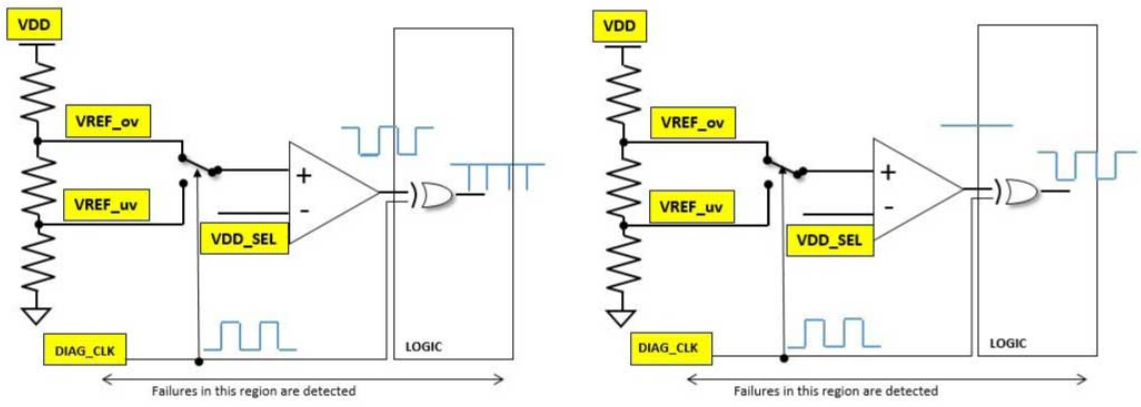
Under Voltage Comparator

Voltage monitor compares regulator feedback value with a reference threshold, independent from the regulator one, to understand if a fault condition is present on regulator output. To prevent latent fault, an analog self-test is implemented in the monitor circuitry: comparator inputs are choppered by a diagnostic clock and the output of the comparator is XORed with diagnostic clock itself (see next figure); in case comparator is not able to toggle its output will start toggling the following diagnostic clock and setting the fault. Self-test is enabled by SPI bit and is kept running until the enable bit is cleared; in case of fault same actions as under voltage fault are taken leading to ASIC reset, setting uv fault bit plus a self test fault bit to let the user know, after recovering from RES condition, that the fault has been generated during self test procedure.

Over Voltage Comparator

Voltage monitor compares regulator feedback value with a reference threshold, independent from the regulator one, to understand if a fault condition is present on regulator output. To prevent latent fault an analog self-test is implemented in the monitor circuitry: comparator inputs are choppered by a diagnostic clock and the output of the comparator is XORed with diagnostic clock itself (see next figure); in case comparator is not able to toggle its output, it will start toggling the following diagnostic clock and setting the fault. Self-test is enabled by SPI bit and is kept running until the enable bit is cleared; in case of fault, the same actions as overvoltage fault (setting OV fault bit and a Selftest fault bit) are taken leading to device reset, and warn, after recovering from RES condition, that the fault has been generated during self-test procedure.

Figure 64. voltage monitor self test basic implementation



No fault

Fault condition

GADG2407171510PS

17.1.2 Power supply electrical characteristics

5.5V ≤ VBATP≤ 19V; -40°C ≤ Tj ≤ 175°C unless otherwise noticed. All voltages refer to GND pin.

Table 62. Power supply electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
VDD3-4 monitor							
t_an_chop_clock	analog chopping period	Guaranteed by scan	58	64	70	µs	-

17.1.3 Power supply error handling

Table 63. Power supply error handling

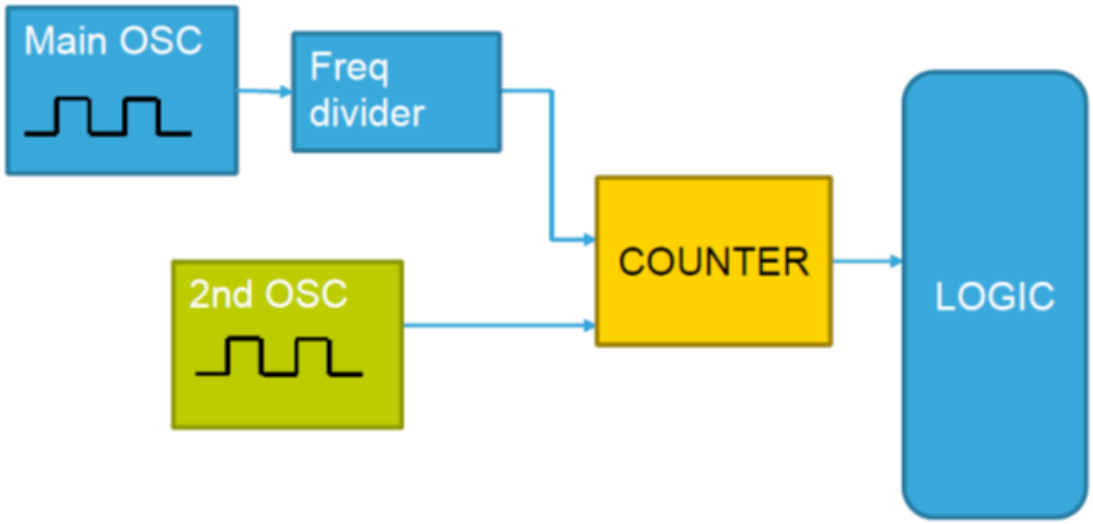
Type of error	Detection condition	Action	Clear SPI flag	Restart condition
VDD3				
VDD3 under voltage self test fail	On state, enabled through SPI bit **VDDx UV/OV Self Test Enable** (16) in **SERVENA** register	**Same as regulator fault detection, with additional VDDx OV/UV Self Test** bit (10) set in **SERVFLT** register	Clear on read	**Same as functional, self test enable to be re-enabled**
VDD3 over voltage self test fail	On state, enabled through SPI bit **VDDx UV/OV Self Test Enable** (16) in **SERVENA** register	**Same as regulator fault detection, with additional VDDx OV/UV Self Test** bit (10) set in **SERVFLT** register	Clear on read	**Same as functional, self test enable to be re-enabled**
VDD4				
VDD4 under voltage self test fail	On state, enabled through SPI bit **VDDx UV/OV Self Test Enable** (16) in **SERVENA** register	**Same as regulator fault detection, with additional VDDx OV/UV Self Test** bit (10) set in **SERVFLT** register	Clear on read	**Same as functional, self test enable to be re-enabled**
VDD4 over voltage self test fail	On state, enabled through SPI bit **VDDx UV/OV Self Test Enable** (16) in **SERVENA** register	**Same as regulator fault detection, with additional VDDx OV/UV Self Test** bit (10) set in **SERVFLT** register	Clear on read	**Same as functional, self test enable to be re-enabled**

17.2 Internal supply monitor

17.2.1 Reference Oscillator

A second trimmed 16 MHz oscillator runs in parallel with the main one and it is used to monitor its accuracy, if a frequency drift on any of the two oscillators happens a power down sequence is triggered with consequent reset generation and channel disabled; safe state lasts until the fail is recovered or the device is restarted by toggling of the wake pin. After system restart, if the fail is still present, the device enters the safe state condition again. Basic implementation of clock monitor is shown in the following figure.

Figure 65. **Oscillator monitor**



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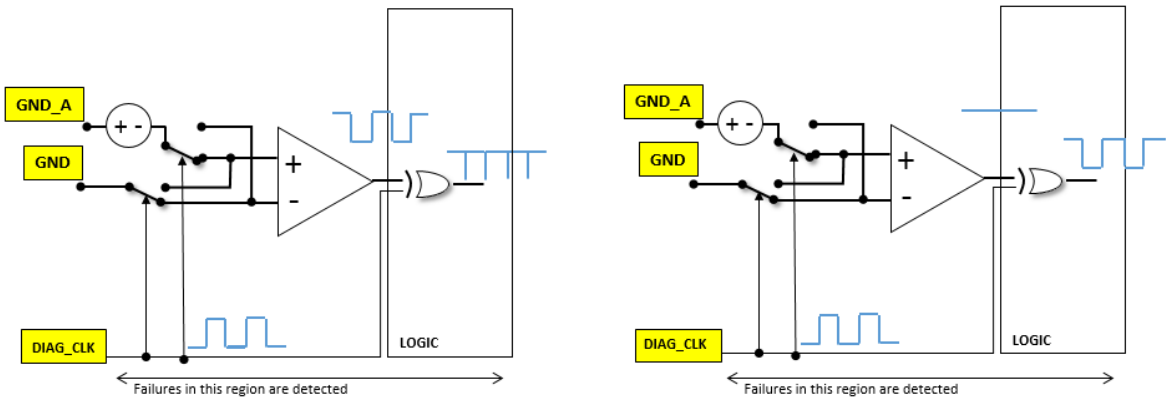
17.2.2 GND Loss Comparators

Ground loss comparators are monitored against latent fault through analog self-test. Self-test is automatically performed after analog trimming data download from EEPROM has been completed. In case of fault the dedicated warning flag is set to “high” in the Temperature sensor register. Structure of the analog self test is shown in the next figure.

Figure 66. **diagnostic analog self test basic implementation**



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17.2.3 Internal supply electrical characteristics

5.5 V ≤ VBATP≤ 19 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise noticed.
All voltages refer to GND pin.

Table 64. Internal supply electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Oscillator monitor							
fOSCINT_MON	Internal monitor Oscillator frequency		-7%	16	7%	MHz	
OSCMON_timeout	Timeout for stuck detection	Guaranteed by scan	7.6	8	8.5	µs	
OSC_freq_error	Max tolerable delta between oscillators	Guaranteed by scan	-17		20	%	
GND loss							
t_an_chop_clock	analog chopping period	Guaranteed by scan	12	16	20	µs	GND, GND_A
t_GND_selftest	GND loss self test duration	Guaranteed by scan	26	32	38	µs	GND, GND_A

17.2.4 Internal supply error Handling

Table 65. Internal supply monitor error type

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
Main/Safety Oscillator Out of frequency	On state	Power down sequence triggered with RES1-2 assertion. SPI fault bit **Main Oscillator Self check (15)** set in **SERVFLT** register	Clear on read	Automatic restart with retrigger of power-up sequence after fault disappears
GND loss self test fail	Power-up	Warning flag **GND Loss Selftest (10)** set in **TEMPSENS** register	Clear on read	N.A.
GND_A loss self test fail	Power-up	Warning flag **GND_A Loss Selftest (11)** set in **TEMPSENS** register	Clear on read	N.A.

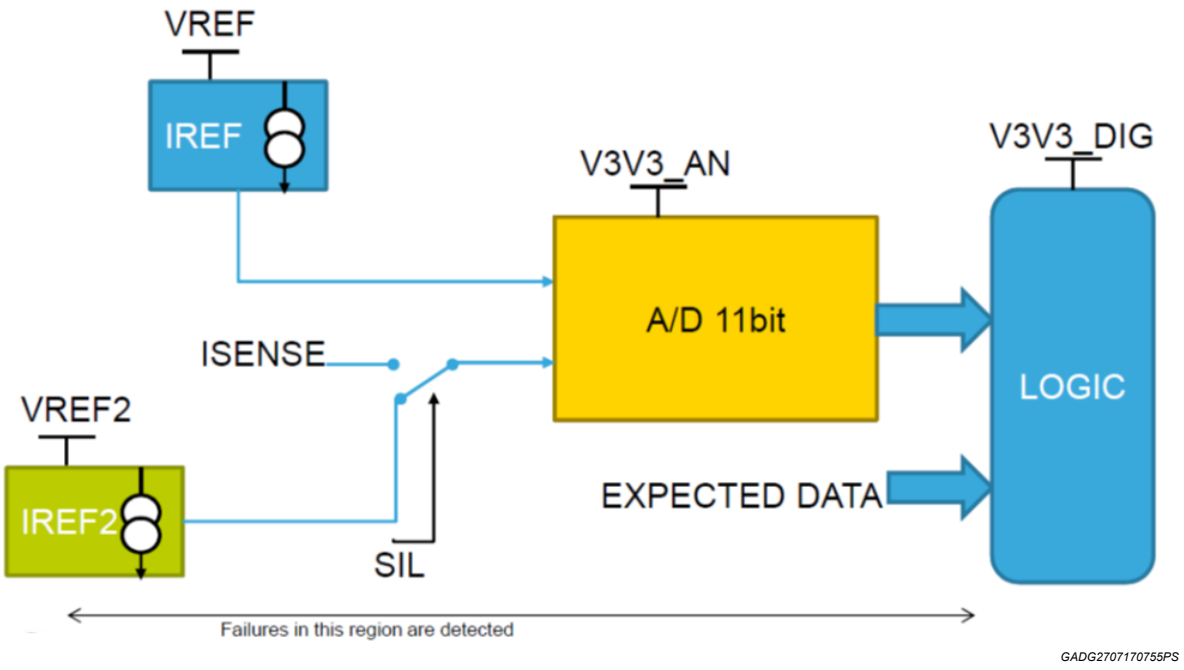
17.3 Valve drivers

17.3.1 Solenoid driver

ADC check

Current monitor function in valve drivers is achieved by means of two independent current sense circuits, one for the HS power stage and one for the LS power stage; their output is then MUXed to the ADC input to close control loop and calibration loop in the digital domain. This check is performed to guarantee ADC functionality using a safety reference in parallel to the main one; the check is available on demand selecting the corresponding bit in solenoid CONFIGURATION registers. This self test can be activated only if the channel is tristated since the current sense circuitry is inhibited during its actuation; solenoid ADC output and its reference are compared with auxiliary independent circuits, in case the output of the two conversions differs more than ±13 LSB a flag is set in the EXCEPTIONS register.

Figure 67. **ADC self-test block diagram**



Digital control loop logic BIST

This check is available on demand selecting the corresponding bit in solenoid CONFIGURATION registers. This self-test can be activated only if the channel is tristated since the control loop is inhibited during its actuation; logic BIST is performed on the logic core in charge of calibration of the solenoid a/d data and on the current control loop. In case the logic BIST fails a warning flag is set in the EXCEPTIONS register, the fault is cleared by reading the related SPI frame. The actual status of the test is mapped on two bits available in the EXCEPTIONS register, the test is in idle state as long as the CONFIGURATION bit is at 0.

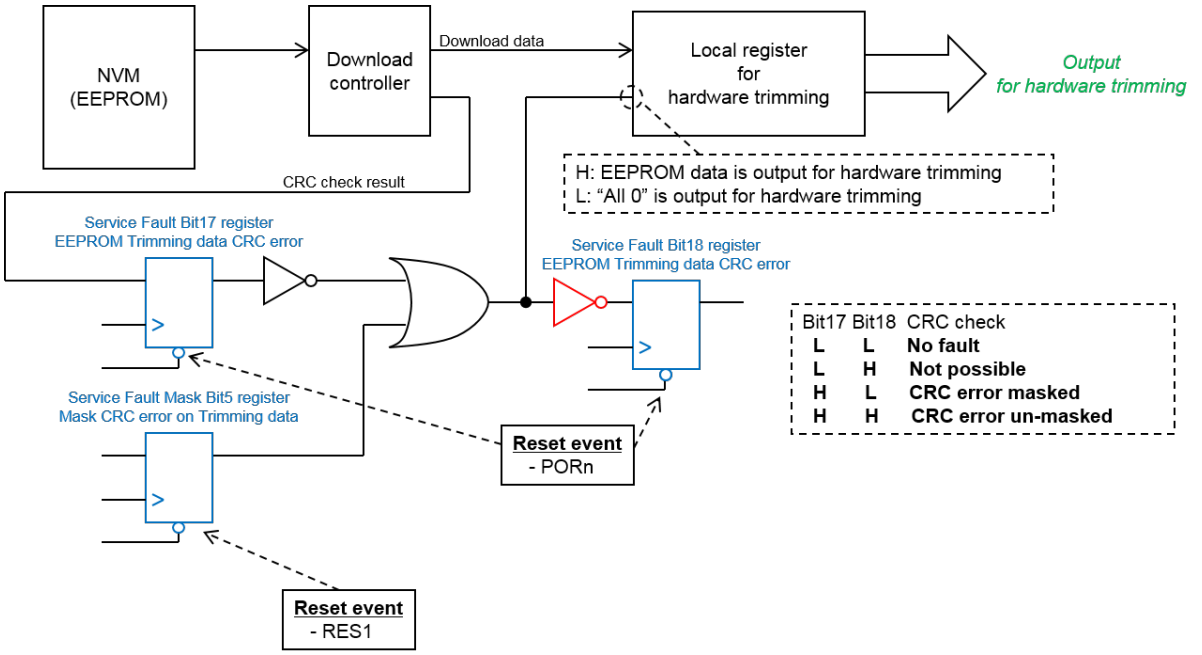
Calibration data check

Calibration data and analog trimming bits to compensate solenoid a/d errors and internal references are stored in an internal 8kbit NVM memory; memory data are combined in 256 bit sectors with the following architecture:

- 120 data bits
- 8 CRC bits
- 120 data bits
- 8 CRC bits

At each power-on reset release the logic core downloads these data into local registers; at each download the data integrity is verified by means of CRC check: in case the CRC check fails, a warning flag is set in the SERVICE FAULT register (error on analog trim) or Exceptions registers (error on channel calibration or ADC trimming) while local registers affected by the fault are loaded with a “all 0” default to avoid unpredictable operation. For debugging purpose, SPI bits are available to mask CRC result and force the usage of NVM memory data; for analog trimming data, the bit in Service Fault Mask register can be used, while for solenoid channels two bits are available for each channel in Driver Fault MASK registers. Analog trimming data, used by internal references, are downloaded only after a power-on reset event; in case CRC error happens and masking of the fault is used the wrong data are downloaded and cannot be reverted to “all 0” value until next turn-on of the device. Since mask bits are cleared by RES1 event the microcontroller could lose during operation the information on actual usage of analog trimming data, so CRC error bit is redunded with information sensitive to Service Fault Mask settings: in this way it is always possible to understand whether analog trimming data in usage are the masked one or the downloaded one. A simplified drawing of the masking concept is shown in the next figure, such a procedure is not implemented on Solenoid NVM data (calibration and ADC trim) since these data are downloaded each time a change in the configuration settings of solenoid channels is requested, so it is always possible to refresh solenoid bits and CRC check after a reset event.

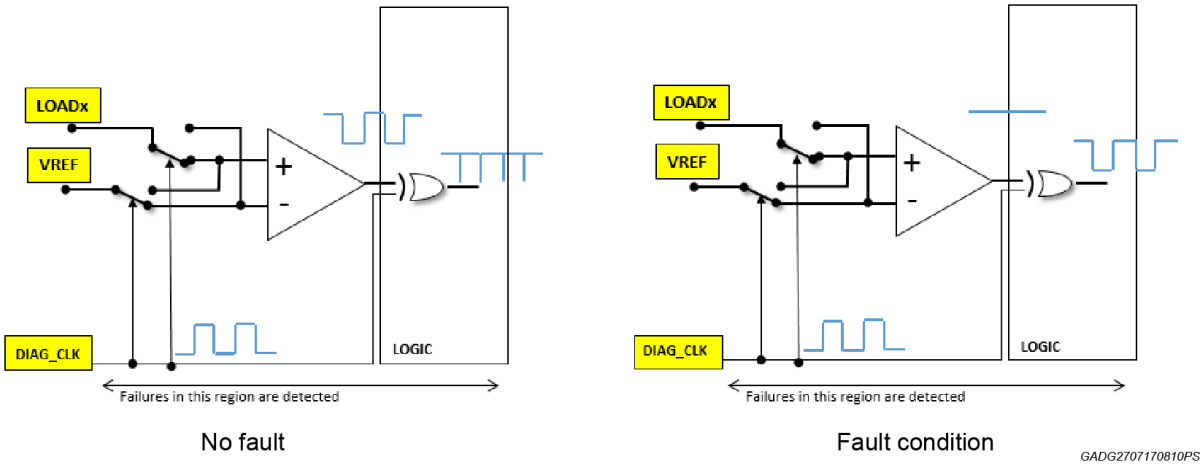
Figure 68. **Analog trimming mask concept**



Diagnostic comparators

The off-state diagnostic comparators have analog self test implemented to detect latent faults. Self test structure is shown in the next figure and it can be enabled through dedicated SPI bit, independent for each channel, only if the off state diagnostic is kept disabled. Once triggered, the self test is kept active until SPI bit removal or until enable of off state diagnostic; if analog self test fails a warning flag is set in the Exception registers, while off state diagnostic output is masked.

Figure 69. **Diagnostic analog self test basic implementation**

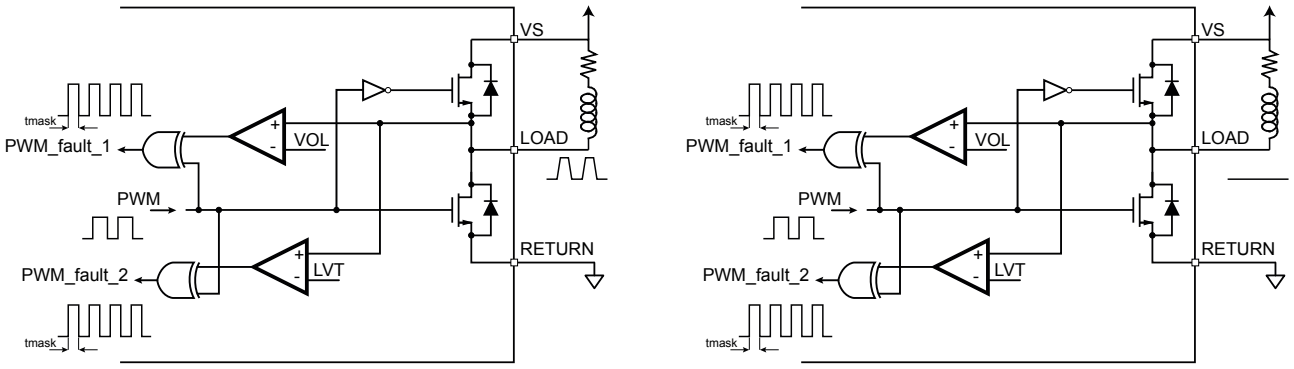


PWM check

Off-state diagnostic comparators can be used during on state functionality to compare the status of output stage with respect to the PWM input coming from control logic. These comparators start working after an auto-adaptative masking time, dependent on the slew rate settings to take into account the time needed for slew rate control to settle the output voltage. If the output status then differs from PWM input a fault bit is latched in the SPI Exception registers (for information only). For redundancy, the fault bit is available for both diagnostic

comparators (open load and lvt) and can be cleared on read. Self test behavior for LS configuration is shown as an example in the figure below. In case self test is activated with PWM functionality already running an initial spurious fail can be triggered and must be cleared to validate the self test result.

Figure 70. PWM test implementation assuming LS configuration



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17.3.2 Valve drivers electrical characteristics

5.5 V ≤ VBATP ≤ 19 V; 5.5 V ≤ VSx ≤ 19 V; -40 °C ≤ Tj ≤ 175 °C unless otherwise noticed. All voltages refer to GND pin.

Table 66. Valve drivers electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
Solenoid Drivers							
ADC_sampling_freq	Sampling frequency	Guaranteed by scan	-5%	8	5%	MHz	
IADC_test	ADC test current		29	30	31	µA	
ADC_LSB	ADC resolution		0.89	0.9375	0.985	µA	
ADC_check	Tolerable mismatch between functional and safety ADCs	Guaranteed by scan	-13		13	LSB	LOADx
t_ADC_check	Self test duration	Guaranteed by scan, all channels monitored	0.1	0.25	0.3	ms	LOADx
t_BIST	Solenoid Logic BIST duration	Guaranteed by scan	1		5	ms	LOADx
t_EEPROM	EEPROM download time	Time to read entire content of EEPROM from CP_uv release Guaranteed by scan	1	3.5	4	ms	
t_EEPROM_sol	EEPROM download time solenoid	Time to read calibration data after 1 configuration change request in a channel pair (ex. CH0/1 LL --> LH) Guaranteed by scan	1	3.5	4	ms	
t_EEPROM_sol2	EEPROM download time solenoid_2	Time to read calibration data after both configurations change in a channel pair (ex. CH0/1 LL --> HH) Guaranteed by scan	1	7	8	ms	
tmask	PWM check masking time	Solenoid ON state, Guaranteed by design	2		200	µs	LOADx
t_an_chop_clock	analog chopping period	Guaranteed by scan	250	300	350	µs	

17.3.3 Valve drivers error handling

Table 67. Valve driver error handling

Type of error	Detection condition	Action	Clear SPI flag	Restart condition
ADC check	Tristate condition	**Solenoid A/D self check** bit set in **Exceptions** registers	Clear on read	N.A.
Logic BIST fail	Tristate condition	Faulted channel kept tristated until fault is present. **Solenoid Logic BIST Status** bit (10:9) available on **Exceptions** registers	Clear on read	Clear diagnostic bits and set DRVENAx bits in SolEnDRV registers
CRC check analog	On state	Trimming bits masked with default configuration, warning flags EEPROM Trimming data CRC (18:17) set in SERVFLT register	Clear on PORn	Restart of the device or masking of CRC result with Mask CRC error on Trimming data bit (5) in SERVFLTMSK register
CRC check Solenoid	On state	Trimming bits masked with default configuration, warning flags CRC error (14:13) set in Exceptions registers	Clear on PORn	Re-enable of the solenoid channels or masking of CRC result with CRC Error Mask (14:13) bits in DRVFLTMSK registers
Off state diagnostic self test	Tristate, diagnostic disabled	Warning flag **Solenoid Diag Self Test(OFF state)** (8:7) in **Exceptions** registers	Clear on read	N.A.
PWM check	On state	Warning flag **Comparators Self Test (Active) status** (12:11) in **Exceptions** registers	Clear on read	N.A.

18 Functional table

The functionality behavior of the device is summarized in the following figure.

Figure 71. Functional table diagram

	VBATP							3V3	Charge pump	VDD1	VDD3		VDD4		Thermal				WDT		EXT-RES	GND-LOSS
	VB_UV1 [V]	VB_UV2 [V]	VB_LV1 [V]	VB_LV2 [V]	Normal [V]	VB_HV [V]	VB_OV [V]	3V3 internal [V]	VCP UV [V] (A)	VDD1_UV [V] during power up	VDD3_UV [V] (B)	VDD3_OV [V]	VDD4_UV [V]	VDD4_OV [V]	Over Temperature [°C] (internal)	Over Temperature [°C] (VDD1)	Over Temperature [°C] (VDD2/TRK)	Over Temperature [°C] (Driver)	O&AWDT	WDT	RES1 driven low by externa	AGND or GND loss
	3 -3.8	3.8 - 55	5.5 - 6	6 - 7.5	7.5 - 19	19 - 27	27 - 36	2.6 - 3	VCP > VBATP + 5V	VDD1 < VDD_STEN	9.1/10-9.6/10	11/10-11.8 /10	9.1/10 - 9.6/10	11/10-11.8/10	175-185	175-185	175-185	185-195	-	-	-	-
V33_AN / V33_D1G	●	To be defined by (A) or (B)	○	○	○	Jump start: degradation allowed	●	●	○	○	○	○	○	○	○	○	○	○	○	○	○	●
VDD1	▲		●	●	○		●	▲	●	-	○	○	○	○	▲	▲	○	○	○	○	○	▲
VDD2	▲		●	○	○		●	▲	△	▲	○	○	○	○	▲	▲	▲ T	○	○	○	○	▲
VDD3	▲		○	○	○		●	▲	●	▲	-	-	○	○	▲	▲	○	○	○	○	○	▲
VDD4	▲		○	○	○		●	▲	●	△	○	○	-	-	▲	▲	○	○	○	○	○	▲
CAN-TX	▲		○	○	○		●	▲	△	○	△	△	△	△	▲	△	○	○	○	○	○	▲
CAN-RX	●		○	○	○		●	●	○	○	○	○	○	○	●	○	○	○	○	○	○	●
Charge Pump	▲		○	○	○		●	▲	-	▲	○	○	○	○	○	○	○	○	○	○	○	●
Pump Pre-Driver	▲		○	○	○		▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲
Failsale Pre-Driver	▲		○	○	○		▲	▲	●	▲	▲	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲
TRK1-4	▲		●	○	○		●	▲	●	▲	○	○	○	○	▲	▲	▲ T	○	○	○	○	▲
Solenoid	▲		●	○	○		▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	○	▲ T	▲	▲	▲	▲
Register	▲		○	○	○	○	○	▲	○	▲	▲	▲	▲	▲	▲	▲	○	○	▲	▲	▲	▲
Power up/down	▲		○	○	○	○	○	▲	○	▲	○	○	○	○	○	○	○	○	○	○	○	▲
Q&A WDT	▲		○	○	○	○	○	▲	△	-	▲	▲	▲	▲	▲	▲	○	○	-	▲	○	▲
PRUN WDT	▲		○	○	○	○	○	▲	△	▲	▲	▲	▲	▲	▲	▲	○	○	▲	-	○	▲
GPO	▲		○	○	○	●	●	▲	△	▲	○	○	○	○	▲	▲	○	○	○	○	○	▲

○	Normal Operation
●	Degradation
▲	Direct Stop Part
△	Possible Stop Part depending on supply/reset domain
T	Disable the circuit in thermic
-	Detection Part

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19 Definitions and acronyms

Table 68. **Definitions and acronyms**

Reference	Description
ASIC	Application specific integrated circuit
BIST	Built-in self-test
ABIST	Analog built-in self-test
LS	Low–side
HS	High–side
HW	Hardware
SW	Software
KA	Keep alive
PHOLD	Power hold
SPI	Serial peripheral interface
SDI	Serial data-in
SDO	Serial data-out
I/O	Input output
CS	Chip select
SCLK	Serial clock
NVM	Non volatile memory
CRC	Cyclic redundancy check
SCG	Short circuit to GND
STB	Short circuit to battery
OL	Open load
UV	Under voltage
OV	Over voltage
OT	Over temperature
TSD	Thermal shutdown
MSB	Most significant bit
LSB	Least significant bit
MCU	Microcontroller unit
µC	Microcontroller
PORn	Power-on reset active low
VDA	Verband der automobilindustrie
WDT	Watchdog timer
Q&A	Query and answer
N.D.	Not detected
N.A.	Not available

20 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

20.1 TQFP80 (14x14x1 mm. exp. pad up) package information

Figure 72. TQFP80 (14x14x1 mm. exp. pad up) package outline

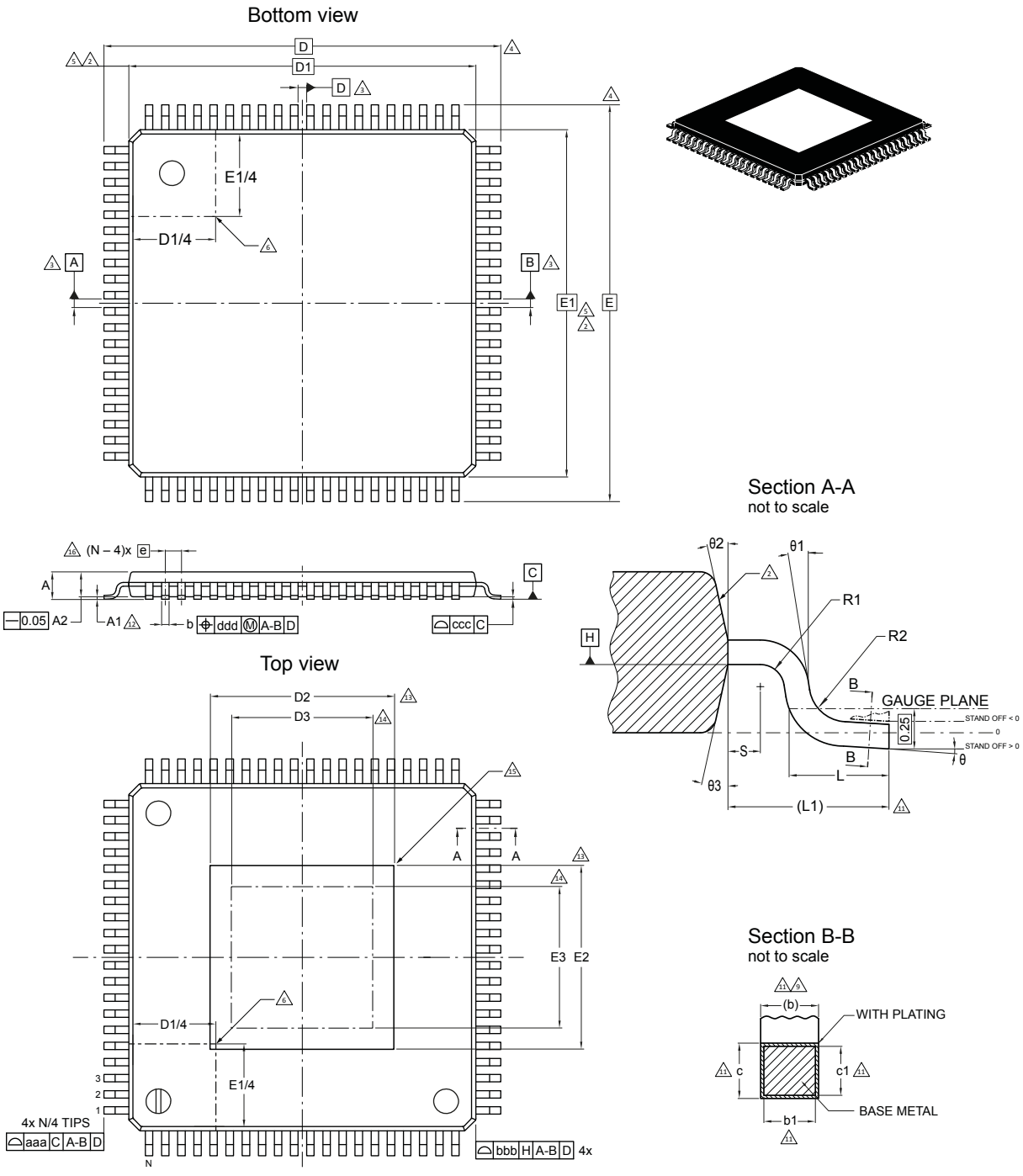


Table 69. TQFP80 (14x14x1 mm. exp. pad up) package mechanical data

Symbol	Min.	Nom.	Max.	Note
ϴ	0°	3.5°	7°	
ϴ1	0°	-	-	

Symbol	Min.	Nom.	Max.	Note
Θ2	10°	12°	14°	
Θ3	10°	12°	14°	
A	-	-	1.09	15
A1	-0.04	-	0.04	12
A2	0.95	1.00	1.05	15
b	0.22	0.32	0.38	9, 11
b1	0.22	0.30	0.33	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	16.00 BSC			4
D1	14.00 BSC			2, 5
D2	-	-	8.27	13
D3	6.78	-	-	14
e	0.65 BSC			
E	16.00 BSC			4
E1	14.00 BSC			2, 5
E2	-	-	8.27	13
E3	6.78	-	-	14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	80			16
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
Tolerance of form and position				
aaa	0.20			1, 7
bbb	0.20			
ccc	0.10			
ddd	0.13			

Notes:

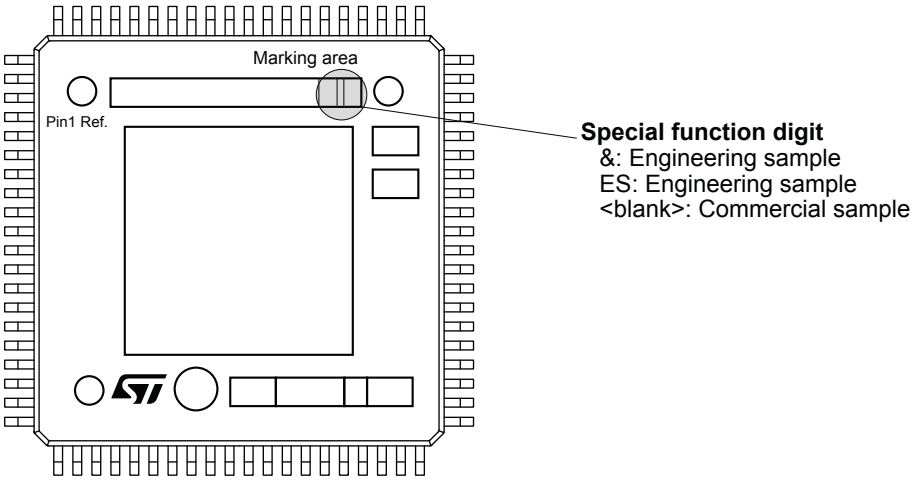
1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower

radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

20.2 TQFP80 (14x14x1 mm. exp. pad up) marking information

Figure 73. TQFP80 (14x14x1 mm. exp. pad up) marking information



Parts marked as ‘ES’ or ‘&’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production.

ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

20.3 TQFP80 (14x14x1 mm. exp. pad down) package information

Figure 74. **TQFP80 (14x14x1 mm. exp. pad down) package outline**

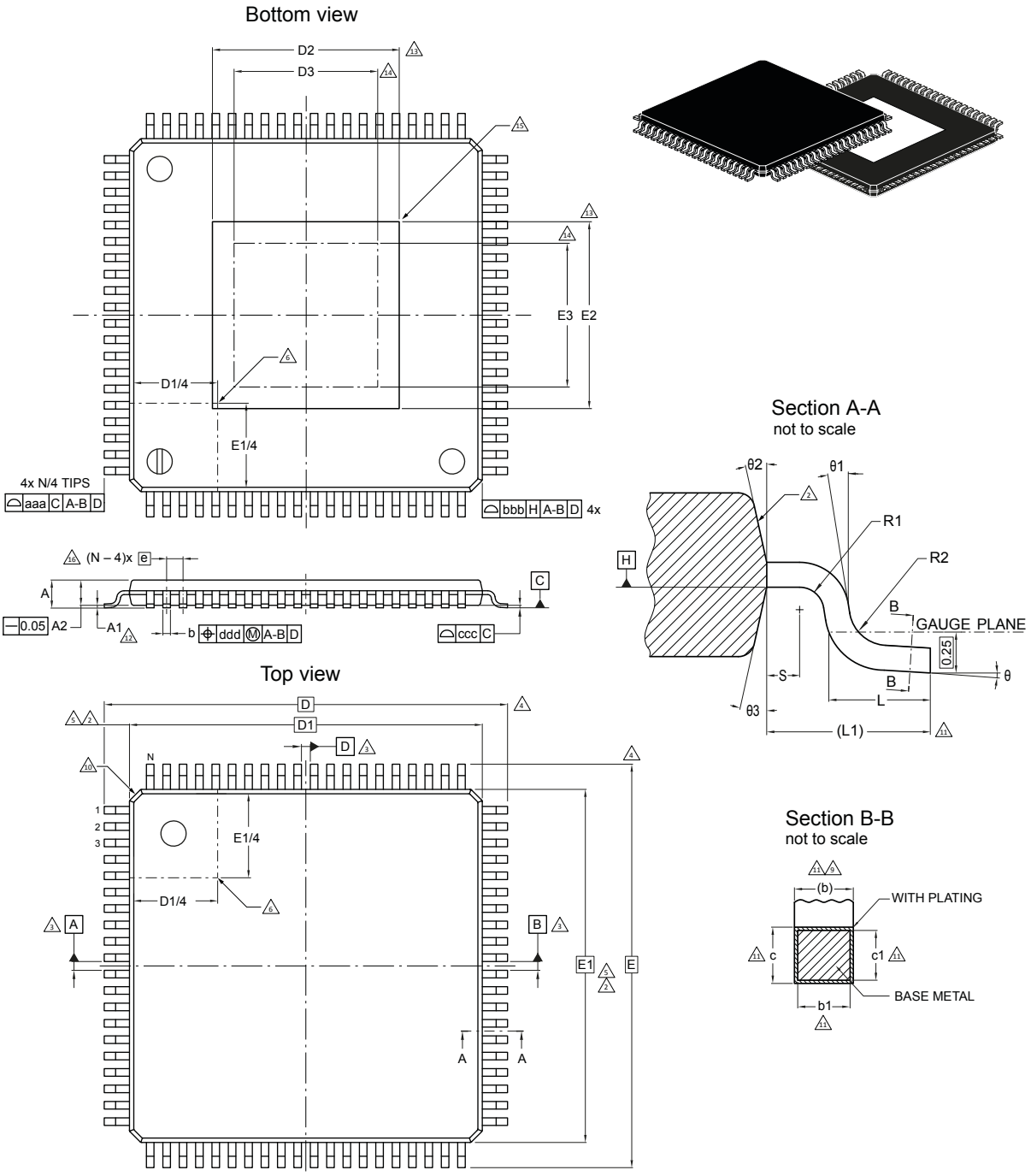


Table 70. **TQFP80 (14x14x1 mm. exp. pad down) package mechanical data**

Symbol	Min.	Nom.	Max.	Note
ϴ	0°	3.5°	7°	
ϴ1	0°	-	-	

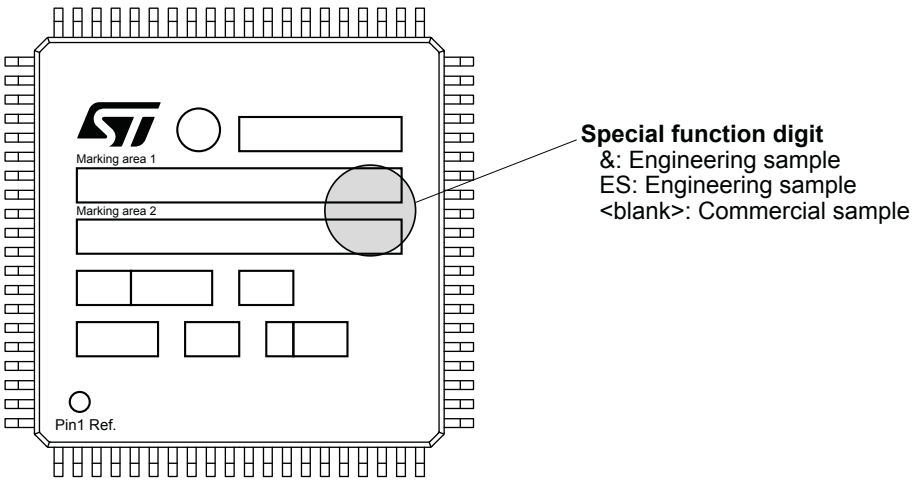
Symbol	Min.	Nom.	Max.	Note
Θ2	10°	12°	14°	
Θ3	10°	12°	14°	
A	-	-	1.20	15
A1	0.05	-	0.15	12
A2	0.95	1.00	1.05	15
b	0.22	0.32	0.38	9, 11
b1	0.22	0.30	0.33	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	16.00 BSC			4
D1	14.00 BSC			2, 5
D2	Variations			13
D3	Variations			14
e	0.65 BSC			
E	16.00 BSC			4
E1	14.00 BSC			2, 5
E2	Variations			13
E3	Variations			14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	80			16
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	
Tolerance of form and position				
aaa	0.20			1, 7
bbb	0.20			
ccc	0.10			
ddd	0.13			
Variations				
PAD OPTION 4.5x4.5				
D2	-	-	4.71	
E2	-	-	4.71	
D3	3.28	-	-	
E3	3.28	-	-	
PAD OPTION 8.0x8.0				
D2	-	-	8.27	
E2	-	-	8.27	
D3	6.78	-	-	
E3	6.78	-	-	

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

20.4 TQFP80 (14x14x1 mm. exp. pad down) marking information

Figure 75. TQFP80 (14x14x1 mm. exp. pad down) marking information



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Parts marked as ‘ES’ or ‘&’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production.

ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 71. **Document revision history**

Date	Version	Changes
02-Oct-2017	1	Initial release.
20-Dec-2017	2	Added Section 7.6 Power up/down electrical characteristics. Revised Section 10.2 Fail-safe pre-driver.
18-Mar-2019	3	Updated various electrical parameters.

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