

AK8772

Shipped in packet-tape reel(5000pcs/Reel)

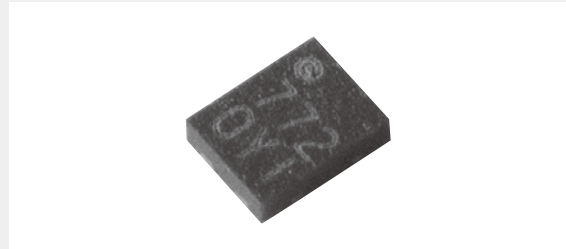
AK8772 is ultra-small Hall effect IC of a single silicon chip composed of Hall element and a signal processing IC.

| | | | | | |
|---------------------------|-------------------------|---------------------|-----------------------------------|-------------|-----|
| Bipolar Hall Effect Latch | Supply Voltage 1.6~5.5V | Power down Function | Ultra High Sensitivity Bop: 1.8mT | Output CMOS | SON |
|---------------------------|-------------------------|---------------------|-----------------------------------|-------------|-----|

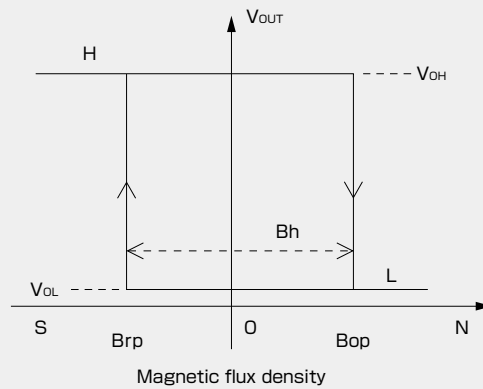
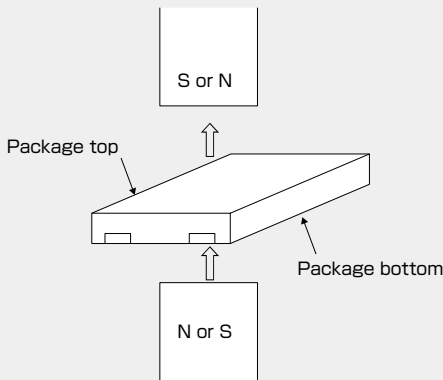
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●Features

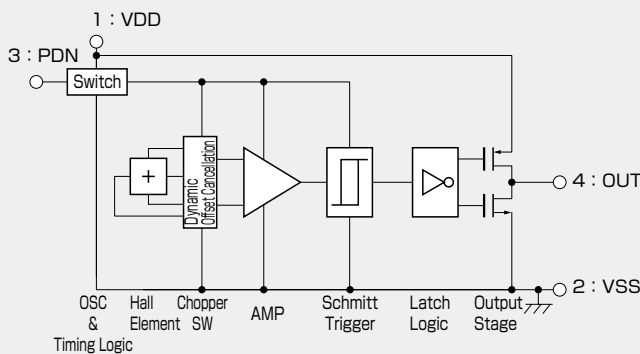
- Precision Bipolar Hall Effect Latch
- Power manageability through "PDN" pin
Current consumption in Power down mode is less than 1 μ A
- Low current consumption at active mode : less than avg. 150 μ A@V_{DD}=3V
- Ultra small SON package : 1.1 × 1.4 × t0.37mm, Halogen free



●Operational Characteristics



●Functional Block Diagram



| Item | Function |
|--------------------------|--|
| OSC | Generates operating clock |
| Timing Logic | Generates timing signal requires for Chopper SW, AMP and other circuits |
| Hall Element | Hall element fabricated by CMOS process |
| Chopper SW | Performs chopping in order to cancel the offset voltage of Hall sensor |
| AMP | Reduce offset voltage and amplifies Hall output voltage |
| Schmitt Trigger | Hysteresis comparator |
| Latch Logic Output Stage | CMOS output, During the power down mode, output is latched in its previous state |

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●Absolute Maximum Ratings

| Item | symbol | Min. | Max. | Unit | Note |
|----------------------|------------------|------|-----------------------|------|------|
| Power supply voltage | V _{DD} | -0.3 | +6.5 | V | |
| Output current | I _{OUT} | -0.5 | +0.5 | mA | OUT |
| Input voltage | V _{IN} | -0.3 | V _{DD} +0.3* | V | PDN |
| Input current | I _{IN} | -10 | +10 | mA | PDN |
| Storage temperature | T _{STG} | -55 | +125 | °C | |

*) Less than +6.5V.

Note) Stress beyond these listed values may cause permanent damage to the device.

●Recommended Operating Conditions

| Item | symbol | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------|------|------|------|------|
| Power supply voltage | V _{DD} | 1.6 | 3.0 | 5.5 | V |
| Operating temperature | T _a | -30 | | +85 | °C |

●Electrical Characteristics (T_a=25°C V_{DD}=3.0V)

| Item | symbol | Min. | Typ. | Max. | Unit | Note |
|----------------------------|------------------|----------------------|------|--------|------|------------------------------|
| Current consumption 1 | I _{DD1} | | | 1 | μA | PDN=0V |
| Current consumption 2 | I _{DD2} | | 60 | 150 | μA | PDN=V _{DD} ,Average |
| PDN input current | I _{IN} | -1 | | 1 | μA | |
| PDN input H voltage | V _{IH} | 0.7V _{DD} | | | V | |
| PDN input L voltage | V _{IL} | | | 0.3 | V | |
| High level output voltage | V _{OH} | V _{DD} -0.4 | | | V | I _{OUT} =-0.5mA |
| Low level output voltage | V _{OL} | | | 0.4 | V | I _{OUT} =+0.5mA |
| PDN mode transition time 1 | T _{PD1} | | | (36.6) | μs | *Active→PDN |
| PDN mode transition time 2 | T _{PD2} | | | 100 | μs | PDN→Active |
| Pulse drive period | T _{PD3} | 0.5 | 1.0 | 1.5 | ms | When PDN=V _{DD} |
| Pulse drive time | T _{PD4} | 12.2 | 24.4 | 36.6 | μs | |
| PDN 'H' input pulse width | T _w | 100 | | | μs | |

*) This transition time is not guaranteed by inspection because PDN input timing and internal timing are asynchronous

●Magnetic Characteristics① (T_a=25°C V_{DD}=3.0V)

| Item | symbol | Min. | Typ. | Max. | Unit |
|-----------------|-----------------|------|------|------|------|
| Operating point | B _{op} | | 1.8 | 4.0 | mT |
| Releasing point | B _{rp} | -4.0 | -1.8 | | mT |
| Hysteresis | B _h | | 3.6 | | mT |

●Magnetic Characteristics② (T_a=-30~+85°C V_{DD}=1.6~5.5V)

| Item | symbol | Min. | Typ. | Max. | Unit |
|-----------------|-----------------|------|------|------|------|
| Operating point | B _{op} | | 1.8 | 4.2 | mT |
| Releasing point | B _{rp} | -4.2 | -1.8 | | mT |
| Hysteresis | B _h | | 3.6 | | mT |

Note) The specifications in Magnetic Characteristics ② are design targets.

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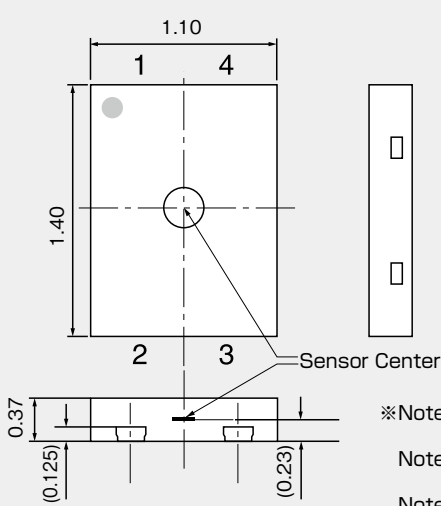
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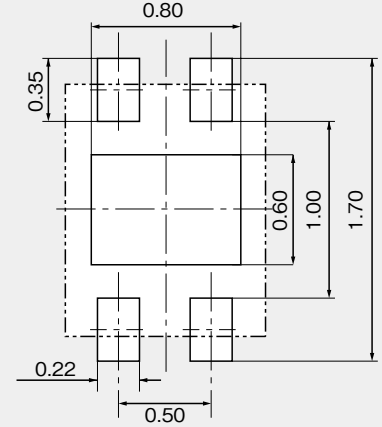
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●Package (Unit:mm)



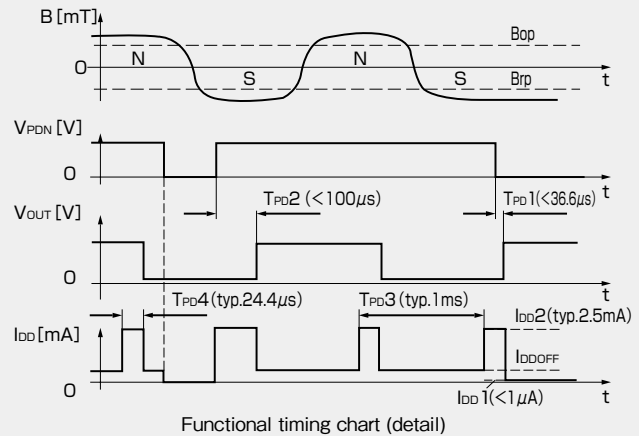
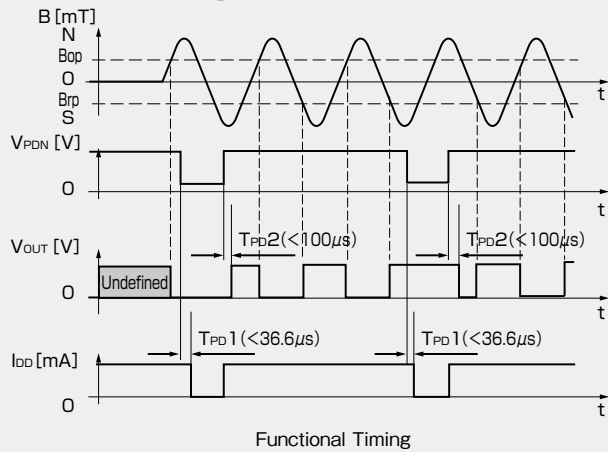
- ※Note 1) Sensitive area position referenced to the center of package within $\phi 0.3\text{mm}$ circle.
- Note 2) Tolerances of dimension otherwise noted is $\pm 0.05\text{mm}$.
- Note 3) Hatched area is plated.
- Note 4) Center pad area (TAB) should be tied to the VSS or floating

●Footprint (for reference)



| No. | Pin name | Function | Note |
|-----|----------|--|---|
| 1 | VDD | Power supply | |
| 2 | VSS | Ground | |
| 3 | PDN | Power down H:Device active L:Device power down | CMOS Input. This pin has to be tied to "H" level when external power control is not used. |
| 4 | OUT | Output | CMOS Output |

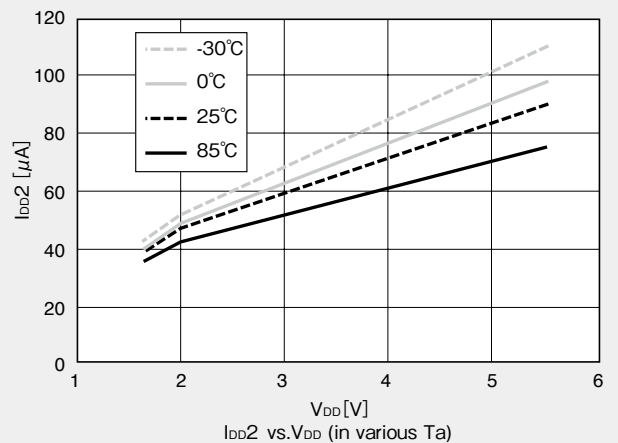
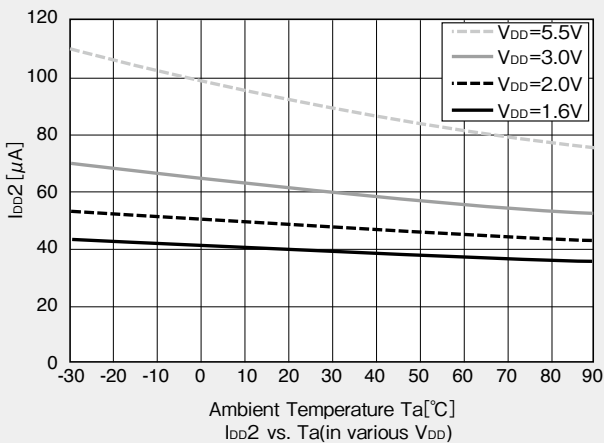
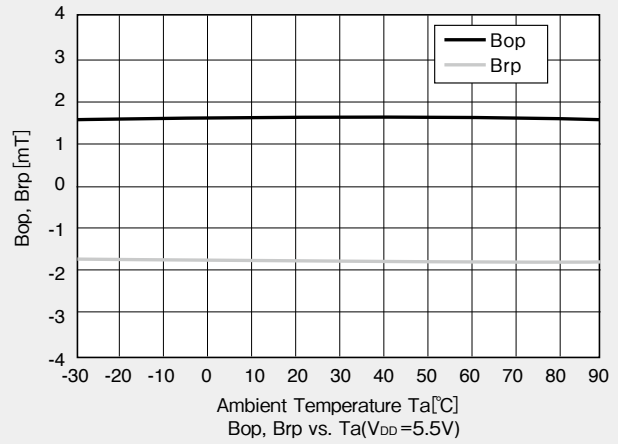
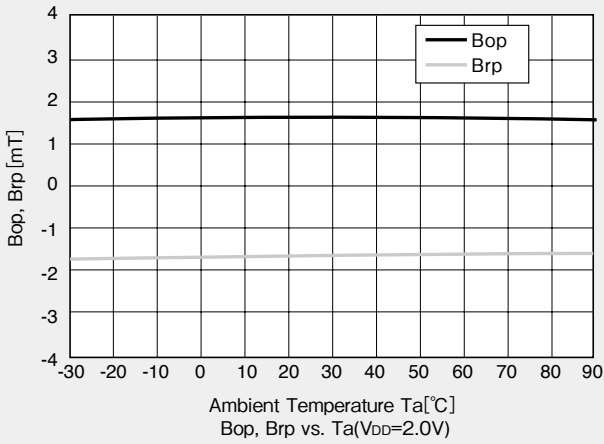
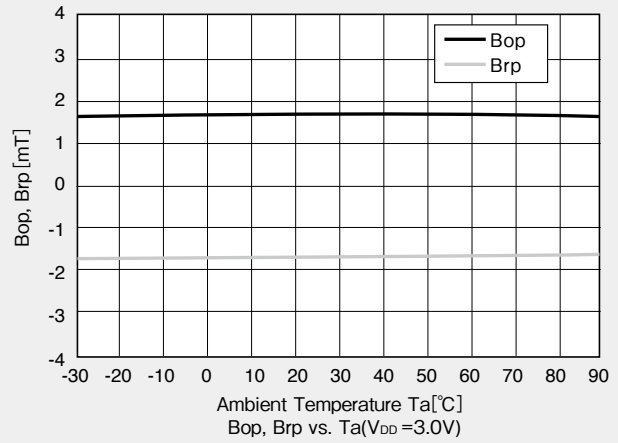
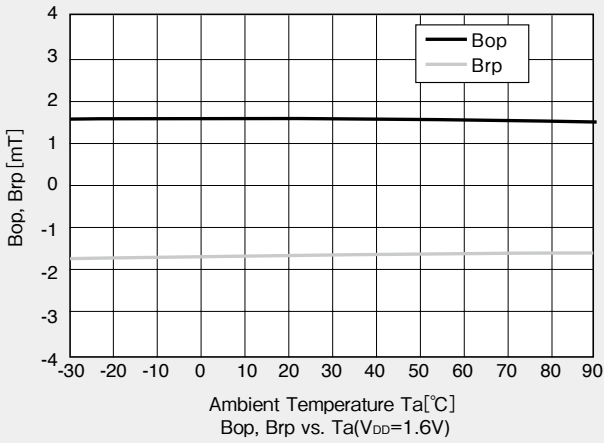
●Function Timing Chart



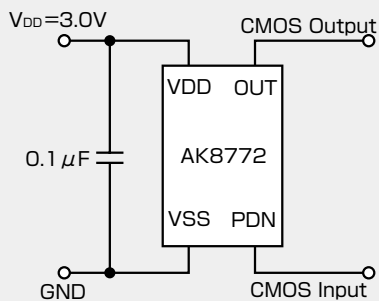
- Note 1) During power down mode, output is latched in its previous state.
- Note 2) When VDD is supplied, the time from reaching $V_{DD} = 1.6\text{V}$ to the update of the output state is equal to T_{PD2} .

When PDN pin set to 'L' from 'H' during sampling is performing, the device transits to power down mode after sampling is completed. And when PDN pin set to 'L' from 'H' while sampling is not performing, the device transits to power down mode immediately.

● Typical Characteristic Data (for reference)



● Application Circuit



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April 1, 2015