

ISL55016

MMIC Silicon Bipolar Differential Amplifier

FN6526
Rev 0.00
Jun 24, 2008

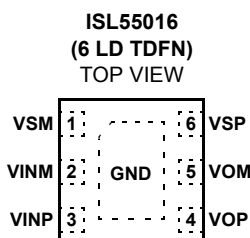
The ISL55016 is a high performance gain block which can match a 75Ω single-ended source to a 100Ω differential load. This feature makes the ISL55016 ideal for a wide range of general-purpose applications such as Satellite TV. The ISL55016 can be used as single-ended to differential converter and eliminates the need for an external balun structure.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55016IRTZ-T7*	M9	-40 to +85	6 Ld TDFN	L6.1.6x1.6B

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VSM	Ground
2	VINM	Single-Ended Input. VINM should be AC-Coupled.
3	VINP	AC Ground
4, 5	VOP, VOM	Differential outputs. VOP and VOM should be AC-Coupled. Differential Impedance 100Ω.
6	VSP	Power supply. +5V

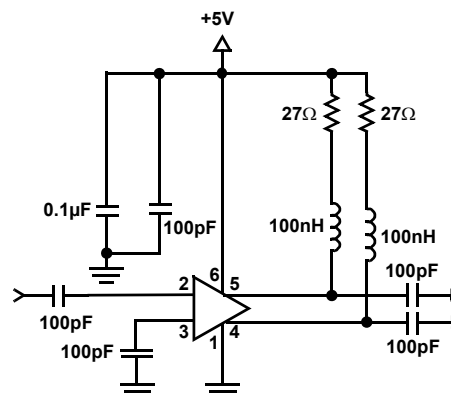
Features

- Input Impedance of 75Ω Single-Ended
- Output Impedance of 100Ω Differential
- Noise Figure of 5.4dB
- OIP3 of 26dBm
- Input Return Loss of 27dB
- Pb-Free (RoHS Compliant)

Applications

- Active Balun Function
- LNB and LNB-T (HDTV) Amplifiers
- IF Gain Blocks for Satellite and Terrestrial STBs
- PA Driver Amplifier
- Wireless Data, Satellite
- Bluetooth/WiFi
- Satellite Locator and Signal Strength Meters

Typical Application Circuit



Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

Supply Voltage from VSP to GND	5.75V
Input Voltage	$V_{S+} + 0.3\text{V}$ to GND -0.3V
ESD Rating	
Human Body Model (Per MIL-STD-883 Method 3015.7)	3kV
Machine Model (Per EIAJ ED-4701 Method C-111)	300V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^\circ\text{C}/\text{W}$)
6 Ld TDFN Package	125
Storage Temperature	-65°C to $+125^\circ\text{C}$
Operating Junction Temperature	$+135^\circ\text{C}$
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications VSP = +5V, $Z_{RSC} = 50\Omega$ single-ended connected to VINM, $Z_{LOAD} = 100\Omega$ differential across VOM and VOP, VINP AC-grounded, $T_A = +25^\circ\text{C}$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
VSP	Supply Voltage		4.5	5.0	5.5	V
I_VSP	Operating Current		91	104	117	mA
Sds21_diff	Small Signal Gain, Differential	50MHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		17.5		dB
		1.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		17.1		dB
		2.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		15.5		dB
Ssd12_diff	Reverse Isolation, Differential	50MHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		28.4		dB
		1.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		30.2		dB
		2.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		36.3		dB
Sss11_SE	Input Return Loss, Single-Ended	50MHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		27.1		dB
		1.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		15.1		dB
		2.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		6.9		dB
Sdd22_diff	Output Return Loss, Differential	50MHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		17.4		dB
		1.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		10.6		dB
		2.0GHz $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$		5.6		dB
S21_SE	Gain of Pin VOP, Single-Ended	50MHz	13.2	14.5	15.7	dB
		1.0GHz	12.9	14.0	15.4	dB
		2.0GHz	12.0	12.9	14.5	dB
S31_SE	Gain of Pin VOM, Single-Ended	50MHz	12.9	14.1	15.4	dB
		1.0GHz	12.4	13.5	14.9	dB
		2.0GHz	11.3	12.1	13.8	dB
P1dB_diff	Output Power at 1dB Compression Point, Differential	50MHz, (Note 2)	15	17.2	19	dBm
		1.0GHz, (Note 2)	13.9	15.8	17.9	dBm
		2.0GHz, (Note 2)	10.4	12.0	14.4	dBm
OIP3_4_SE	Output Third Order Intercept Point at VOP Pin, Single-Ended	f1 = 50MHz, f2 = 55MHz	22.7	27.5	32.7	dBm
		f1 = 1.0GHz, f2 = 1.1GHz	22.1	24.2	29.1	dBm
		f1 = 2.0GHz, f2 = 2.1GHz	16.2	18.1	22.2	dBm
OIP3_5_SE	Output Third Order Intercept Point at VOM Pin, Single-Ended	f1 = 50MHz, f2 = 55MHz	22.6	26.6	32.6	dBm
		f1 = 1.0GHz, f2 = 1.1GHz	21.9	23.6	27.9	dBm
		f1 = 2.0GHz, f2 = 2.1GHz	14.9	17.3	21.4	dBm

Electrical Specifications VSP = +5V, Z_{RSC} = 50Ω single-ended connected to VINM, Z_{LOAD} = 100Ω differential across VOM and VOP, VINP AC-grounded, T_A = +25°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
OIP3_diff	Output Third Order Intercept Point, Differential	f1 = 50MHz, f2 = 55MHz		29.1		dBm
		f1 = 1.0GHz, f2 = 1.1GHz		26.2		dBm
		f1 = 2.0GHz, f2 = 2.1GHz		20.2		dBm
OIP2_diff	Output Second Order Intercept Point, Differential	f1 = 50MHz, f2 = 55MHz, IM2 @105MHz		54.5		dBm
		f1 = 1.0GHz, f2 = 1.1GHz, IM2 @ 2.1GHz		58.6		dBm
		f1 = 2.0GHz, f2 = 2.1GHz, IM2 @ 4.1GHz		61.7		dBm
BW_diff	3dB Bandwidth, Differential	3dB below Gain @ 50MHz		2.2		GHz
NF_diff	Noise Figure, Differential	1.0GHz		5.4		dB
FREQ	Frequency Range		0.05		3	GHz

NOTE:

- The numbers are derived from the single-ended results.

Typical Performance (I) $Z_{RSC} = 75\Omega$, $Z_{LOAD} = 100\Omega$ Differential, $Z_{LOAD} = 25\Omega$. Common

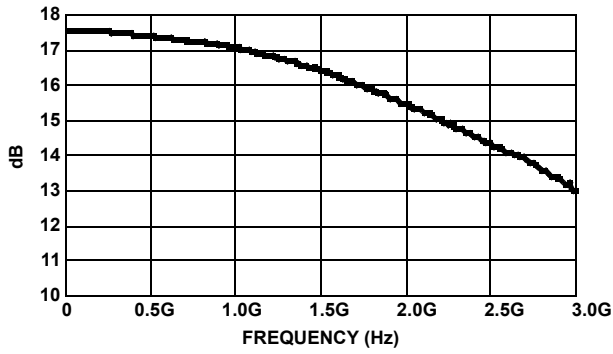


FIGURE 1. |Sds21| vs FREQUENCY

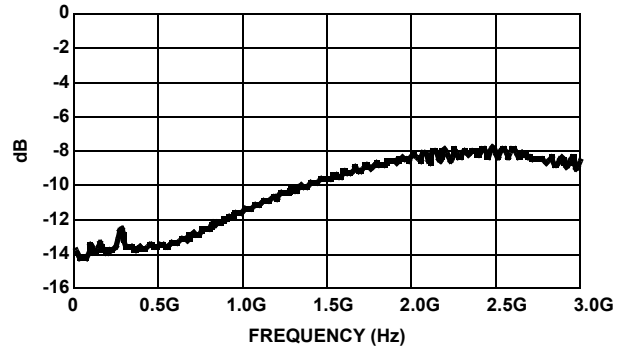


FIGURE 2. |Scs21| vs FREQUENCY

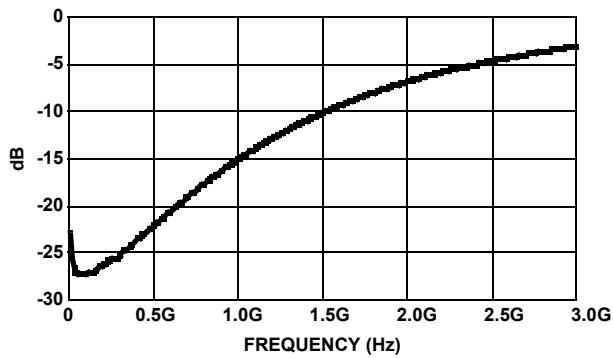


FIGURE 3. |S11| vs FREQUENCY

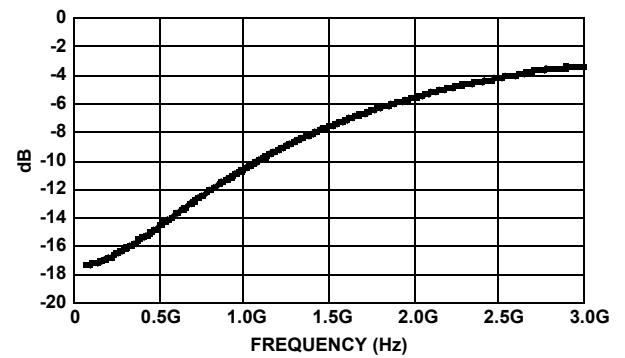


FIGURE 4. |Sdd22| vs INPUT POWER

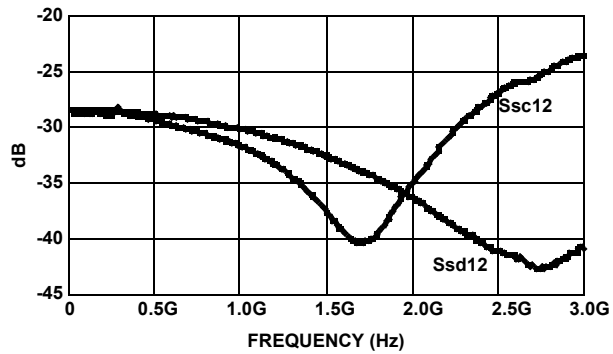


FIGURE 5. |Ssd12| AND |Ssc12| vs FREQUENCY

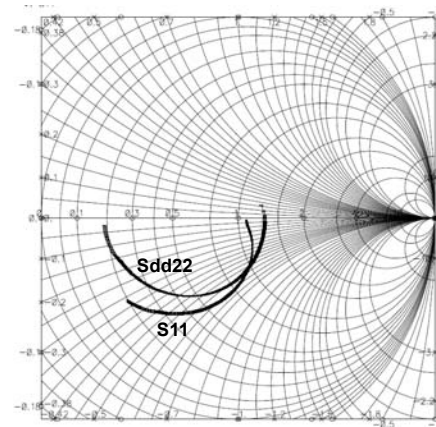


FIGURE 6. SMITH CHART OF S11 AND Sdd22

Typical Performance (II) 50Ω Environment, $Z_{RSC} = 50\Omega$, Z_{LOAD} Port 2 = 50Ω, Z_{LOAD} Port 3 = 50Ω; Measured on Probe Station.

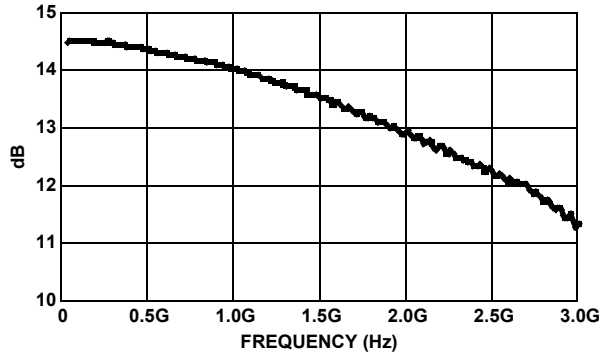


FIGURE 7. |S21| vs FREQUENCY

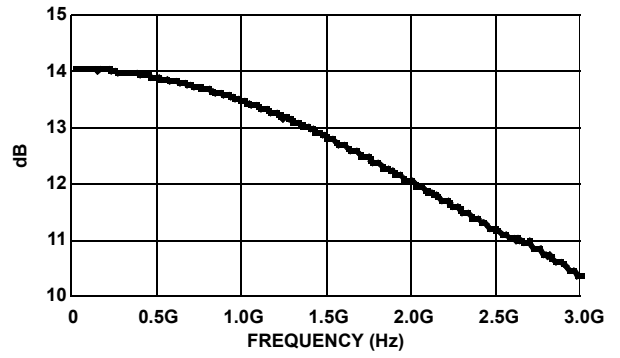


FIGURE 8. |S31| vs FREQUENCY

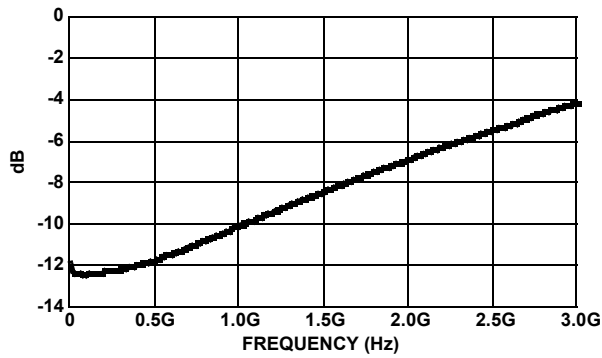


FIGURE 9. |S11| vs FREQUENCY

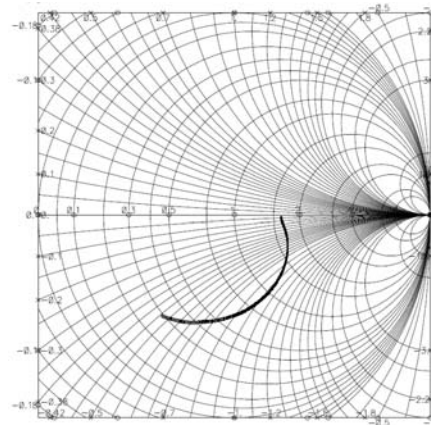


FIGURE 10. SMITH CHART OF S11

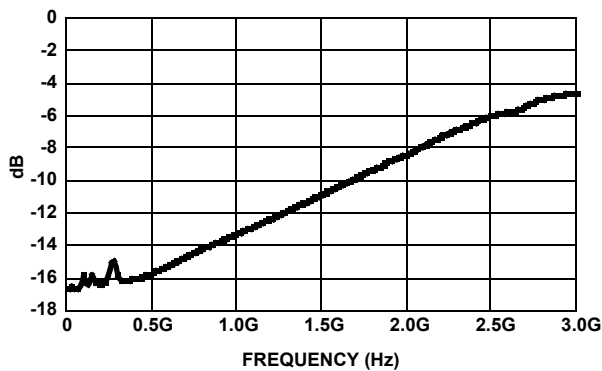


FIGURE 11. |S22| vs FREQUENCY

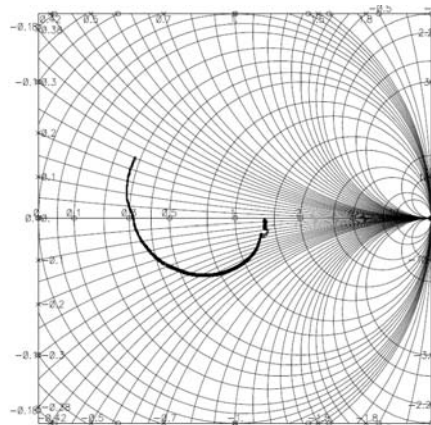


FIGURE 12. SMITH CHART OF S22

Typical Performance (III) 50Ω Environment, $Z_{RSC} = 50\Omega$, $Z_{LOAD} \text{ Port 2} = 50\Omega$, $Z_{LOAD} \text{ Port 3} = 50\Omega$, Measured on Probe Station

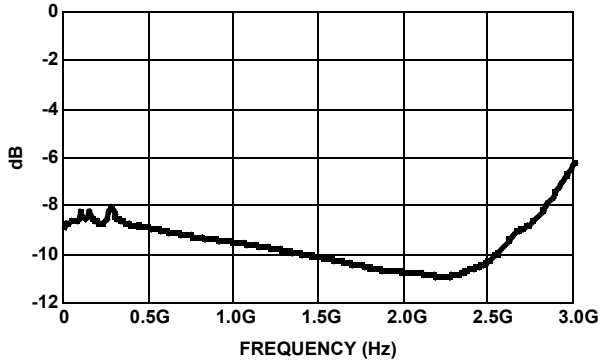


FIGURE 13. |S33| vs FREQUENCY

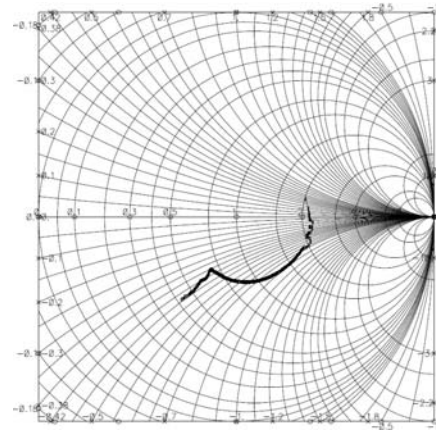


FIGURE 14. SMITH CHART OF S33

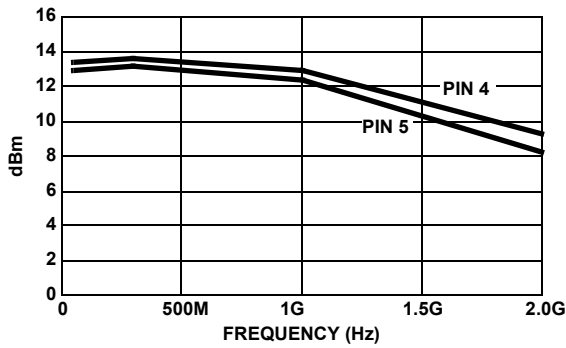


FIGURE 15. 1dB COMPRESSION POINT vs FREQUENCY

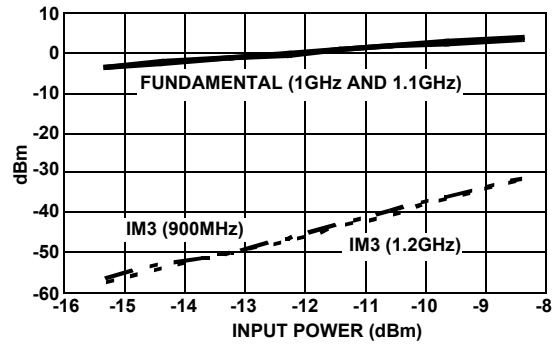


FIGURE 16. IM3 OF PIN 4 vs INPUT POWER

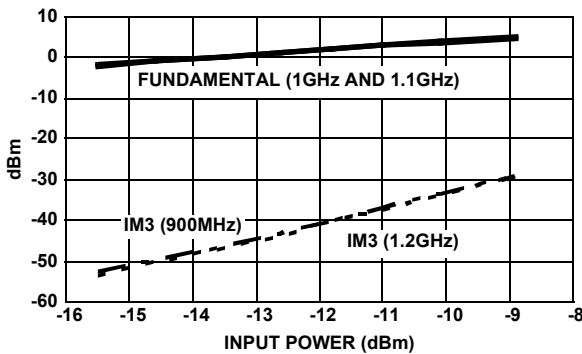


FIGURE 17. IM3 OF PIN 5 vs INPUT POWER

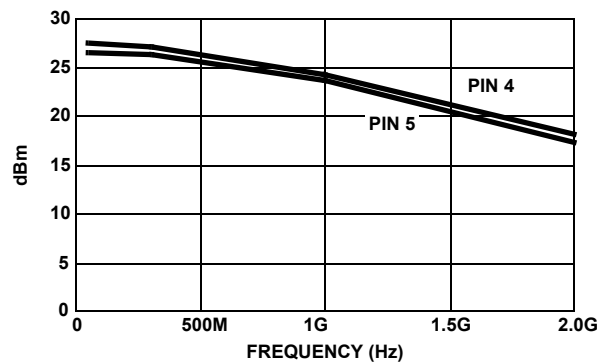


FIGURE 18. OIP3 vs FREQUENCY

Typical Performance (IV) 50Ω Environment, $Z_{RSC} = 50\Omega$, Z_{LOAD} Port 2 = 50Ω, Z_{LOAD} Port 3 = 50Ω, Measured on Probe Station

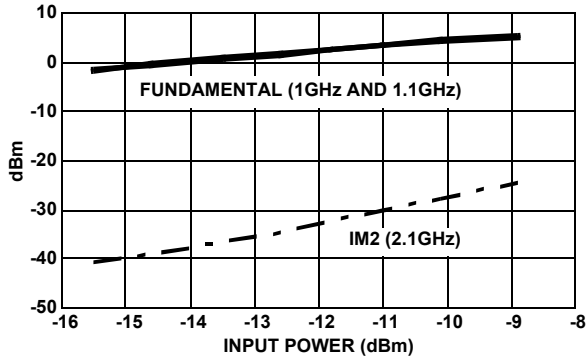


FIGURE 19. IM2 OF PIN 4 vs INPUT POWER

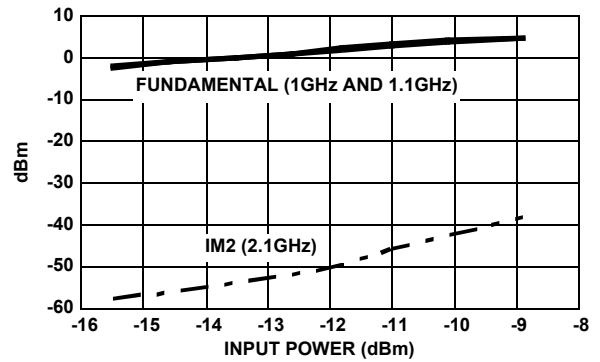


FIGURE 20. IM2 OF PIN 5 vs INPUT POWER

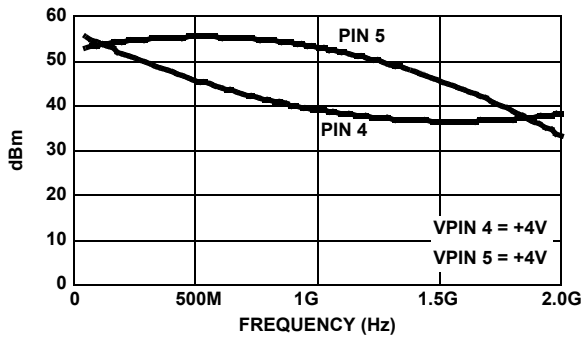


FIGURE 21. OIP2 vs FREQUENCY

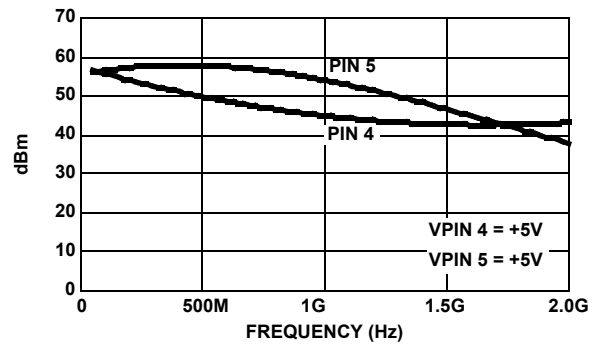


FIGURE 22. OIP2 vs FREQUENCY

Typical Performance (V) 50Ω Environment, $Z_{RSC} = 50\Omega$, Z_{LOAD} Port 2 = 50Ω, Z_{LOAD} Port 3 = 50Ω, Measured on Evaluation Board.

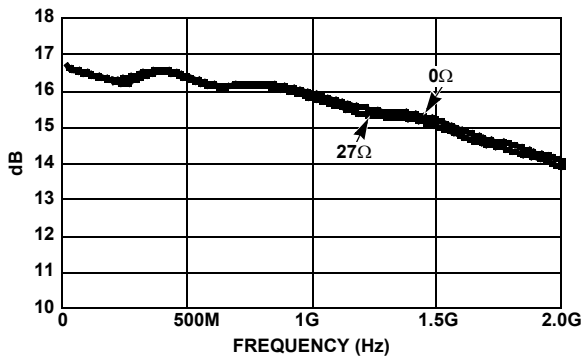


FIGURE 23. |Sds21| vs FREQUENCY

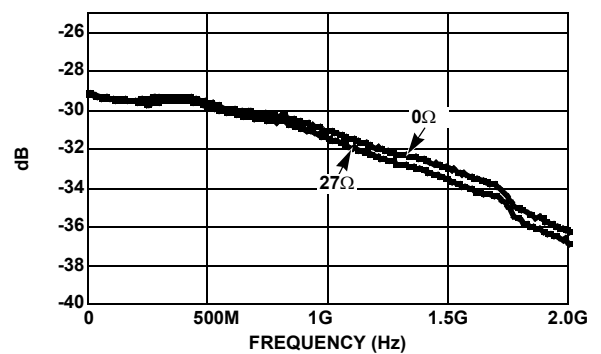


FIGURE 24. |Sds12| vs FREQUENCY

Typical Performance (V) 50Ω Environment, Z_{RSC} = 50Ω, Z_{LOAD} Port 2 = 50Ω, Z_{LOAD} Port 3 = 50Ω, Measured on Evaluation Board. (Continued)

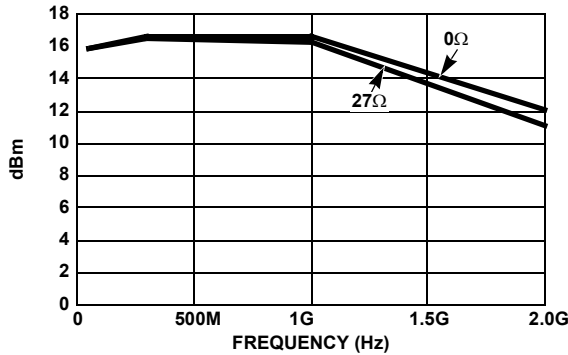


FIGURE 25. DIFFERENTIAL P1dB vs FREQUENCY

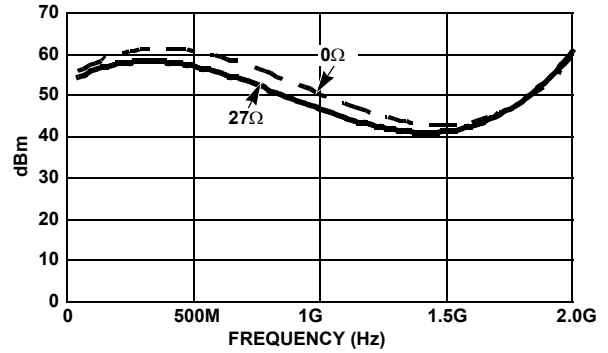


FIGURE 26. DIFFERENTIAL OIP2 vs FREQUENCY

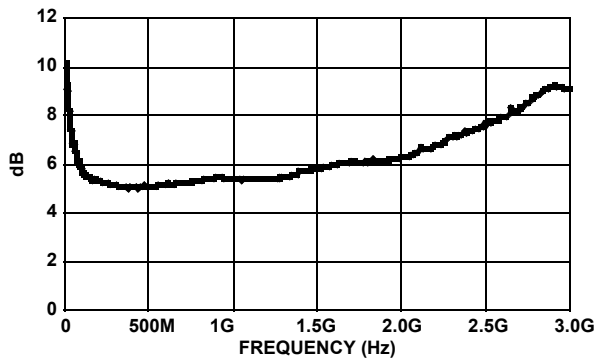


FIGURE 27. NOISE FIGURE vs FREQUENCY

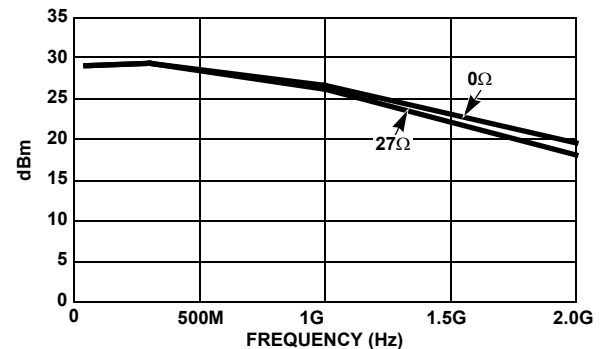


FIGURE 28. DIFFERENTIAL OIP3 vs FREQUENCY

Applications Information

Product Description

The ISL55016 Silicon Bipolar amplifier can match a 75Ω single-ended source to a 100Ω differential load. This feature makes the ISL55016 ideal for a wide range of general purpose applications, such as Satellite TV.

Typical Application Circuit

ISL55016 is a true differential amplifier. Figure 29 shows the Typical Application Circuit of ISL55016. Pins 2 and 3 are equivalent.

The ISL55016 can be configured so that it is driven with a single-ended input. If either pin 2 or pin 3 is used as a single-ended input, the other needs to be connected to an AC ground. The input is internally matched to 75Ω single-ended and the output is matched to 50Ω single-ended or 100Ω differential.

The ISL55016 can be used as differential-in and differential-out as well since pin 2 and pin 3 are equivalent, balanced inputs.

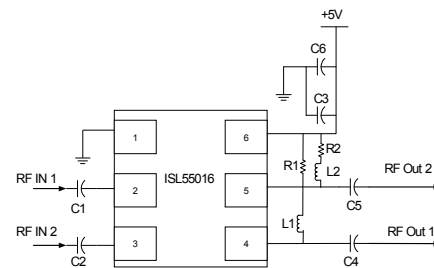


FIGURE 29. APPLICATION CIRCUIT

Balun Function

In many applications of ISL55012, the amplifier will be followed with a Balun structure to transfer the single-ended signal to a differential tuner. The ISL55016 will eliminate the need for an external balun structure and provide significant savings in BOM cost and PCB real-estate (see Figure 30).

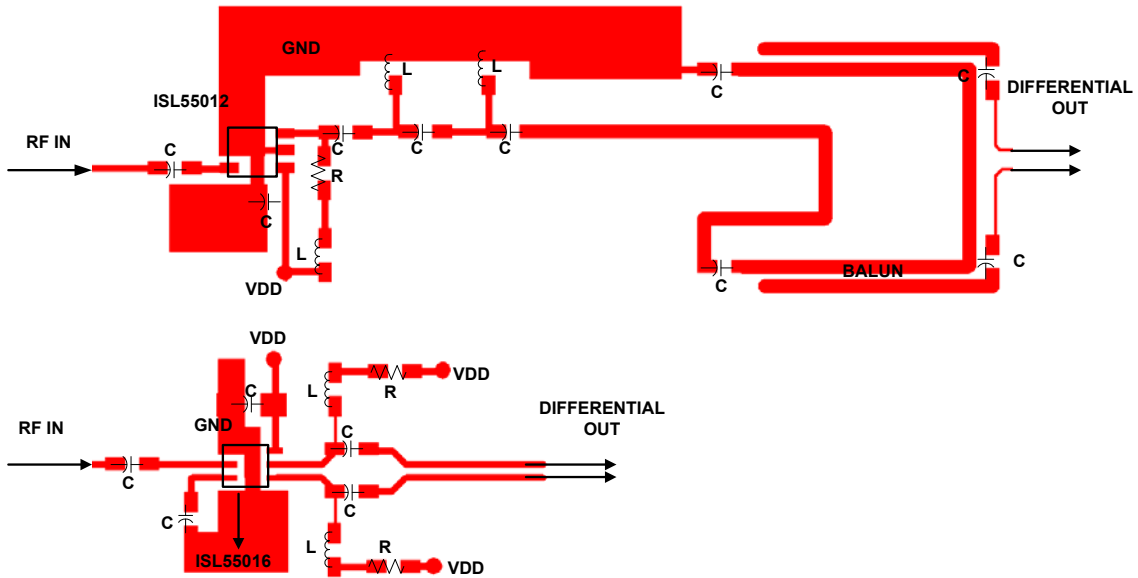


FIGURE 30. COMPARISON OF ISL55012 WITH A BALUN AND ISL55016 (RELATIVE SIZE)

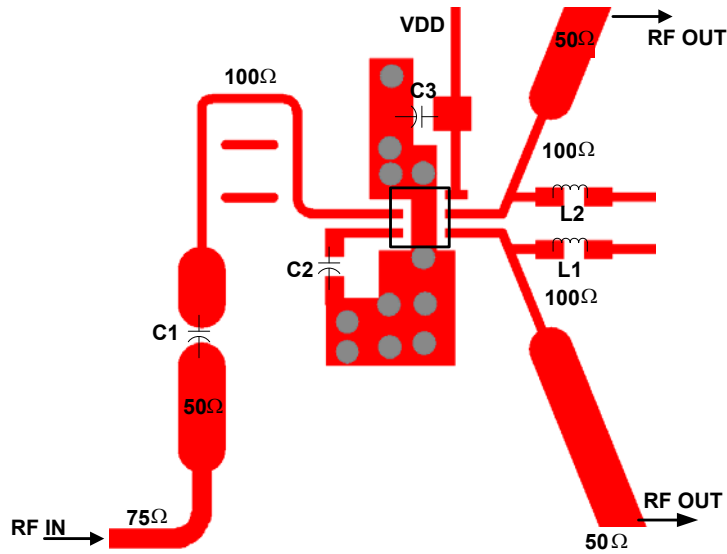


FIGURE 31. PCB LAYOUT OF MATCHING NETWORK

Trade-off Between Power and OIP2

The values of R_1 and R_2 (Figure 29) have two options; 27Ω and 0Ω . Decreasing the R_1 and R_2 value will increase the voltage across the output transistor leading to an increase in the dissipation power. At the same time, it will increase the amplitude of the compression, OIP2 and OIP3. Figures 21, 22 and 26 show this effect on OIP2. Figure 25 shows the compression point changed with different resistors. Figure 28 shows the OIP3 changed with different resistors. One needs to trade-off between the power dissipation and higher OIP2.

Matching at the Input and Output

In the PCB Layout Design, a matching network is needed, especially at the input. Figure 31 shows the matching network used for the ISL55016 Evaluation Board. 12mm 100Ω trace and 6mm 50Ω trace are used to form the input matching network and 4mm 100Ω trace to form the output matching network on the FR4 material.

In Figure 31, the S11 is improved at 2GHz with the matching network, to less than -10dB.

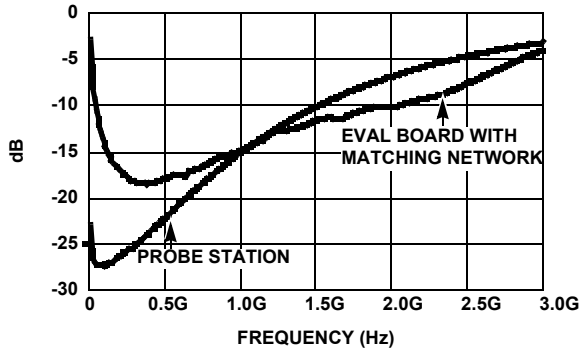


FIGURE 32. |S11| vs FREQUENCY

Thermal Management

The power dissipation of ISL55016 is about 500mW. The recommended layout is shown in Figure 31. The ground pad should be placed under the bottom of the device. At least two thermal vias are needed to lower the temperature.

Choices of Components

ISL55016 is designed for wide bandwidth applications, from 50MHz to 3GHz. The decoupling and RF choke components should be chosen carefully for different frequency applications. Tables 1 and 2 list the components used on the evaluation board.

TABLE 1. LIST OF COMPONENTS (50MHz~300MHz)

FREQUENCY BAND	VALUE	DESCRIPTION/ DIMENSIONS
C1, C2	2200pF	0603
C4, C5	2200pF	0603
L1, L2	2.2μH	Multilayer Ferrite/0603
C3	1nF	0603
C6	0.1μF	1206
R1, R2	27Ω/0Ω	0402

TABLE 2. LIST OF COMPONENTS (300MHz~3GHz)

FREQUENCY BAND	VALUE	DESCRIPTION/ DIMENSIONS
C1, C2	100pF	0603
C4, C5	100pF	0603
L1, L2	100nH	Surface Mount/0402
C3	100pF	0603
C6	0.1μF	1206
R1, R2	27Ω/0Ω	0402

Evaluation Board Setup

The Evaluation board is designed to connect directly to the 2-way 180° Power combiner to recombine signals from -2GHz and allow single-ended assessment with good phase matching the two differential signals into one single-ended output. For lower frequencies, a different choice of power combiner is needed and short matched coaxial cables should be used to connect to the combiner. This setup is used on noise figure measurement and differential OIP2/OIP3 measurements.

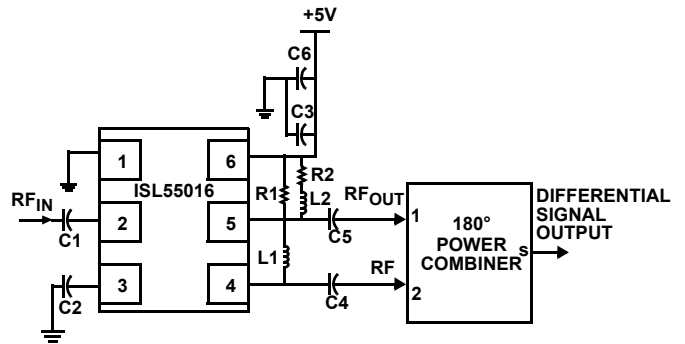


FIGURE 33. EVALUATION BOARD WITH 2-WAY 180° POWER COMBINER

© Copyright Intersil Americas LLC 2008. All Rights Reserved.

All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

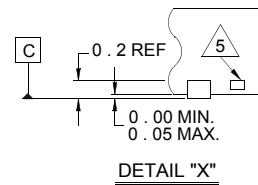
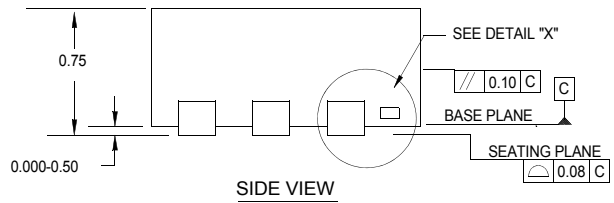
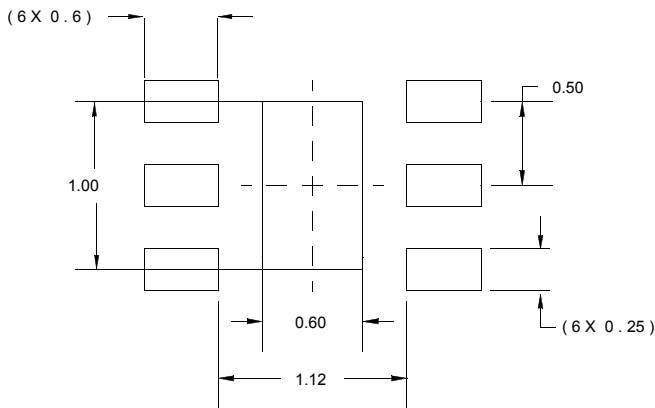
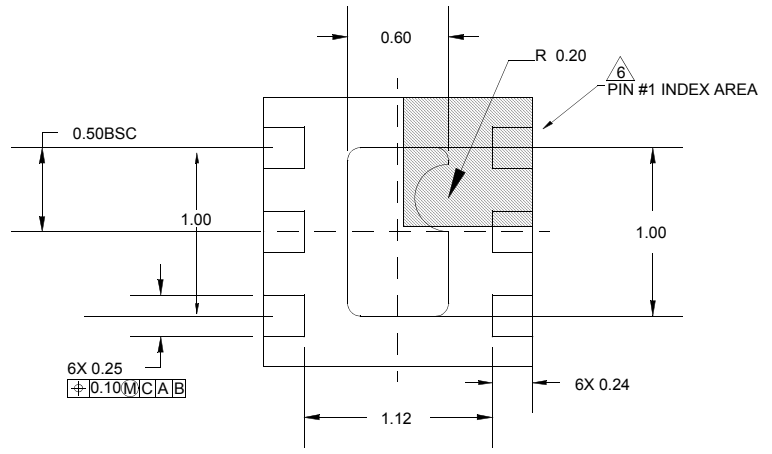
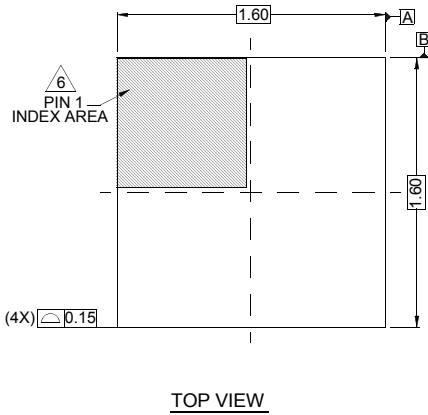
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

L6.1.6x1.6B

6 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN)

Rev 1, 03/07



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.0
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.