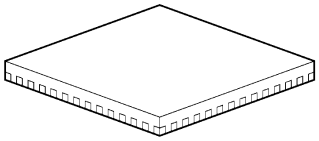
TOSHIBA CD Process Integrated Circuit Silicon Monolithic

TC78S121FTG

PWM Chopper Type Dual-Stepping Motor Driver

The TC78S121FTG is a PWM chopper type dual-stepping motor driver.

Two stepping motor drivers can drive up to four brushed DC motors. Incorporating two pairs of H-bridge drivers, the TC78S121FTG can drive two DC motors or a single stepping motor.



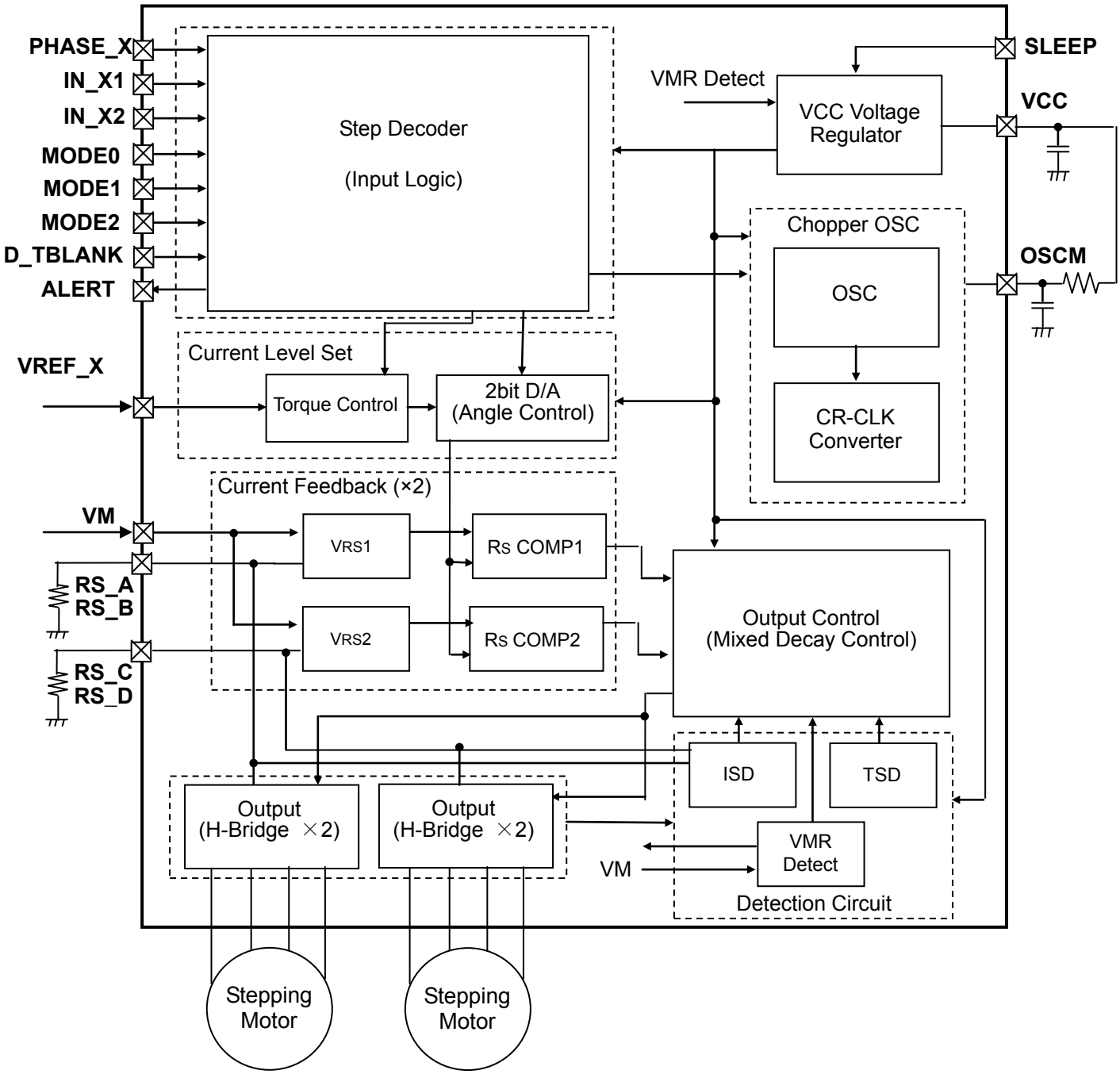
QFN48-P-0707-0.50

Weight: 0.137 (g)

Features

- Single-chip motor driver for bipolar stepping motor control
- Monolithic IC structured by CD process.
- Low ON-resistance**:** R_{on} = 0.6 Ω
  In large mode, ON-resistance of combined H-bridges is (R_{on}) is 0.3 Ω
- Over-current detection (ISD), thermal shutdown (TSD) and V_M power-on reset circuits
- Since the IC incorporates the V_{CC} regulator for internal circuit operation, an external power supply (5 V) is not required.
- Package**:** QFN48-P-0707-0.50
- Maximum output withstand voltage**:** 40 V (max)
- Output current**:** 2.0 A (max) in DC Motor (S) mode; 1.5 A (max) in Stepping Motor (S) mode
- Chopping frequency can be set by external capacitor and resistor. High-speed chopping is possible at 100 kHz or higher.

Block Diagram (Stepping Motor (S) × 2-ch Control Mode)



*: "X" means the ellipsis of A / B / C / D of each Ch. (PHASE_X, IN_X1/X2, and VREF_X)

Note: GND wiring: We recommend that a heat sink be grounded at all points, and the board be grounded at only one GND pin for single point ground. Take the heat dissipation into consideration when designing the board. When in controlling the setting pins for each mode by SW, those pins should be pulled up to power supply like V_{CC} or pulled down to GND not to go into a high-impedance (Hi-Z) state.
Utmost care is necessary in the design of the output line, V_M line and GND line since IC may be destroyed due to short-circuit between outputs, to supply, or to ground.
Especially for those pins that are connected to power supply and get a large current flow (such as V_M, RS, OUT and GND), they should be properly wired; otherwise troubles including destruction may occur to this IC. If the logic input pins are not wired properly, malfunction that would destroy the IC may occur due to a large current exceeding the absolute maximum ratings. Care should be taken in the design of board layouts and implementation of the IC.

Pin Assignment

PIN No.	Pin name	①Stepping Motor (S)×2	②DC Motor (L)×2	③Stepping Motor (L)	④DC Motor (S)×4	⑤DC Motor (L) + Stepping Motor (S)	⑥DC Motor (S)×2 + Stepping Motor (S)
1	IN_C1	C ch current control pin	CD ch IN1	CD ch current contorl pin	C ch IN1	C ch current control pin	
2	IN_D2	D ch current control pin	–	–	D ch IN2	D ch current control pin	
3	OUT_C–	C ch output pin (–)	CD ch output pin (–)		C ch output pin (–)		
4	RS_C	C ch sensing Rs connection pin	CD ch sensing Rs connection pin *1		C ch sensing Rs connection pin		
5	RS_C	C ch sensing Rs connection pin	CD ch sensing Rs connection pin *1		C ch sensing Rs connection pin		
6	OUT_C+	C ch output pin (+)	CD ch output pin (+)		C ch output pin (+)		
7	OUT_D+	D ch output pin (+)	CD ch output pin (+)		D ch output pin (+)		
8	RS_D	D ch sensing Rs connection pin	CD ch sensing Rs connection pin *1		D ch sensing Rs connection pin		
9	RS_D	D ch sensing Rs connection pin	CD ch sensing Rs connection pin *1		D ch sensing Rs connection pin		
10	OUT_D–	D ch output pin (–)	CD ch output pin (–)		D ch output pin (–)		
11	IN_D1	D ch current control pin	–	–	D ch IN1	D ch current control pin	
12	VREF_A	A ch Vref iput	AB ch Vref input		A ch Vref iput	AB ch Vref pin	A ch Vref iput
13	VREF_B	B ch Vref iput	–		B ch Vref iput	–	B ch Vref iput
14	VREF_C	C ch Vref iput	CD ch Vref input		C ch Vref iput	C ch Vref input	C ch Vref iput
15	VREF_D	D ch Vref iput	–		D ch Vref iput	D ch Vref input	D ch Vref iput
16	OSCM	Setting pin of oscillation circuit frequency for chopping					
17	VCC	Monitoring pin for internal generated 5V bias					
18	GND	GND					
19	VM	VM power input pin					
20	VM	VM power input pin					
21	SLEEP	Sleep pin					
22	ALERT	Alert pin					
23	PHASE_A	A ch phase input	AB ch PWM pin	AB ch phase input	A ch PWM pin	AB ch PWM pin	A ch PWM pin
24	PHASE_B	B ch phase input	–	–	B ch PWM pin	–	B ch PWM pin
25	PHASE_C	C ch phase input	CD ch PWM pin	CD ch phase input	C ch PWM pin	C ch phase input	C ch phase input
26	PHASE_D	D ch phase input	–	–	D ch PWM pin	D ch phase input	D ch phase input
27	OUT_A–	A ch output pin (–)	AB ch output pin (–)		A ch output pin (–)	AB ch output pin (–)	A ch output pin (–)
28	RS_A	A ch sensing Rs connection pin	AB ch sensing Rs connection pin		A ch sensing Rs connection pin	AB ch sensing Rs connection pin	A ch sensing Rs connection pin
29	RS_A	A ch sensing Rs connection pin	AB ch sensing Rs connection pin		A ch sensing Rs connection pin	AB ch sensing Rs connection pin	A ch sensing Rs connection pin
30	OUT_A+	A ch output pin (+)	AB ch output pin (+)		A ch output pin (+)	AB ch output pin (+)	A ch output pin (+)
31	OUT_B+	B ch output pin (+)	AB ch output pin (+)		B ch output pin (+)	AB ch output pin (+)	B ch output pin (+)
32	RS_B	B ch sensing Rs connection pin	AB ch sensing Rs connection pin		B ch sensing Rs connection pin	AB ch sensing Rs connection pin	B ch sensing Rs connection pin
33	RS_B	B ch sensing Rs connection pin	AB ch sensing Rs connection pin		B ch sensing Rs connection pin	AB ch sensing Rs connection pin	B ch sensing Rs connection pin
34	OUT_B–	B ch output pin (–)	AB ch output pin (–)		B ch output pin (–)	AB ch output pin (–)	B ch output pin (–)
35	D_TBLANK_AB	AB ch Decay setting pin	Tblank setting pin	–	Tblank setting pin	Tblank setting pin	
36	NC	NC					
37	D_TBLANK_CD	CD ch Decay setting pin	Tblank setting pin	CD ch Decay setting pin	Tblank setting pin	CD ch Decay setting pin	
38	MODE2	"H" input fixed	"H" input fixed	"H" input fixed	"H" input fixed	"L" input fixed	"L" input fixed
39	MODE1	"H" input fixed	"H" input fixed	"L" input fixed	"L" input fixed	"H" input fixed	"H" input fixed
40	MODE0	"H" input fixed	"L" input fixed	"H" input fixed	"L" input fixed	"H" input fixed	"L" input fixed
41	VM	VM power input pin					
42	VM	VM power input pin					
43	NC	NC					
44	IN_A2	A ch current control pin	AB ch IN2	AB ch current control pin	A ch IN2	AB ch IN2	A ch IN2
45	IN_A1	A ch current control pin	AB ch IN1	AB ch current control pin	A ch IN1	AB ch IN1	A ch IN1
46	IN_B2	B ch current control pin	–	–	B ch IN2	–	B ch IN2
47	IN_B1	B ch current control pin	–	–	B ch IN1	–	B ch IN1
48	IN_C2	C ch current control pin	CD ch IN2	CD ch current control pin	C ch IN2	C ch current control pin	

*1: When Large mode is used, please use to connect the corresponding pins to each other.

■ Descriptions of Motor Drive Modes

(1) Stepping Motor (S) × 2 control mode pin name and assignment

(2) DC Motor (L) × 2 control mode pin name and assignment

(3) Stepping Motor (L) × 1 control mode pin name and assignment

(4) DC Motor (S) × 4 control mode pin name and assignment

(5) Stepping Motor (S) × 1 control mode + DC Motor (L) × 1 control mode pin name and assignment

(6) Stepping Motor (S) × 1 control mode + DC Motor (S) × 2 control mode pin name and assignment

*: In the modes that include DC Motor (S) mode, the D_TBLANK can be separately set for each channel pair, channels A and B and channels C and D.

Channels A and B: D_TBLANK_AB pin

Channels C and D: D_TBLANK_CD pin

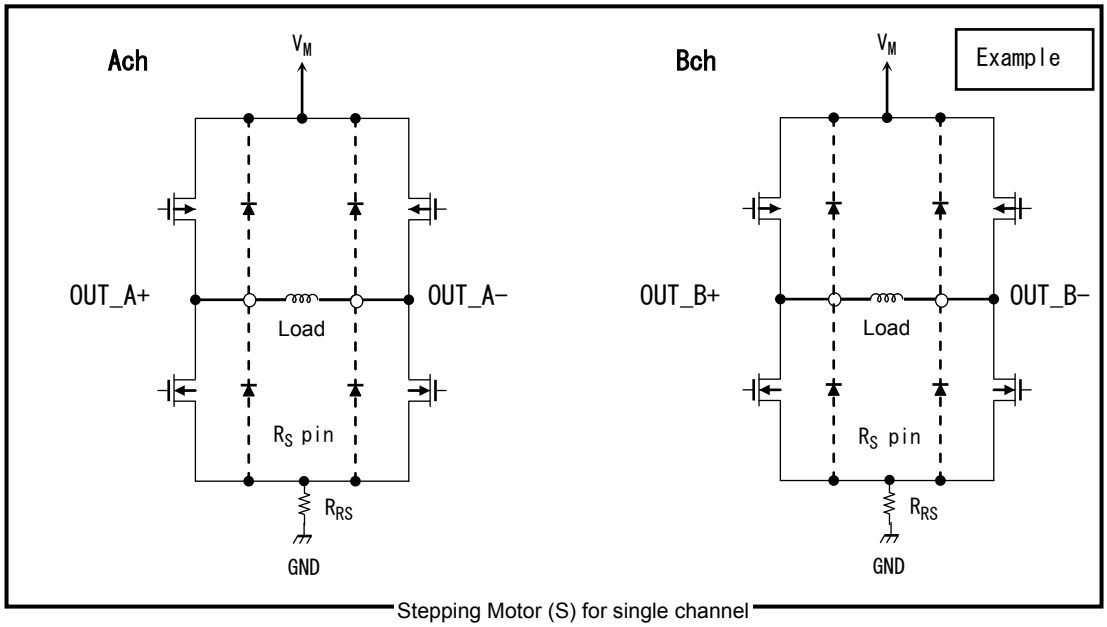
The motor drive Mode (2, 1, 0)= (L, L, H) is provided only for production test and must not be used during normal operation.

Note1: In Combination mode, such as Stepping Motor (L) and DC Motor (L) modes, the impedance outside the IC should be balanced.

Note2: In Large mode, if the impedance of wiring to mutually connected output transistors is unbalanced, the current that flows through the transistor also becomes unbalanced and may exceed the absolute maximum rating of the transistor, thus permanently damaging the transistors.

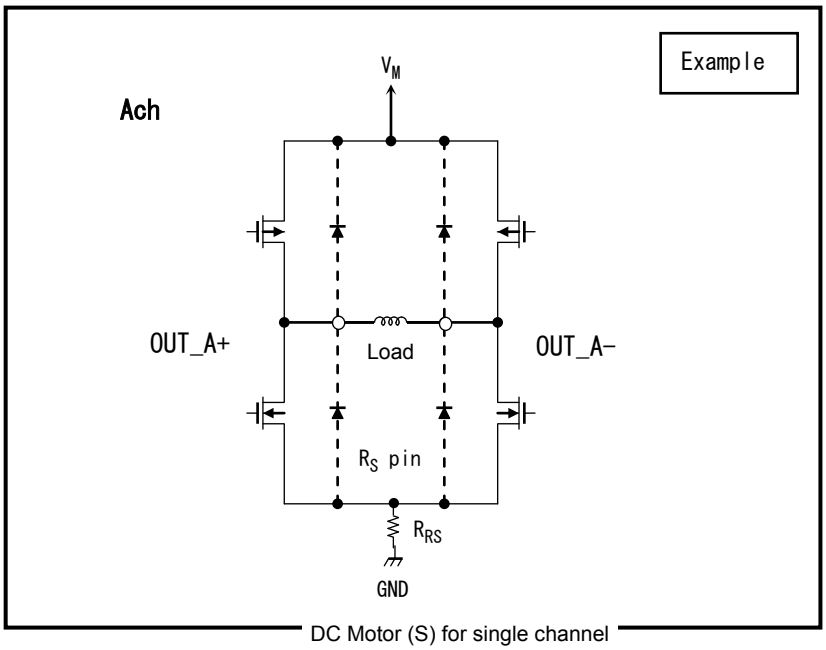
■H-bridge Combination (connection method) for Each Type of Motor Driver

- **Stepping Motor (S) Combination**



Stepping Motor (S) for single channel

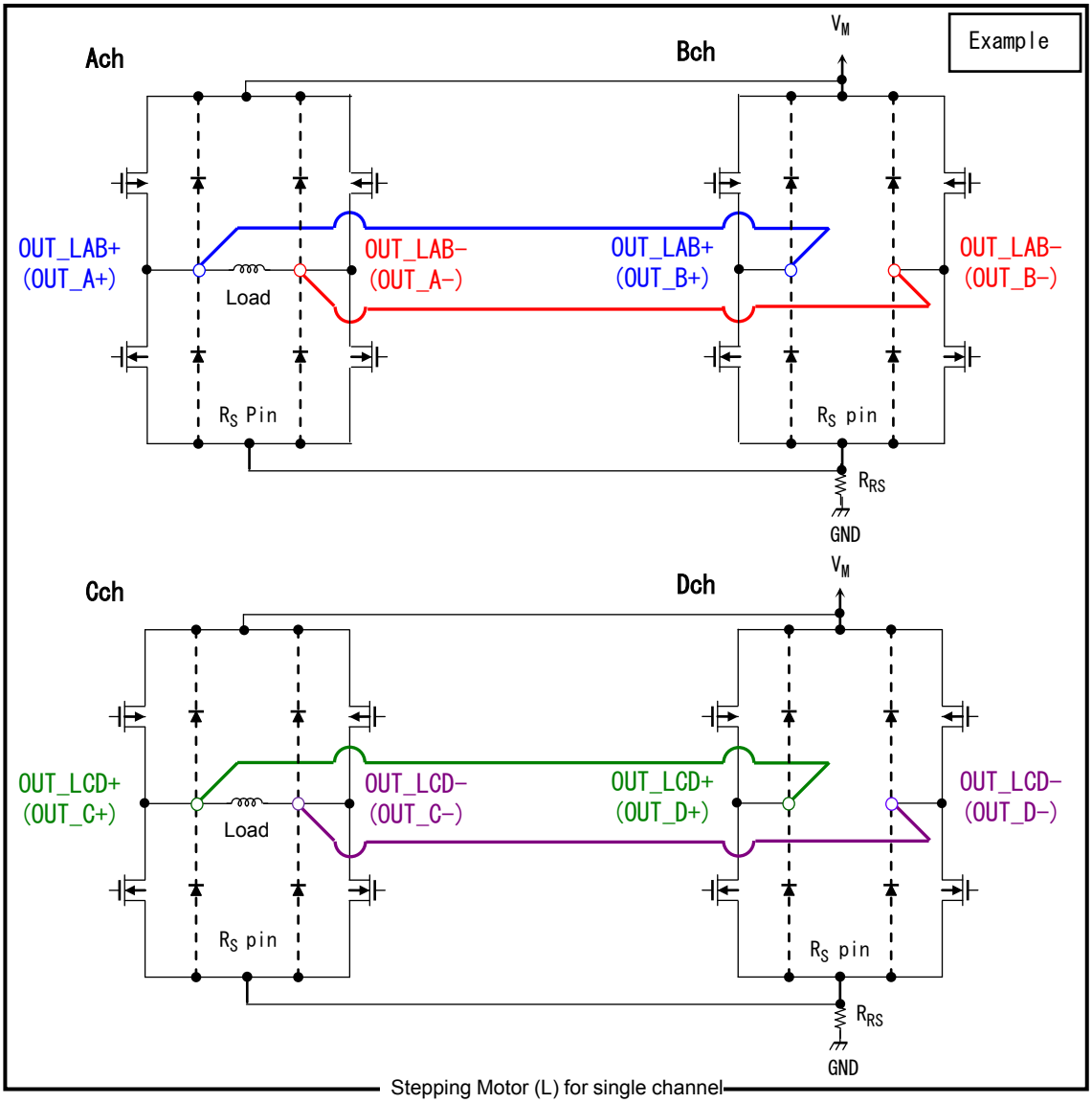
- **DC Motor (S) Combination**



DC Motor (S) for single channel

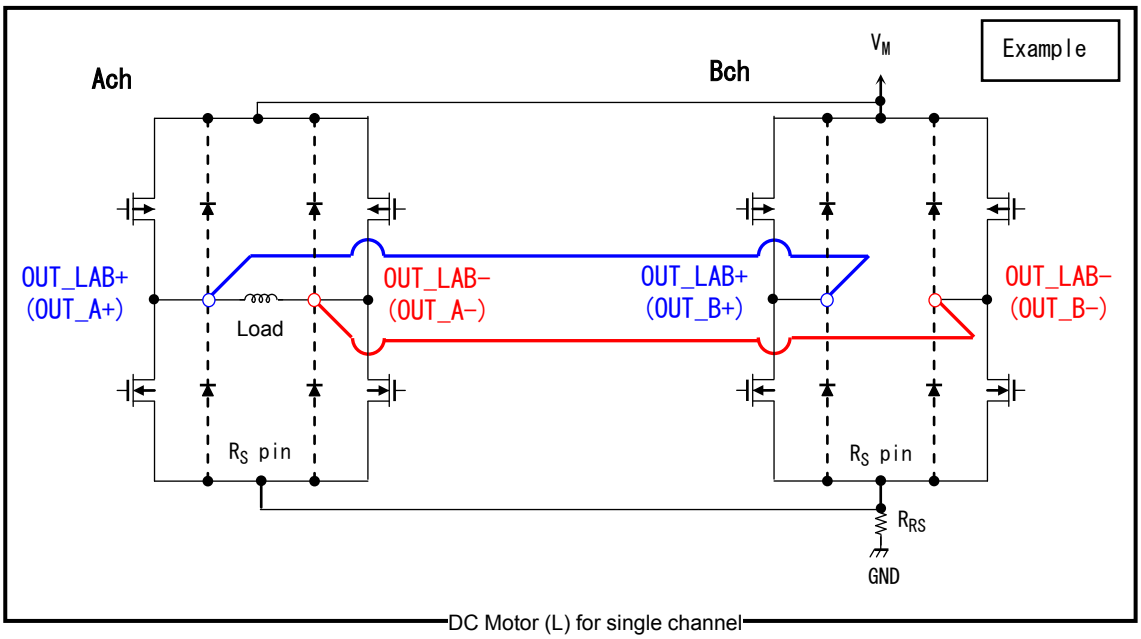
○ …Indicates an IC output pin connected to a motor.

- **Stepping Motor (L) Combination**



Stepping Motor (L) for single channel

- **DC Motor (L) Combination**

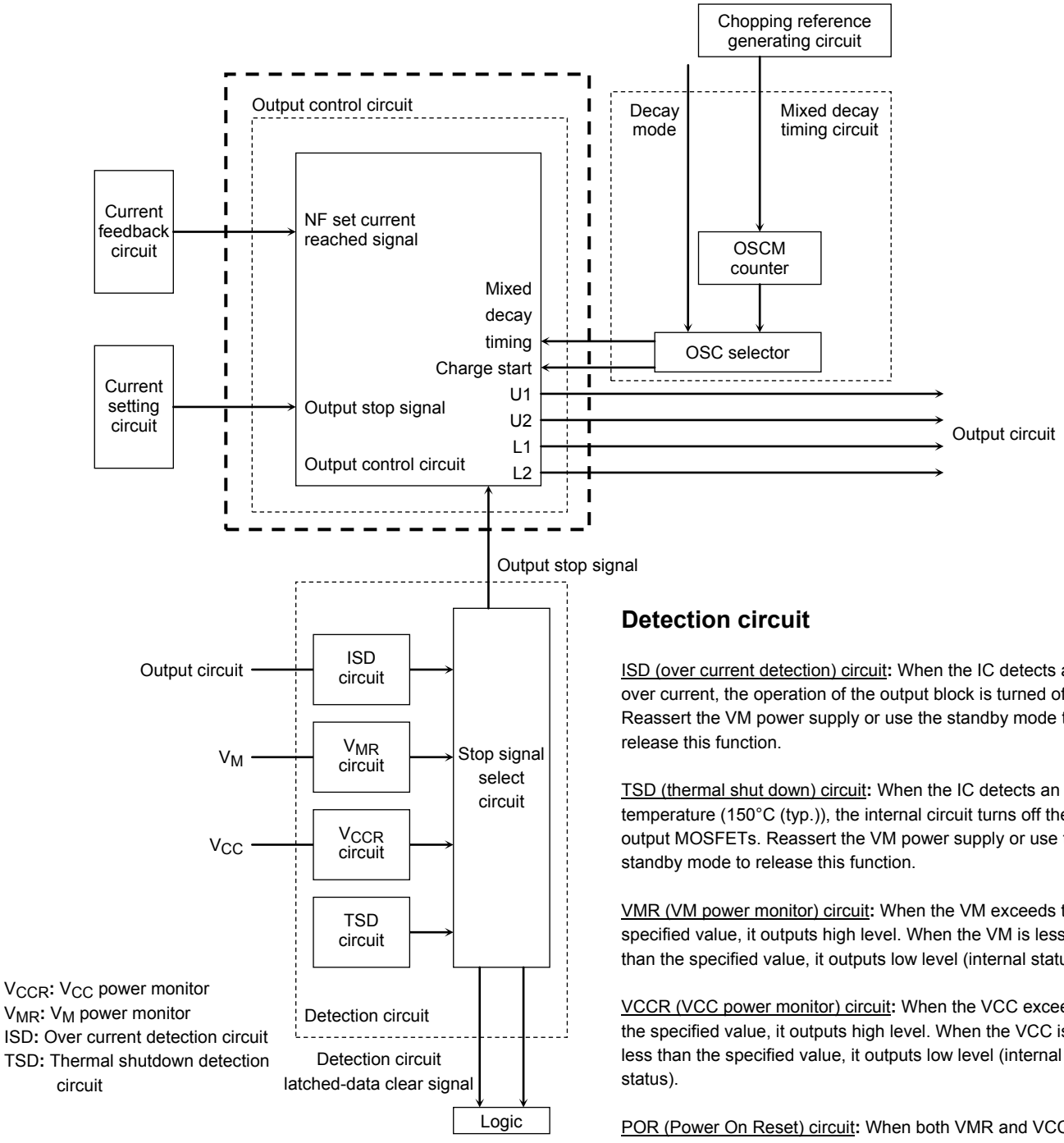


DC Motor (L) for single channel

○ …Indicates an IC output pin connected to a motor.

Output Control Circuit, Current Feedback Circuit, and Current Setting Circuit for Motor Driver

Note: Logic input pins are internally connected to pull-down resistors of about 100 kΩ.



V_{CCR}: V_{CC} power monitor
V_{MR}: V_M power monitor
ISD: Over current detection circuit
TSD: Thermal shutdown detection circuit

Detection circuit

ISD (over current detection) circuit: When the IC detects an over current, the operation of the output block is turned off. Reassert the VM power supply or use the standby mode to release this function.

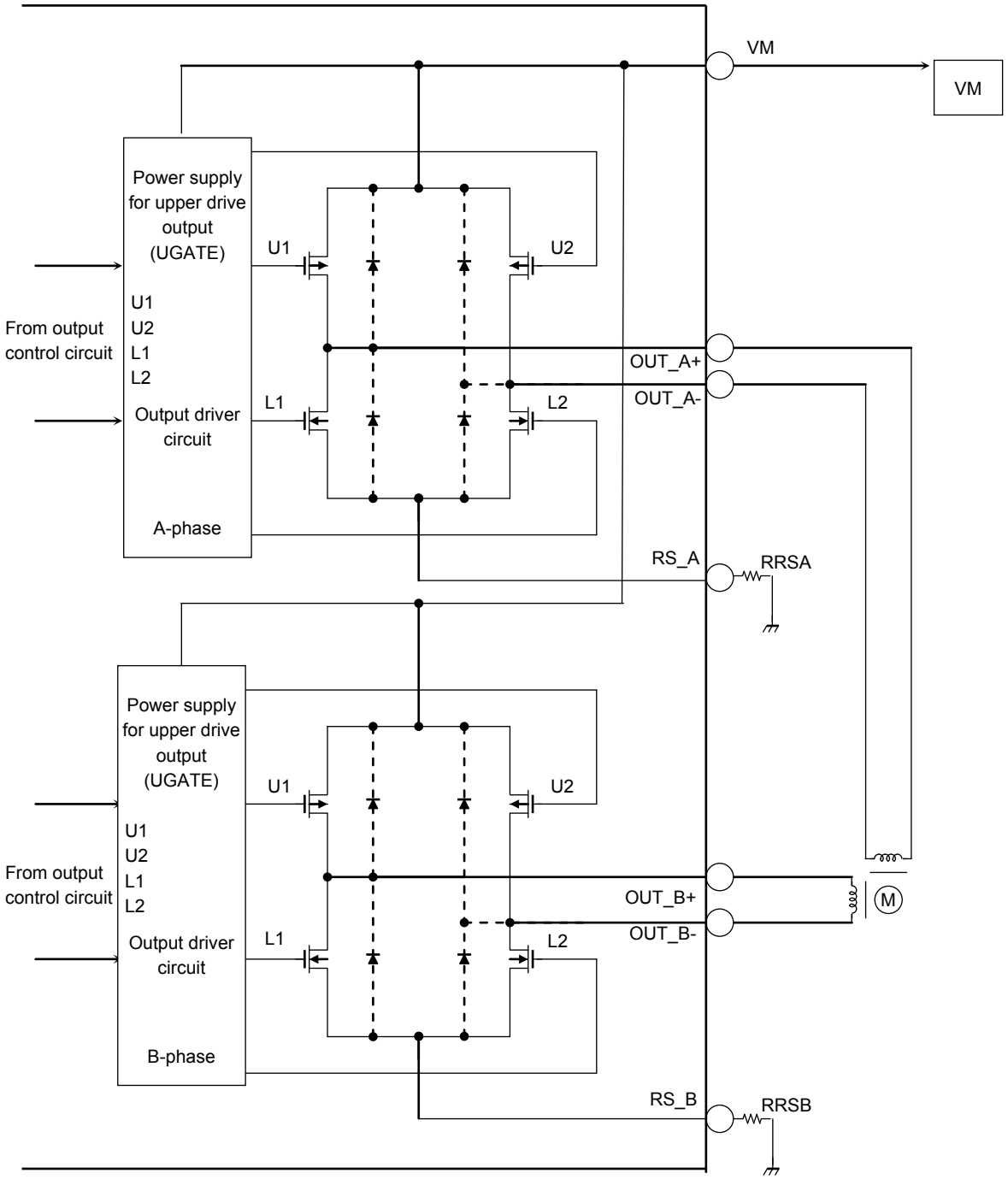
TSD (thermal shut down) circuit: When the IC detects an over temperature (150°C (typ.)), the internal circuit turns off the output MOSFETs. Reassert the VM power supply or use the standby mode to release this function.

VMR (VM power monitor) circuit: When the VM exceeds the specified value, it outputs high level. When the VM is less than the specified value, it outputs low level (internal status).

VCCR (VCC power monitor) circuit: When the VCC exceeds the specified value, it outputs high level. When the VCC is less than the specified value, it outputs low level (internal status).

POR (Power On Reset) circuit: When both VMR and VCCR output high level, the logic circuit is activated. Otherwise, the logic circuit is turned off.

Output Equivalent Circuit of A/B-phase (C/D conforms to A/B.)



1. Function Table for Motor Drive Mode Selection

Motor drive modes can be selected depending on the type of motors to be driven.
The configuration of H-bridge drivers and control category are changed according to the selected mode.
There is basically no need to change drive modes during motor operation. Thus, the TC78S121FTG does not support dynamic mode switching.
Changing the settings of these pins changes the functions and timing of control pins.
The setting of mode select pins must not be changed after the TC78S121FTG is powered on.

Mode 0	Mode 1	Mode 2	Drive Mode
H	H	H	Stepping Motor (S) × 2
L	H	H	DC Motor (L) (Combination) × 2
H	L	H	Stepping Motor (L) (Combination) × 1
L	L	H	DC Motor (S) × 4
H	H	L	DC Motor (L) (Combination) × 1 + Stepping Motor (S)
L	H	L	DC Motor (S) × 2 + Stepping Motor (S)
H	L	L	Inhibited (For production test only)
L	L	L	Standby mode

- **Stepping Motor Mode**
  This mode is used to drive stepping motors.
  The tBLANK time is specified as a fixed analog value (about 300 ns).
  Each motor is controlled via three logic control inputs, PHASE (current direction) and IN_X1/2, and via the Vref input for constant-current control.

- **Brushed DC Motor Mode**
  This mode is used to drive brushed DC motors.
  The tBLANK time can be specified as a fixed analog value, or as four OSC cycles in digital tBLANK mode, where OSC is a reference signal for chopper circuit.
  When DC motors are driven under PWM control, a discharge current spike can occur due to a varistor. To prevent this current spike from erroneously tripping the constant-current sensor, the constant-current sensor is digitally blanked for a period of time that is determined by tBLANK, which is derived from the OSC signal.
  Using this blanking function enables constant-current limiter control, as well as external PWM control. An over-current can be observed only during blank times.

- **Combination Mode**
  The Combination mode, such as DC Motor (L) and Stepping Motor (L) modes can be selected when two units of H-bridges with the same characteristics are operated in parallel.
  In this mode, the actual ON-resistance is reduced by half while the current capability is doubled. (Specifications actually include the thermal capacitance as well. See electrical characteristics for more details.)
  To use this mode, the power supply, ground, and output pins that have identical names should be shorted together on the board.
  At the same time, the wirings of a board should be routed to balance the impedance at each pin. Otherwise, the shorted pins may experience a current imbalance and more current may flow into either one of them than the other.

2. Input Signal Function (In Stepping Motor Mode)

Input			Output		
PHASE_A PHASE_B	IN_X2	IN_X1	OUT_X+	OUT_X-	IOUT
H	H	H	H	L	100 %
	H	L	H	L	71 %
	L	H	H	L	38 %
	L	L	Output OFF	Output OFF	0 %
L	H	H	L	H	-100 %
	H	L	L	H	-71 %
	L	H	L	H	-38 %
	L	L	Output OFF	Output OFF	0 %

3. D_TBLANK Function (DC Motor MODE only)

D_TBLANK_AB D_TBLANK_CD	Motor Drive Mode
L	OFF: Digital Blanking Time = OSC × 0
H	ON: Digital Blanking Time = OSC × 4

*: If it is set to "L", only analog tBLANK width can be available.

4. Decay Switching Function (Stepping Motor MODE only)

D_TBLANK_AB D_TBLANK_CD	Constant current control mode
L	Mixed Decay:37.5 % fixed
H	Mixed Decay: 12.5 %(During the current decay is 37.5 %)

5. Control Signal Functions in Brushed DC Motor Mode

Control Input			State of the Output Stage		
IN_X1	IN_X2	PHASE_X	OUT_X+	OUT_X-	Mode
H	H	H	L	L	Short brake
		L			
L	H	H	L	H	Forward/reverse
		L	L	L	Short brake
H	L	H	H	L	Reverse/forward
		L	L	L	Short brake
L	L	H	OFF (Hi-Z)	OFF (Hi-Z)	Stop
		L			

*: "X" means the ellipsis of A / B / C / D of each Ch. (IN_X1, IN_X2, and PHASE_X)

- **External PWM Control Function**

The motor speed can be controlled by applying 0 V and 5 V (higher than TTL level) PWM signals to the PWM pin.
In PWM mode, the PWM chopper circuit alternates between on and short brake.

When the PWM speed control is not required, the PWM pin (short brake pin) should be held high level.

When the constant-current limiter is used, the TC78S121FTG enters 37.5 % Mixed Decay mode after an output current reaches the predefined current value. Since the dead band time (typ.300 ns) is internally inserted to prevent a shoot-through current eliminating, the special arrangement is not required.

The short brake function is disabled in Stepping Motor mode (Large or Small).

Stepping motors can also be driven in Brushed DC motor mode.
To perform such operation, the short brake function should not be used and the D_TBLANK pin should be set low level.
At the same time, input signal functions should also be confirmed.

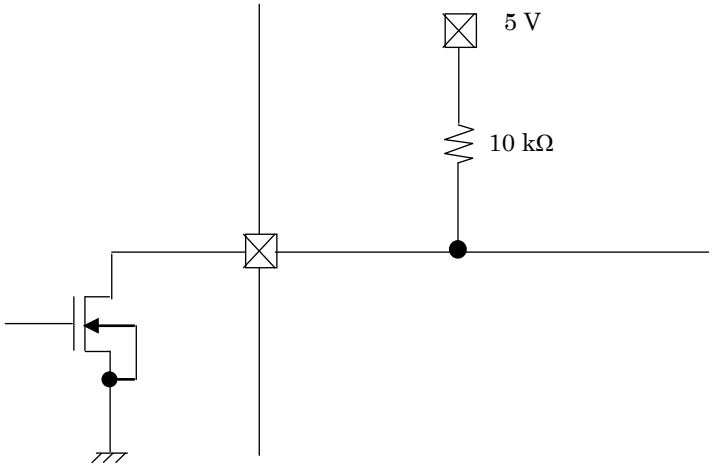
6. SLEEP Function

In the SLEEP pin, it is possible to control the low power consumption mode (VCC OFF) and the normal operation mode (VCC ON).
When SLEEP pin is low level, VCC regulator is turned OFF, completely logic will stop.
After SLEEP pin is set to high level, it can return to the normal operation mode in 1ms.

SLEEP	Function
L	Low power consumption mode (VCC OFF)
H	Normal operation mode (VCC ON)

7. ALERT Function

The ALERT pin outputs low level when an error occasion (TSD/ISD) is detected.



The ALERT is an open drain output pin. When the output pin is pulled up to the VCC with resistance, the low level is output (MOSFET ON) at the Reset, and the high level (internal Hi-Z) is output at the non-reset.
Please connect it to the VCC.

Absolute Maximum Ratings (Ta=25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	VM	40	V	
Motor output voltage	VOUT	40	V	
Motor output current (Note1)	IOUT_(ST_S)	2.0	A	
	IOUT_(ST_L)	3.0	A	
	IOUT_(DC_S)	3.5	A	(tw ≤ 500 ns)
	IOUT_(DC_L)	5.0	A	(tw ≤ 500 ns)
Internal Logic power supply	VCC	6.0	V	
Logic input voltage	VIN (H)	6.0	V	
	VIN (L)	-0.4	V	
Power dissipation (single) (Note2)	PD	1.3	W	
Operating temperature	TOPR	-20 to 85	°C	
Storage temperature	TSTR	-55 to 150	°C	
Junction temperature	Tj (max)	150	°C	

Note1: As a guide, the maximum output current should be kept below 1.4 A per phase. The maximum output current may be further limited in view of thermal considerations, depending on ambient temperature and board conditions.

Note2: Stand-alone (Ta =25°C)
When Ta exceeds 25°C, it is necessary to do the derating with 10.4 mW/°C.

Ta: Ambient temperature

Topr: Ambient temperature while the TC78S121FTG is active

Tj: Junction temperature while the TC78S121FTG is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry.

It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (max), will not exceed 120°C.

Caution: Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The TC78S121FTG does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.

All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

Operation Ranges(Ta=0 to 85°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Internal logic power supply voltage	VCC	DC	(Automatically generated)	4.5	5.0	5.5	V
Motor power supply voltage	VM	DC	—	8	24	38	V
Motor output current	Iout (ST_S)	DC	Ta = 25°C per phase	—	0.8	1.5	A
	Iout (ST_L)	DC	Ta = 25°C per phase	—	1.5	2.1	
	Iout (DC_S)	DC	Ta = 25°C per phase	—	1.0	2.0	
	Iout (DC_L)	DC	Ta = 25°C per phase	—	2.0	3.8	
Logic input voltage	VIN	DC	—	GND	3.3	5.5	V
ALERT output pin voltage	V_{ALERT}	DC	Voltage of pull-up destination	—	3.3	5.5	V
Chopping frequency setting range	fchop	DC	VCC=5.0 V	40	100	150	kHz
Vref voltage	Vref	DC	VM=24 V	GND	3.0	4.0	V
Current detect pin voltage	VRS	DC	VM=24 V	-0.5	—	1.5	V

Note**:** Use the maximum junction temperature (T_j) at 120°C or less. The Maximum current cannot be used under certain thermal conditions.

Electrical Characteristics 1 (Unless otherwise specified, Ta=25°C, VM=24 V)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Logic input voltage (Other than SLEEP pin)	High	VIH	DC	Logic input pins (Other than SLEEP pin)	2.2	—	5.5	V
	Low	VIL			GND	—	0.8	
Logic input voltage (SLEEP pin only)	High	VIH	DC	SLEEP pin only	2.0	—	5.5	V
	Low	VIL			GND	—	0.6	
Logic input hysteresis voltage		His	DC	Logic input pins	0.3	0.4	0.5	V
Logic input current		IIN(H)	DC	VIN=5 V, Input pins with resistor	—	50	75	μA
		IIN(L)			—	—	1	
ALERT output voltage		V_{OL}	DC	IOL=4 mA, Output: Low	—	—	0.5	V
Current consumption (VM pin)		IM1	DC	Output=OPEN, SLEEP=H, other logic pins=L All output stages are not operating.	—	2	3	mA
		IM2		Output=OPEN, SLEEP=H, Motor mode: Stepping ×2 ch (MODE0/1/2=H level) IN_X1/IN_X2/PHASE_X=L, OSCM=1.6 MHz	—	3.5	5	
		IM3		Output=OPEN, SLEEP=H, Motor mode: Stepping ×2 ch (MODE0/1/2=H level) IN_X1,IN_X2=H fixed PHASE_X=L/H[1kHz input] (Full step resolution function) D_TBLANK_AB/D_TBLANK_CD= L fixed (Decay 37.5% fixed) OSCM=1.6 MHz, Vref=3.0 V RS_X=0.5 V	—	8	10	
		IM4		SLEEP=L, other logic pins=L VCC regulator = OFF	—	10	20	μA
Output leakage current	Upper side	IOH	DC	VM=24 V, Vout=0 V, ENABLE ALL=L	-1	—	—	μA
	Lower side	IOL		VM=Vout=24 V, ENABLE ALL=L	—	—	1	μA
Output current differential		ΔIout1	DC	Iout=1.0 A	-5	—	5	%
Output current setting differential		ΔIout2	DC	Iout=1.0 A	-5	—	5	%
RS pin current		IRS	DC	VRS=0V, VM=24V, ENABLE ALL=L (MOSFET = OFF)	—	—	10	μA
Output transistor drain-source ON-resistance (H-side + L-side)		Ron (DS: H-side + L-side) S	DC	Iout=1.0 A, Tj=25°C, Drain-source, (Upper + Lower) Small Mode	0.4	0.6	0.8	Ω
		Ron (DS: H-side + L-side) L		Iout=1.0 A,VCC=5.0 V, Tj=25°C, Drain-source, (Upper + Lower) Large Mode	—	0.3	0.4	

Electrical Characteristics 2 (Unless otherwise specified, Ta=25°C, VM=24 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Vref input voltage	VREF	DC	VM=24 V,VCC=5 V	GND	3.0	4.0	V
Vref input current	IREF	DC	VREF=3.0 V	—	0	1	μA
VCC output voltage	VCC	DC	ICC=5.0 mA	4.5	5.0	5.5	V
VCC output current	ICC	DC	VCC=5.0 V	—	2.5	5	mA
Vref attenuation ratio	VREF(gain)	DC	VREF=2.0 V	1/5.2	1/5.0	1/4.8	—
TSD temperature (Note 1)	TjTSD	DC	—	140	150	170	°C
VM return voltage	VMR	DC	—	6.8	7.0	7.3	V
Detection current of over-current detection circuit (Note 2)	ISD	DC	—	2.1	4.0	5.0	A

Note 1: Thermal shut down (TSD) circuit

When the IC junction temperature reaches the specified value and become overheated under irregular conditions causing the TSD circuit to be activated, the internal halt circuit is activated shutting down all the outputs to off.
When the temperature is set between 140°C (min) to 170°C (max), the TSD circuit operates (design target value). When the TSD circuit is operating, it can be returned by re-starting the VM power supply or setting the standby mode. The TSD function aims at detecting abnormal heating of ICs. Please avoid positively using the TSD function.

Note 2: Over-current detection (ISD) circuit

When the current exceeding the specified value flows to the output under irregular conditions, the internal halt circuit is activated switching all the outputs to off. The dead band time is set to avoid the incorrect operation by switching. (For details, refer to "ISD Dead Band Time and ISD Operating Time.") When the ISD function is operating, the output is stopped until power-on-reset of the VM power supply. The output operation can be returned by re-starting the VM power supply or setting the standby mode. The ISD function aims at detecting abnormal current of ICs. Please avoid positively using the ISD function.

Note 3: The circuit is designed to avoid EMF or leakage current when the logic signal is inputted in the state that the VM voltage is not supplied. But for fail-safe, please control the logic signal timing correctly in order that the motor may not operate before the VM power is resupplied.

Back-EMF

- While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF. If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the device or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

- The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short circuit; they do not necessarily guarantee complete IC safety.
- If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged owing to an output short circuit.
- The ISD circuit is only intended to provide temporary protection against an output short circuit. If such a condition persists for a long time, the device may be damaged owing to overstress. Overcurrent conditions must be removed immediately by external hardware.

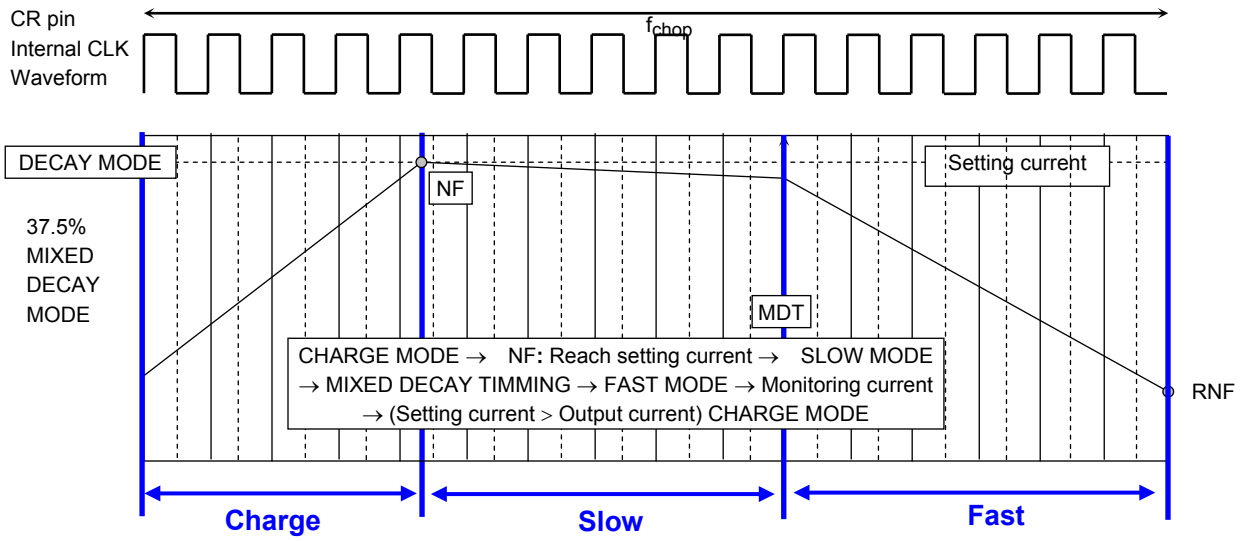
IC Mounting

Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause device breakdown, damage and/or deterioration.

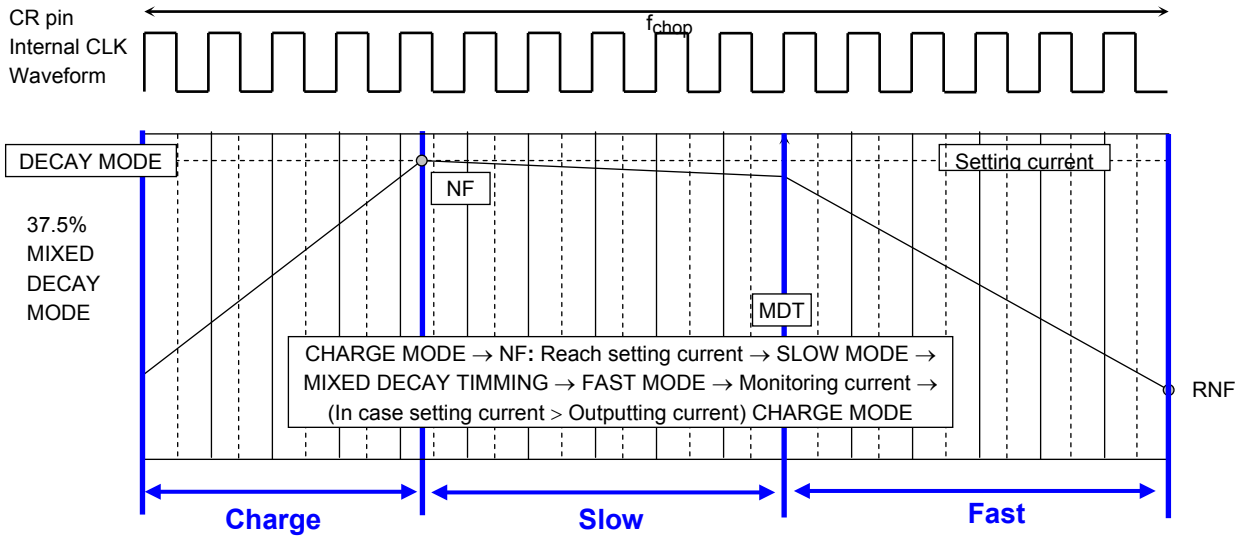
AC Electrical Characteristics (Unless otherwise specified, Ta = 25°C, V_M = 24 V, Load = 6.8 mH/5.7 Ω)

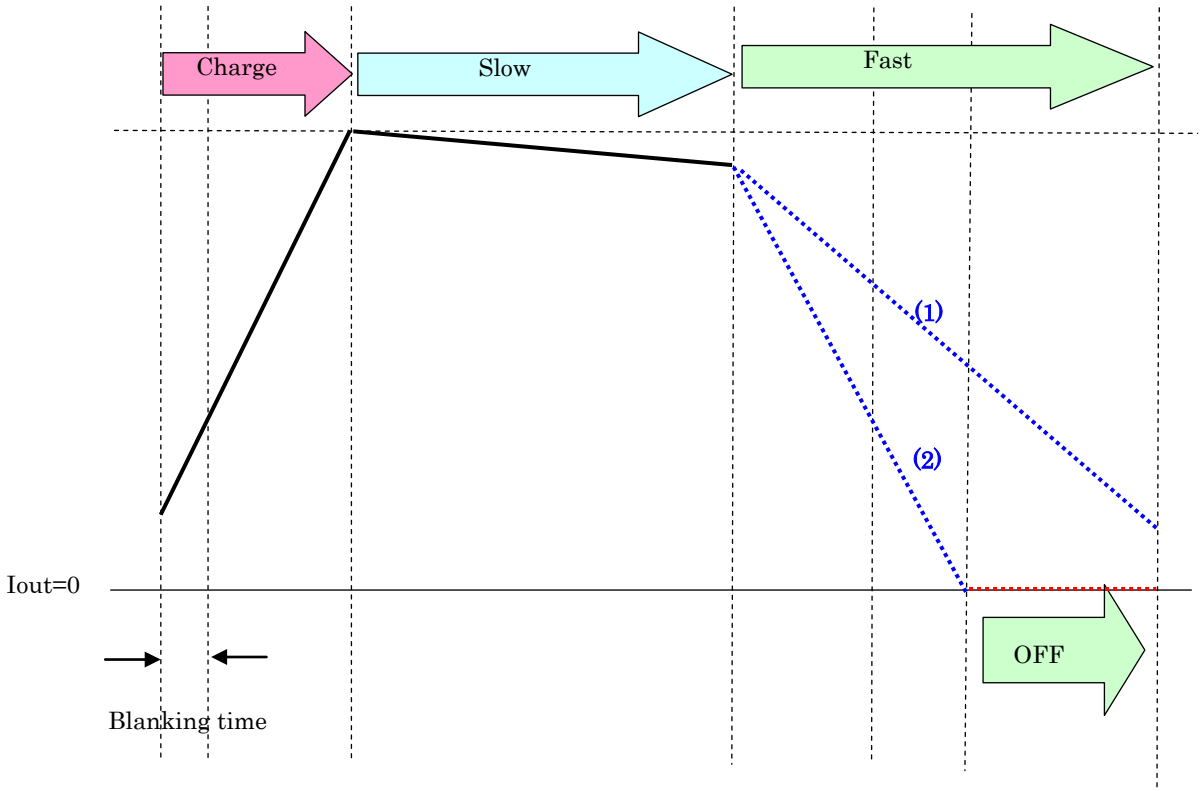
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Logic input frequency	f_{Logic}	AC	—	1.0	—	200	kHz
Minimum signal pulse width	tw (t_{Logic})	AC	—	100	—	—	ns
	twp			50	—	—	
	twn			50	—	—	
Output transistor switching characteristic	tr	AC	Output load: 6.8 mH/5.7 Ω	60	120	200	ns
	tf			30	70	130	
	tpLH		Between Signal and OUT Output load: 6.8 mH/5.7 Ω	—	120	500	
	tpHL			—	120	500	
Noise rejection dead band time	t_{BLANK}_AB(L) t_{BLANK}_CD(L)	AC	Iout=0.6 A,VM=24 V, Analog tBLANK width	450	550	700	ns
	t_{BLANK}_AB(H) t_{BLANK}_CD(H)	AC	Iout=0.6A,OSC=1.6 MHz, 4×OSC setting	2.0	2.5	3.0	μs
OSCM reference signal oscillation frequency	fOSCM	AC	C_{OSC}=270 pF,R_{OSC}=100 kΩ	1200	1600	2000	kHz
Chopping frequency range	fchop	AC	Output operation (Iout=1.0 A)	40	100	150	kHz
Chopping frequency	fchop	AC	Output operation (Iout=1.0 A) OSC=1.6MHz	—	100	—	kHz

Decay Mode: Charge to Slow to Fast



Mixed Decay Mode / Detecting zero point



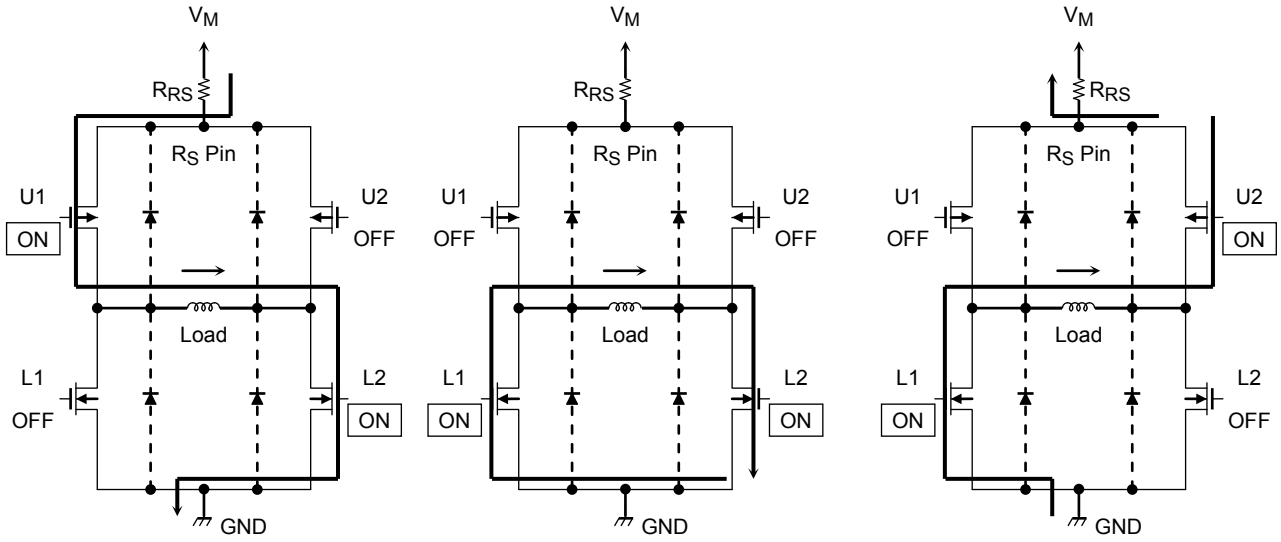


The [NF] shows the point where the output current reaches the setting current value. The [Charge] shows the different value depending on the step resolution characteristics (inductance or resistance).

Status (1)**:** When Fast->Charge operation starts before reaching zero point (Iout=0 A)
Status (2)**:** When reaching zero point (Iout=0 A)

Mixed Decay mode**:** Charge -> NF**:** Reaching setting current -> Slow -> Fast -> Charge -> ...

Output Transistor Operating Modes



Charge Mode
A current flows into the motor coil.

Slow Mode
A current circulates around the motor coil and this device.

Fast Mode
The energy of the motor coil is fed back to the power

Output Transistor Operating Function

CLK	U1	U2	L1	L2
Charge Mode	ON	OFF	OFF	ON
Slow Mode	OFF	OFF	ON	ON
Fast Mode	OFF	ON	ON	OFF

Note**:** This table shows an example of when the current flows as indicated by the arrows in the figures shown above. If the current flows in the opposite direction, refer to the following table.

CLK	U1	U2	L1	L2
Charge Mode	OFF	ON	ON	OFF
Slow Mode	OFF	OFF	ON	ON
Fast Mode	ON	OFF	OFF	ON

The TC78S121FTG switches among Charge, Slow-Decay and Fast-Decay modes automatically for constant-current control.

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Calculation of the Setting Output Current

For PWM constant-current control, the TC78S121FTG uses a clock generated by OSCM oscillator. The peak output current can be set via the current-sensing resistor (RRS) and the reference voltage (V_{ref}), as follows:

$$Iout\ (max) = Vref\ (gain) \times \frac{Vref\ (V)}{RRS\ (\Omega)}$$

Vref (gain): Vref decay ratio is 1 / 5.0 (typ.).

Ex.: In case of 100 % setting,

When Vref = 3.0 V, Torque = 100 %, and RRS = 0.51 Ω,

constant current output of the motor (peak current) is calculated as follows;

I_{out} = 3.0 V / 5.0 / 0.51 Ω= 1.18 A.

OSCM oscillation frequency

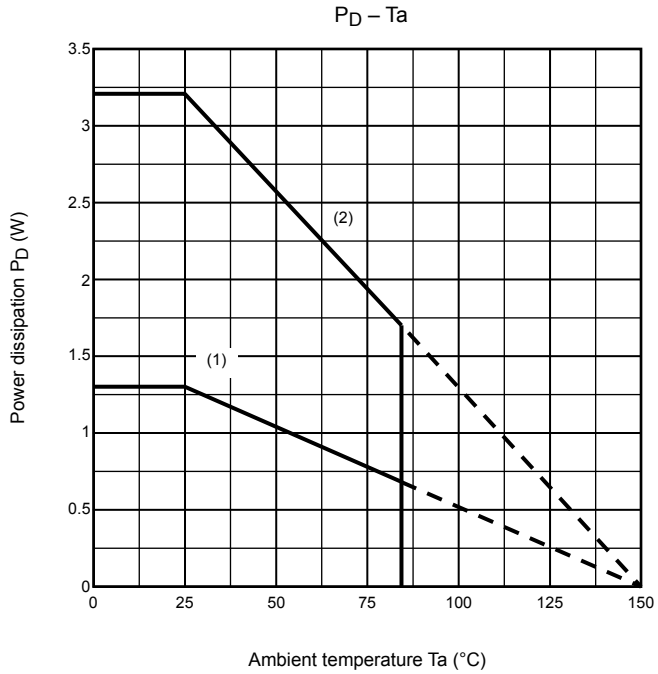
For OSCM oscillation frequency, the frequency can be changed by an external capacitor and a resistor.

By changing the frequency of the OSCM, the chopping frequency can be also changed.

Please perform the adjustment of chopping frequency referring to the following table.

Chopping frequency [kHz]	C [pF]	R [kΩ]
150	180	100
140	180	150
130	220	75
120	220	120
110	270	68
100	270	120
90	330	75
80	330	150
70	390	130
60	470	110
50	560	120
40	680	180

PD – Ta (Package Power Dissipation)

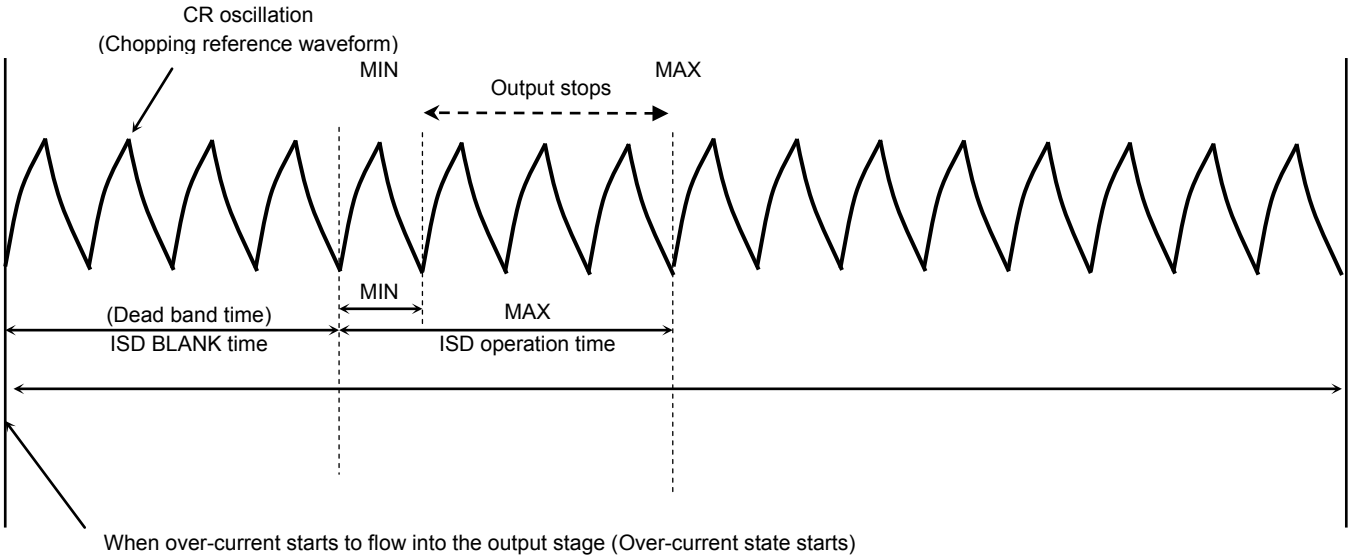


(1) IC only: R_{th} (j-a): 113°C/W

(2) When mounted on the board (100 mm × 200 mm × 1.6 mm 2-layer board: 37°C/W (typ.))

Operating Time for Over-current Detection Circuit

ISD Dead Band Time and ISD Operating Time



The over-current detection circuit has a dead band time to prevent erroneous detection of I_{RR} or spike current at switching. The dead band time being synchronized with the frequency of the OSC for setting chopping frequency is expressed as follows.

Dead band time =4 × CR time

Time required to stop the output after over-current flows into the output stage is expressed as follows.

Minimum time**:** 4 × CR time

Maximum time**:** 8 × CR time

Note that the above-mentioned operating times are achieved only when over-current flows as it is expected. Depending on the timing of output control mode, the circuit may not be triggered.

Thus, to ensure safe operation, please insert a fuse in the motor power supply.

The capacity of the fuse is determined according to the usage conditions. Please select one whose capacity does not exceed the power dissipation for the IC to avoid any operating problems.

● **tBLANK (noise rejection dead band time)**

The TC78S121FTG has two different dead band times (blank times) for different motors to be driven so as to prevent malfunctions because of switching noise.

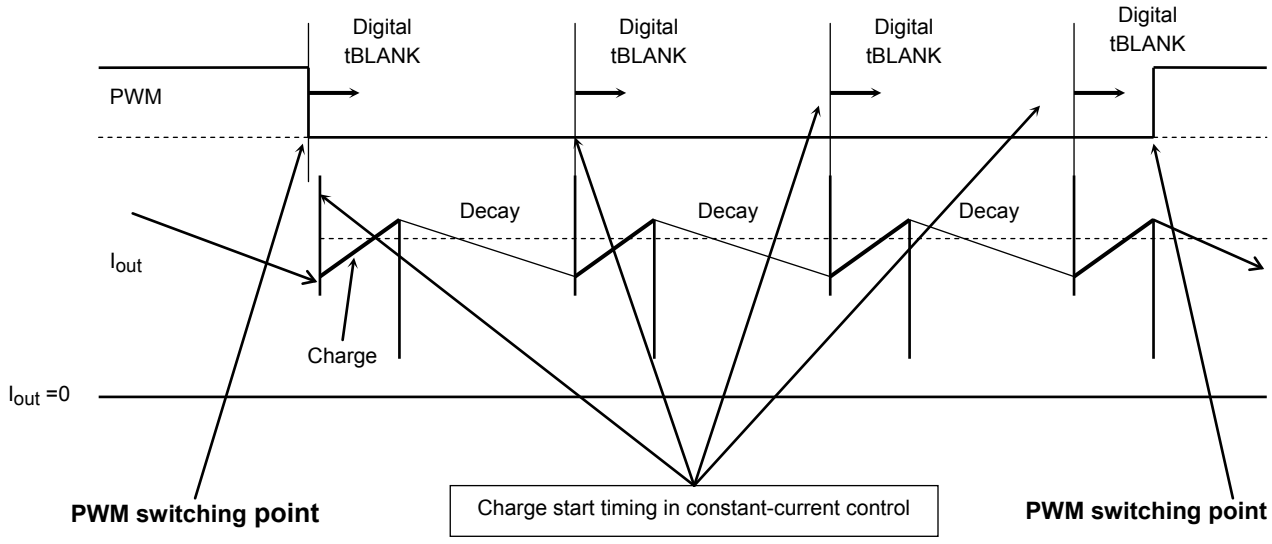
(1) Analog tBLANK Functions (in Stepping Motor Mode)

The noise rejection dead band time (analog tBLANK) defined by the AC characteristics of the motor block is fixed within the IC. It is mainly used to avoid misjudging the I_{RR} (diode recovery current) when a stepping motor is driven by constant current.
It is fixed within the IC and thus cannot be altered.

(2) Digital tBLANK (in Brushed DC Motor mode)

In addition to analog tBLANK, the digital tBLANK time, which is set in the initial mode select, is generated digitally from an external chopping period. This blank time is used to prevent false detections of over-current conditions due to recovery currents of a varistor generated during PWM operation of DC motors in DC Motor mode.
When Stepping Motor mode is selected via the mode select pins, the digital tBLANK time is nullified (0 μs) and the analog tBLANK time, which is internally fixed, becomes effective.
Since this blank time is generated based on the OSCM signal, the time can be adjusted by changing the OSCM signal frequency.
(Please note that the characteristics other than the blank time, such as motor chopping frequency and the dead band time inserted at power on, are also changed when the OSCM signal frequency is changed.)

Digital tBLANK Insertion Timing in Brushed DC Motor Mode



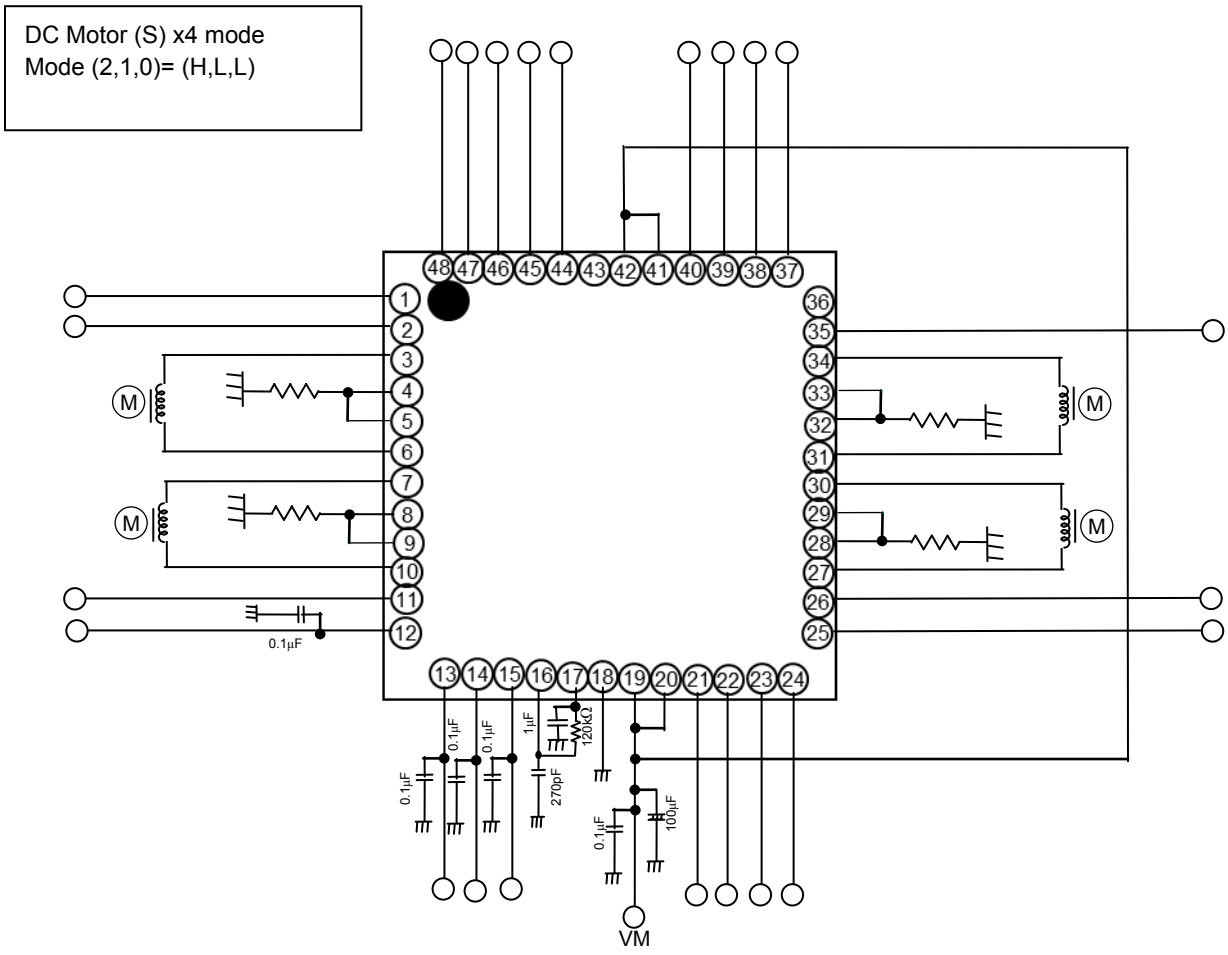
The digital tBLANK time is inserted immediately after the switching timing of externally applied PWM signals, PHASE_X (such as the switching timing between short brake and charging), and also when the charging in constant-current chopper drive is started.

The digital tBLANK time becomes effective only in DC Motor mode.

The TC78S121FTG enters 37.5 % Mixed-Decay mode when starting DC motor operation. In this mode, the TC78S121FTG stays in Charge mode for the first 4 CLK cycles of the whole period, which is also a digital tBLANK time. Thus, depending on the timing, operation mode might be switched directly to Fast-Decay mode.

Application Circuit Example

The values shown in the following figure are typical values. For input conditions, see the Operating Ranges.



Note**:** It is recommended that a bypass capacitor is added if necessary. The GND wiring must become one-point-earth as much as possible.

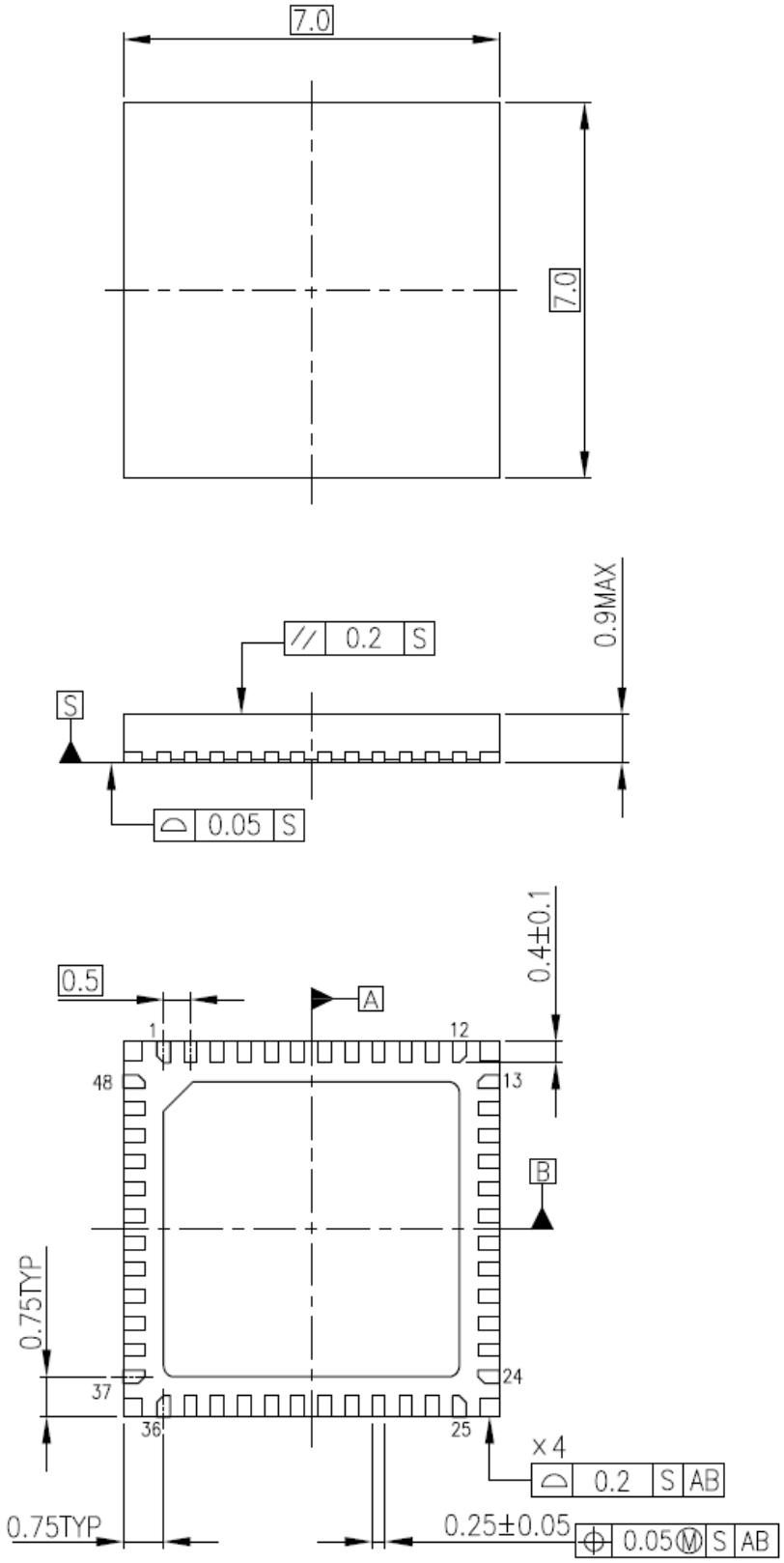
The example of an applied circuit is for reference, and enough evaluation should be done before the mass-production design.

Moreover, it is not the one to permit the use of the industrial property.

Package Dimensions

QFN48-P-0707-0.50

Unit: mm



Weight: 0.137 g (Typ.)

Notes on Contents

(1) Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

(2) Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

(3) Timing Charts

Timing charts may be simplified for explanatory purposes.

(4) Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Any license to any industrial property rights are not granted by providing these examples of application circuits.

(5) Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as Fast-blow fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback capacitor, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, over-current or IC failure can cause smoke or ignition. (The over-current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Over-current Protection Circuit
Over-current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over-current protection circuits operate against the over-current, clear the over-current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over-current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over-current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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