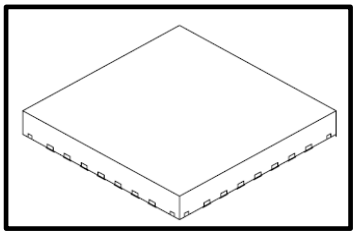
Bi-CMOS Integrated Circuit Silicon Monolithic

TB9120FTG

Bipolar stepping motor driver with a clock input interface for automotive applications



P-VQFN28-0606-0.65-002

1 Overview

TB9120FTG is a two-phase bipolar stepping motor driver with a clock input interface and a PWM constant-current control system. It can be used for a small stepping motor in a wide range of automotive applications.

2 Applications

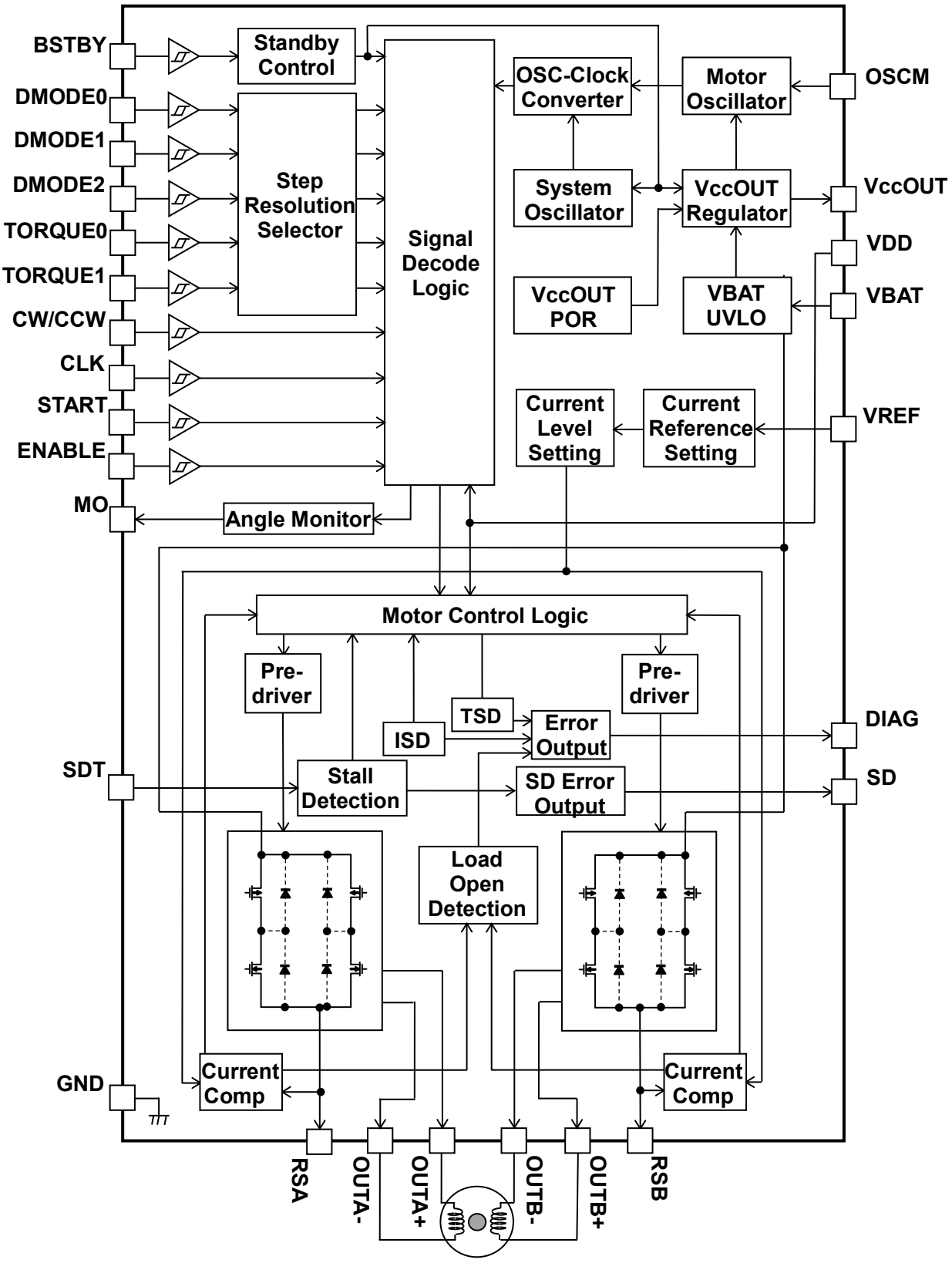
Small stepping motors for automotive applications such as an adjustment to an angle of a concave mirror in HUD, valves in motorcycles and valves/dampers for HVAC

3 Features

- A two-phase bipolar stepping motor can be driven with a single chip.
- Adoption of PWM constant-current control
- Built-in a mixed decay mode
- Excitation mode selectable: full, half, quarter, 1/8, 1/16, and 1/32 step
- On-resistance of power MOSFETs: Ron(H+L)=0.8Ω(typ.)
- Input power supply voltage(VBAT): 40V(max)
- Maximum output driving current: Overcurrent detection value, 2A(typ.)
- Internal voltage 5V(VccOUT)
- Anomaly detection functions: Over temperature detection, overcurrent detection, load open detection, OSCM pin anomaly detection and low voltage detection
- DIAG output: Over temperature detection, overcurrent detection, load open detection and OSCM pin anomaly detection
- Stall detection function and flag output function if detected
- Standby function
- Operating power supply voltage range: VBAT(opr.)=7V to 18V. Only some of the functions are guaranteed in 4.5V to 7V.
- Maximum clock input frequency: fCLK(max)＝100kHz
- Operating temperature: -40 to 125°C
- Package: VQFN28(0.65)
- AEC-Q100 qualified

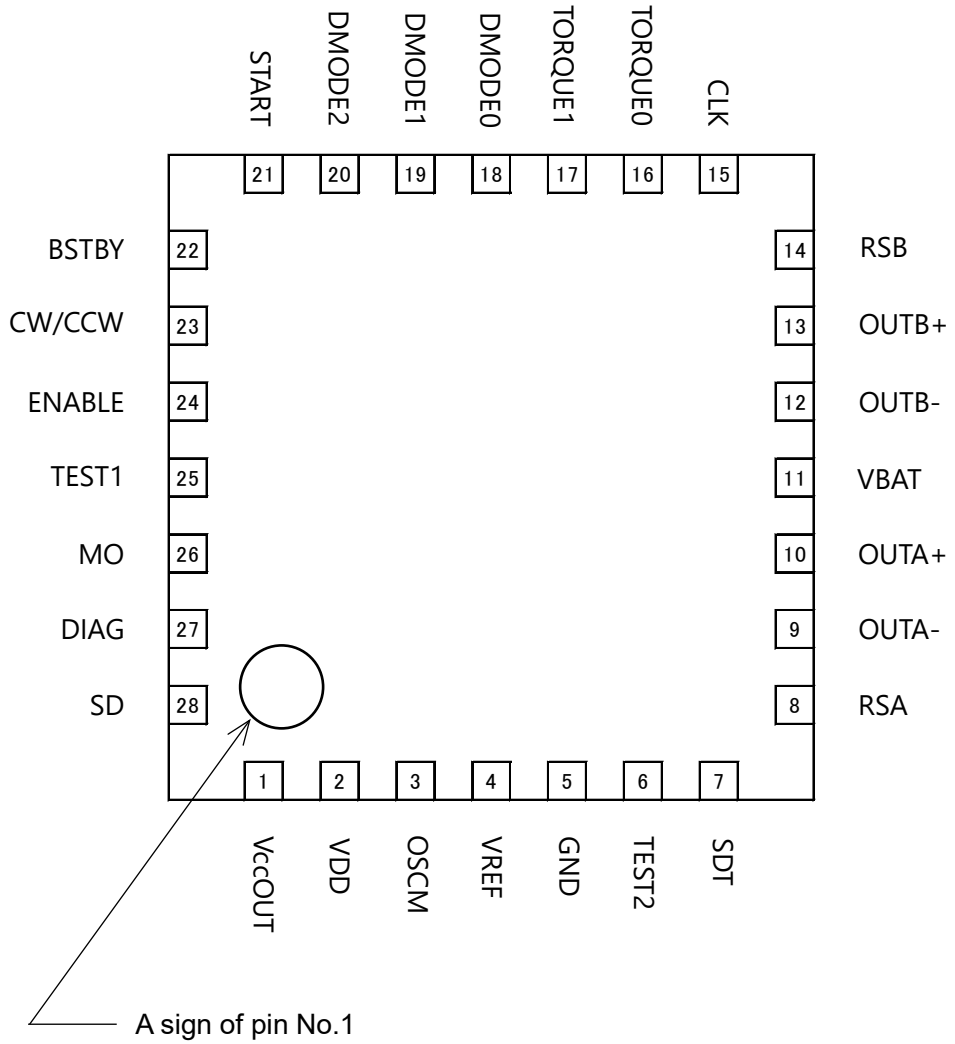
Start of commercial production
2019-03

4 Block diagram



Besides the above, there are TEST 1 and TEST 2 as the test pins for shipping inspection.
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

5 Pin Assignment (TOP View)



6 Pin Arrangement and Function Description

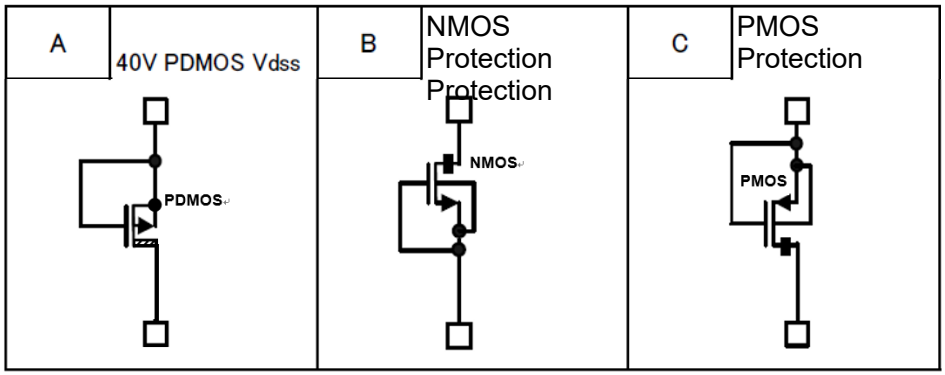
6.1 Pin Arrangement and Function Description

Pin No.	Pin name	Description
1	VccOUT	5V output. Connect it to a power smoothing capacitor.
2	VDD	5V input. Connect it to VccOUT pin (pin No.1) at the IC outside.
3	OSCM	Resistor connected pin to set an output PWM frequency
4	VREF	Voltage applied pin to set an output current value
5	GND	GND pin
6	TEST2	Test pin in shipping inspection. Do not connect anything.
7	SDT	Resistor connected pin to set a stall detection threshold. When not using the stall detection function, do not connect anything.
8	RSA	Current sensing resistor connected pin to set an output current value for phase A
9	OUTA-	Negative pin in phase A of a motor
10	OUTA+	Positive pin in phase A of a motor
11	VBAT	Battery power pin
12	OUTB-	Negative pin in phase B of a motor
13	OUTB+	Positive pin in phase B of a motor
14	RSB	Current sensing resistor connected pin to set an output current value for phase B
15	CLK	Step clock input pin. Built-in pull-down resistor 100 kΩ
16	TORQUE0	Constant current setting input 0. Built-in pull-down resistor 100 kΩ
17	TORQUE1	Constant current setting input 1. Built-in pull-down resistor 100 kΩ
18	DMODE0	Excitation mode setting input 0. Built-in pull-down resistor 100 kΩ
19	DMODE1	Excitation mode setting input 1. Built-in pull-down resistor 100 kΩ
20	DMODE2	Excitation mode setting input 2. Built-in pull-down resistor 100 kΩ
21	START	Electrical angle initializing input. Built-in pull-down resistor 100 kΩ
22	BSTBY	Standby input. Built-in pull-down resistor 100 kΩ
23	CW/CCW	Rotation direction setting input. Built-in pull-down resistor 100 kΩ
24	ENABLE	Motor driving output enabling input. Built-in pull-down resistor 100 kΩ
25	TEST1	Test pin in shipping inspection. Connect it to GND.
26	MO	Electrical angle monitoring signal output. Open drain output pin.
27	DIAG	Anomaly detection flag signal output. Open drain output pin.
28	SD	Stall detection flag signal output. Open drain output pin.
-	E-PAD	Reverse side of bed mounted with IC chip. Connect it to GND.

6.2 Layout of protection elements

Pin name	Pull-down resistor	I／O	Absolute maximum rating, upper limit voltage (V)	Protection elements		Connect to	
				Power supply side	GND side	Power supply side	GND side
VccOUT	—	O	6.0	A	B	VBAT	GND
VDD	—	Power supply	6.0	A	B	VBAT	GND
OSCM	—	O	6.0	C	B	VccOUT	GND
VREF	—	Power supply	6.0	—	B	—	GND
GND	—	GND	—	—	—	—	—
TEST2	—	O	6.0	C	B	VccOUT	GND
SDT	—	O	6.0	C	B	VccOUT	GND
RSA	—	-	1.0	C	B	VccOUT	GND
OUTA-	—	O	40	—	—	—	—
OUTA+	—	O	40	—	—	—	—
VBAT	—	Power supply	40	—	A	—	GND
OUTB-	—	O	40	—	—	—	—
OUTB+	—	O	40	—	—	—	—
RSB	—	—	1.0	C	B	VccOUT	GND
CLK	Pull-down resistor	I	6.0	—	B	—	GND
TORQUE0	Pull-down resistor	I	6.0	—	B	—	GND
TORQUE1	Pull-down resistor	I	6.0	—	B	—	GND
DMODE0	Pull-down resistor	I	6.0	—	B	—	GND
DMODE1	Pull-down resistor	I	6.0	—	B	—	GND
DMODE2	Pull-down resistor	I	6.0	—	B	—	GND
START	Pull-down resistor	I	6.0	—	B	—	GND
BSTBY	Pull-down resistor	I	6.0	—	B	—	GND
CW/CCW	Pull-down resistor	I	6.0	—	B	—	GND
ENABLE	Pull-down resistor	I	6.0	—	B	—	GND
TEST1	Pull-down resistor	I	6.0	—	B	—	GND
MO	—	O	6.0	—	B	—	GND
DIAG	—	O	6.0	—	B	—	GND
SD	—	O	6.0	—	B	—	GND

Protection elements



7 Description of operation

7.1 BSTBY Function

When BSTBY=L, the IC is kept in the standby mode.

BSTBY	Function
L	Standby mode (Internal oscillator circuits, OSCS and OSCM stop and operation of output MOSFETs to drive a motor stops)
H	Active mode

Note: 0.5ms at the most is required so that the internal circuit related to 5V in the IC becomes stable right after switching from the standby mode state to the active mode. Refer to 7.2.

Truth table

Input					Output state	Mode
CLK	CW/CCW	START	ENABLE	BSTBY		
↑	H	L	H	H	CW (Clockwise)	Normal operation
↑	L	L	H	H	CCW (Counterclockwise)	Normal operation
X	X	H	H	H	Initialization of electrical angle	Initial (Note 1)
X	X	X	L	H	High-impedance	Enable OFF (Note 2)
X	X	X	X	L	High-impedance	Standby (Note 3)

X: Don't care.

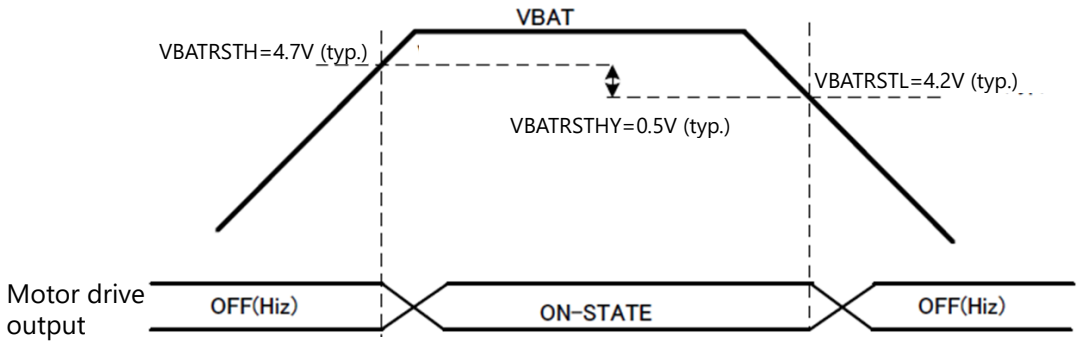
Note 1. Initial: The current level that is fixed to the initial electrical angle indicated by the function of START is output.
Note 2. Enable OFF: The outputs enter a high-impedance state. On the other hand, when START=L and a signal is being input to CLK, the internal counter proceeds.
Note 3. Standby: BSTBY has higher priority than ENABLE. Therefore, regardless of a state of ENABLE, when BSTBY=L, which makes the IC become a standby mode.

7.2 Power supply

VBAT is a battery power supply pin. VccOUT is an output pin of an internal generated power 5V. This IC has a power supply monitoring function.

VBAT low-voltage detection circuit

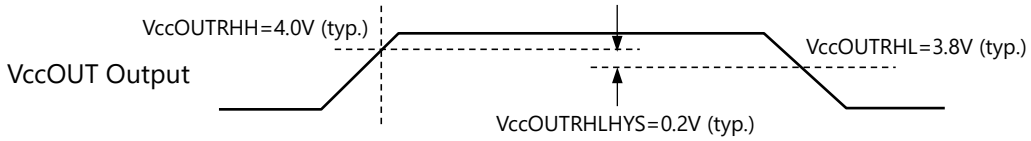
Each output pin (OUTA +, OUTA-, OUTB +, and OUTB-) turns off (high-impedance state) when VBAT voltage drops below the detection voltage 4.2V(typ.). It has 0.5V(typ.) hysteresis. Therefore, it recovers at 4.7V(typ.).



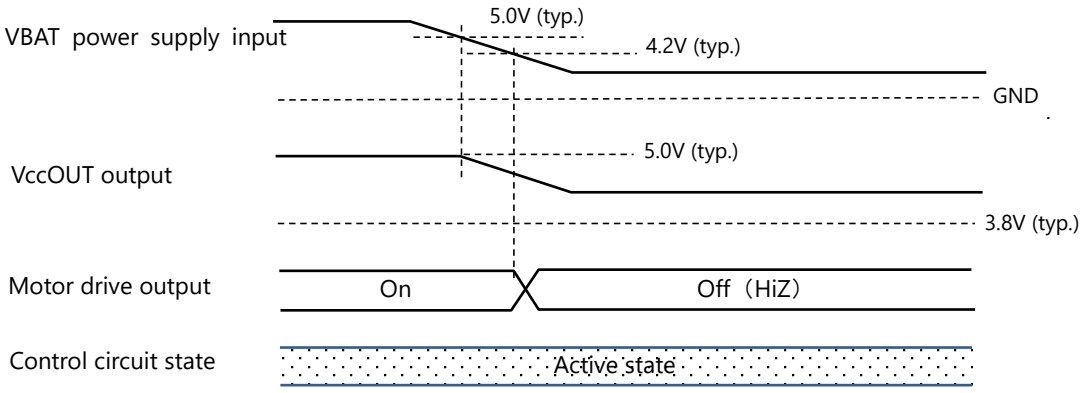
Threshold of VBAT low-voltage detection

VccOUT low-voltage detection circuit

Each output pin (OUTA +, OUTA-, OUTB +, and OUTB-) turns off (high-impedance state) and all control circuits including logic circuits are also reset when VccOUT output voltage drops below the detection voltage 3.8V(typ.). It has 0.2V(typ.) hysteresis. Therefore, it recovers at 4.0V(typ.).



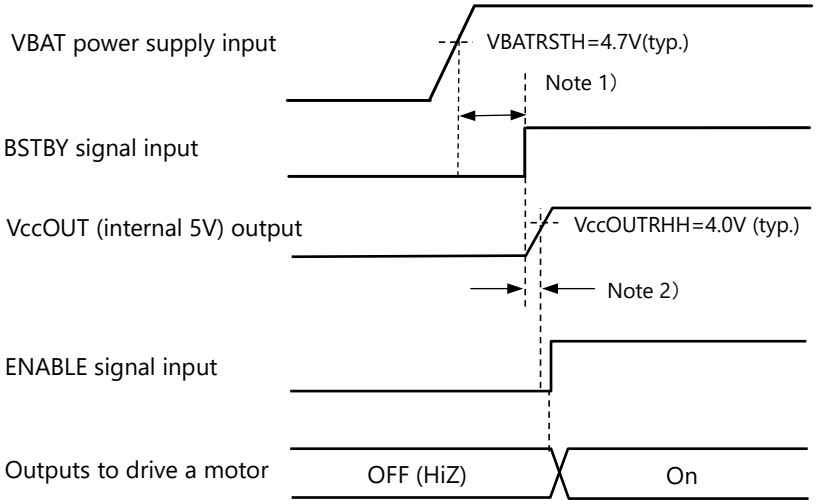
Each input control signal is reflected when VBAT voltage is less than VBAT low-voltage detection threshold 4.2V(typ.) and VccOUT voltage is more than POR threshold 3.8V(typ.). However, each output pin (OUTA +, OUTA-, OUTB +, and OUTB-) is kept in high-impedance state if VBAT voltage still stays less than VBAT low-voltage detection threshold 4.2V(typ.).



Timing charts may be simplified for explanatory purposes.

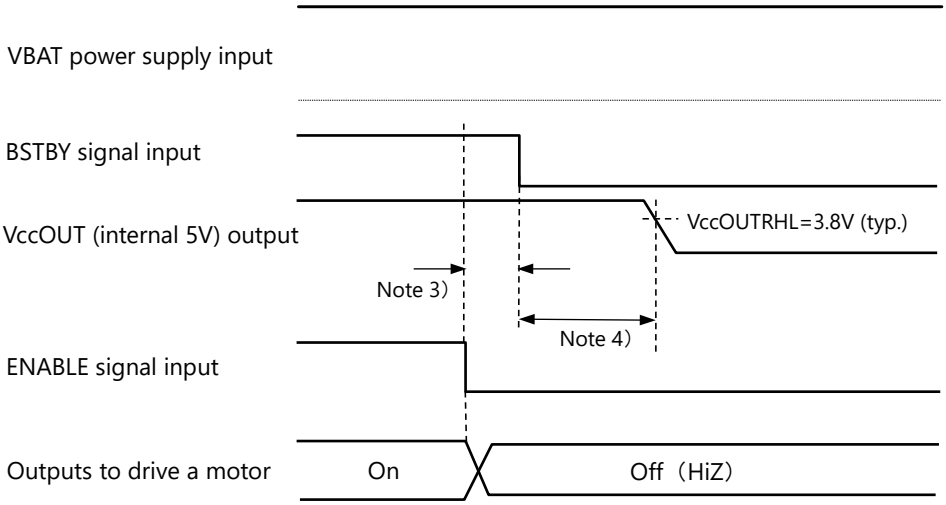
7.3 Power supply / control signal input sequence

(1) Start-up



Note 1） Make sure that VBAT voltage is more than 4.7V before a standby mode is released (BSTBY signal: L→H).
Note 2） It takes about 0.5ms at the most from releasing a standby mode to starting up VccOUT. Therefore, ENABLE signal should be input 0.5ms or more later than BSTBY signal.

(2) Shutdown



Note 3） Make sure that the outputs to drive a motor are switched off by using ENABLE signal input before a standby mode is turned on.
Note 4） After BSTBY signal input switched(H→L), pay attention to the fact that It takes 5ms until VccOUT voltage becomes less than 3.8V, in which the internal logic circuit is off.

Timing charts may be simplified for explanatory purposes.

7.4 CLK input

The electrical angle advances by 1 for each CLK input. The signal is reflected at a rising edge.

CLK input	Function
	Goes to the next step at a rising edge.
	No change (stays in the previous state)

7.5 ENABLE circuit

Switches ON/OFF outputs to drive a motor. When ENABLE input is turned from H to L under the standby mode released (BSTBY=H), constant current operation starts, an internal counter which is synchronized with CLK input moves forward and then a motor begins to run.
Be sure to fix ENABLE pin to the L level during a power supply start-up and shutdown.
ENABLE controls only switching ON/OFF for the outputs to drive a motor. However, the internal counter proceeds because the internal logic circuit counter is still working even when ENABLE=L; the outputs to drive a motor turns off.

ENABLE input	Output MOSFET
H	ON
L	OFF

In addition, in the case where DIAG pin is latched to L level after either overcurrent detection or over temperature detection or OSCM pin anomaly detection from a power fault, a ground fault or an open, refer to 7.10, the latch can be released by setting ENABLE pin to L level whose duration should be 0.2ms or more(Note). However, if an overcurrent state, an over temperature state or an OSCM pin anomaly state continues, DIAG outputs L level again.

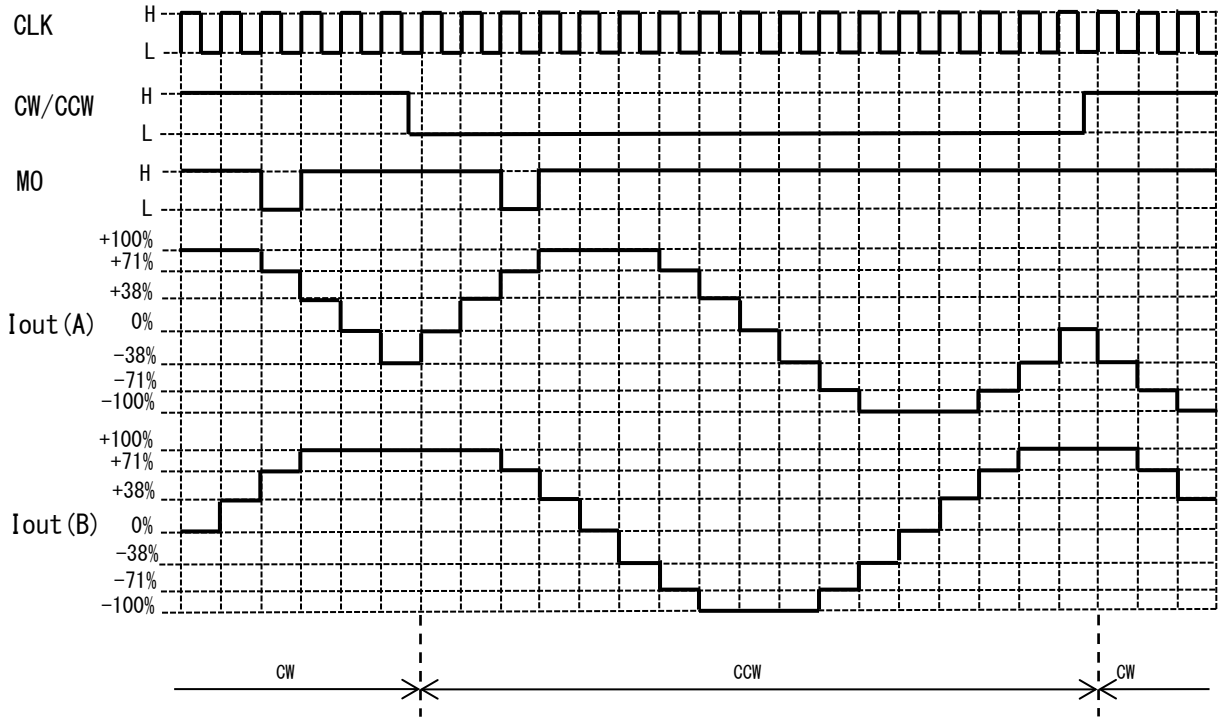
Note) Inspection for it is not conducted at the time of shipment.

7.6 CW/CCW control circuit

Switches the rotation direction of the stepping motor. When CW/CCW=H, the current in the phase A is output with a phase advance of 90° relative to that in the phase B. When CW/CCW=L, the current in the phase B is output with a phase advance of 90° relative to that in the phase A.

CW/CCW input	Function
H	Clockwise (CW)
L	Counterclockwise (CCW)

e.g. when CW/CCW is changed at quarter step resolution:



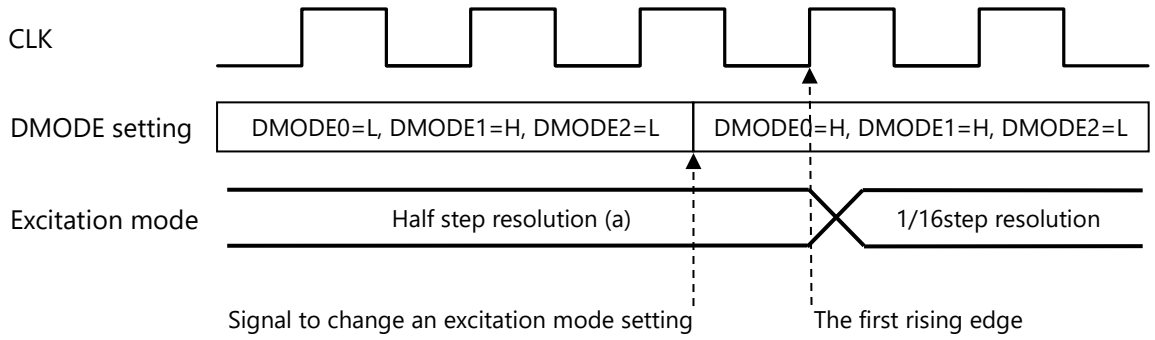
Timing charts may be simplified for explanatory purposes.

7.7 Excitation mode setting (DMODE)

DMODE0, DMODE1 and DMODE2 switch step resolution.
When DMODE 0 = DMODE 1 = DMODE 2 = L, the current setting of the phase A is set to 71% and the current setting of the phase B is also set to 71%. At this time, the L level is output from the MO pin.

DMODE0 input	DMODE1 input	DMODE2 input	Function
L	L	L	A phase 71%, B phase 71%
L	L	H	Full step resolution setting
L	H	L	Half step resolution (a) setting
L	H	H	Quarter step resolution setting
H	L	L	Half step resolution (b) setting
H	L	H	1/8 step resolution setting
H	H	L	1/16 step resolution setting
H	H	H	1/32 step resolution setting

As shown in the figure below, when step resolution is switched with DMODE pins, it is reflected at the first rising edge of CLK after the change.



Timing charts may be simplified for explanatory purposes.

7.8 START Function

Initializes an internal counter and sets an electrical angle to an initial position.

START input	Input function
H	Initialization of electrical angle (Setting to initial position)
L	Normal operation

When START is set to H, an electrical angle stays in the initial position, and then L level is output from MO pin.

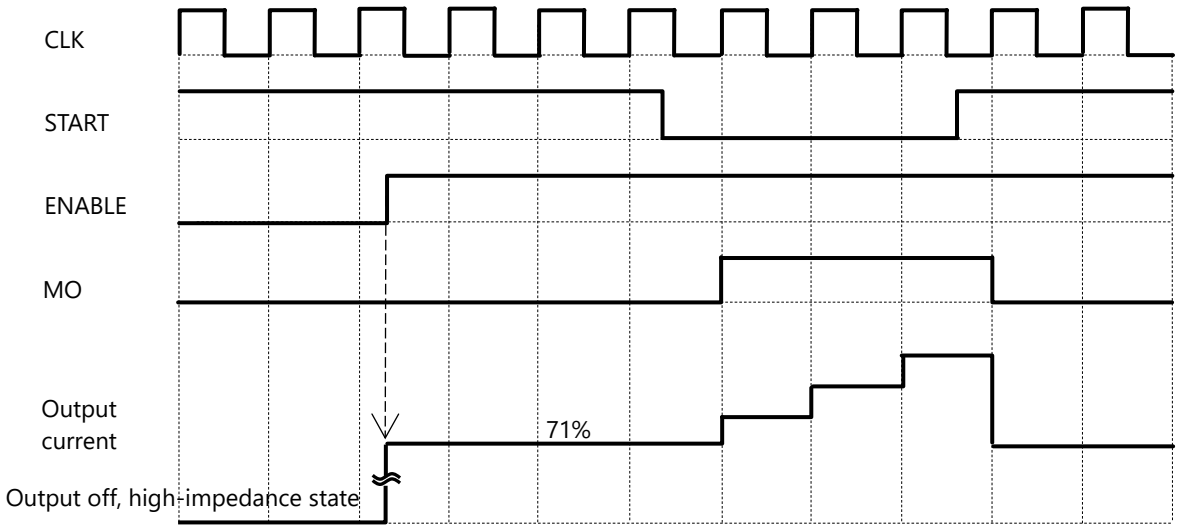
When START is set to H, a current setting in each phase is as follows.

Excitation mode	Current setting in A phase	Current setting in B phase	Initial electrical angle and initial position
Full step resolution	100%	100%	45°
Half step resolution (a)	100%	100%	45°
Half step resolution (b)	71%	71%	45°
Quarter step resolution	71%	71%	45°
1/8 step resolution	71%	71%	45°
1/16 step resolution	71%	71%	45°
1/32 step resolution	71%	71%	45°

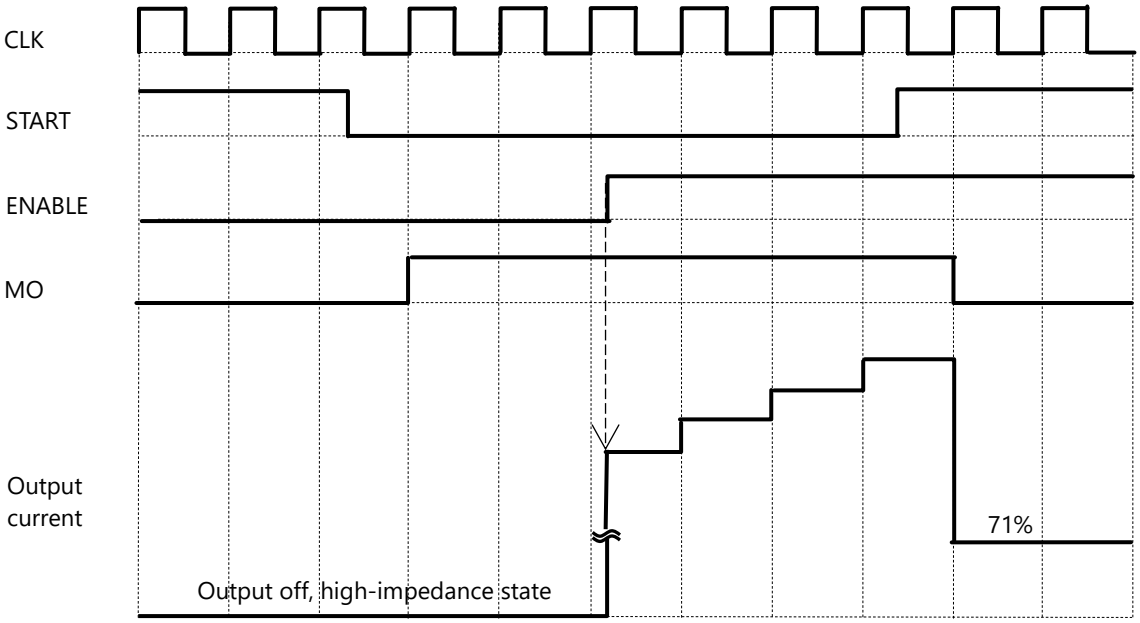
A position of the initial electrical angle in the above table is defined as the initial position, and when it reaches the initial position during motor rotation, an L level is output from MO pin.
In addition, a change of the state of START pin is reflected in outputs as synchronized with a CLK signal.

Examples of motor function operation

(1) Timing chart (In the case of ENABLE to START)



(2) Timing chart (In the case of START to ENABLE)



Regarding (1) and (2) above, the rise of output current starts coming out at the timing of a charge mode of output PWM chopping period after switching ENABLE from L to H.
The output PWM chopping period is not synchronized with CLK input signal.

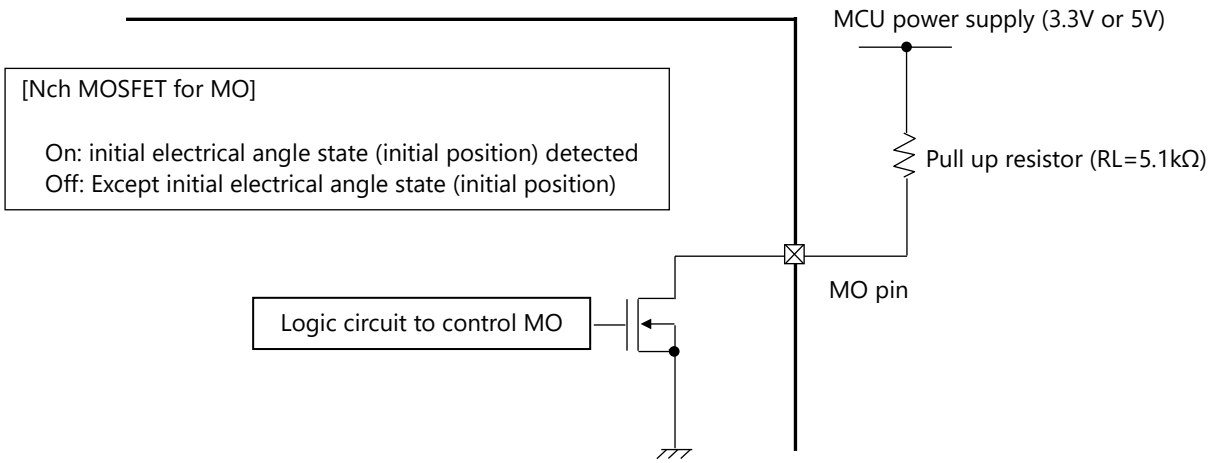
Timing charts may be simplified for explanatory purposes.

7.9 MO output

Monitors an electrical angle. MO pin outputs L in a state of an initial electrical angle (an initial position).

State of electrical angle	MO output
Except initial state (initial position)	High-impedance
Initial state (initial position)	L

MO is an open drain pin of Nch MOSFET output; therefore, please pull up the pin with an external resistor to the same potential (3.3 V or 5.0 V) as an MCU power supply. The pin stays in high-impedance except for an initial electrical angle state(initial position), on the other hand, the internal Nch MOSFET turns on if an initial electrical angle state (initial position) is detected. If the pin is not used, please leave it open.



The above circuit diagram is partially omitted and simplified in order to explain the operations.

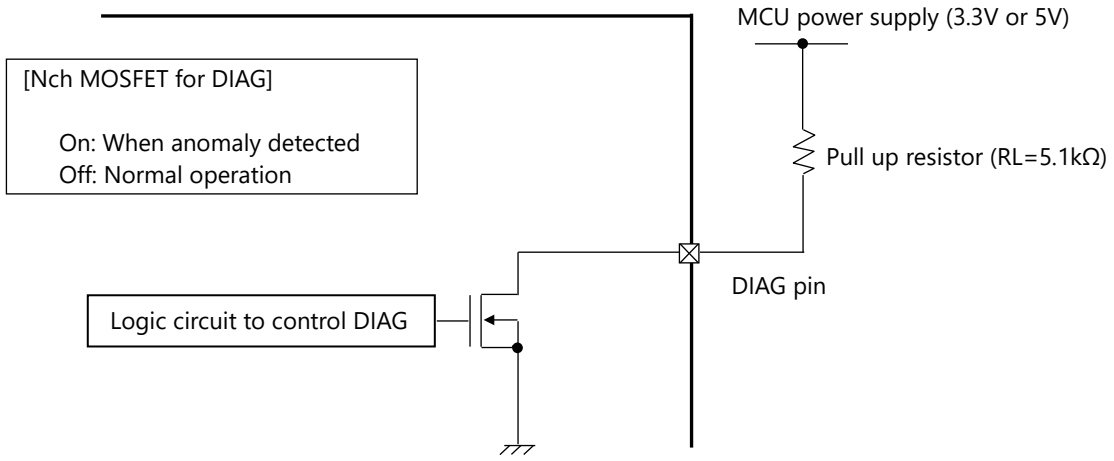
7.10 DIAG function (Anomaly state diagnosis)

If an anomaly state (a motor load open, over temperature (TSD), overcurrent (ISD) or an OSCM pin anomaly (an open, a power supply fault or a ground fault)) is detected, L is output from DIAG pin.

Anomaly detection	Output from DIAG
Normal state (normal operation)	High-impedance
Motor load open	L
Over temperature (TSD)	L
Overcurrent (ISD)	L
OSCM pin anomaly (open, power supply fault or ground fault))	L

DIAG is an open drain pin of Nch MOSFET output; therefore, please pull up the pin with an external resistor to the same potential (3.3 V or 5.0 V) as an MCU power supply. The pin stays in high impedance during normal operation, on the other hand, the internal Nch MOSFET turns on If an anomaly state (a motor load open, over temperature (TSD), overcurrent (ISD) or an OSCM pin anomaly (an open, a power supply fault or a ground fault)) is detected. When over temperature (TSD), overcurrent (ISD) or an OSCM pin anomaly (an open, a power supply fault or a ground fault)) is detected, DAIG works as a latch circuit. The latch can be released by either rebooting VBAT or setting ENABLE pin to L level whose duration should be 0.2ms or more(Note). If the pin is not used, please leave it open.

Note) Inspection for it is not conducted at the time of shipment.



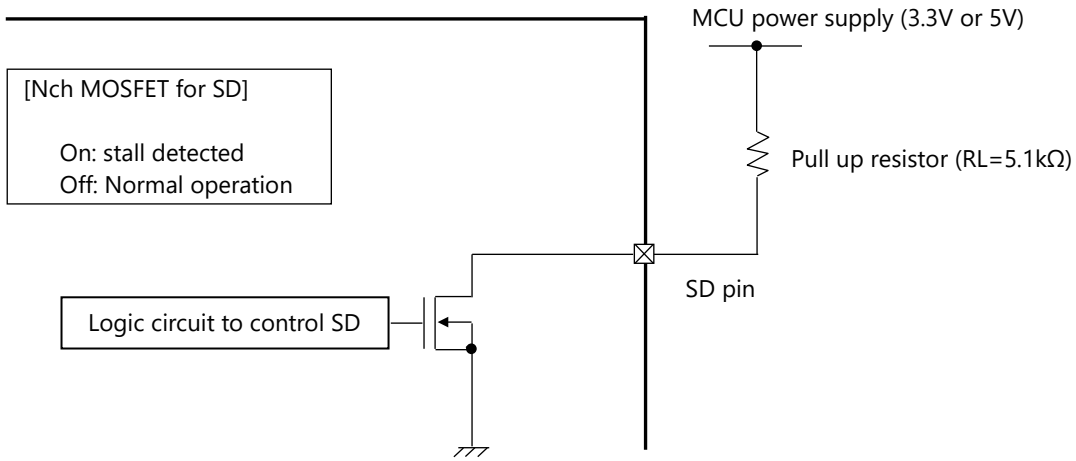
The above circuit diagram is partially omitted and simplified in order to explain the operations.

7.11 Stall detection (SD: Stall detection) function

When a stall (step-out) is detected, L is output from SD pin.

Mode	Output from SD
In normal state (normal operation)	High impedance
When stall (step-out) detected	L pulse, 100μs(typ.)

SD is an open drain pin of Nch MOSFET output; therefore, please pull up the pin with an external resistor to the same potential (3.3 V or 5.0 V) as an MCU power supply. The pin stays in high impedance during normal operation, on the other hand, if a stall detected, the internal Nch MOSFET turns on and L pulse (100μs(typ.)) is output from the pin at every detection. If the pin is not used, please leave it open.

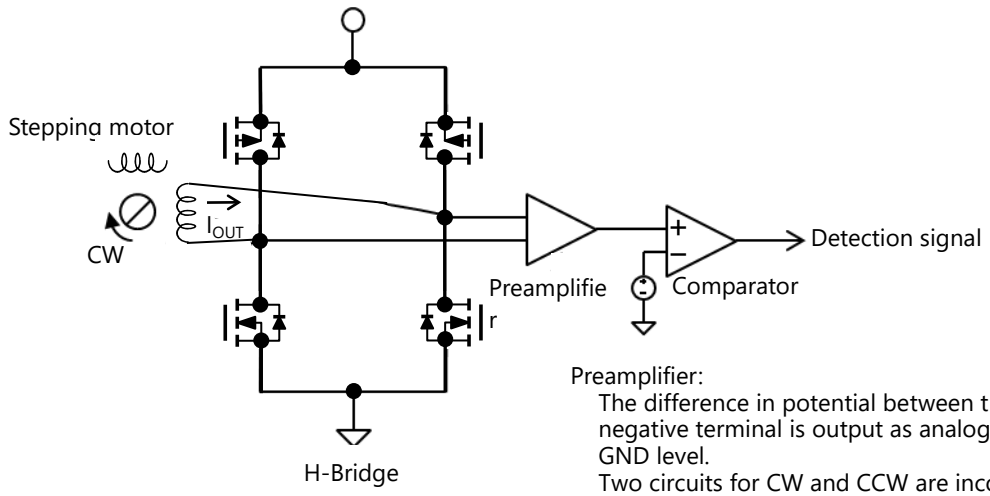


The above circuit diagram is partially omitted and simplified in order to explain the operations.

Description of operation

Certain voltage as the potential difference between both terminals of each coil of a motor (that is, OUTA + pin and OUTA- pin, and OUTB + pin and OUTB- pin) is normally generated by induced voltage during the period when a current level is set at 0 (zero) A as a motor is running. On the other hand, unless a motor runs, no voltage at both terminals of each coil of a motor can be generated because of no induced voltage.
In this function, unless induced voltage is generated more than the defined voltage at that period, the IC recognizes that a motor doesn't run and then judges that it is a stall.

Configuration of stall detection circuit



Preamplifier:
The difference in potential between the positive and negative terminal is output as analog voltage from GND level.
Two circuits for CW and CCW are incorporated in each of the phase A and B.

Setting of stall detection threshold

A stall detection threshold is set by either connecting an external resistor RSDT between SDT pin and GND or by applying DC voltage VSDT to SDT pin.

(1) In the case of an external resistor RSDT connected between SDT pin and GND

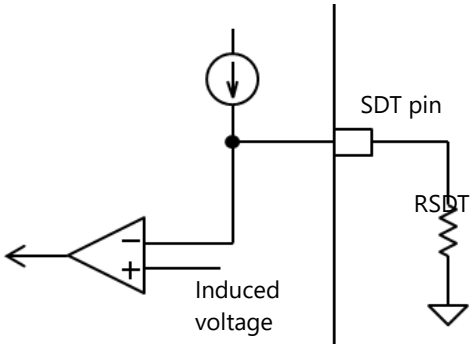
- The product of an SDT pin external resistance RSDT multiplied by an SDT pin current ISDT is an SDT pin threshold setting voltage VSDT.

  VSDT(V) = RSDT(Ω) × ISDT(A)
- Induced voltage from a motor is directly compared to the SDT pin voltage VSDT inside the IC.
- RSDT should be set as follows. 0kΩ ≦ RSDT ≦ 230kΩ

(2) In the case of DC voltage VSDT applied to SDT pin.

- Induced voltage from a motor is directly compared to applied voltage VSDT inside the IC.
- Applied voltage to SDT pin should range from 0V to 3.0V.

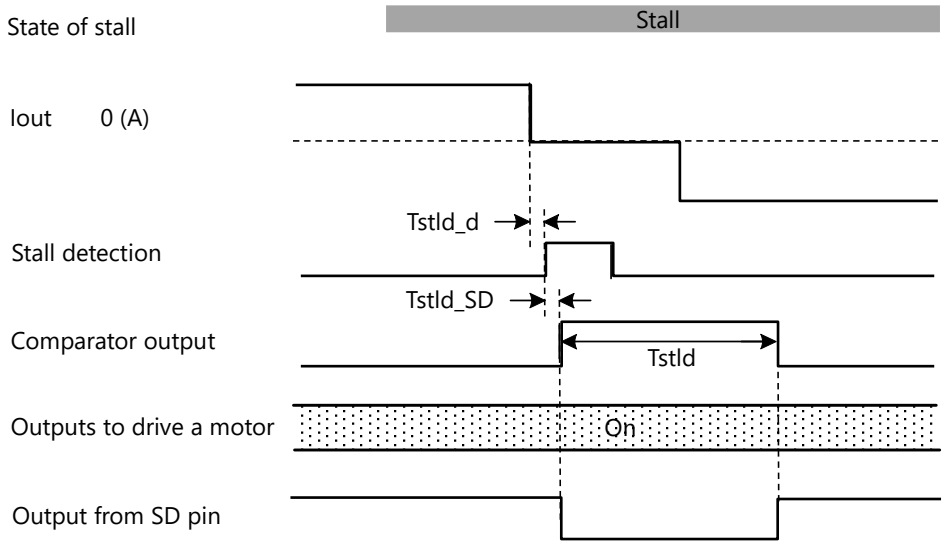
If the pin is not used, please leave it open.



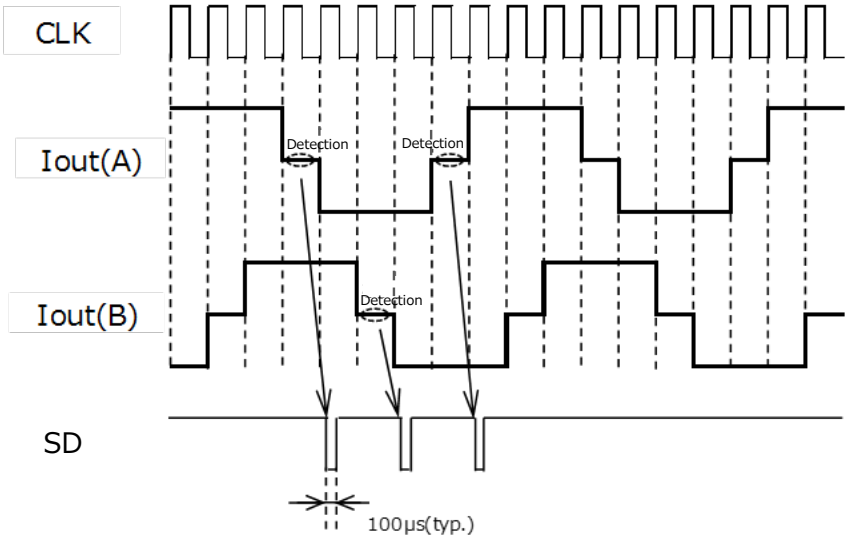
Notes on the stall detection function

- When a motor runs with full step resolution, the stall detection function does not work because there is no period of current level 0 (zero) A setting in that step resolution.
- If either rotation speed of a motor is low or induced voltage is not sufficiently induced due to a type of motor, the stall detection function may not work properly. Therefore, a threshold value should be set after characteristics of a motor, driving conditions and so on have been validated certainly in advance.
- While a motor runs at low speed, for example, during a start-up from stopping, because induced voltage is not sufficiently induced, there is a possibility that the stall detection function may not work properly. This period need to be exempted to use the stall detection function effectively.
- Even if a stall is being detected, outputs to drive a motor keep turning on continuously. The stall detection circuit doesn't change the state of outputs to drive a motor.
- SD pin outputs L pulse, whose width is 100μs(typ.), as a stall detection signal while current is 0A, on the other hand, in other periods a state of SD pin stays in high-impedance. When a stall is being detected, that routine repeats.

Timing chart (1) when stall detected



Timing chart (2) when stall detected



Timing of neither a rising nor a falling edge of output signals from SD pin is synchronized with CLK and other signals.

Timing charts may be simplified for explanatory purposes.

7.12 OSC circuit

This IC has two oscillator circuits, OSCM and OSCS. They are used as a reference clock for other circuits.

- OSCM oscillator circuit : generation of a clock signal to set PWM chopping frequency
- OSCS oscillator circuit : generation of a clock signal to work internal circuits except PWM chopping one in the IC

(1) OSCM oscillation (to set PWM chopping frequency)

OSCM oscillation frequency is determined by an external resistor connected between OSCM pin and GND, and then PWM chopping frequency fPWM is set.

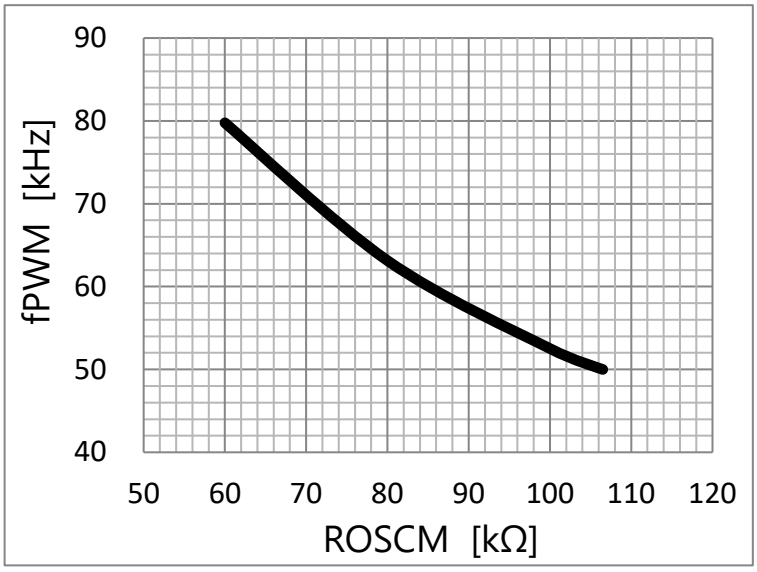
PWM chopping frequency fPWM and OSCM oscillation frequency should be set as the following ranges:

- 50kHz ≦ fPWM ≦ 80kHz
- 1600kHz ≦ fOSCM ≦ 2560kHz

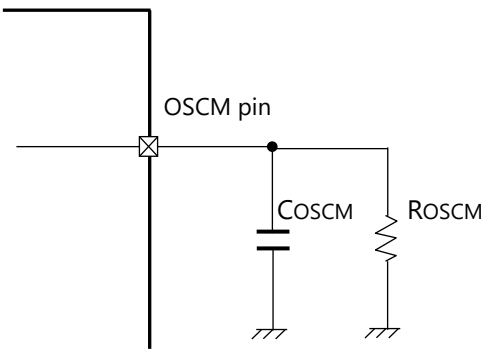
OSCM oscillation frequency fOSCM and PWM frequency fPWM is calculated by the following equation.

- fPWM = 1 / 32 × fOSCM

The relationship between fPWM and ROSCM is shown in the below chart. This is just reference data and can be changed under some conditions.

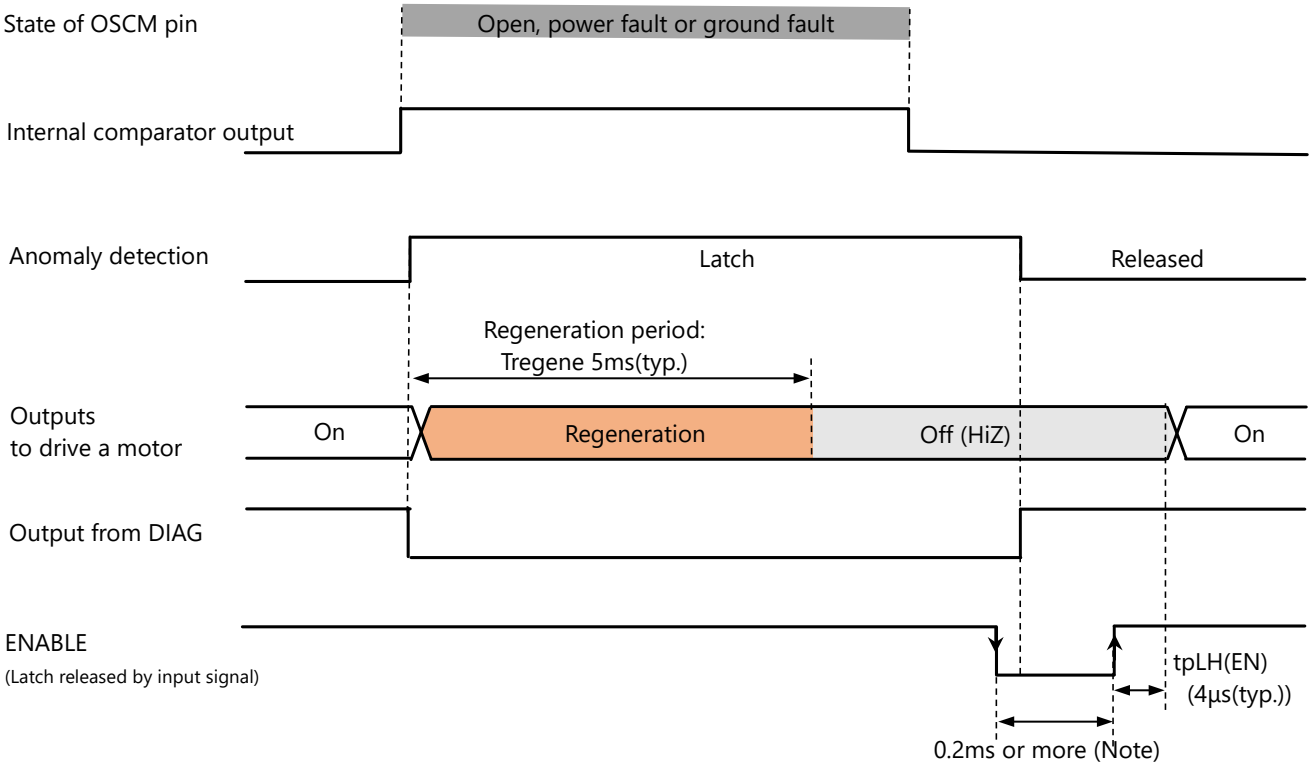


An external resistor ROSCM is required between OSCM pin and GND, moreover, an external capacitor COSCM, whose recommended value is 0.1μF, should also be placed between them to stabilize the pin.



The above circuit diagram may be simplified for explanatory purposes.

If either a power fault or a ground fault or an open occurs at OSCM pin, outputs to drive a motor turn off, that is, high-impedance, and then DIAG pin is latched to L level. It recovers right after either rebooting VBAT or setting ENABLE pin to L level whose duration should be 0.2ms or more(Note). In the case where L is input to ENABLE pin to release a latch, the release is done during L period on ENABLE and an output signal from DIAG changes from L to H at the same time. Outputs to drive a motor switch from off to on 4μs(typ.) (=tpLH(EN)) after the rising edge of L signal which is input to ENABLE



Note) Inspection for it is not conducted at the time of shipment.

Timing charts may be simplified for explanatory purposes.

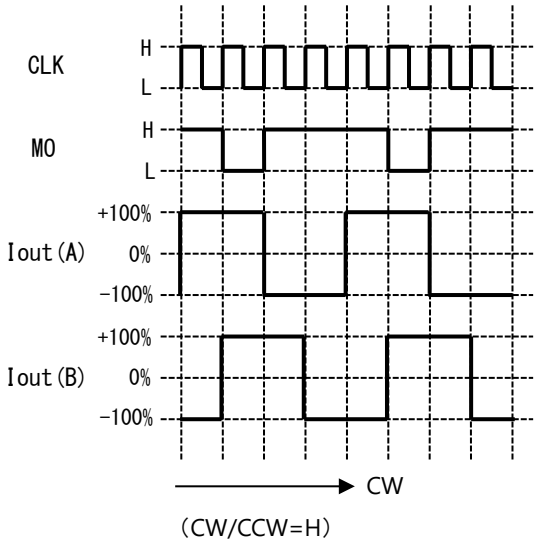
(2) OSCS oscillation (to work internal circuits in the IC)

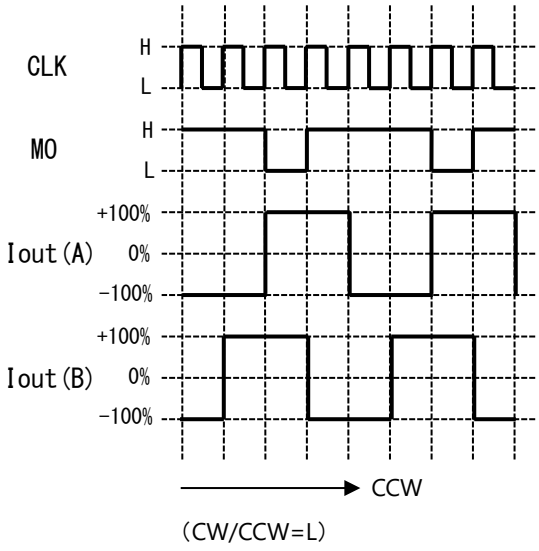
OSCS oscillation frequency is set at 4MHz(typ.) by internal circuit in the IC.

7.13 Operation of motor function

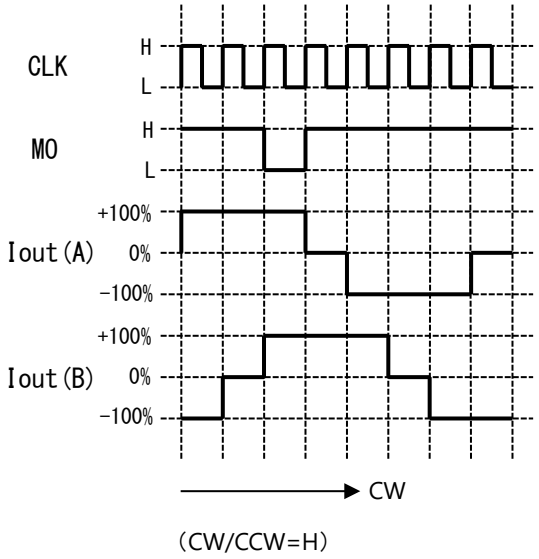
Electrical angle and initial position in excitation mode setting

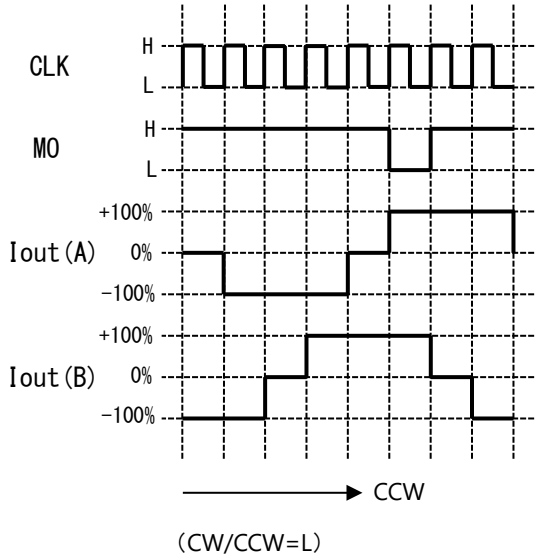
[Full step resolution setting] when ENABLE=H, START=L





[Half step resolution (a) setting] when ENABLE=H, START=L

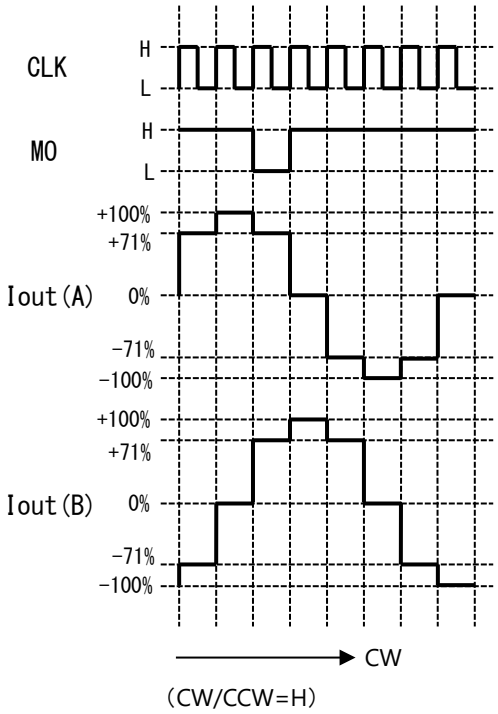


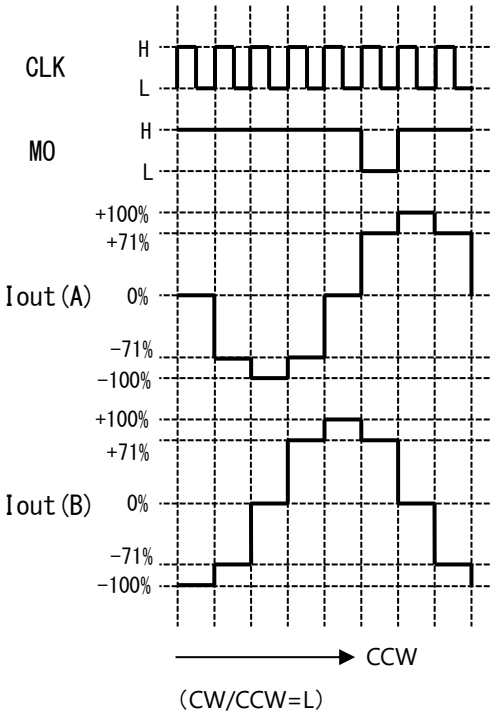


∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

[Half step resolution (b) setting] when ENABLE=H, START=L

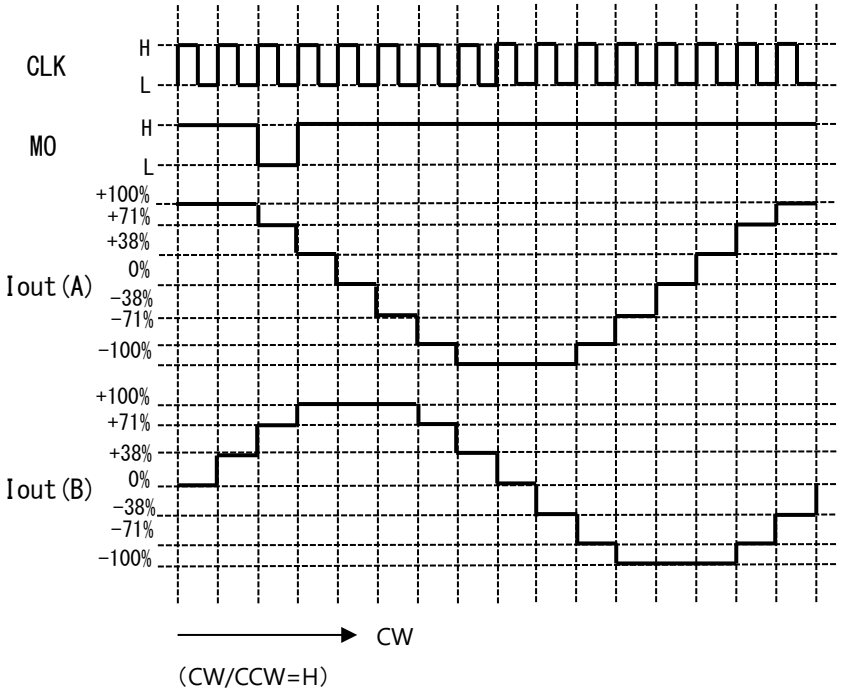




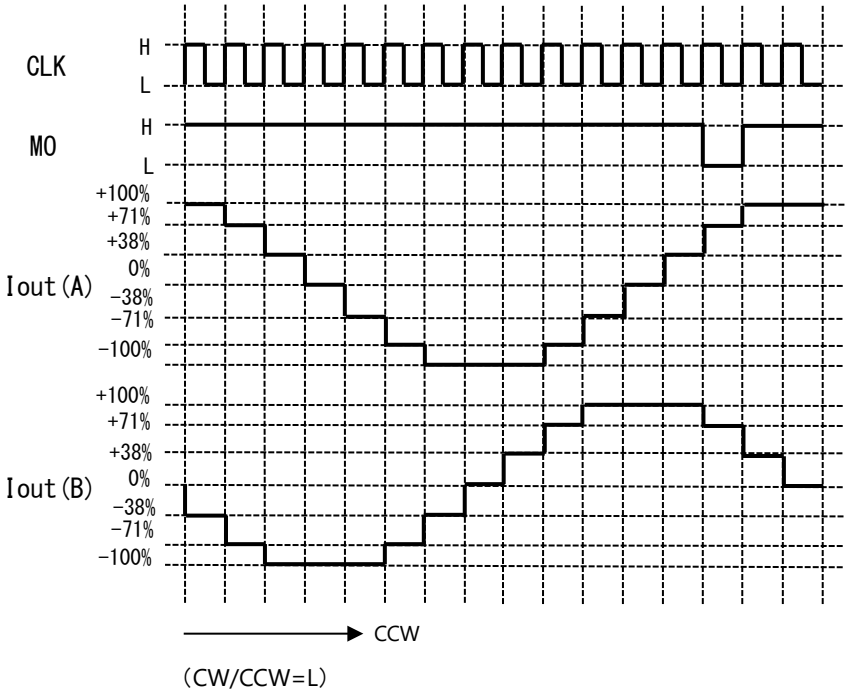
∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

[Quarter step resolution setting] when ENABLE=H, START=L



(CW/CCW=H)

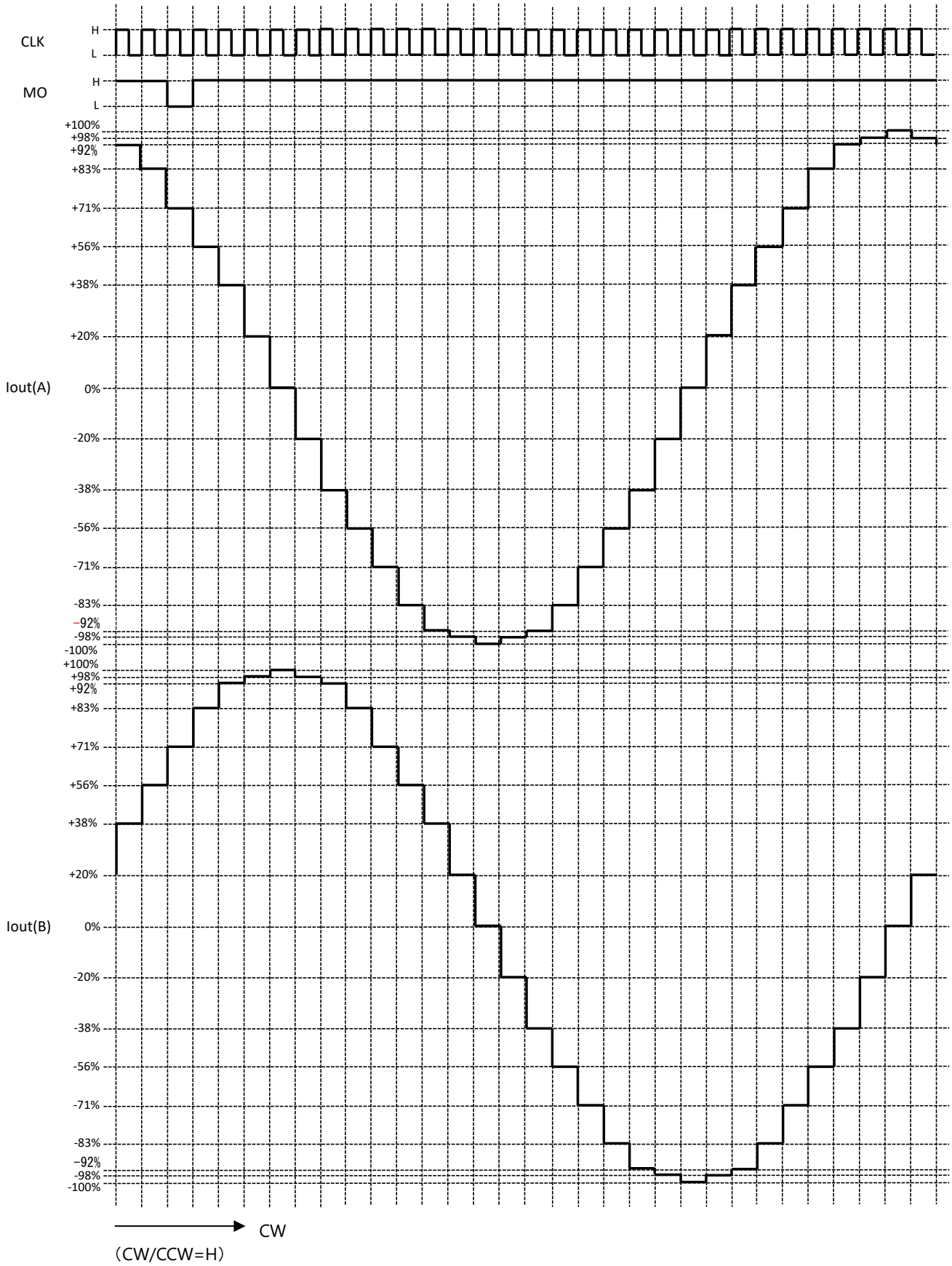


(CW/CCW=L)

∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

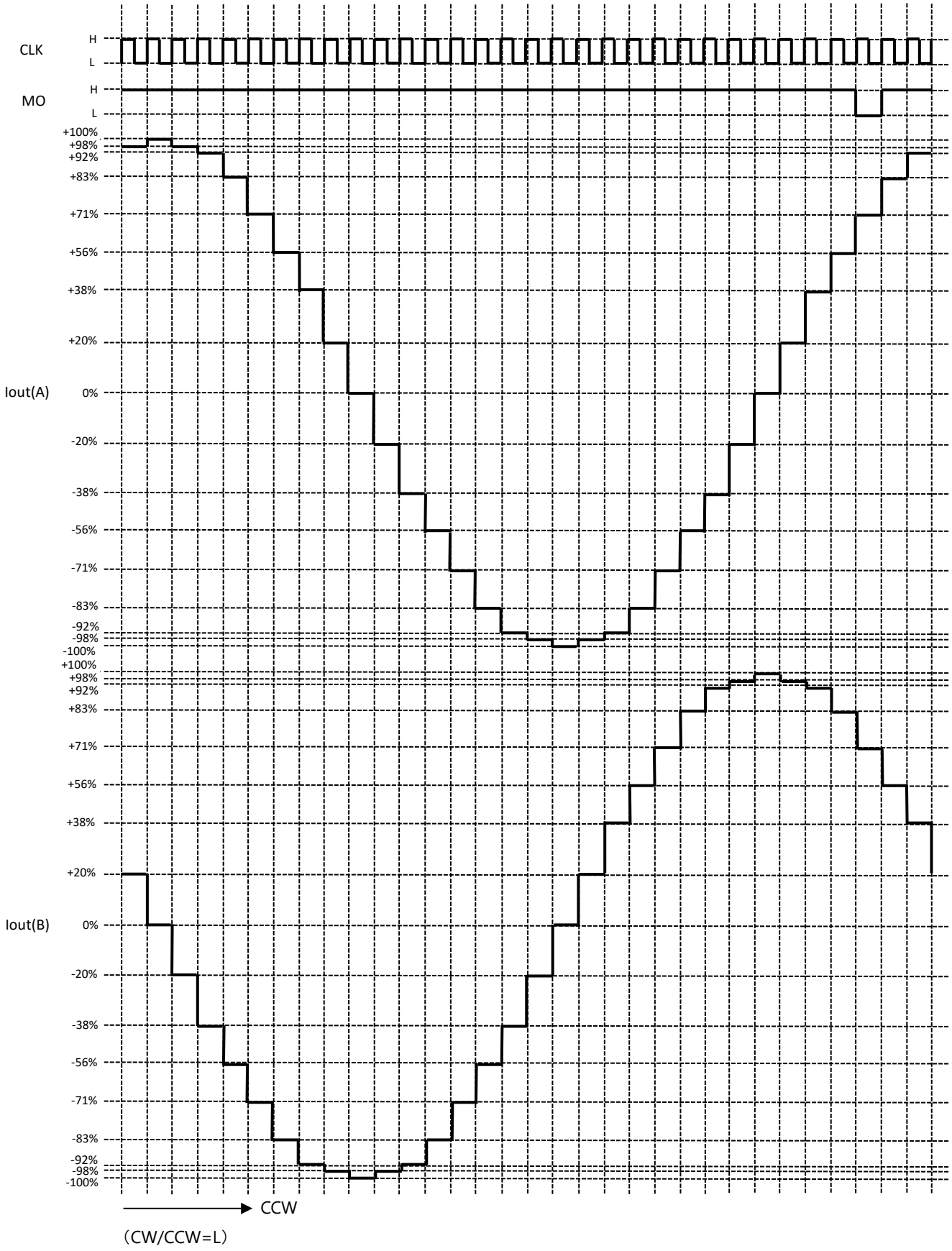
[1/8 step resolution excitation setting] when ENABLE=H, START=L



∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

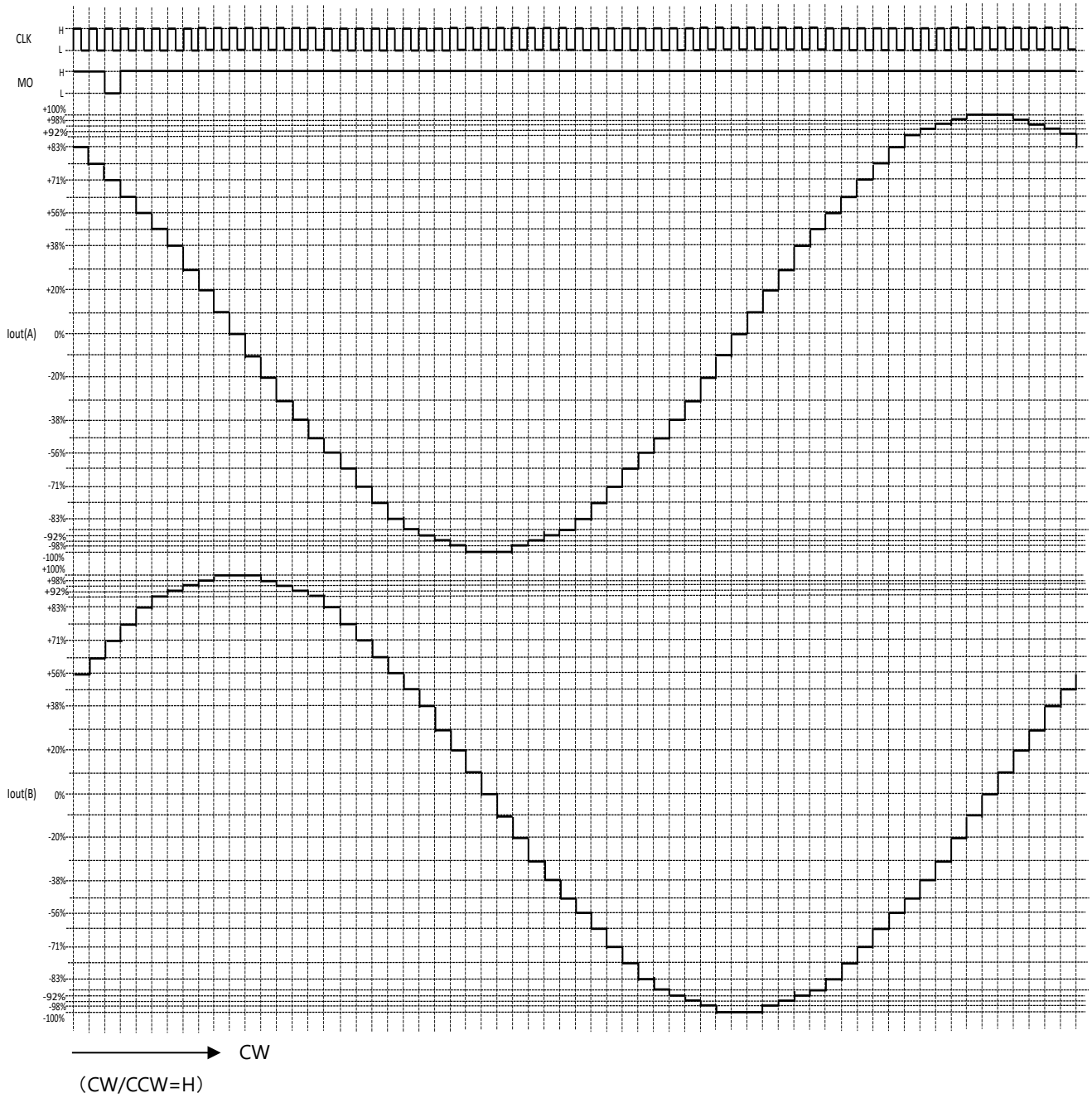
[1/8 step resolution setting] when ENABLE=H, START=L



∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

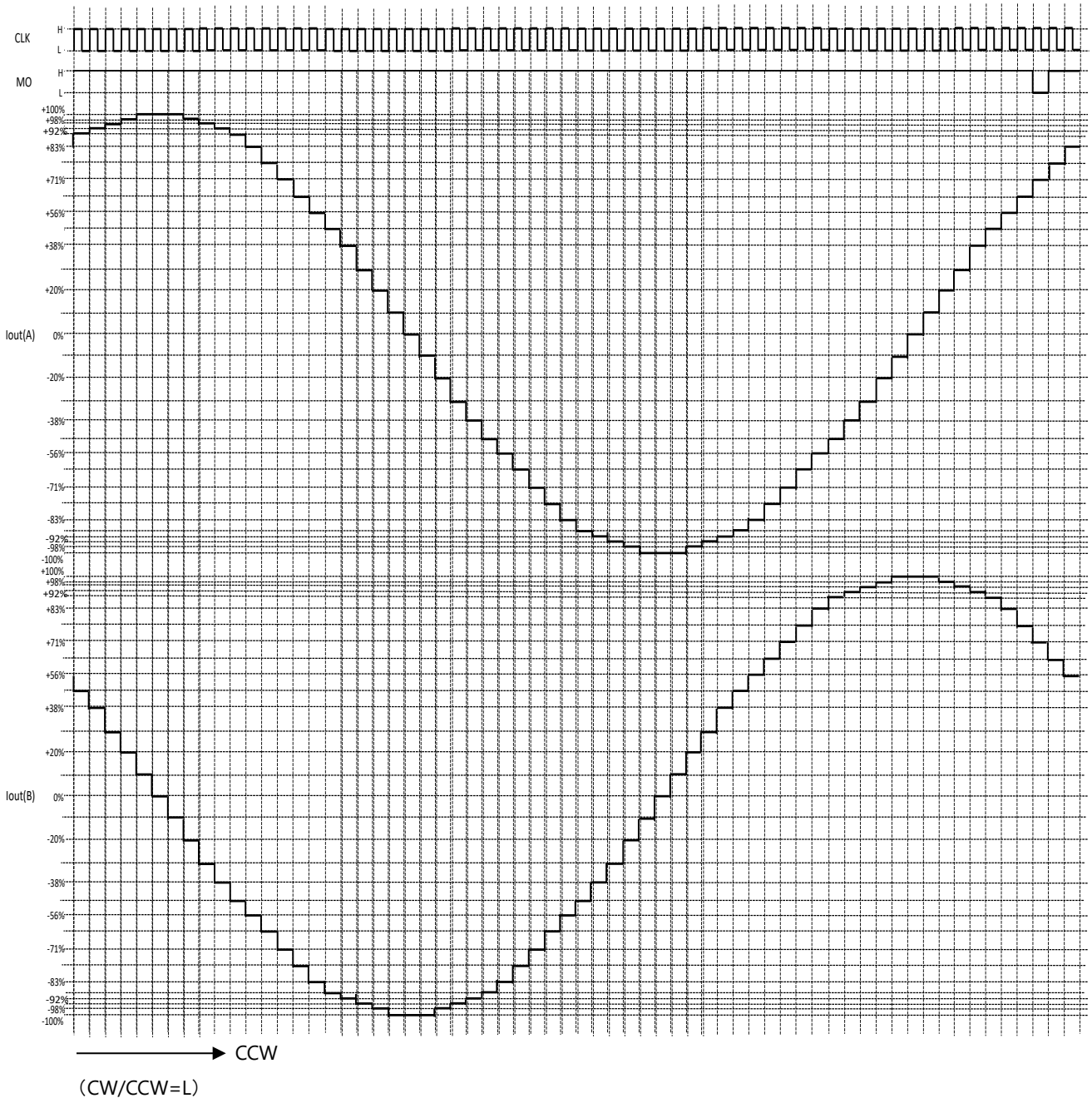
[1/16 step resolution setting] when ENABLE=H, START=L



∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

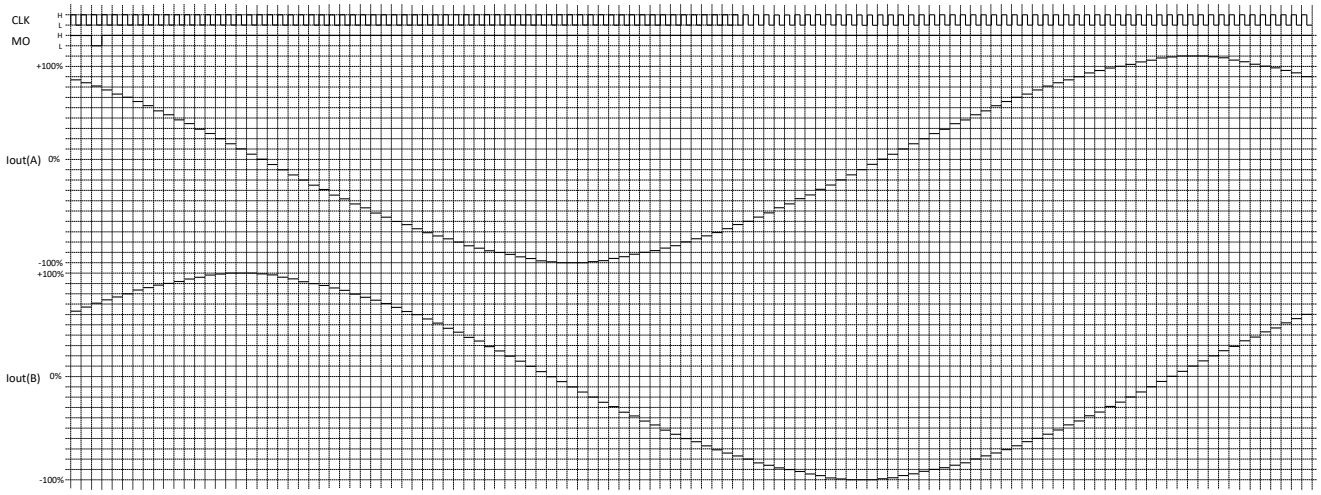
[1/16 step resolution setting] when ENABLE=H, START=L



∗ The waveform can be output from MO pin when pulled up.

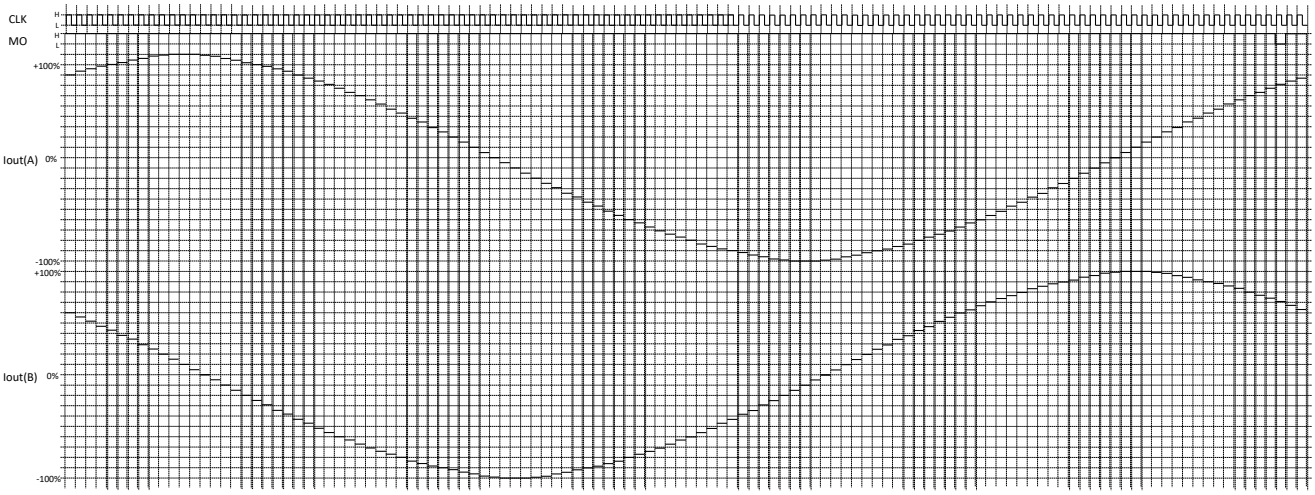
Timing charts may be simplified for explanatory purposes.

[1/32 step resolution setting] when ENABLE=H, START=L



CW

（CW/CCW=H）



CCW

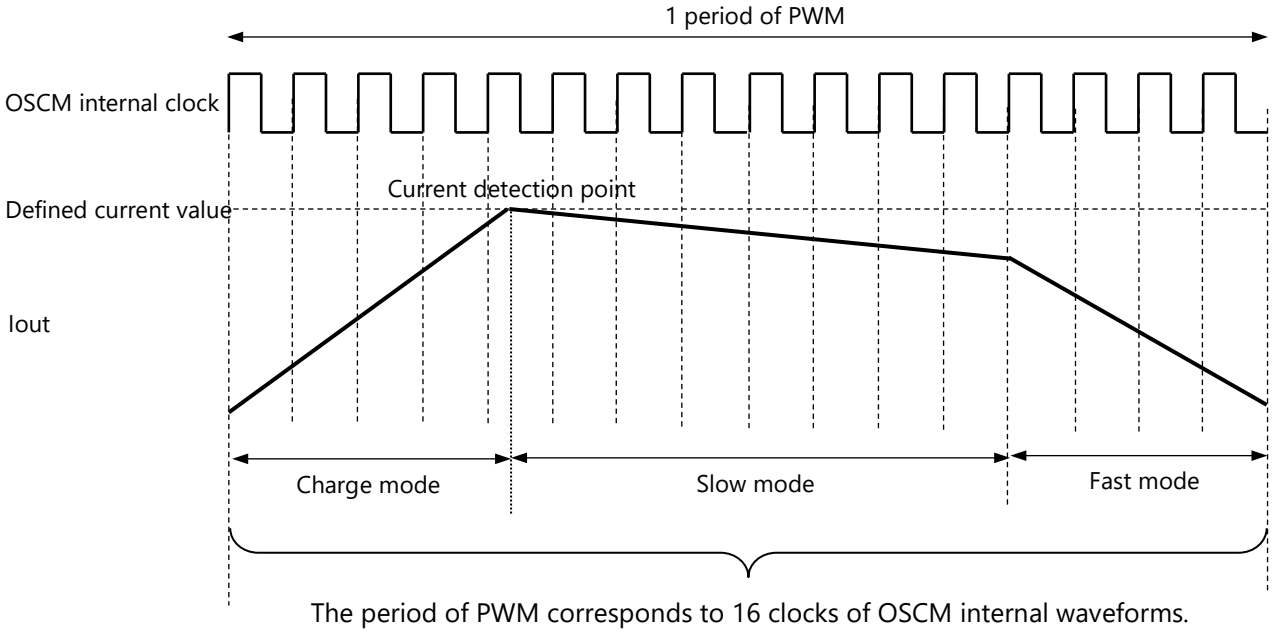
（CW/CCW=L）

∗ The waveform can be output from MO pin when pulled up.

Timing charts may be simplified for explanatory purposes.

7.14 Constant current PWM control

Mixed decay mode and operation of zero point detection



The period of PWM corresponds to 16 clocks of OSCM internal waveforms.

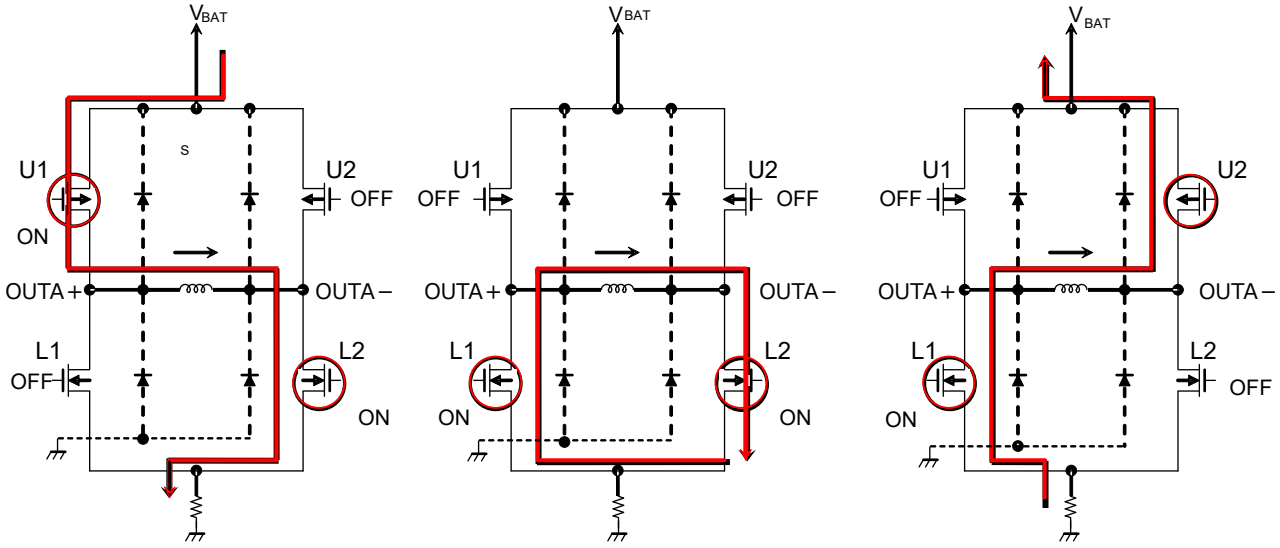
- Charge mode: A charge mode starts as synchronized with an OSCM internal clock.
- Slow mode : A slow mode starts at the point where output current Iout reaches a defined current value
- Fast mode : A period of a fast mode is between the 13th and 16th clock from the beginning of a charge mode, which is 25% of 1 period of PWM

Note: If output current Iout reaches the zero point (0A) during 1 period of PWM, which corresponds to 16 clocks of OSCM internal clocks, outputs become high-impedance.

Timing charts may be simplified for explanatory purposes.

Output stage transistor operation mode (Mixed decay mode)

(Ach is taken as an example. Bch is the same as Ach.)



∗ Shoot-through preventive time is set inside the IC to prevent shoot-through current at the timing of a change of modes.

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Function of transistor operation at output stage

〈 When current path through a coil in a charge mode is from U1 to L2 〉

Mode	U1	U2	L1	L2
Charge	ON	OFF	OFF	ON
Slow decay	OFF	OFF	ON	ON
Fast decay	OFF	ON	ON	OFF

〈 When current path through a coil in a charge mode is from U2 to L1 〉

Mode	U1	U2	L1	L2
Charge	OFF	ON	ON	OFF
Slow decay	OFF	OFF	ON	ON
Fast decay	ON	OFF	OFF	ON

Current value setting

Current value at 100% to control constant currnet is determined by both an external resistor RRS to detect motor current and reference voltage Vref input from external power supply voltage.
RRSs are resistors between RSA pin and GND, and between RSB pin and GND, which should be the same value.
In addition, the external input reference voltage Vref is attenuated inside the IC and its attenuation ratio Vref(gain) is 1/10 (typ.).

$$Iout(Max) = Vref(gain) \times \frac{Vref(V)}{RRS(\Omega)}$$

e.g. When RRS=0.4Ω, Vref=2.0V input and TORQUE=100%, a defined current value at 100% is shown below:

$$Iout(Max) = 1/10 \times 2.0\ (V) / 0.4\ (\Omega)$$
$$= 0.5\ (A)$$

TORQUE pin

A weak excitation mode can be set by using TORQUE0 and TORQUE1 pin. Both TORQUE0 and TORQUE1 pin should always be set at L, unless a weak excitation mode is used.

TORQUE0	TORQUE1	Function
L	L	Defined current value × 100%
H	L	Defined current value × 70%
L	H	Defined current value × 50%
H	H	Defined current value × 30%

7.15 Load open detection

This IC incorporates a load open detection function at output pins (OUTA +, OUTA-, OUTB +, and OUTB-). If a load connected to output pins becomes disconnected, a load open at the output pin is detected.

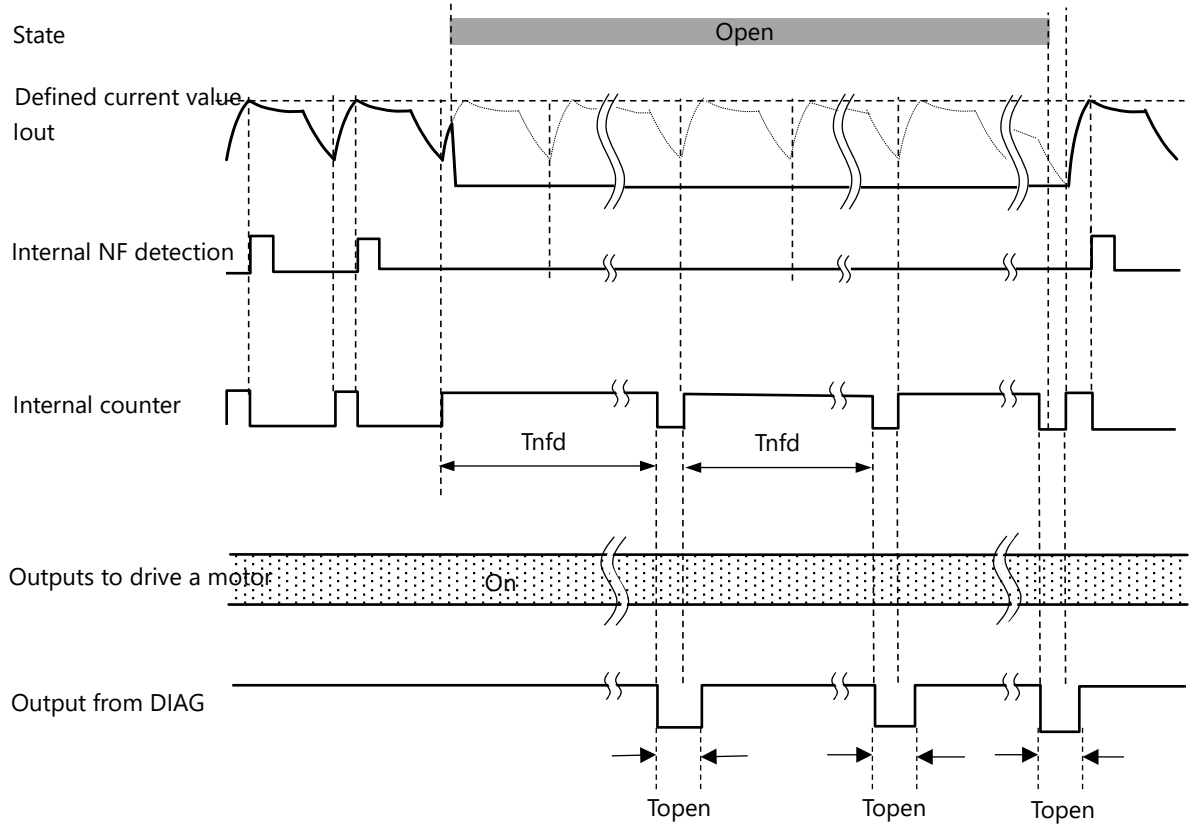
Description of operation

An internal counter starts to count at the starting point of a charge mode while constant current is operating. Moreover, when output current Iout reaches a defined value within Tnfd (50ms(typ.)), an internal NF detection signal is output and the counter is reset.

On the other hand, unless output current Iout reaches a defined value due to a load open, both an internal NF detection signal isn't output and an internal counter gets over Tnfd, and then L pulse Topen, whose width is 100μs(typ.), is output from DIAG pin. An OSCM internal clock for a constant current PWM control keeps operating and an internal counter starts to count at every starting point of a charge mode, in other words at intervals of 16 periods of OSCM internal clocks, refer to 7.14, except during Tnfd. Therefore, if a load open, where no output current passes, is still going on after a period of Tnfd, an internal counter starts to count again, and then L pulse is output from DIAG pin after Tnfd in the same way.

When a state changes from a load open to normal connection, output current Iout begins to pass at the first charge mode after the last period of Tnfd, and the original sequence is recovered.

〈 Timing chart for one phase when a load open detected 〉



Timing charts may be simplified for explanatory purposes.

Note) It takes more than 50ms(typ.) to detect a load open because periods of PWM need to be counted again from an initial state, for example, if a load open occurs under the condition that output current Iout is 0A.

7.16 Overcurrent Detection (ISD)

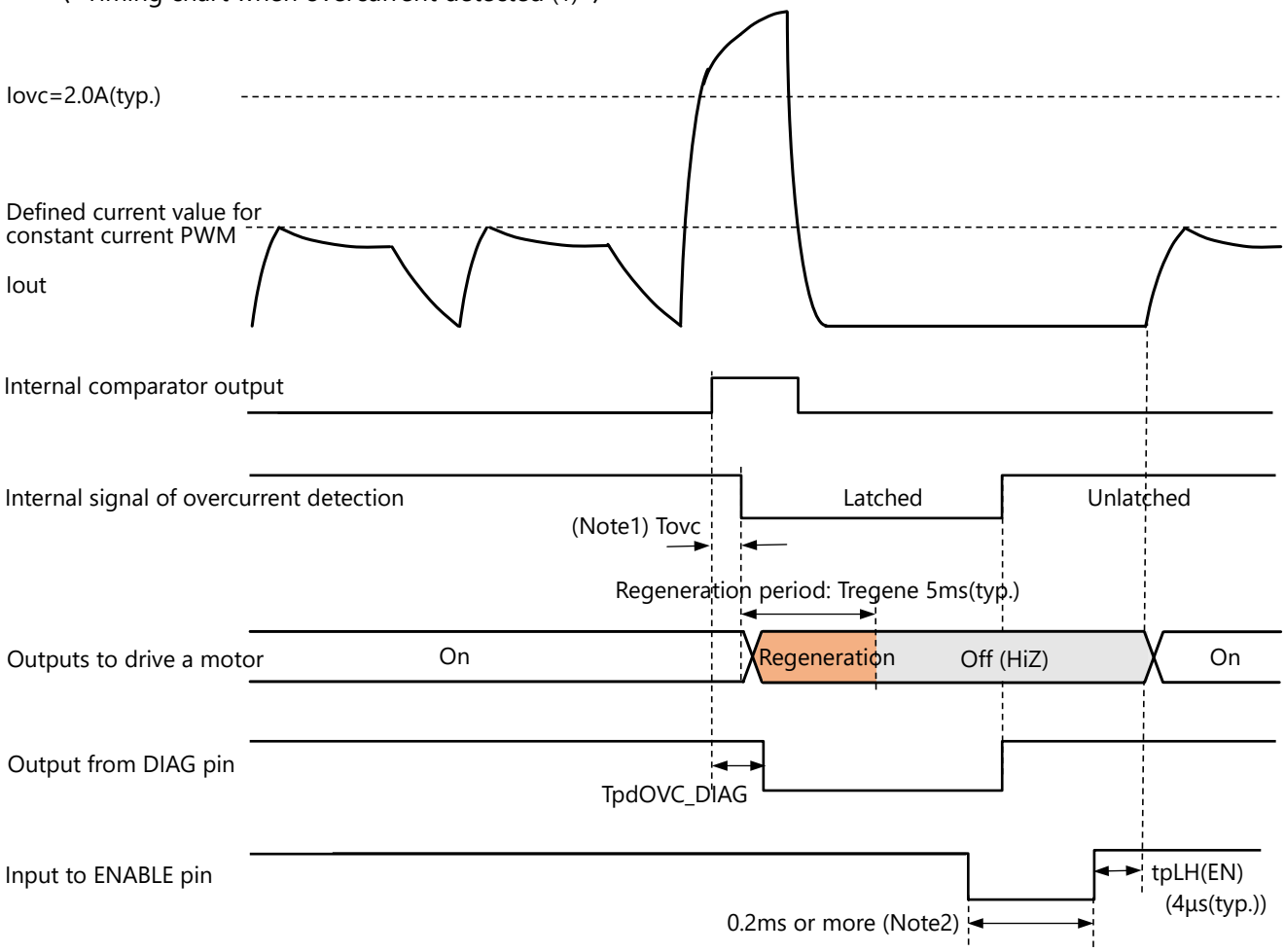
If either a power fault or a ground fault occurs at output pins to a motor, an overcurrent is detected at that time and L is output from DIAG pin. This IC incorporates overcurrent detection circuits as shown below:

(1) Dain current detection circuits on upper Pch MOSFETs

If dain current which passes through upper Pch MOSFETs in either phase A or B exceeds the threshold Iovc=2A(typ.), outputs to drive a motor turn off.

- If current which exceeds the threshold passes through upper Pch MOSFETs, outputs to drive a motor turn off and L is output from DIAG pin.
- If overcurrent is detected, outputs to drive a motor turn off and are latched. During a transitional period from on to off state a period of the current regeneration mode Tregene 5ms(typ.) is provide.
- An output from DIAG pin is turned from H to L after TpdOVC_DIAG (3.5μs(typ.)) from a rising edge of an internal comparator output.
- The latch can be released by either rebooting VBAT or setting ENABLE pin to L level whose duration should be 0.2ms or more(Note). In the case where L is input to ENABLE pin to release a latch, the release is done during L period on ENABLE and an output signal from DIAG changes from L to H at the same time.
- Outputs to drive a motor change from off to on after tpLH(EN) (4μs(typ.)) from a rising edge from L input to ENABLE.
- A power fault and a ground fault have different regeneration modes. In the case of a power fault, a slow decay mode consists of an on state of upper Pch MOSFETs and an off state of lower Nch MOSFETs. On the other hand, in the case of a ground fault, a slow decay mode consists of an off state of upper Pch MOSFETs and on state of lower Nch MOSFETs.

〈 Timing chart when overcurrent detected (1) 〉



Note1) A masking period Tovc (1.2μs(typ.)) is provided so that circuits doesn't work due to noise
Note2) Inspection for it is not conducted at the time of shipment.

Timing charts may be simplified for explanatory purposes.

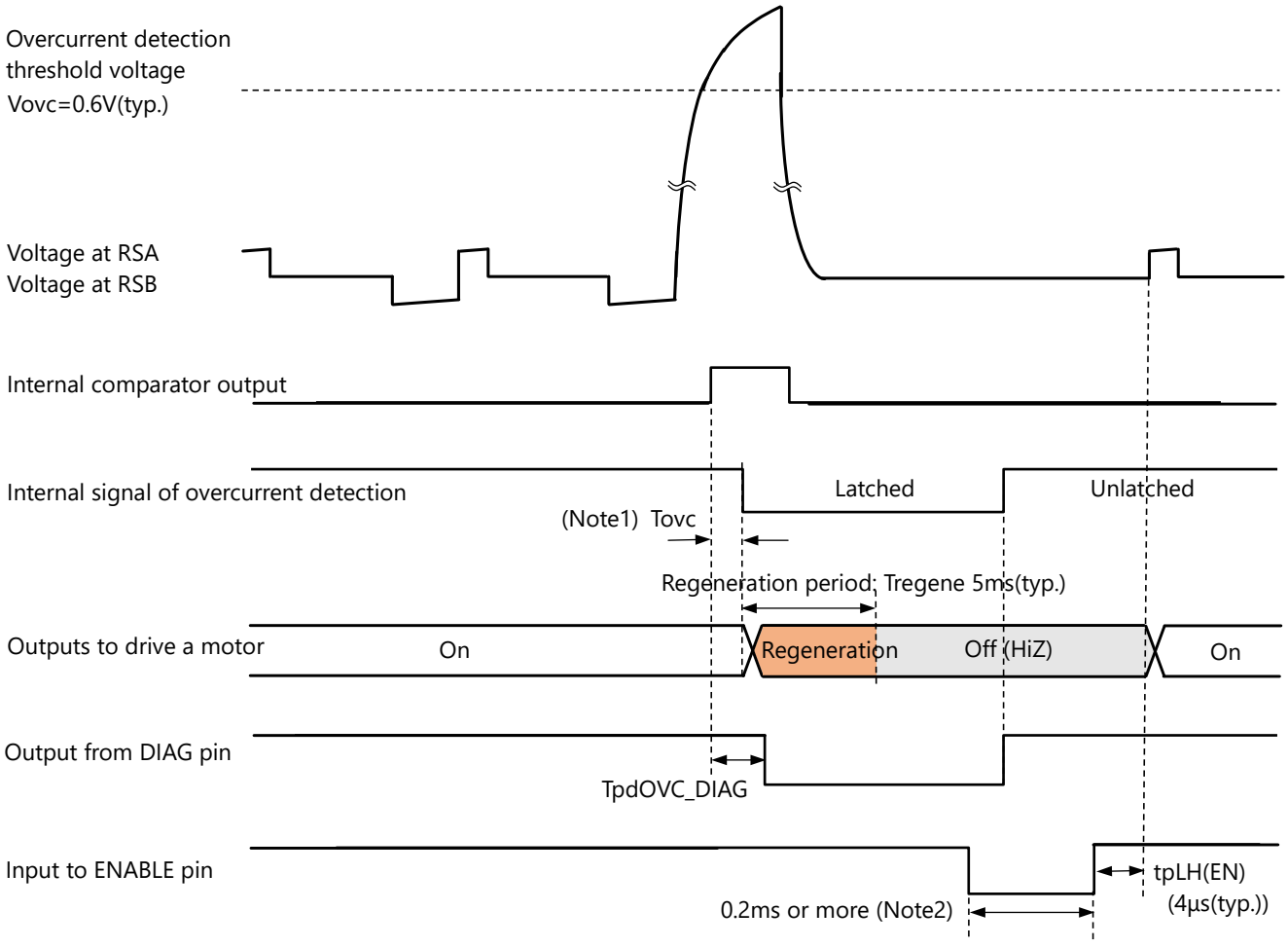
(2) Current detection circuit with external resistor RRS

If voltage which is generated by current passing through each external resistor RRS connected to RSA and RSB exceeds the threshold 600mV(typ.), outputs to drive a motor turn off.

$$Vovc \leqq Iout \times RRS$$

- If voltage between terminals of an external resistor RRS, through which current passes, exceeds the threshold 600mV(typ.), outputs to drive a motor turn off and L is output from DIAG pin.
- If overcurrent is detected, outputs to drive a motor turn off and are latched. During a transitional period from on to off state a period of the current regeneration mode Tregene 5ms(typ.) is provide.
- An output from DIAG pin is turned from H to L after TpdOVC_DIAG (3.5μs(typ.)) from a rising edge of an internal comparator output.
- The latch can be released by either rebooting VBAT or setting ENABLE pin to L level whose duration should be 0.2ms or more(Note). In the case where L is input to ENABLE pin to release a latch, the release is done during L period on ENABLE and an output signal from DIAG changes from L to H at the same time.
- Outputs to drive a motor change from off to on after tpLH(EN) (4μs(typ.)) from a rising edge from L input to ENABLE.
- A power fault and a ground fault have different regeneration modes. In the case of a power fault, a slow decay mode consists of an on state of upper Pch MOSFETs and an off state of lower Nch MOSFETs. On the other hand, in the case of a ground fault, a slow decay mode consists of an off state of upper Pch MOSFETs and on state of lower Nch MOSFETs.

〈 Timing chart when overcurrent detected (2) 〉



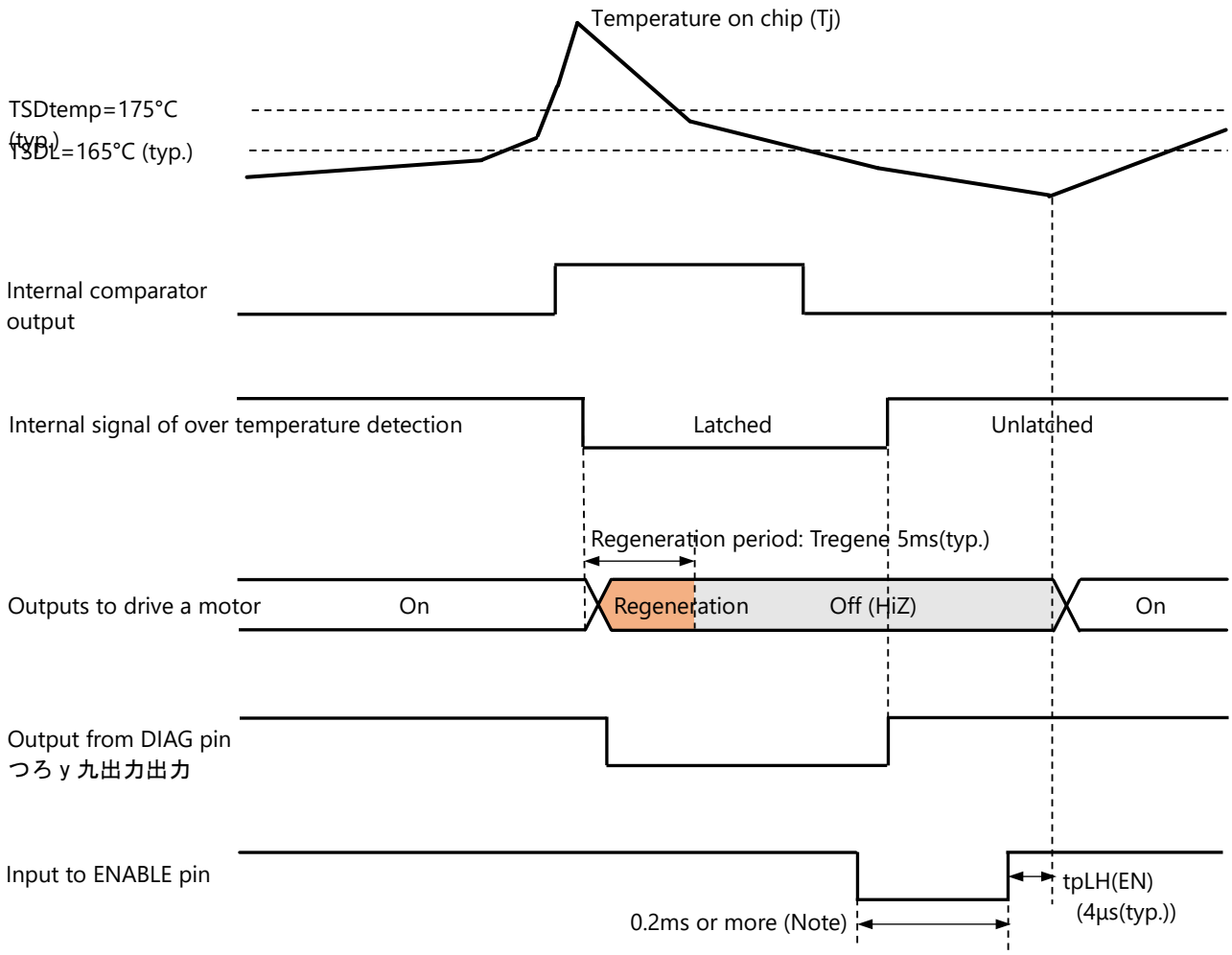
Note1) A masking period Tovc (1.2μs(typ.)) is provided so that circuits doesn't work due to noise
Note2) Inspection for it is not conducted at the time of shipment.

Timing charts may be simplified for explanatory purposes.

7.17 Over temperature detection (TSD)

If temperature on the chip reaches defined temperature TSDtemp, outputs to drive a motor turn off, moreover, the IC are latched, and then L is output from DIAG pin. If over temperature is detected, the outputs turn off after the regeneration period Tregene 5ms(typ.)
Over temperature detection shutdown temperature TSDtemp is set at 175°C (typ.) and it exhibits 10°C (typ.) of hysteresis.
It recovers right after either rebooting VBAT or setting ENABLE pin to L level whose duration should be 0.2ms or more (Note) after the temperature on the chip is less than the recovery temperature TSDL 165°C (typ.). In the case where L is input to ENABLE pin to release a latch, the release is done during L period on ENABLE and an output signal from DIAG changes from L to H at the same time.

〈 Timing chart when over temperature detected 〉



Note) Inspection for it is not conducted at the time of shipment.

Timing charts may be simplified for explanatory purposes.

Notes:

The absolute maximum rating of the guaranteed storage temperature range of this product is 150°C (max.). Storage and use beyond this temperature cannot guarantee the normal operation of the IC afterwards, and it may also cause smoking and ignition. Please do not store or use it beyond this temperature in any case.
Although this IC incorporates the following over temperature detection function, this function does not suppress the temperature of this IC below the over temperature detection shutdown temperature TSDtemp, and it is a function outside the guaranteed operation range. Please regard it as an auxiliary function.
Regarding this function, although an actual temperature inspection is not conducted for each product at the time of shipment, circuit operation is checked as a substitute inspection.

7.18 Operation outside the scope of the operation voltage range

In the case of operation voltage range 7 V to 18 V, electrical characteristics values described in this document are guaranteed.
Operation at 4.5 V to 7 V, which isn't the above operation voltage range is described as follows.
Only function operation is guaranteed, on the other hand, electrical characteristics values are not guaranteed.
The function operation mentioned here is that outputs operates corresponding to the truth tables with signals to input pins.

Functions and circuits which work at 4.5 V to 7.0 V	Operation
・ VccOUT circuit ・ OSC circuit ・ Each control logic circuit ・ MO circuit ・ DIAG circuit ・ SD circuit ・ Motor function (CW/CCW rotation, each step resolution mode) ・ Each detection circuit (overcurrent, over temperature, load open, stall) ・ Constant current chopping control	Function operation works. Electrical characteristics values are not guaranteed.

7.19 Regeneration Operation

In the following cases, outputs to drive a motor is switch into a high-impedance state after regeneration operation is done during a transitional period or a regeneration period Tregene.

1. When either TSD or ISD operates.
2. When either TSD or ISD operates after a load open occurs.
3. When an abnormity of OSC pin is detected (OSC pin is not connected (open state), short to power or short to GND).
4. When ENABLE = H, moreover, BSTBY pin changes from H level to L level.
5. When ENABLE pin changes from H level to L level.

8. Absolute maximum rating (Ta = 25°C)

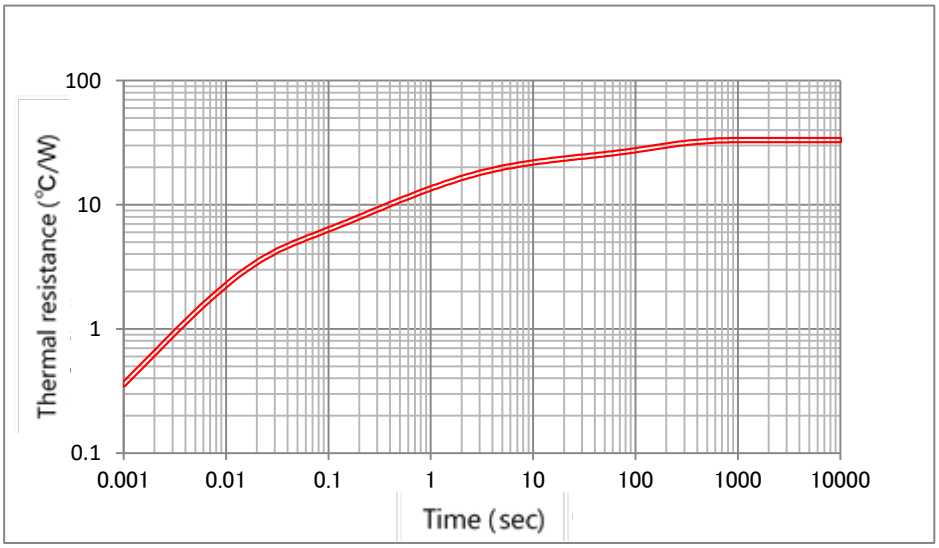
Characteristics		Symbol	Applicable pins	Conditions	Rating	Unit
Power supply voltage		VBAT	VBAT	DC	-0.3 to 18	V
				1min (Note1)	30	V
				Transient 0.5s (Note2)	40	V
Input voltage		VIN1	CLK, TORQUE0, TORQUE1, DMODE0, DMODE1, DMODE2, START, ENABLE, CW/CCW and BSTBY	DC	-0.3 to 6.0	V
			VREF	DC (Note3)	-0.3 to 6.0	
			VDD	DC	-0.3 to 6.0	V
		VIN2	RSA and RSB	—	-0.3 to 1.0	V
Output voltage 1		VOUT	VccOUT	DC	-0.3 to 6.0	V
Output voltage 2			DIAG, SD and SDT	DC	-0.3 to 6.0	V
Output voltage 3			SDT	DC	-0.3 to 6.0	V
Output voltage 4			OUTA+, OUTA-, OUTB+ and OUTB-	DC (Note4, 5 and 6)	-VF to VBAT+VF and VBAT+VF≦ 40V	V
Output current 1		Iout	OUTA+, OUTA-, OUTB+ and OUTB-	(Note7)	Overcurrent detection value	A
Output current 2			DIAG, SD and MO	DC	2.5	mA
Allowable power dissipation	QFN28	PD	—	(Note8)	3.9	W
Operation temperature		Topr	—	—	-40 to 125	°C
Storage temperature		Tstr	—	—	-55 to 150	°C
Junction temperature		Tj(max)	—	—	150	°C

* The inflow current to this IC is indicated by "+", and the outflow current from this IC is indicated by "-".
* Inspections for some characteristics in the absolute maximum rating are not conducted at the time of shipment.

Note1) The voltage over the upper limit of the operation voltage range; 18 V can be applied only for a jump start. In the case of a use at 18 V or more, thermal performance should be carefully designed.
Note2) Voltage gap between VBAT and GND should be less than the maximal voltage 40V.
Note3) Voltage gap between VREF and GND should be less than the maximal voltage 6V.
Note4) The maximum rating including back-EMF voltage should not exceed.
Note5) Voltage value which is generated by current flowing through a body diode in output MOSFET in a regeneration mode after outputs are turned off due to a load short circuit is taken into account as a VF value.
Note6) The difference between GND, and each output pin OUTA+, OUTA - , OUTB+ and OUTB - in voltage should not exceed 40 V.
Note7) Thermal performance should be carefully designed, moreover, evaluations should be thoroughly undergone so that the junction temperature can be less than 150°C,
Note8) Under measurement conditions; Ta = 25°C, no wind and JEDEC 4-layer printed circuit board with 9 via holes right underneath the IC

The maximum rating is the rating that should never be exceeded, even for a shortest of moments. If the maximum rating is exceeded, it could result in damage and/or deterioration of the IC as well as other devices beside the IC. Regardless of the operating conditions, please design so that the maximum rating is never exceeded. Please use within the specified operating range.

Thermal resistance data on P-VQFN28-0606-0.65, for reference



＜Measurement conditions＞

- Ambient temretature Ta = 25 °C
- 1W dissipated
- With no wind
- JEDEC 4-layer board with 9 via holes

＜Saturation thermal resistance, for reference＞

- Rthj-a = 31.3 °C/W

9. Operation Range (Ta = -40 to 125°C)

Characteristics		Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply voltage 1		VBAT	4.5	—	7	V	Function operation only, Note
Motor power supply voltage 2		VBAT	7	13	18	V	—
Clock frequency input range		fCLK	—	—	100	kHz	—
Chopping frequency setting range		fPWM(range)	50	—	80	kHz	—
Vref voltage input range		Vref	0.3	1.5	3.0	V	—
Power supply slew	rising	VBSLEW	—	—	2	V/μs	—
	falling	VBSLEW	-2	—	—	V/μs	

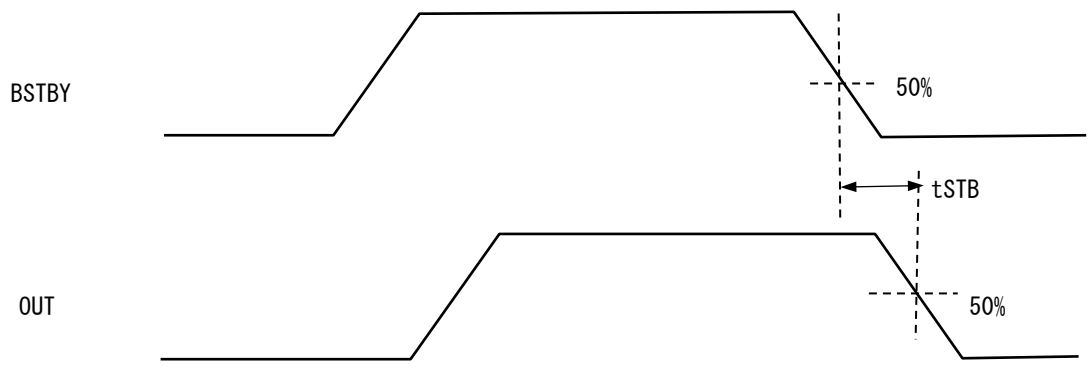
Note) Refer to 7.18 Operation outside the scope of the operation voltage range

10 Electrical characteristics

10.1 Electrical characteristics 1 (Unless otherwise specified, Ta = -40 to 125°C, VBAT = 7 to 18 V)

Characteristics		Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
Logic input pin input voltage 1	HIGH	VIN1(H)	CLK, TORQUE0, TORQUE1, CW/CCW, DMODE0, DMODE1, DMODE2, START and ENABLE	—	2.0	—	5.5	V
	LOW	VIN1(L)		—	0	—	0.8	V
Input hysteresis 1		VIN1(HYS)		—	0.1	—	1.0	V
Logic input pin input current 1	HIGH	IIN1(H)		Measurement LOGIC input pin=5V	30	50	100	μA
	LOW	IIN1(L)		Measurement LOGIC input pin=0V	-5	—	5	μA
Logic input pin input voltage 2	HIGH	VIN2(H)	BSTBY	—	2.2	—	5.5	V
	LOW	VIN2(L)		—	0	—	0.5	V
Input hysteresis 2		VIN2(HYS)		—	0.1	—	1.2	V
Logic input pin input current 2	HIGH	IIN2(H)		BSTBY=5V	36	60	120	μA
	LOW	IIN2(L)		BSTBY=0V	-5	—	5	μA
Standby settled period		tSTB	BSTBY	BSTBY from H to L and fixed	—	5	—	ms
Regeneration period		Tregene	—	After ISD, TSD and OSCM pin anomaly	—	5	—	ms
MO pin output voltage		VOL(MO)	MO	BSTBY=H, MO=L, RL=5.1kΩ and Pull-up to 5V	—	0.2	0.5	V
DIAG pin output voltage		VOL(DIAG)	DIAG	BSTBY=H, DIAG =L, RL=5.1kΩ and Pull-up to 5V	—	0.2	0.5	V
MD pin output voltage		VOL(SD)	SD	BSTBY=H, SD=L, RL=5.1kΩ and Pull-up to 5V	—	0.2	0.5	V
Current consumption		IBAT1	VBAT	Output: open and standby mode	—	1	10	μA
		IBAT2		Output: open, standby released and ENABLE=L	—	3	9	mA
		IBAT3		Output: open, standby released and ENABLE=H	—	3	9	mA

∗ BSTBY signal input to the BSTBY pin and output pin OUTA+, OUTA-, OUTB+ and OUTB-



Timing charts may be simplified for explanatory purposes.

10.2 Electrical characteristics 2 (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V)

Characteristics		Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
MO pin output leakage current		IMO	MO	VOL(MO)=5V and Off	—	1	3	μA
DIAG pin output leakage current		IDIAG	DIAG	VOL(DIAG)=5V and Off	—	1	3	μA
SD pin output leakage current		I_SD	SD	VOL(SD)=5V and Off	—	1	3	μA
Motor pin output leakage current	Upper	IOHout	OUTA+, OUTA-, OUTB+ and OUTB-	VBAT=18V and OUT A/B±=0V	—	1	10	μA
	Lower	IOLout		VBAT= OUT A/B± =18V	—	1	10	μA
Error of motor output current between channels		ΔIout1		Error of output current between channels	-10	0	10	%
Error of set current value for motor output		ΔIout2		Iout=0.5A or more (TORQUE：100%)	-10	0	10	%
Dead time of motor output		TDEAD		—	100	400	700	ns
Motor output on-resistance (Sum of upper and lower)		Ron(H+L)		Ta=25°C, VBAT=13.0V and Iout=0.5A	—	0.8	1.8	Ω
				Ta=125°C, VBAT=13.0V and Iout=0.5A	—	1.1	2.2	Ω
				Ta=25°C, VBAT=7.0V and Iout=0.5A	—	0.8	1.8	Ω

10.3 Electrical characteristics 3 (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
Vref input current	Iref	Vref	Vref=2.0V	—	0	1	μA
VccOUT pin voltage	VccOUT	VccOUT	IccOUT=1mA	4.75	5.0	5.25	V
Vref attenuation ratio	Vref(gain)	Vref	Vref=2.0V	1/11	1/10	1/9	—

10.4 AC electrical characteristics

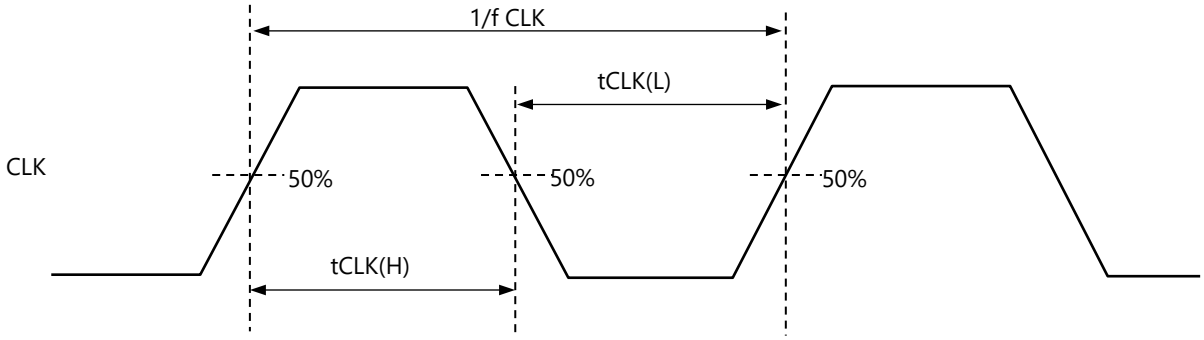
Characteristics related to CLK (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V／ROSCM=100kΩ)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
CLK input pulse width (high)	tCLK(H)	CLK	CLK(H) pulse width	2.5	—	—	μs
CLK input pulse width (low)	tCLK(L)		CLK(L) pulse width	2.5	—	—	μs
DMODE set-up time	tDMODE(set)	CLK and DMODE	—	2	—	—	μs
START set-up time	tSTART(set)	CLK and START	—	1	—	—	μs
START hold time	tSTART(hold)	CLK and START	—	1	—	—	μs
Output transistor switching characteristics	tr	OUTA+, OUTA-, OUTB+ and OUTB-	27 Ω between output pins, and 10%-90%	80	300	600	ns
	tf		27 Ω between output pins, and 10%-90%	80	300	600	ns
	tpLH(CLK)		Between CLK and output voltage	0.5	3	6	μs
	tpHL(CLK)		Between CLK and output voltage	0.5	3	6	μs
	tpHL(EN)		Between ENABLE and output voltage	1	4	7	μs
	tpLH(EN)		Between ENABLE and output voltage	1	4	7	μs
Dead band time for noise removal	tBLK	RSGND	VBAT=12V and Iout=0.5A	0.5	3	5	μs

AC characteristics timing chart

- **CLK signal input to the CLK pin**

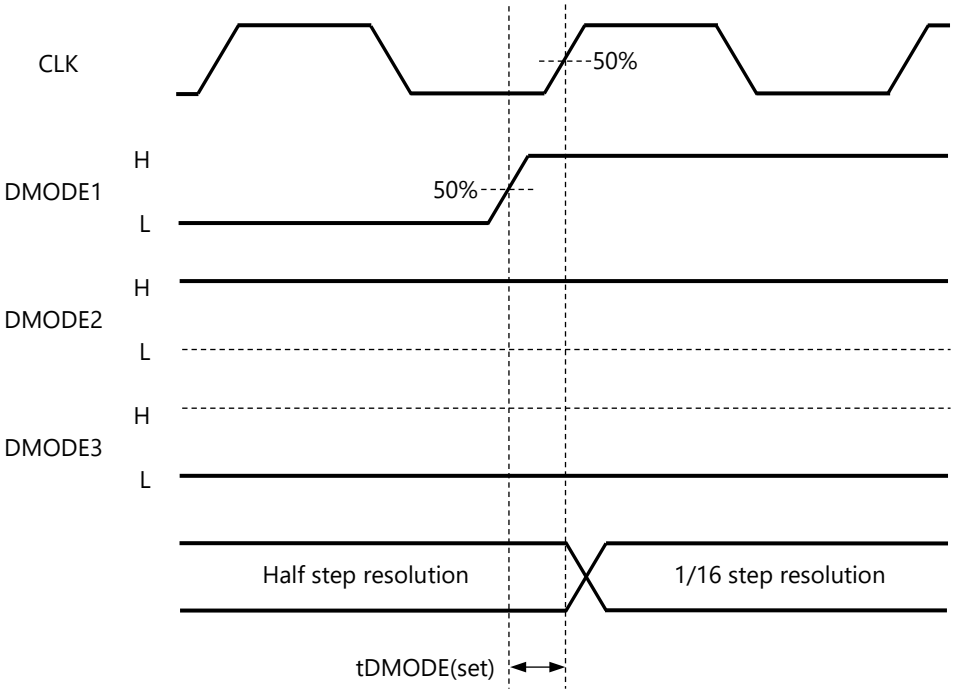
CLK input pulse width (H) tCLK(H)
CLK input pulse width (L) tCLK(L)



- **CLK signal input to the CLK pin and signals input to the DMODE0, DMODE1 and DMODE2 pins**

Set-up time tDMODE(set)

e.g. When changing from half step resolution to 1/16 step resolution

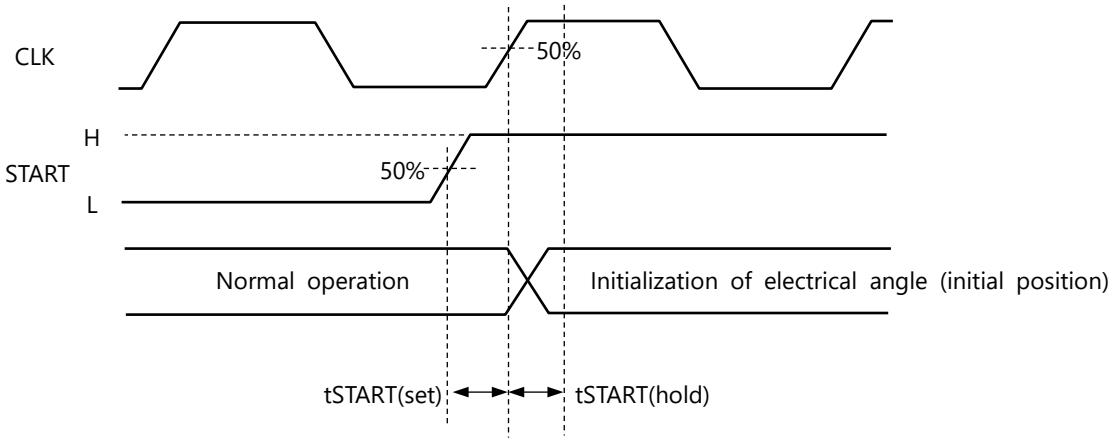


Timing charts may be simplified for explanatory purposes.

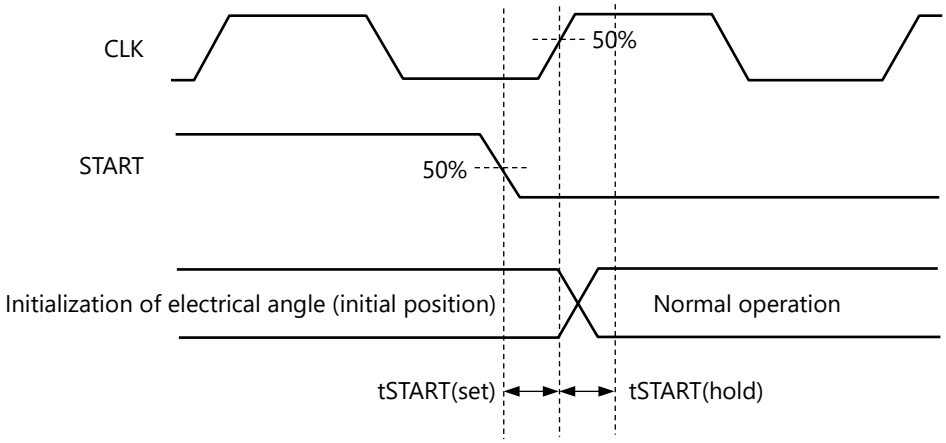
- **CLK signal input to the CLK pin and signals input to the START pin**

Set-up time tSTART(set)
Hold-up time tSTART(hold)

(a) When START is changed from L to H



(b) When START is changed from H to L

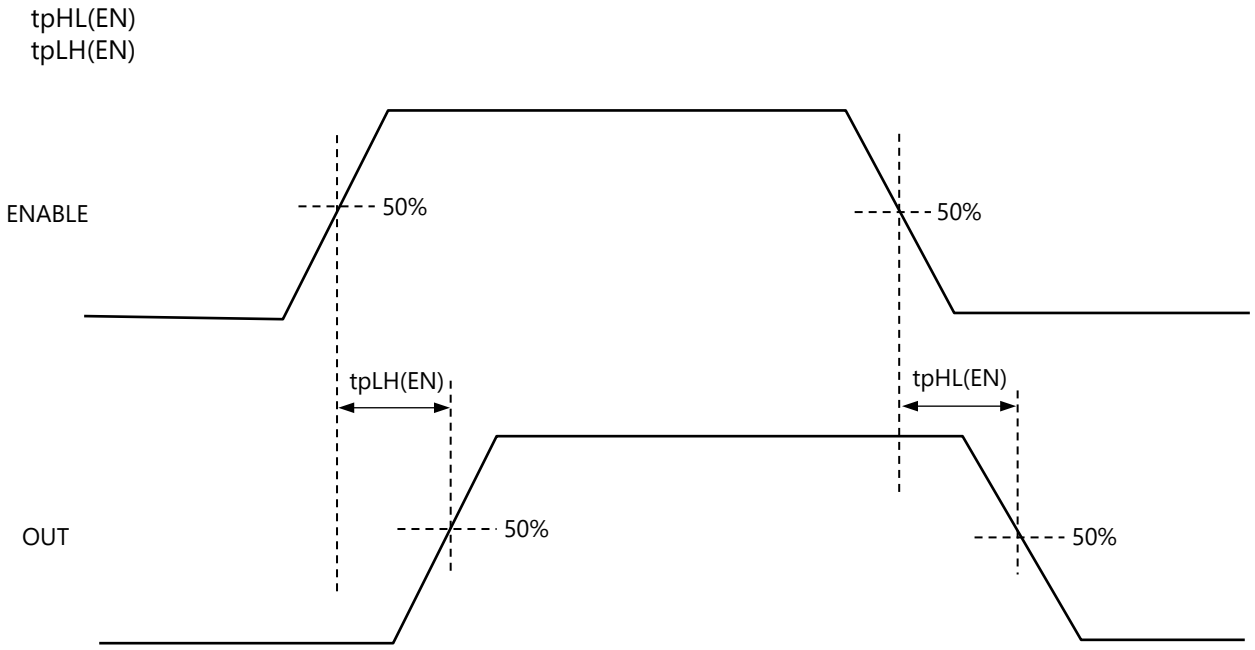


Timing charts may be simplified for explanatory purposes.

- **tr, tf of the output pins, OUTA+,OUTA-,OUTB+ and OUTB-**

Timing charts may be simplified for explanatory purposes.

- **ENABLE signal input to the ENABLE pin, output pin OUTA+, OUTA-, OUTB+ and OUTB-**



Timing charts may be simplified for explanatory purposes.

OSCM (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
OOSC oscillation frequency accuracy	⊿fOSCM	OSCM	BSTBY=H and ROSCM=100kΩ	-25	—	25	%
OSCM oscillation frequency	fOSCM			1200	1600	2000	kHz

fPWM (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
Chopping setting frequency	fPWM	OSCM	BSTBY=H, ROSCM=100kΩ and Output active (Iout=0.5A)	—	50	—	kHz

10.5 Characteristics related to the safety function and electrical characteristics

Power supply monitoring (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V／ROSCM=100kΩ)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
VBAT low-voltage detection voltage	VBATRSTL	VBAT	—	3.95	4.20	4.49	V
VBAT low-voltage cancellation voltage	VBATRSTH	VBAT	—	4.45	4.70	5.10	V
VBAT low-voltage detection hysteresis width	VBATRSTHY	VBAT	—	0.1	0.5	1.0	V
VccOUT low-voltage POR detection voltage	VccOUTRHL	VccOUT	—	3.55	3.80	3.95	V
VccOUT low-voltage POR cancellation voltage	VccOUTRHH	VccOUT	—	3.75	4.00	4.15	V
VccOUT low-voltage POR detection hysteresis width	VccOUTRHLHYS	VccOUT	—	0.1	0.2	0.3	V

Stall detection (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V／ROSCM=100kΩ)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
SDT pin external resistance	RSDT	SDT	—	0	—	230	kΩ
SDT pin threshold setting voltage	VSDT	SDT	—	—	0.5	3.0	V
SDT pin current	ISDT	SDT	VSDT=0V and 3V	7	10	13	μA
Error of difference between stall detection induced voltage	ΔVinduced	—	VSDT=3V	-0.4	—	0.4	V
Stall detection delay	Tstld_d	—	—	10	20	40	μs
Stall alert period	Tstld	SD	—	67	100	200	μs
Stall alert response delay	Tstld_SD	—	—	0.5	3.5	6.5	μs

＊ The product of an SDT pin external resistance RSDT multiplied by an SDT pin current ISDT is an SDT pin threshold setting voltage VSDT, or

VSDT(V) = RSDT(Ω) × ISDT(A)

Load open detection (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V／ROSCM=100kΩ)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
Current detection period threshold	Tnfd	—	—	30	50	100	ms
Load open DIAG period	Topen	DIAG	—	67	100	200	μs

Overcurrent detection (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V／ROSCM=100kΩ)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
Upper side overcurrent circuit threshold	Iovc	OUTA+, OUTA-, OUTB+ and OUTB-	—	1.5	2.0	2.5	A
Lower side overcurrent detection voltage	Vovc		—	450	600	750	mV
Detection filter time	Tovc		—	0.8	1.2	2.4	μs
Overcurrent detection DIAG output response delay	TpdOVC_DIAG	DIAG	—	1	3.5	6.5	μs

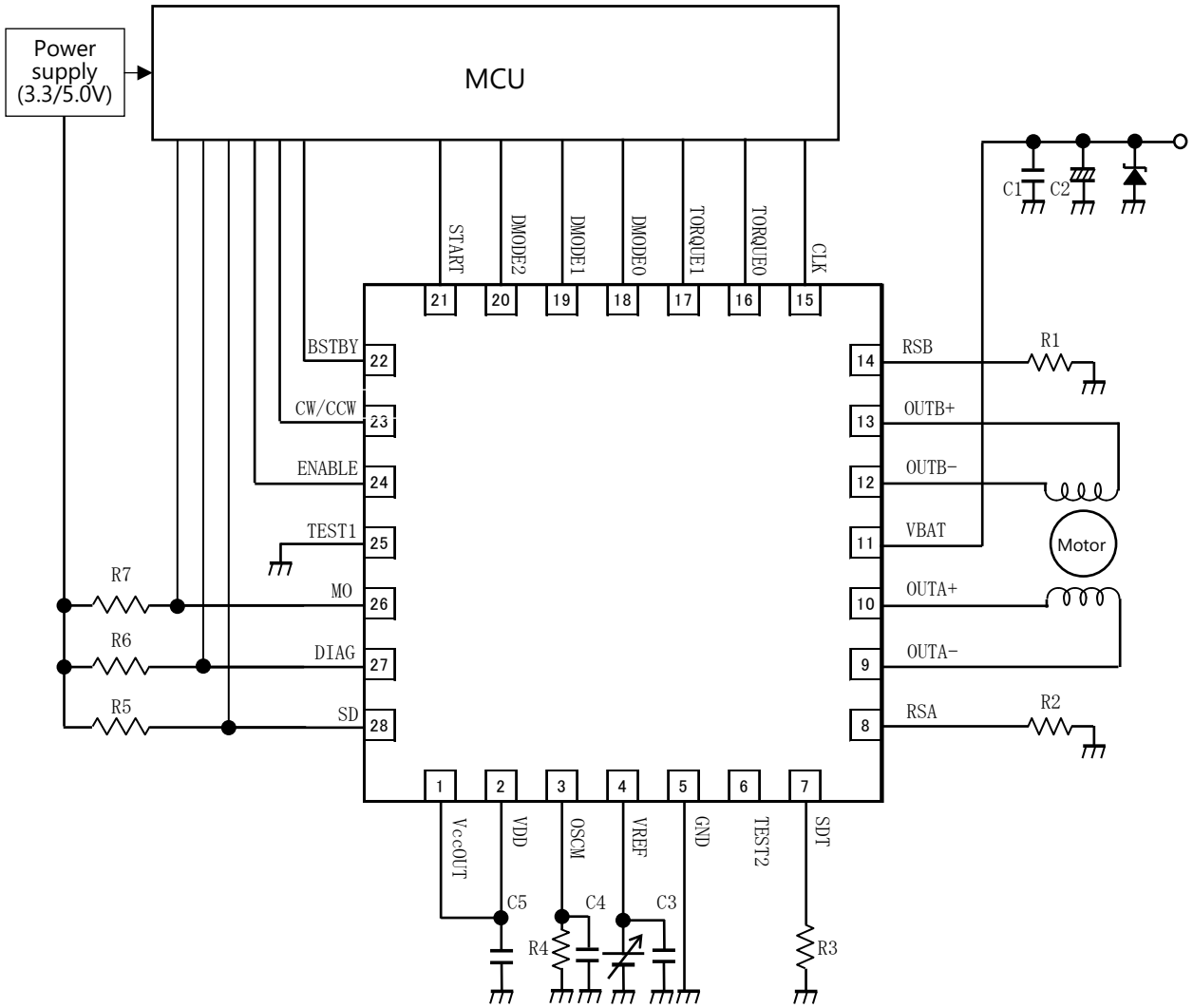
Over temperature detection (Unless otherwise specified, Ta=-40 to 125°C／VBAT=7 to 18V／ROSCM=100kΩ)

Characteristics	Symbol	Applicable pin	Measurement conditions	Min	Typ.	Max	Unit
Over temperature detection shutdown temperature	TSDtemp	—	—	155	175	195	°C
Over temperature detection hysteresis temperature	TSDhys	—	—	—	10	—	°C
Recovery temperature	TSDL	—	—	150	165	185	°C

Notes:

The absolute maximum rating of the guaranteed storage temperature range of this product is 150°C (max.). Storage and use beyond this temperature cannot guarantee the normal operation of the IC afterwards, and it may also cause smoking and ignition. Please do not store or use it beyond this temperature in any case. Although this IC incorporates the following over temperature detection function, this function does not suppress the temperature of this IC below the over temperature detection shutdown temperature TSDtemp, and it is a function outside the guaranteed operation range. Please regard it as an auxiliary function. Regarding this function, although an actual temperature inspection is not conducted for each product at the time of shipment, circuit operation is checked as a substitute inspection.

11 Example of Application Circuit



- The above is just one example of an application circuit, therefore, it can't be guaranteed as a design for a mass-produced product.
- GND wiring should be a GND plane and a point on the GND plane to connect to other areas outside the PCB should be a single point ground. Moreover, thermal performance should be paid attention to when a layout of circuit patterns is designed.
- VBAT lines, GND lines, and output lines should be designed with the utmost care because the IC may be destroyed if either the GND lines and outputs short-circuit, the power lines and outputs short-circuit or two of outputs short-circuit. If there is any wrong wiring, especially at pins for large currents such as VBAT, OUTA+/-, OUTB+/-, RSA, RSB and GND, the IC may malfunction and/or be destroyed.
- If there is any wrong wiring at input pins for logic signals, the IC may malfunction. Moreover, the malfunction may make over current pass over the specifications and finally the IC may be destroyed. With the utmost care, not only should circuit patterns around the IC on the PCB be designed, the IC should also be soldered.
- Please do not use VccOUT pin as pull-up power supply for input signal pins such as CLK, TORQUE0, TORQUE1, CW/CCW, DMODE0, DMODE1, DMODE2, START, ENABLE and BSTBY, as power supply for VREF, and as pull-up power supply for detection flag output signal pins such as MO, DIAG and SD although VccOUT pin outputs 5 voltage.
- Regarding OSCM pin, an external resistor ROSCM should be placed between OSCM pin and GND to set PWM chopping frequency fPWM. Moreover, an external capacitor COSCM should also be placed between them to stabilize the pin.

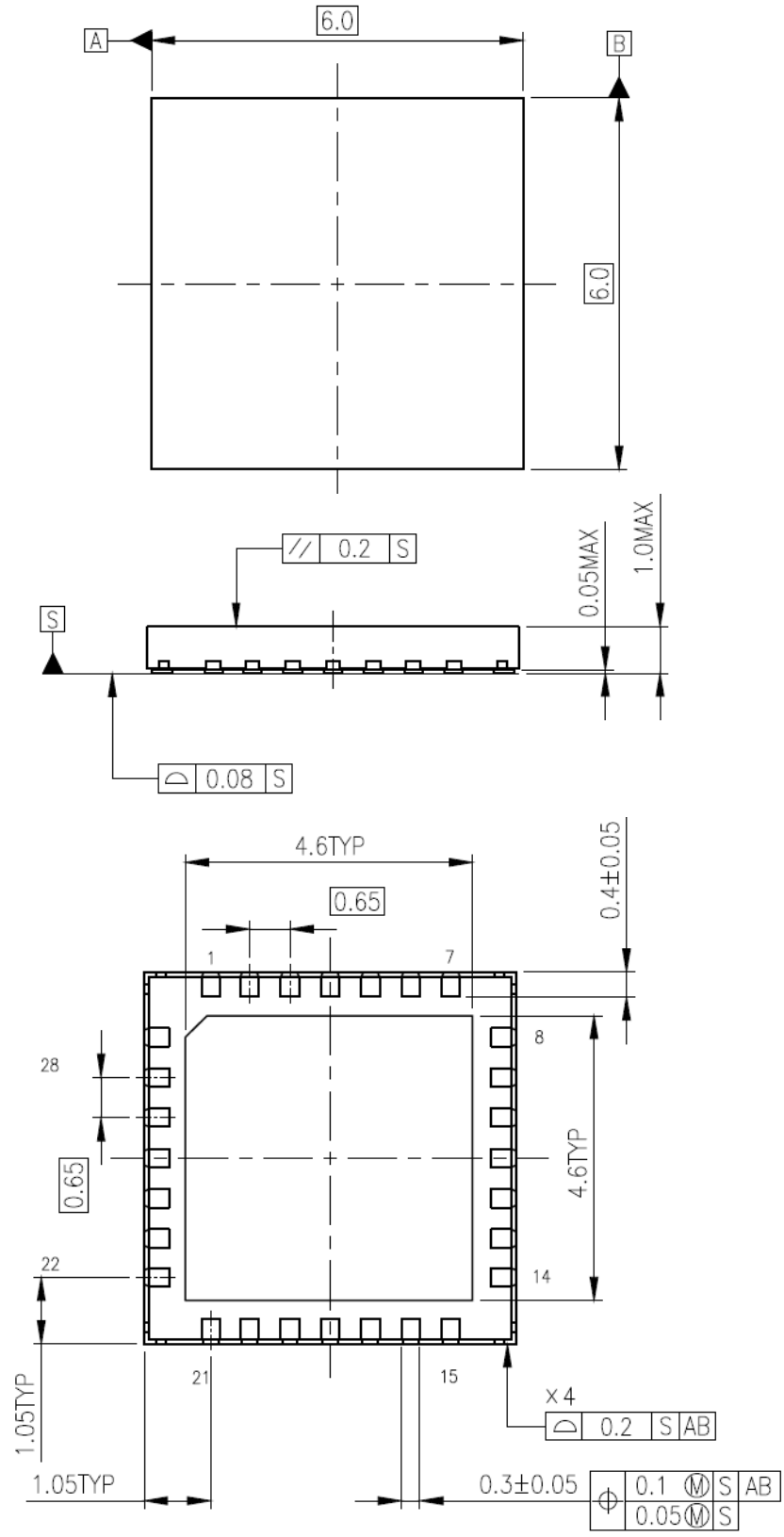
Reference value for parts

Symbol	Reference value	Remarks
R1	Resistor defined at Current value setting in 7.14 Constant current PWM control	-
R2	Resistor defined at Current value setting in 7.14 Constant current PWM control	-
R3	0 to 230kΩ	-
R4	60kΩ to 100kΩ	Tolerance within 5% is recommended
R5	51kΩ	-
R6	51kΩ	-
R7	51kΩ	-
C1	0.1μF	Multilayer ceramic capacitor
C2	10μF to 100μF	Electrolytic capacitor
C3	0.1μF	Multilayer ceramic capacitor
C4	0.047μF to 0.22μF	Multilayer ceramic capacitor
C5	0.1μF	Multilayer ceramic capacitor

12. Package dimensions

P-VQFN28-0606-0.65-002

(Unit:mm)



13. Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

14. IC Usage Considerations
Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the ratings may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

[3] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[4] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in detection functions. If the power supply is unstable, the detection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[5] Carefully select external parts (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

[6] Anomaly detection functions, such as ISD and TSD, are functions which detects or avoids abnormal conditions temporarily, and don't guarantee that IC does not break down. In addition, not only may the detection functions not work properly but also IC may not break down when IC is used out of the range described specifications.

15. Points to remember on handling of ICs

Over current detection circuit

Over current detection circuit do not necessarily protect ICs under all circumstances. If a short circuit continues for a long time, IC may break down due to severe stress. Therefore, a system should be designed to release a status of over current detection circuit immediately.
Depending on the method of use and/or usage conditions, such as exceeding absolute maximum ratings can cause over current detection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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