



FCAB21350L1

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

- Low source-source ON resistance: $R_{ss(on)}$ typ. = 2.2 m Ω (VGS = 3.8 V)
- CSP(Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

■ Marking Symbol: 3M

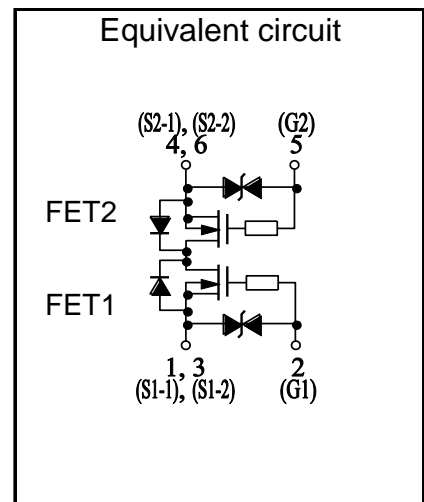
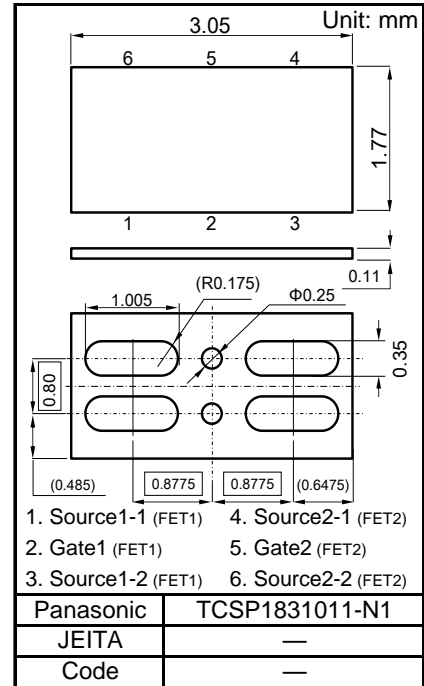
■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	±8	V
Source Current	DC ^{*1}	IS1	12
	DC ^{*2}	IS2	27
	Pulse ^{*3}	ISp	120
Total Power Dissipation	DC ^{*1}	PD1	0.45
	DC ^{*2}	PD2	2.1
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Thermal Resistance (ch-a)	DC ^{*1}	Rth1	278
	DC ^{*2}	Rth2	59

- Note *1 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm)
 using the minimum recommended pad size (36 μ m Copper).
 *2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).
 *3 t = 10 μ s, Duty Cycle ≤ 1 %



■ Electrical Characteristics Ta = 25 °C ± 3 °C

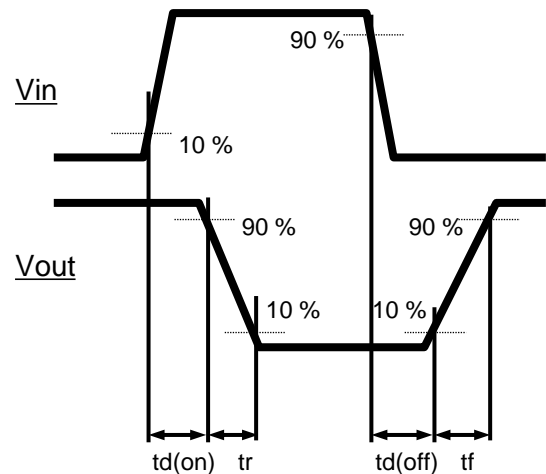
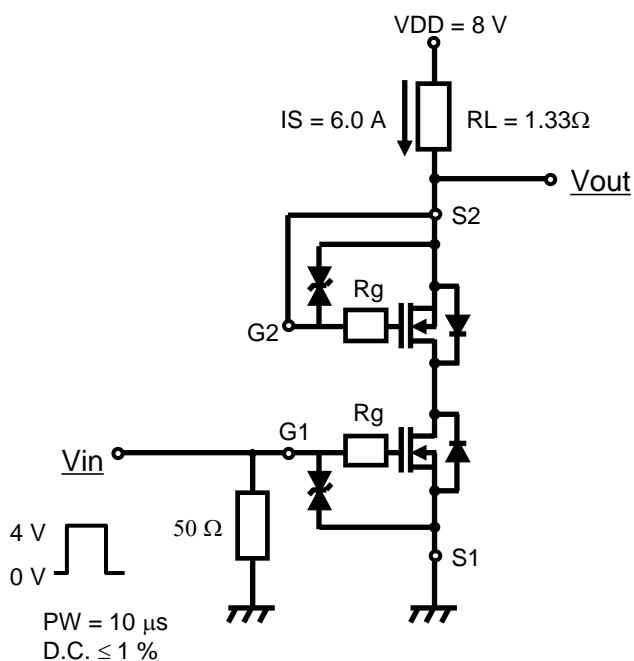
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
		VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 1.41 mA, VSS = 10 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 6.0 A, VGS = 4.5 V	1.55	2.1	2.75	mΩ
	RSS(on)2	IS = 6.0 A, VGS = 3.8 V	1.6	2.2	2.85	
	RSS(on)3	IS = 6.0 A, VGS = 3.1 V	1.65	2.4	3.95	
	RSS(on)4	IS = 6.0 A, VGS = 2.5 V	1.9	3.1	6.1	
Body Diode Forward Voltage	VF(s-s)	IF = 6.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance ^{*1}	Ciss	VSS = 10 V, VGS = 0 V, f = 1 KHz		4650		pF
Output Capacitance ^{*1}	Coss			580		
Reverse Transfer Capacitance ^{*1}	Crss			530		
Turn-on delay Time ^{*1,2}	td(on)	VDD = 8 V, VGS = 0 to 4.0 V		1.2		μs
Rise Time ^{*1,2}	tr	IS = 6.0 A		2.3		
Turn-off delay Time ^{*1,2}	td(off)	VDD = 8 V, VGS = 4.0 to 0 V		9		μs
Fall Time ^{*1,2}	tf	IS = 6.0 A		5.0		
Total Gate Charge ^{*1}	Qg	VDD = 8 V		43		nC
Gate-source Charge ^{*1}	Qgs	VGS = 0 to 4.0 V,		10		
Gate-drain Charge ^{*1}	Qgd	IS = 6.0 A		10		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

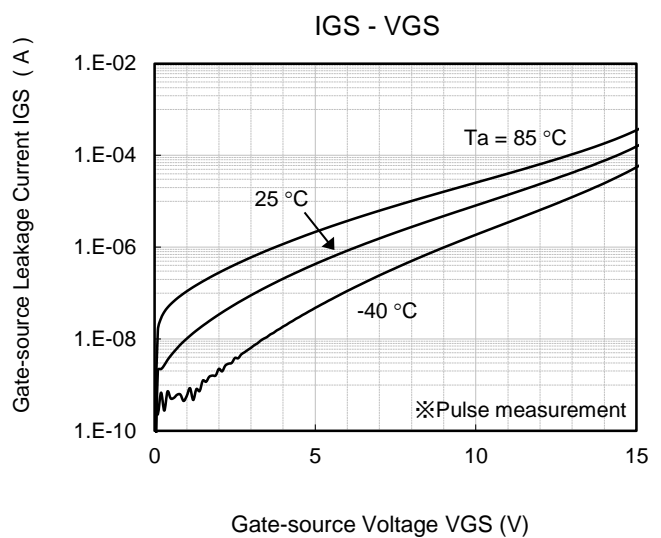
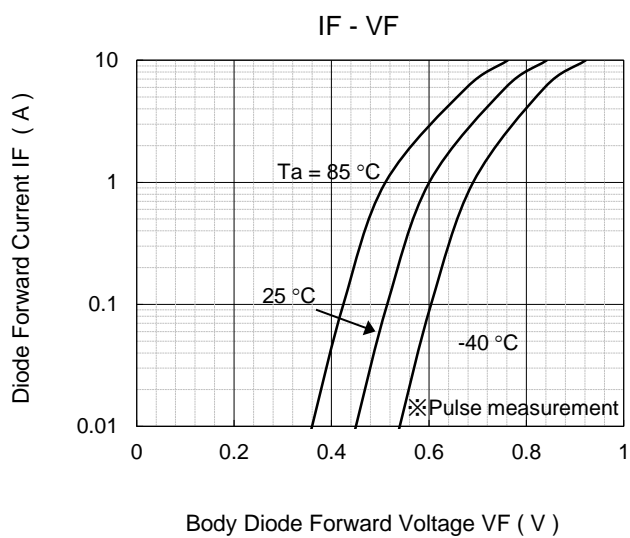
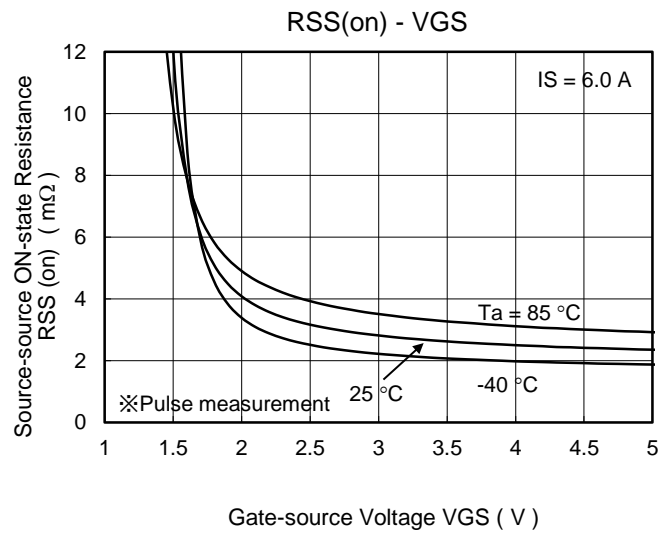
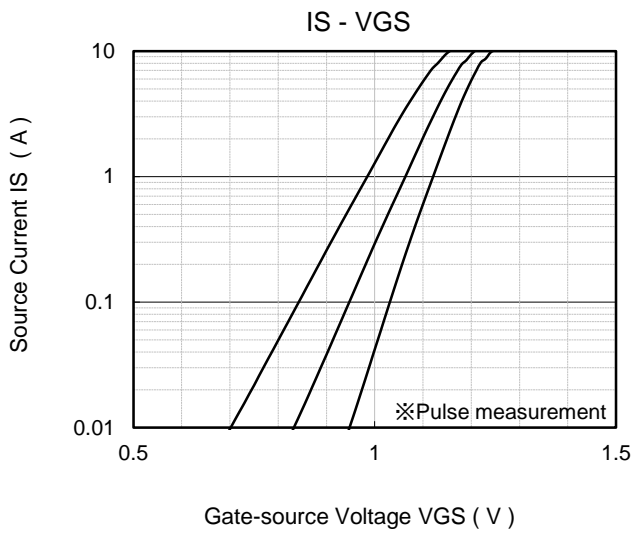
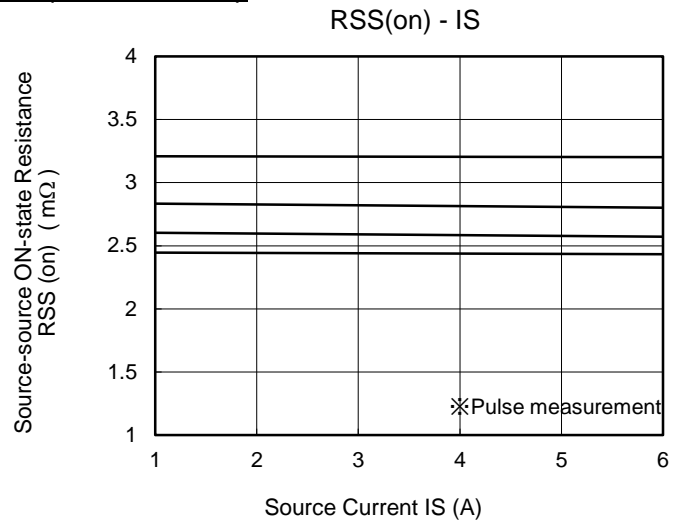
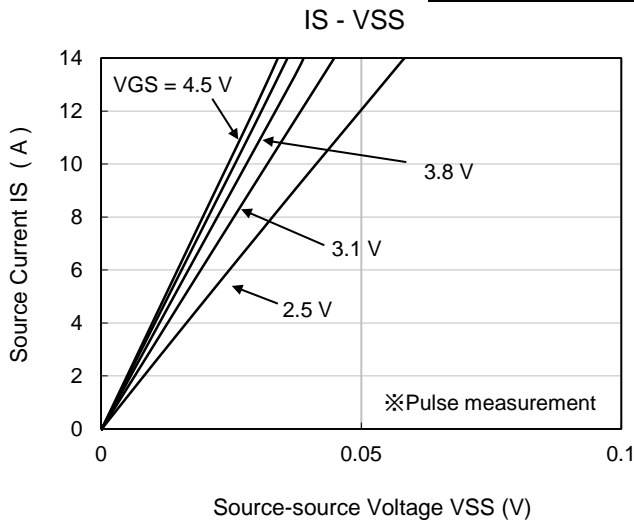
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2 : Measurement circuit

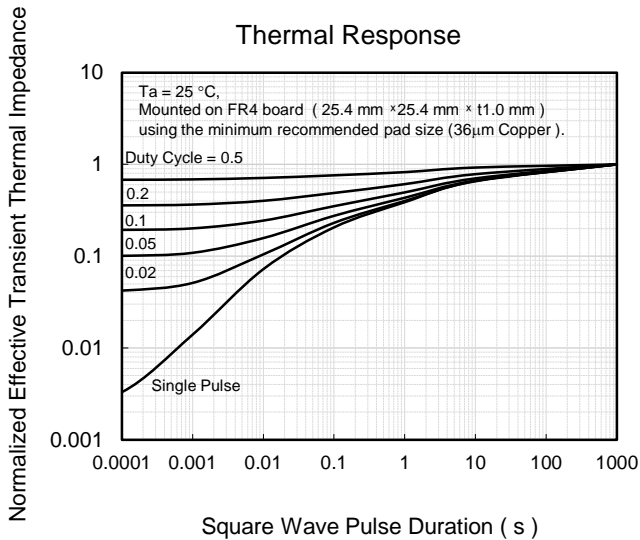
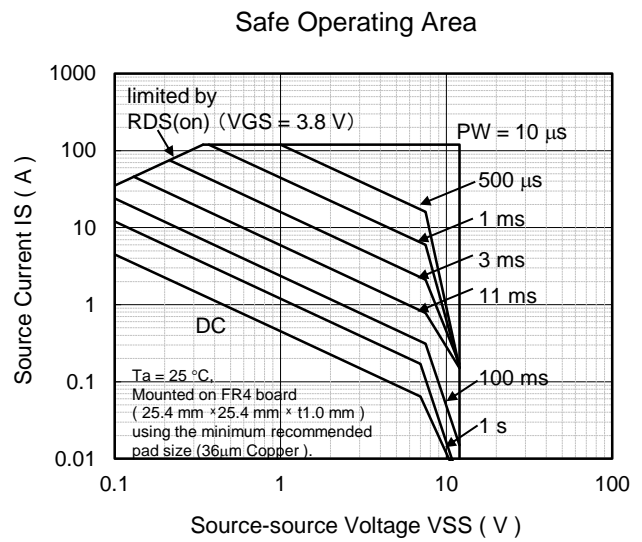
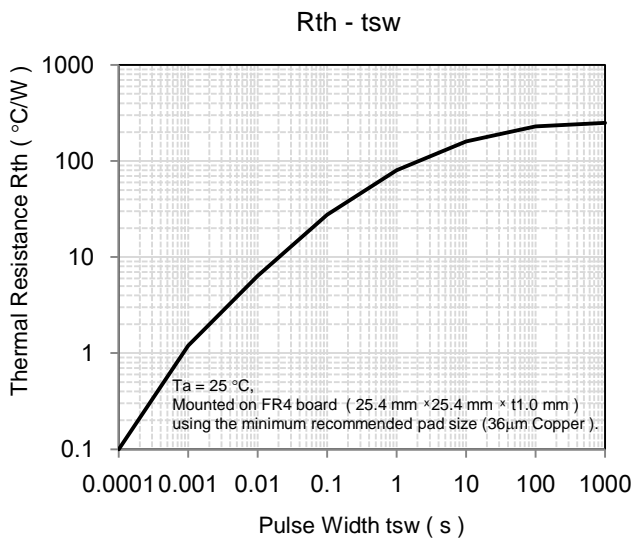
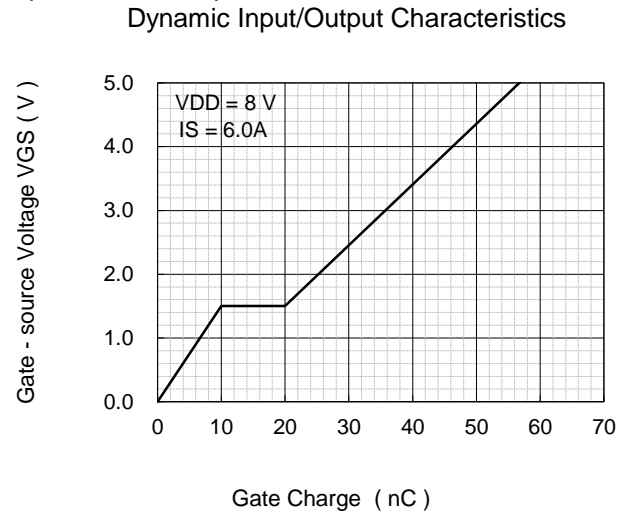
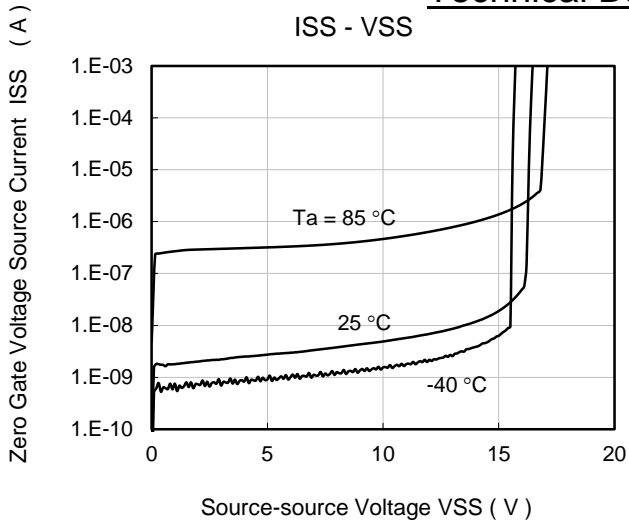


Technical Data (reference)



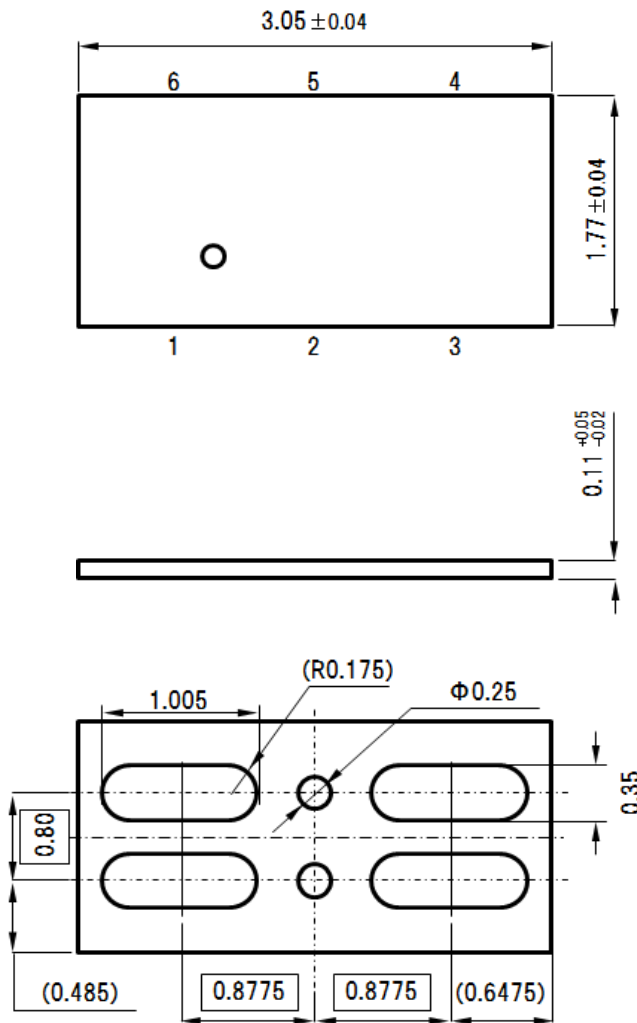


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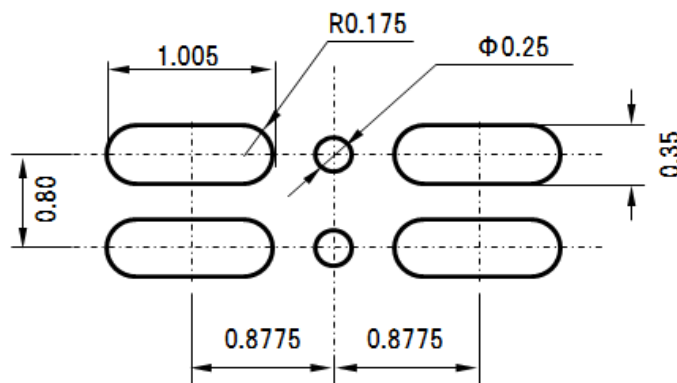
■ Outline (TCSP1831011-N1)

Unit: mm



■ Land Pattern (Reference)

Unit: mm



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