ARG81801

Wide Input Voltage, 2.4 MHz, 3.0 A Asynchronous Buck Regulator with Sleep Mode, External Synchronization, and POK Output

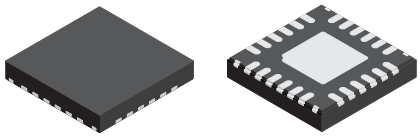
FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Withstands surge voltages up to 40 V
- Operates as low as 3.6 V_{IN} (max) with V_{IN} decreasing
- Delivers up to 3.0 A of output current with integrated 110 mΩ high voltage MOSFET
- $\overline{\text{SLEEP}}$ input pin commands ultralow current shutdown mode
- Adjustable output voltage with ±1.0% accuracy from 0°C to 85°C, ±1.5% from –40°C to 150°C
- Programmable switching frequency: 250 kHz to 2.4 MHz
- Applying a clock input to the SYNC pin will increase the PWM frequency
- Power OK (POK) open-drain output
- Maximized duty cycle for low dropout
- Enhanced idle-stop recovery during V_{IN} transients
- Pre-bias startup capable, V_{OUT} will not cause a reset

Continued on next page...

PACKAGE:

24-pin wettable flank QFN
with exposed thermal pad (suffix ES)



Not to scale

DESCRIPTION

Designed to provide the power supply requirements of next generation car audio and infotainment systems, the ARG81801 provides all the control and protection circuitry to produce a high current regulator with ±1.0% output voltage accuracy. After startup, the ARG81801 operates down to at least 3.6 V_{IN} (V_{IN} falling).

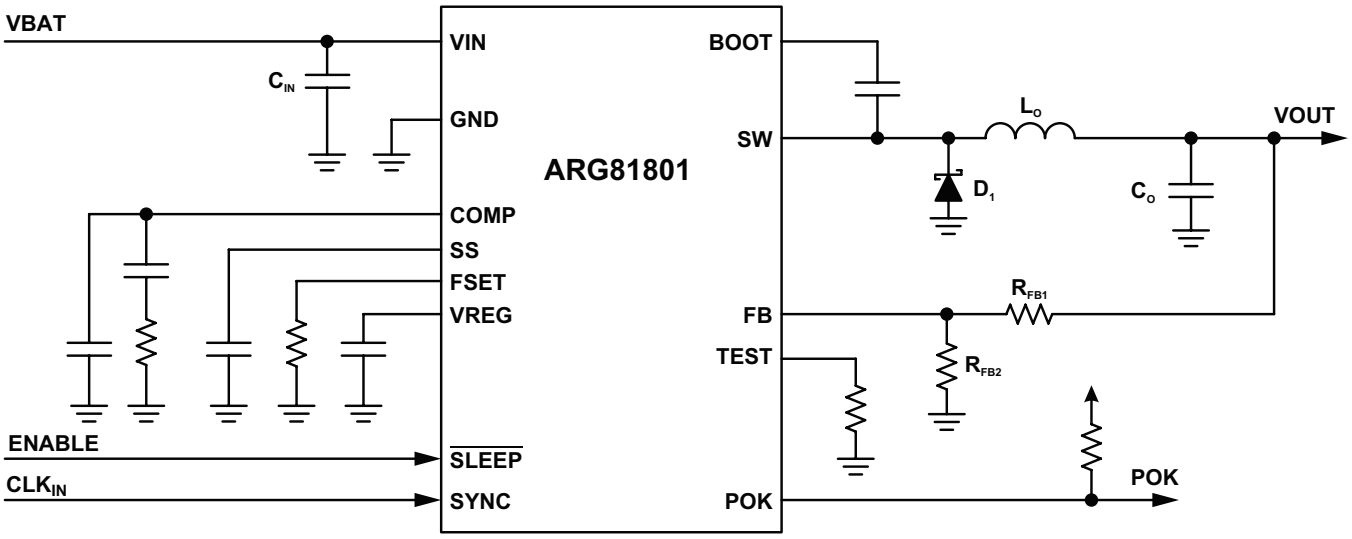
If the SYNC input is driven by an external clock signal higher than the base frequency (f_{OSC}), the PWM frequency synchronizes to the incoming clock frequency. The $\overline{\text{SLEEP}}$ input pin commands an ultralow current shutdown mode requiring less than 5 µA for internal circuitry and 10 µA (max) for MOSFET leakage at 16 V_{IN}, 85°C.

The ARG81801 has external compensation to accommodate a wide range of frequencies and external components, and provides a Power OK (POK) signal validated by the output voltage.

The ARG81801 uses an Enhanced Idle/Stop-Start Recovery technique to reduce or eliminate output overshoot when V_{IN} recovers from levels below V_{IN} minimum (i.e. V_{OUT} drops out of regulation).

Extensive protection features of the ARG81801 include pulse-by-pulse current limit, hiccup mode short circuit protection, open/short asynchronous diode protection, BOOT open/short voltage protection, V_{IN} undervoltage lockout, V_{OUT} overvoltage protection, and thermal shutdown.

Continued on next page...



Typical Application Diagram

ARG81801

Wide Input Voltage, 2.4 MHz, 3.0 A Asynchronous Buck Regulator with Sleep Mode, External Synchronization, and POK Output

FEATURES AND BENEFITS

- External compensation for maximum flexibility
- Excellent set of protection features to satisfy the most demanding applications
- Overvoltage, pulse-by-pulse current limit, hiccup mode short circuit, and thermal protection

DESCRIPTION

The ARG81801 is supplied in a 24-pin wettable flank QFN package with exposed power pad (suffix ES). It is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Operating Ambient Temperature Range T_A, (°C)	Packing
ARG81801KESJSR	–40 to 150	6000 pieces per 13-in. reel

Table of Contents

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, $\overline{\text{SLEEP}}$, SS Pin Voltage			–0.3 to 40	V
SW Pin Voltage	V_{SW}	Continuous (minimum limit is a function of temperature)	–0.3 to V_{IN} + 0.3	V
		t < 50 ns	–1.0 to V_{IN} + 0.3	V
BOOT Pin Voltage	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		BOOT OV Fault Condition	V_{SW} – 0.3 to V_{SW} + 7.0	V
All Other Pin Voltages			–0.3 to 5.5	V
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

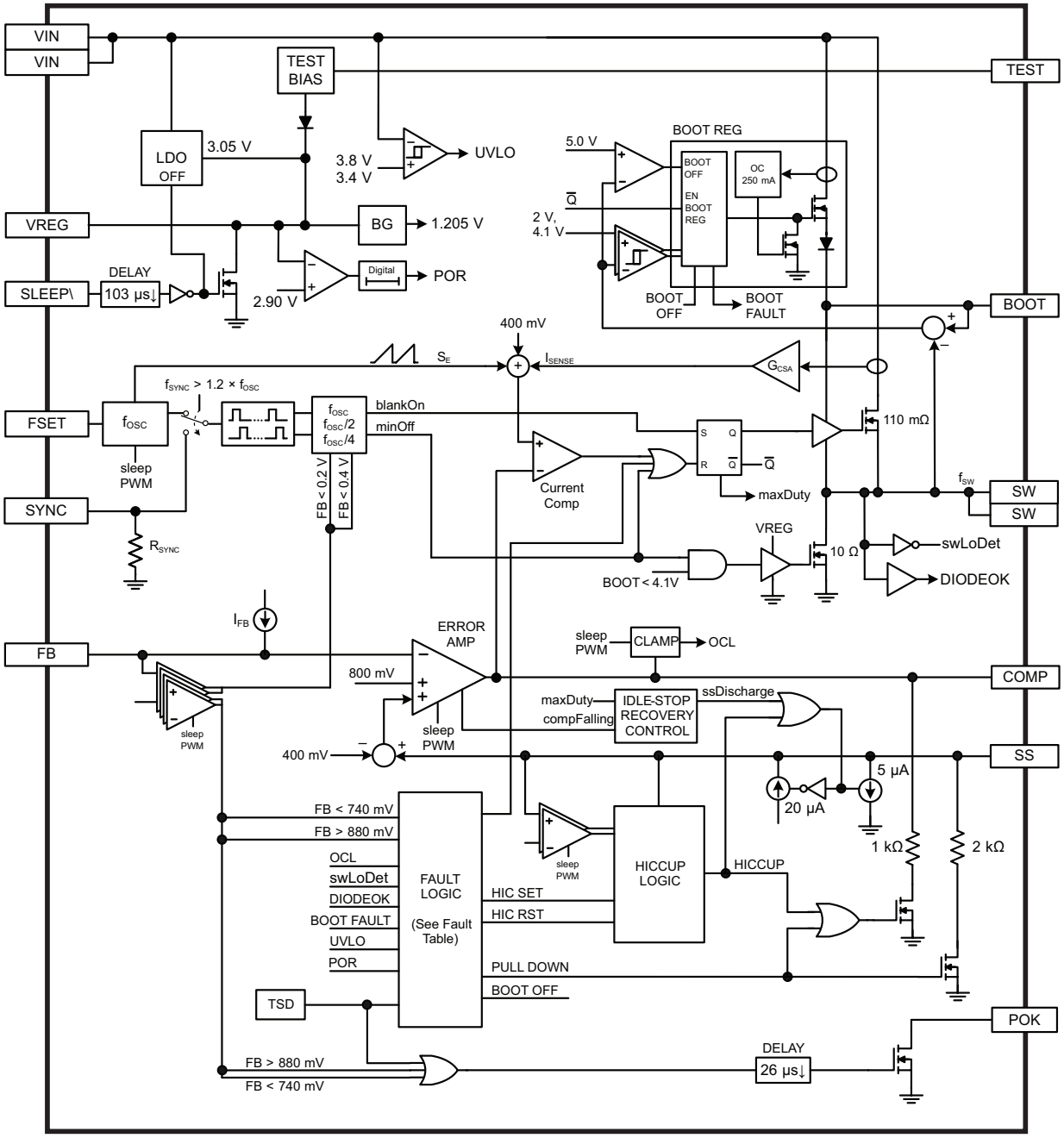
[1] Operation at levels beyond the ratings listed in this table may cause permanent damage to the device. The Absolute Maximum ratingsare stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS: May require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	37	°C/W

[2] Additional thermal information available on the Allegro website.

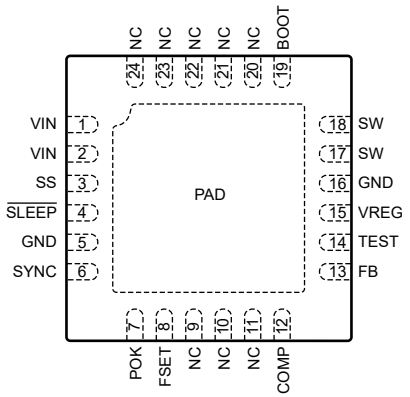
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST



Package ES, 24-Pin QFN Pinout Diagram

Terminal List Table

Name	Number	Function
VIN	1, 2	Power input for the control circuits and the drain of the high-side N-channel MOSFET. Connect this pin to a power supply providing from 4.0 to 35 V. A ceramic capacitor should be placed and grounded very close to this pin.
SS	3	Soft start and hiccup pin. Connect a capacitor, C_{SS}, from this pin to GND to set soft start mode duration. The capacitor also determines the hiccup period during overcurrent.
$\overline{\text{SLEEP}}$	4	Setting this pin low forces sleep mode (very low current shutdown mode: V_{OUT} = 0 V). This pin must be set high to enable the ARG81801. If the application does not require a sleep mode, then this pin can be tied directly to VIN. Do not float this pin.
GND	5, 16	Ground pins.
SYNC	6	Applying an external clock input to this pin forces synchronization of PWM to the clock input rate (f_{SYNC}), at a rate higher than f_{OSC}. $\overline{\text{SLEEP}}$ low overrides this pin.
POK	7	Power OK output signal. This pin is an open drain output that transitions from low to high impedance after the output has maintained regulation for $t_{d(POK)}$, typically 26 µs.
FSET	8	Frequency setting pin. A resistor, R_{FSET}, from this pin to GND sets the base PWM switching frequency (f_{OSC}). See the Design and Component Selection section for information on determining the value of R_{FSET}.
NC	9-11, 20-24	No connect pins. These should be connected to ground to aid thermal transfer.
COMP	12	Output of the error amplifier and compensation node for the current mode control loop. Connect a series RC network from this pin to GND for loop compensation. See the Design and Component Selection section of this datasheet for further details.
FB	13	Feedback (negative) input to the error amplifier. Connect a resistor divider from the regulator output, V_{OUT}, to this pin to program the output voltage.
TEST	14	Test mode pin. This pin should be connected to ground. Allegro recommends using a resistor from this pin to ground to limit the regulator output voltage in the event the FB pin becomes shorted to this pin.
VREG	15	Internal voltage regulator bypass capacitor pin. Connect a 1 µF ceramic capacitor from this pin to ground and place it close to the ARG81801.
SW	17, 18	The source of the high-side N-channel MOSFET. The external free-wheeling diode (D_1) and output inductor (L_O) should be connected to this pin. Both D_1 and L_O should be placed close to this pin and connected with relatively wide traces.
BOOT	19	High-side gate drive boost input. This pin supplies the drive for the high-side N-channel MOSFET. Connect a 47 nF ceramic capacitor from BOOT to SW.
PAD	–	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 6 vias, directly in the pad land.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE						
Input Voltage Range [1]	V_{IN}		4.0	–	35	V
VIN UVLO Start	$V_{INUV(ON)}$	V_{IN} rising	3.6	3.8	4.0	V
VIN UVLO Stop	$V_{INUV(OFF)}$	V_{IN} falling	3.2	3.4	3.6	V
VIN UVLO Hysteresis	$V_{INUV(HYS)}$		–	400	–	mV
INPUT SUPPLY CURRENT						
Sleep Mode Input Supply Current [2][3]	$I_{IN(SLEEP)}$	$V_{\overline{SLEEP}}$ ≤ 0.5 V, T_J = 85°C, V_{IN} = 16 V	–	5	15	µA
		$V_{\overline{SLEEP}}$ ≤ 0.5 V, T_J = 85°C, V_{IN} = 35 V	–	7	25	µA
PWM Mode Input Supply Current [2]	$I_{IN(PWM)}$	I_{OUT} = 0 mA	–	2.5	5.0	mA
VOLTAGE REGULATION						
Feedback Voltage Accuracy [4]	V_{FB}	0°C < T_J < 85°C, V_{IN} ≥ 4.1 V, V_{FB} = V_{COMP}	792	800	808	mV
		–40°C < T_J < 150°C, V_{IN} ≥ 4.1 V, V_{FB} = V_{COMP}	788	800	812	mV
Output Dropout Voltage [5]	$V_{OUT(SAT)}$	T_A = 85°C, $R_{DC(LO)}$ ≤ 75 mΩ, V_{IN} = 3.6 V, I_{OUT} = 1 A, f_{SW} = 425 kHz	3.27	3.295	–	V
		T_A = 85°C, $R_{DC(LO)}$ ≤ 75 mΩ, V_{IN} = 5.3 V, I_{OUT} = 1 A, f_{SW} = 425 kHz	4.95	5.0	–	V
		T_A = 85°C, $R_{DC(LO)}$ ≤ 50 mΩ, V_{IN} = 3.75 V, I_{OUT} = 1 A, f_{SW} = 2 MHz	3.25	3.3	–	V
		T_A = 85°C, $R_{DC(LO)}$ ≤ 50 mΩ, V_{IN} = 5.5 V, I_{OUT} = 1 A, f_{SW} = 2 MHz	4.89	5.0	–	V
ERROR AMPLIFIER						
Feedback Input Bias Current [2]	I_{FB}		–38	–	–16	nA
Open Loop Voltage Gain	A_{VOL}	V_{COMP} = 1.2 V	–	65	–	dB
Transconductance	gm	400 mV < V_{FB}	500	750	950	µA/V
		0 V < V_{FB} < 400 mV	275	375	475	µA/V
Output Current	I_{EA}	V_{COMP} = 1.2 V	–	±75	–	µA
COMP Pull-Down Resistance	R_{COMP}	FAULT = 1 or HICCUP = 1	–	1	–	kΩ

Continued on next page...

[1] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[2] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[3] Performance at 85°C ensured by design and characterization, not production tested.
[4] Performance at the 0°C and 85°C ranges ensured by design and characterization, not production tested.
[5] Ensured by design and characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PULSE WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM(OFFS)}$	V_{COMP} level required for 0% duty cycle	–	400	–	mV
Minimum Controllable On-Time	$t_{ON(MIN)}$	12 V < V_{IN} < 16 V, I_{OUT} = 1 A, V_{BOOT} – V_{SW} = 4.5 V	–	95	135	ns
Minimum Switch Off-Time	$t_{OFF(MIN)}$		–	95	130	ns
COMP to SW Current Gain	gm_{POWER}		–	4.0	–	A/V
Slope Compensation [6]	S_E	f_{OSC} = 2.44 MHz	2.31	3.30	4.30	A/µs
		f_{OSC} = 1.00 MHz	0.66	1.00	1.32	A/µs
		f_{OSC} = 252 kHz	0.15	0.22	0.29	A/µs
MOSFET PARAMETERS [7]						
High-Side MOSFET On-Resistance [8]	$R_{DS(on)HS}$	T_J =25°C, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 0.4 A	–	110	125	mΩ
		T_J =150°C, V_{BOOT} – V_{SW} = 4.5 V, I_{DS} = 0.4 A	–	190	215	mΩ
High-Side MOSFET Leakage [9][10]	$I_{LKG(HS)}$	T_J < 85°C, $V_{\overline{SLEEP}}$ ≤ 0.5 V, V_{SW} = 0 V, V_{IN} = 16 V	–	–	10	µA
		T_J ≤ 150°C, $V_{\overline{SLEEP}}$ ≤ 0.5 V, V_{SW} = 0 V, V_{IN} = 16 V	–	60	150	µA
SW Node Slew Rate [6]	SR_{SW}	12 V < V_{IN} < 16 V	–	0.72	–	V/ns
Low-Side MOSFET On-Resistance [8]	$R_{DS(on)LS}$	T_J = 25°C, V_{IN} ≥ 6 V, I_{DS} = 0.1 A	–	–	10	Ω
PWM SWITCHING FREQUENCY						
Base Switching Frequency	f_{OSC}	R_{FSET} = 8.06 kΩ	2.20	2.44	2.70	MHz
		R_{FSET} = 23.7 kΩ	0.90	1.00	1.10	MHz
		R_{FSET} = 102 kΩ	–	252	–	kHz
PWM SYNCHRONIZATION TIMING						
Synchronization Frequency Range	$f_{SYNC(MULT)}$		1.2 × f_{OSC}(typ)	–	1.5 × f_{OSC}(typ)	–
Synchronized Frequency	f_{SYNC}		–	–	2.9	MHz
Synchronization Input Duty Cycle	D_{SYNC}		–	–	80	%
Synchronization Input Pulse Width	$t_{w(SYNC)}$		200	–	–	ns
Synchronization Input Rise Time [6]	$t_{r(SYNC)}$		–	10	15	ns
Synchronization Input Fall Time [6]	$t_{f(SYNC)}$		–	10	15	ns
Synchronization High Threshold	$V_{SYNC(H)}$		–	–	2.0	V
Synchronization Low Threshold	$V_{SYNC(L)}$		0.8	–	–	V
Synchronization Hysteresis [6]	$V_{SYNC(HYS)}$		–	200	–	mV
Synchronization Input Resistance	R_{SYNC}		120	200	280	kΩ

Continued on next page...

[6] Ensured by design and characterization, not production tested.
[7] Thermally limited depending on input voltage, output voltage, duty cycle, regulator load currents, PCB layout, and airflow.
[8] Performance at 25°C ensured by design and characterization, not production tested.
[9] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[10] Performance at 85°C ensured by design and characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{\text{SLEEP}}$ PIN INPUT THRESHOLDS						
$\overline{\text{SLEEP}}$ High Threshold	$V_{\overline{SLEEP}(H)}$	$V_{\overline{SLEEP}}$ rising	–	1.3	2.1	V
$\overline{\text{SLEEP}}$ Low Threshold	$V_{\overline{SLEEP}(L)}$	$V_{\overline{SLEEP}}$ falling	0.5	1.2	–	V
$\overline{\text{SLEEP}}$ Delay	$t_{d(\overline{SLEEP})}$	$V_{\overline{SLEEP}}$ transitioning low	55	103	150	µs
$\overline{\text{SLEEP}}$ Input Bias Current	$I_{\overline{SLEEP}(BIAS)}$	$V_{\overline{SLEEP}}$ = 5 V	–	500	–	nA
VREG PIN OUTPUT						
VREG Output Voltage	V_{VREG}	V_{TEST} = 0 V	–	3.05	–	V
BOOT REGULATOR						
BOOT Charging Frequency [11]	f_{BOOT}		–	f_{SW}	–	–
BOOT Voltage Enable Threshold	$V_{BOOT(EN)}$	V_{BOOT} rising	1.7	2.0	2.2	V
BOOT Voltage Enable Hysteresis	$V_{BOOT(HYS)}$		–	200	–	mV
BOOT Voltage Low-Side Switch Disable Threshold	$V_{BOOT(LS,DIS)}$	V_{BOOT} rising	–	4.1	–	V
SOFT START PIN						
FAULT, HICCUP Reset Voltage	$V_{SS(RST)}$	V_{SS} falling due to $R_{SS(FLT)}$	–	200	275	mV
Hiccup OCP Threshold	$V_{HIC(EN)}$	V_{SS} rising	–	2.3	–	V
Maximum Charge Voltage	$V_{SS(MAX)}$		–	V_{VREG}	–	V
Startup (Source) Current	$I_{SS(SU)}$	HICCUP = FAULT = 0	–30	–20	–10	µA
Hiccup (Sink) Current	$I_{SS(HIC)}$	HICCUP = 1	2.4	5	10	µA
Pull-Down Resistance	$R_{SS(FLT)}$	FAULT = 1 or $V_{\overline{SLEEP}}$ = low	–	2	–	kΩ
Soft Start Frequency Foldback	$f_{SW(SS)}$	0 V < V_{FB} < 200 mV	–	f_{OSC} / 4	–	–
		200 mV < V_{FB} < 400 mV	–	f_{OSC} / 2	–	–
		400 mV < V_{FB}	–	f_{OSC}	–	–
Soft Start Delay Time [11]	$t_{d(SS)}$	C_{SS} = 22 nF	–	440	–	µs
Soft Start Output Ramp Time [11]	t_{SS}	C_{SS} = 22 nF	–	880	–	µs
HICCUP MODES						
Hiccup, OCP Count	OCP_{LIM}	V_{SS} > 2.3 V and OCL = 1	–	120	–	counts
Hiccup, BOOT Undervoltage (Shorted) Count	$BOOT_{UV}$		–	120	–	counts
Hiccup, BOOT Overvoltage (Open) Count	$BOOT_{OV}$		–	7	–	counts

Continued on next page...

[11] Ensured by design and characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS (continued): Valid at 4.0 V ≤ V_{IN} ≤ 35 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

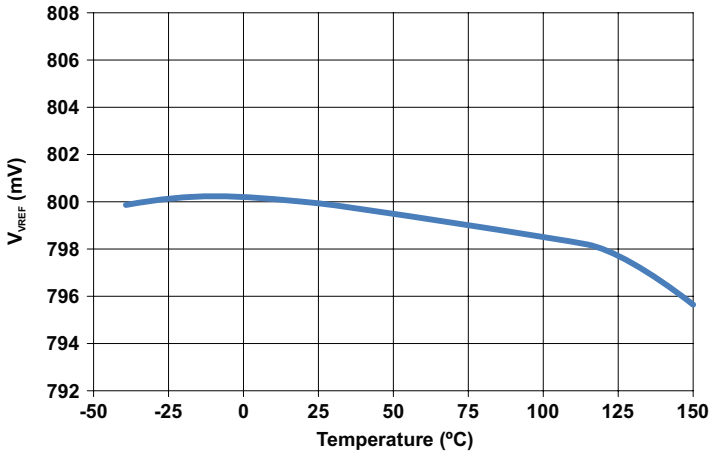
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OVERCURRENT PROTECTION (OCP)						
PWM Pulse-by-Pulse Limit	$I_{LIM(TON,MIN)}$	$t_{ON} = t_{ON(MIN)}$	4.8	5.5	6.1	A
	$I_{LIM(TON,MAX)}$	$t_{ON} = (1/f_{SW}) – t_{OFF(MIN)}$, no synchronization	3.0	4.1	5.1	A
OUTPUT VOLTAGE PROTECTION (OVP)						
VOUT Overvoltage Threshold	$V_{OUT(OV)}$	V_{FB} rising, PWM mode	860	880	902	mV
VOUT Overvoltage Hysteresis	$V_{OUT(OV)HYS}$	V_{FB} falling, relative to $V_{OUT(OV)}$	–	–10	–	mV
VOUT Undervoltage Threshold	$V_{OUT(UV)}$	V_{FB} falling, PWM mode	715	740	765	mV
VOUT Undervoltage Hysteresis	$V_{OUT(UV)HYS}$	V_{FB} rising, relative to $V_{OUT(UV)}$	–	10	–	mV
POWER OK (POK) OUTPUT						
POK Rising Delay	$t_{d(POK)}$	V_{FB} rising only	19	30	41	µs
POK Low Output Voltage	$V_{POK(L)}$	I_{POK} = 5 mA	–	185	400	mV
POK Leakage Current [12]	$I_{POK(LKG)}$	V_{POK} = 5.5 V	–1	–	1	µA
THERMAL PROTECTION						
Thermal Shutdown Rising Threshold [13]	T_{SD}	PWM stops immediately and COMP and SS are pulled low	155	170	185	°C
Thermal Shutdown Hysteresis [13]	$T_{SD(HYS)}$		–	20	–	°C

[12] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[13] Ensured by design and characterization, not production tested.

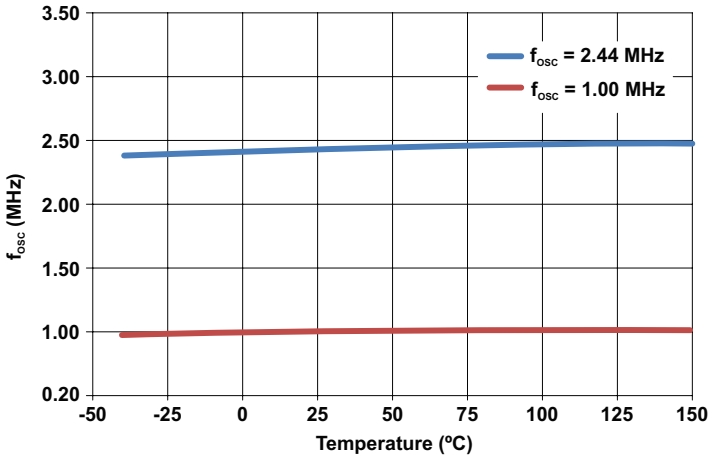
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TYPICAL PERFORMANCE CHARACTERISTICS

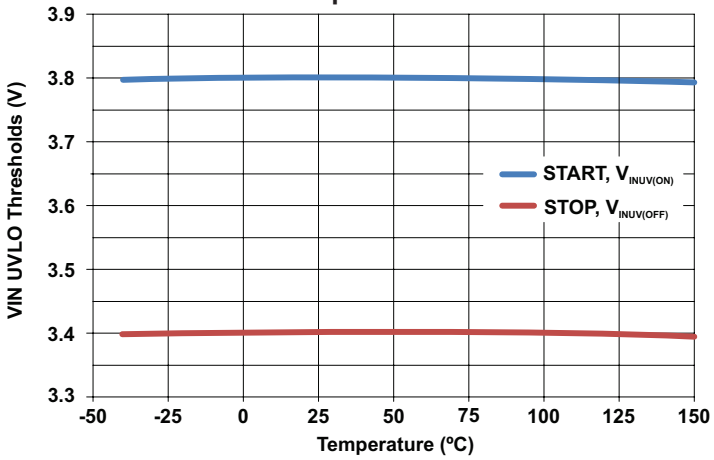
Reference Voltage versus Temperature



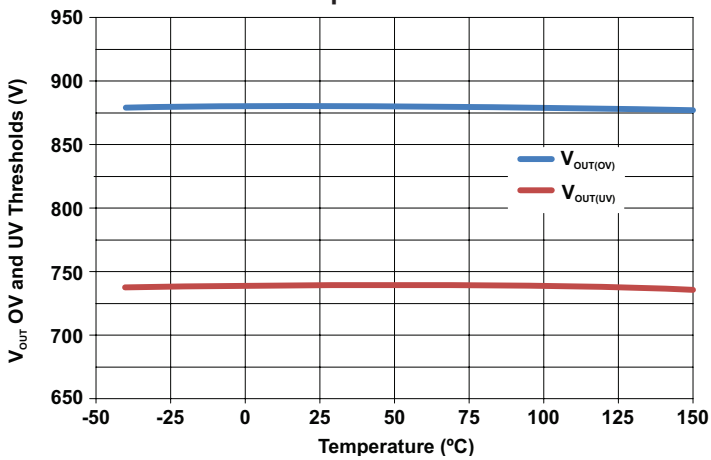
Oscillator Frequency versus Temperature



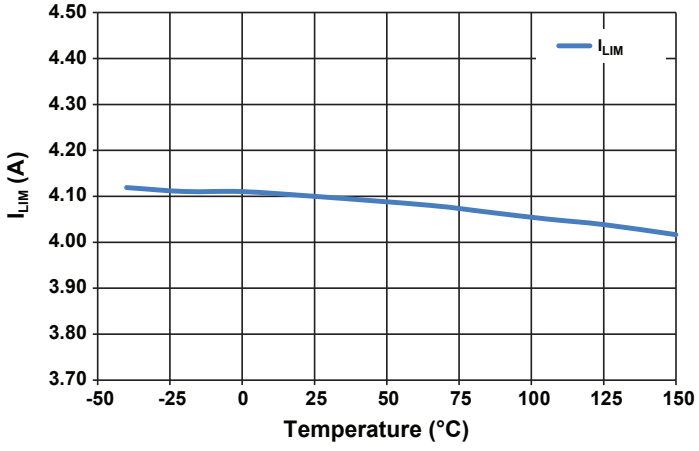
VIN UVLO Start and Stop Thresholds versus Temperature



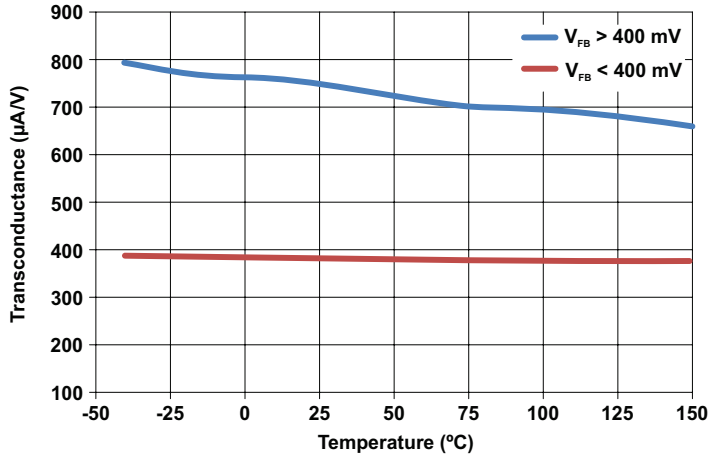
V_{OUT} Overvoltage and Undervoltage Thresholds versus Temperature



Pulse-by-Pulse Current Limit at $t_{ON(MIN)}$ ($I_{LIM(TON,MIN)}$) versus Temperature

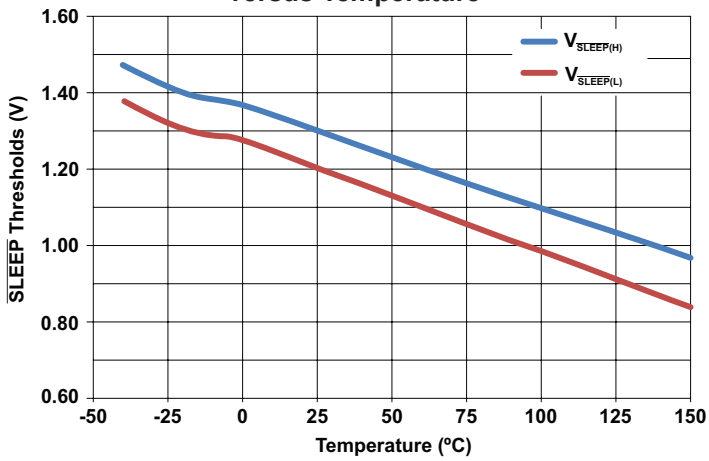


Error Amplifier Transconductance versus Temperature

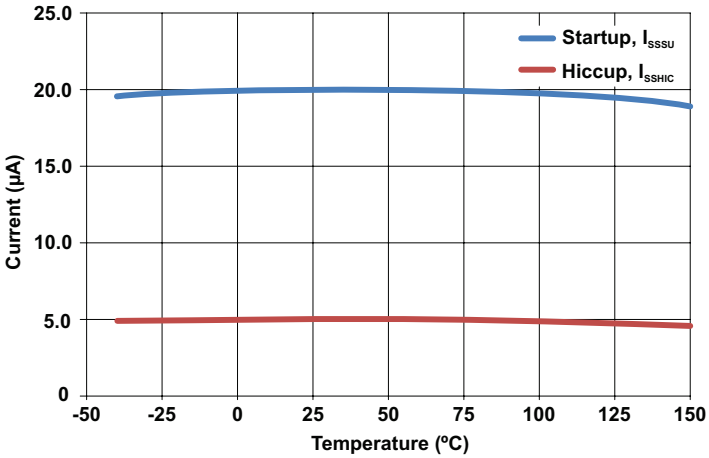


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

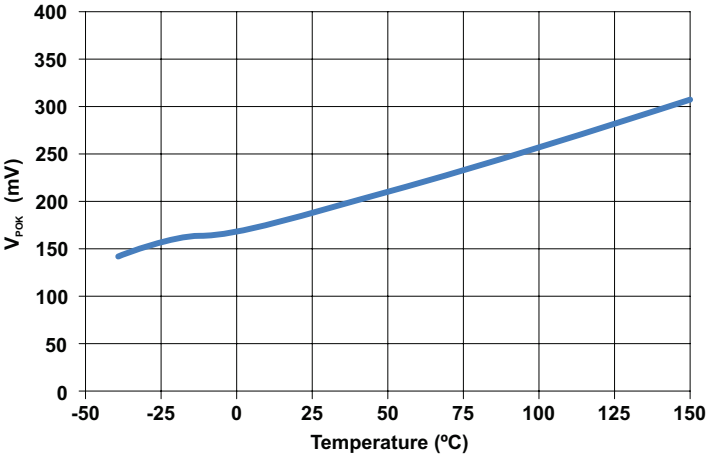
$\overline{\text{SLEEP}}$ High and Low Voltage Thresholds Thresholds versus Temperature



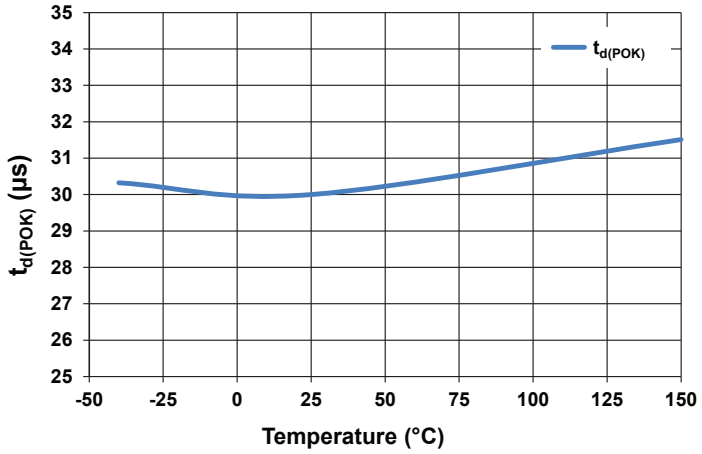
SS Start and Hiccup Currents versus Temperature



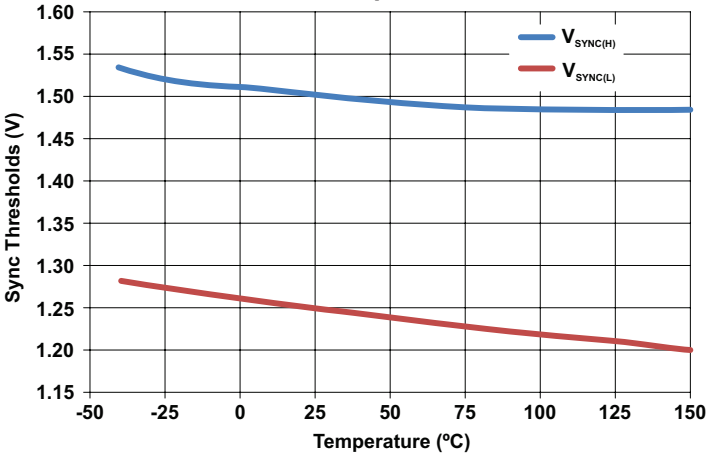
POK Low Output Voltage at 5 mA versus Temperature



POK Time Delay versus Temperature



Sync High and Low Voltage Thresholds versus Temperature



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Overview

The ARG81801 is an asynchronous current mode buck regulator that incorporates all the control and protection circuitry necessary to provide the power supply requirements of car audio and infotainment systems.

The ARG81801 has two modes of operation. First, the ARG81801 can deliver up to 3.0 A in pulse-width modulation (PWM) mode. Second, with the $\overline{\text{SLEEP}}$ pin low, the ARG81801 will enter an ultralow current shutdown (sleep) mode where V_{OUT} = 0 V and the total current drawn from V_{IN} will typically be less than 10 µA.

The ARG81801 was designed to support up to 3.0 A. However, the exact amount of current it will supply, before possible thermal shutdown, depends heavily on duty cycle, ambient temperature, airflow, PCB layout, and PCB construction. Figure 1 shows calculated current ratings versus ambient temperature for V_{IN} = 12 V and V_{OUT} = 3.3 V and 5.0 V, at f_{SW} = 425 kHz and f_{SW} = 2 MHz. This analysis assumed a 4-layer PCB constructed according to the JEDEC standard (yielding a thermal resistance of 37°C/W), with no nearby heat sources, and no airflow.

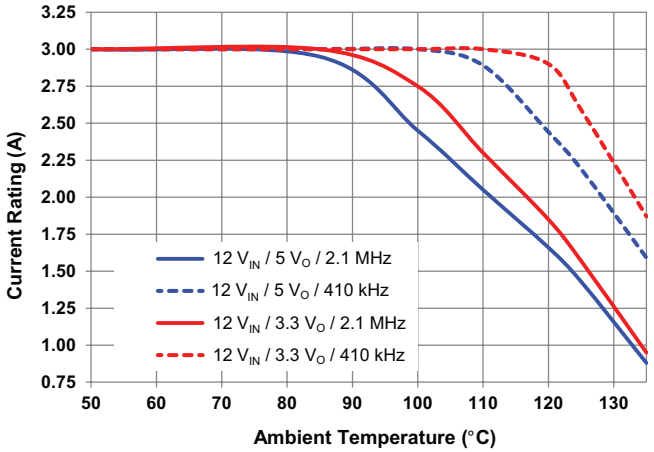


Figure 1: ARG81801 Typical Current Derating

Reference Voltage

The ARG81801 incorporates an internal reference that allows output voltages (V_{OUT}) as low as 0.8 V. The accuracy of the internal reference is ±1.0% from 0°C to 85°C and ±1.5% from −40°C to 150°C. The output voltage is programmed by connecting a resistor divider from V_{OUT} to the FB pin of the ARG81801, as shown in the Typical Applications schematics.

PWM Switching Frequency

The PWM switching frequency of the ARG81801 is adjustable from 250 kHz to 2.4 MHz and has an accuracy of about ±10% across the operating temperature range.

During startup, the PWM switching frequency changes from 25% to 50% and finally to 100% of f_{OSC}, as V_{OUT} rises from 0 V to the regulation voltage. The startup switching frequency is discussed in more detail in the section describing soft start.

If the regulator output is shorted to ground, $V_{FB} \approx 0$ V, the PWM frequency will be 25% of f_{OSC}. In this case, the extra low switching frequency allows extra off-time between SW pulses. The extra off time allows the output inductor current to decay back to 0 A before the next SW pulse occurs. This prevents the inductor current from climbing to a value that could damage the ARG81801 or the output inductor.

$\overline{\text{SLEEP}}$ Input

The ARG81801 has a $\overline{\text{SLEEP}}$ logic level input pin. To get the ARG81801 to operate, the $\overline{\text{SLEEP}}$ pin must be a logic high (>2.1 V). The $\overline{\text{SLEEP}}$ pin is rated to 40 V, allowing the $\overline{\text{SLEEP}}$ pin to be connected directly to V_{IN} if there is no suitable logic signal available to wake up the ARG81801.

When $\overline{\text{SLEEP}}$ transitions low, the ARG81801 waits approximately 103 µs before shutting down. This delay provides plenty of filtering to prevent the ARG81801 from prematurely entering sleep mode because of any small glitch coupling onto the PCB trace or $\overline{\text{SLEEP}}$ pin.

Synchronization Input

If an external clock is applied to the SYNC pin, the ARG81801 synchronizes its PWM frequency to the external clock. The external clock may be used to increase the ARG81801's base PWM frequency ($f_{OSC(TYP)}$) set by R_{FSET}. Synchronization operates from 1.2 × $f_{OSC(TYP)}$ to 1.5 × $f_{OSC(TYP)}$. The external clock pulses must satisfy the pulse width, duty-cycle, and rise/fall time requirements shown in the Electrical Characteristics table in this datasheet.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Transconductance Error Amplifier

The transconductance error amplifier primary function is to control the regulator output voltage. The error amplifier is shown in Figure 2. Here, it is shown as a three-terminal input device with two positive and one negative input. The negative input is simply connected to the FB pin and is used to sense the feedback voltage for regulation. The two positive inputs are used for soft start and steady-state regulation. The error amplifier performs an analog OR selection between its two positive inputs. The error amplifier regulates to either the soft start pin voltage (minus 400 mV) or the ARG81801 internal reference, V_{REF}, whichever is lower.

To stabilize the regulator, a series RC compensation network (R_Z and C_Z) must be connected from the error amplifier output (the COMP pin) to GND, as shown in the Typical Applications schematics. In most instances, an additional relatively low value capacitor (C_P) should be connected in parallel with the R_Z-C_Z components to reduce the loop gain at very high frequencies. However, if the C_P capacitor is too large, the phase margin of the regulator may be reduced. Calculating R_Z, C_Z, and C_P is covered in detail in the Design and Component Selection section of this datasheet.

If a fault occurs or the regulator is disabled ($\overline{SLEEP}$ = low), the COMP pin is pulled to GND via approximately 1 kΩ and PWM switching is inhibited.

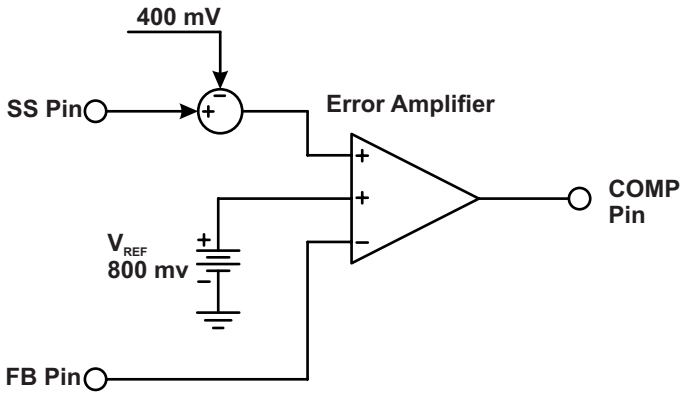


Figure 2: ARG81801 Error Amplifier

Slope Compensation

The ARG81801 incorporates internal slope compensation (S_E) to allow PWM duty cycles above 50% for a wide range of input/output voltages and inductor values. The slope compensation signal is added to the sum of the current sense amplifier output and the PWM ramp offset. As shown in the Electrical Characteristics table, the amount of slope compensation scales with the base switching frequency set by R_{FSET} (f_{OSC}). The amount of slope compensation does not change when the regulator is synchronized to an external clock.

The value of the output inductor should be chosen such that S_E is from 0.5× to 1× the falling slope of the inductor current (S_F).

Current Sense Amplifier

The ARG81801 incorporates a high-bandwidth current sense amplifier to monitor the current in the high-side MOSFET. This current signal is used by the PWM control circuitry to regulate the peak current. The current signal is also used by the protection circuitry to prevent damage to the ARG81801.

Power MOSFETs

The ARG81801 includes a 40 V, 110 mΩ high-side N-channel MOSFET, capable of delivering at least 3.0 A. The ARG81801 also includes a 10 Ω, low-side MOSFET to help ensure the BOOT capacitor is always charged. The typical $R_{DS(on)}$ increase versus temperature is shown in Figure 3.

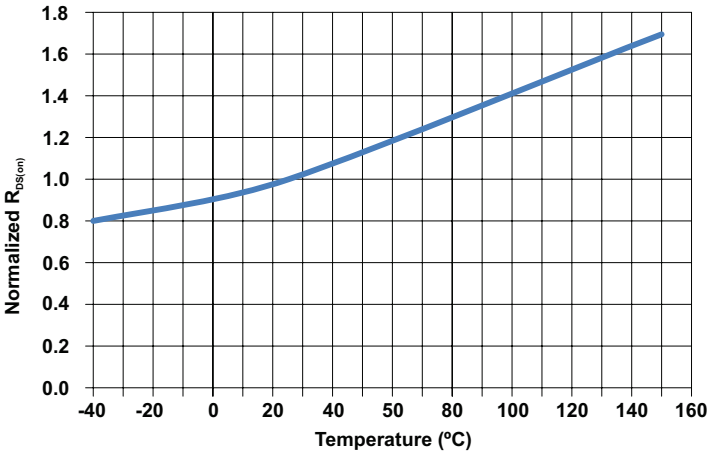


Figure 3: Typical MOSFET $R_{DS(on)}$ versus Temperature

BOOT Regulator

The ARG81801 contains a regulator to charge the boot capacitor. The voltage across the BOOT capacitor is typically 5.0 V. If the BOOT capacitor is missing, the ARG81801 detects a boot overvoltage. Similarly, if the BOOT capacitor is shorted, the ARG81801 detects a boot undervoltage. Also, the BOOT regulator has a current limit to protect itself during a short circuit condition. The details of how each type of boot fault is handled by the ARG81801 are summarized in Table 1 and shown in Figure 10.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pulse-Width Modulation (PWM)

The ARG81801 uses fixed-frequency, peak current mode control to provide excellent load and line regulation, fast transient response, and ease of compensation. A high-speed comparator and control logic, capable of typical pulse widths of 95 ns, are included in the ARG81801. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation, and a DC offset voltage ($V_{PWM(OFFS)}$, 400 mV_{TYP}).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop and the high-side MOSFET is turned on. When the summation of the DC offset, slope compensation, and current sense signal rises above the error amplifier voltage, the PWM flip-flop is reset and the high-side MOSFET is turned off. The PWM flip-flop is reset-dominant, so the error amplifier may override the CLK signal in certain situations. For example, at very light loads or extremely high input voltages, the error amplifier will reduce its output voltage below the 400 mV DC offset and the PWM flip-flop will ignore one or more of the incoming CLK pulses. The high-side MOSFET will not turn on, and the regulator will skip pulses to maintain output voltage regulation.

The ARG81801 includes a comprehensive set of protection circuits. See Figure 10 for a timing diagram showing how faults are handled. Also, the Protection Features section of this datasheet provides a detailed description of each fault and Table 1 presents a summary.

Soft Start (Startup) and Inrush Current Control

Inrush current is controlled by a soft start function. When the ARG81801 is enabled and all faults are cleared, the soft start pin will source $I_{SS(SU)}$ and the voltage on the soft start capacitor, C_{SS}, will ramp upward from 0 V. When the voltage at the soft start pin exceeds approximately 400 mV, the error amplifier will slew its output voltage above the PWM Ramp Offset ($V_{PWM(OFFS)}$). At that instant, the high-side and low-side MOSFETs will begin switching. As shown in Figure 4, there is a small delay ($t_{d(SS)}$) between when the enable pin transitions high, and when both the soft start voltage exceeds 400 mV and the error amplifier slews its output high enough to initiate PWM switching.

After the ARG81801 begins switching, the error amplifier will regulate the voltage at the FB pin to the soft start pin voltage minus approximately 400 mV. During the active portion of soft start, the voltage at the soft start pin rises from 400 mV to 1.2 V (a difference of 800 mV), the voltage at the FB pin rises from 0 V to 800 mV, and the regulator output voltage rises from 0 V to the targeted setpoint, which is determined by the feedback resistor divider on the FB pin.

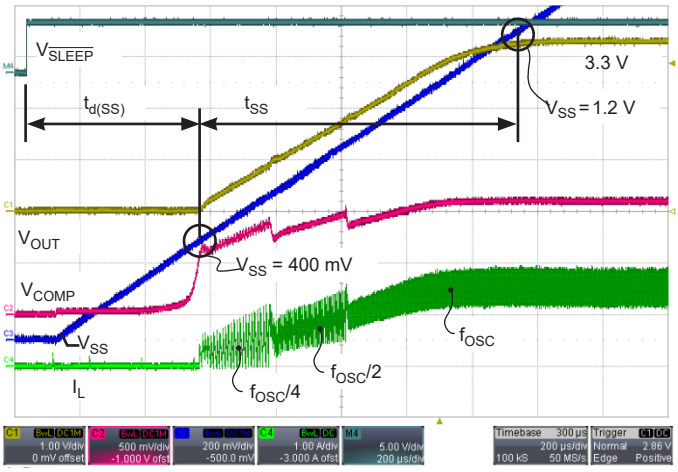


Figure 4: Normal Startup to V_{OUT} = 3.3 V, I_{OUT} = 1.6 A, $\overline{SLEEP}$ Transitions High

During startup, the PWM switching frequency is reduced to 25% of f_{OSC} while V_{FB} is below 200 mV. If V_{FB} is above 200 mV but below 400 mV, the switching frequency is reduced to 50% of f_{OSC}. Also, if V_{FB} is below 400 mV, the gm of the error amplifier is reduced to gm/2. When V_{FB} is above 400 mV the switching frequency will be f_{OSC} and the error amplifier gain will be gm. The reduced switching frequencies and error amplifier gain are necessary to help improve output regulation and stability when V_{OUT} is at a very low voltage. When V_{OUT} is very low, the PWM control loop requires on-times near the minimum controllable on-time, as well as extra-low duty cycles that are not possible at the base operating switching frequencies.

When the voltage at the soft start pin reaches approximately 1.2 V, the error amplifier will change mode and begin regulating the voltage at the FB pin to the ARG81801 internal reference, 800 mV. The voltage at the soft start pin will continue to rise to approximately V_{REG}. Complete soft start operation from V_{OUT} = 0 V is shown in Figure 4.

If the ARG81801 is disabled or a fault occurs, the internal fault latch will be set and the capacitor on the soft start pin will be discharged to ground very quickly by an 2 kΩ pull-down resistor. The ARG81801 will clear the internal fault latch when the voltage at the soft start pin decays to approximately 200 mV ($V_{SS(RST)}$). Conversely, if the ARG81801 enters hiccup mode, the capacitor on the soft start pin is slowly discharged by a current sink, $I_{SS(HIC)}$. Therefore, the soft start capacitor (C_{SS}) not only controls the startup time but also the time between soft start attempts in hiccup mode. Hiccup mode operation is discussed in more detail in the Protection Features section of this datasheet.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pre-Biased Startup

If the output of the regulator (V_{OUT}) is pre-biased to some voltage, the ARG81801 will modify the normal startup routine to prevent discharging the output capacitors. As described previously, the error amplifier usually becomes active when the voltage at the soft start pin exceeds 400 mV. If the output is pre-biased, the FB pin will be at some non-zero voltage. The ARG81801 will not start switching until the voltage at the soft start pin increases to approximately V_{FB} + 400 mV. When the soft start pin voltage exceeds this value, the error amplifier becomes active, the voltage at the COMP pin rises, PWM switching starts, and V_{OUT} ramps upward from the pre-bias level. Figure 5 shows startup when the output voltage is pre-biased to 1.6 V.

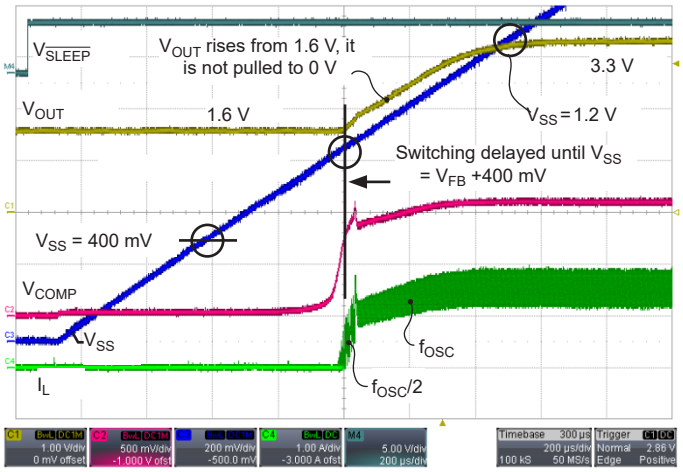


Figure 5: Pre-biased Startup from V_{OUT} = 1.6 V to V_{OUT} = 3.3 V, at I_{OUT} = 1.6 A

Power OK (POK) Output

The ARG81801 has a Power OK output (POK) with a fixed delay of its rising edge ($t_{d(POK)}$). The POK output is an open drain output so an external pull-up resistor must be used, as shown in the Typical Applications schematics. POK transitions high when the output voltage (V_{OUT}), sensed at the FB pin, is within regulation. POK is high when the output voltage is typically within 92.5% to 110% of the target value. The POK overvoltage and undervoltage comparators incorporate a small amount of hysteresis (10 mV typically) and filtering (5 µs typically) to help reduce chattering due to voltage ripple at the FB pin.

The POK output is immediately pulled low either: if an output overvoltage or an undervoltage condition occurs, or if the ARG81801 junction temperature exceeds the thermal shutdown threshold (T_{SD}). For other faults, POK behavior depends on the output voltage. Table 1 summarizes all the ARG81801 fault modes and their effect on POK.

At power-up, POK must be initialized (set to a logic low) when V_{IN} is relatively low. Figure 6 shows V_{IN} ramping up, and also POK being set to a logic low when V_{IN} is only 2.2 V. For this test, POK was pulled up to an external 3.3 V supply via a 2 kΩ resistor.

At power-down, POK must be held in the logic low state as long as possible. Figure 7 shows V_{IN} ramping down and also POK being held low until V_{IN} is only 1.3 V. For this test, POK was pulled up to an external 3.3 V supply via a 2 kΩ resistor.

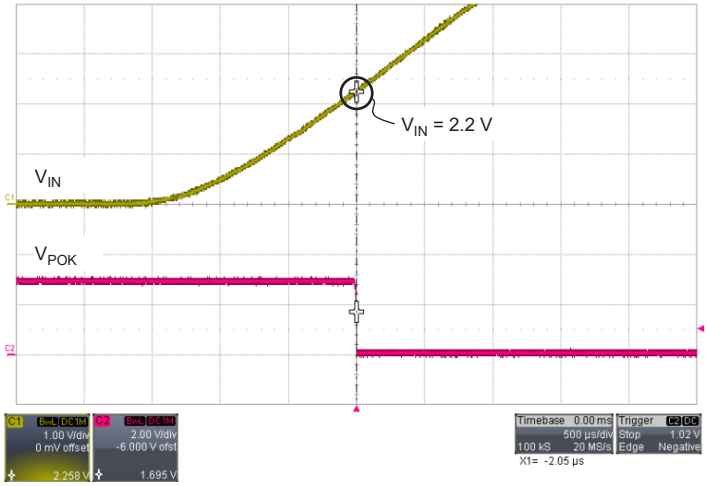


Figure 6: Initialization of POK as V_{IN} Ramps Up

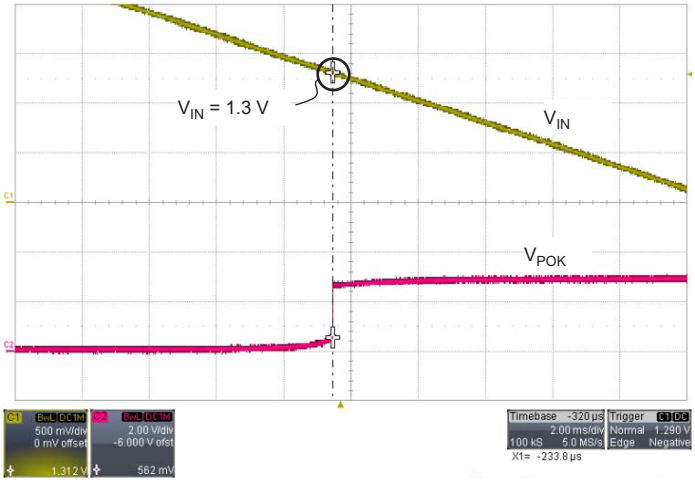


Figure 7: POK being Held Low as V_{IN} Ramps Down

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Protection Features

The ARG81801 was designed to satisfy the most demanding automotive and non-automotive applications. In this section, a description of each protection feature is described and Table 1 summarizes the protection features and operation.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the stop threshold ($V_{INUV(OFF)}$). The UVLO comparator incorporates some hysteresis ($V_{INUV(HYS)}$) to help reduce on-off cycling of the regulator due to resistive or inductive drops in the V_{IN} path during heavy loading or during startup.

PULSE-BY-PULSE OVERCURRENT PROTECTION (OCP)

The ARG81801 monitors the current in the high-side MOSFET and if the current exceeds the pulse-by-pulse overcurrent threshold (I_{LIM}) then the high-side MOSFET is turned off. Normal PWM operation resumes on the next clock pulse from the oscillator. The ARG81801 includes leading edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the high-side MOSFET is turned on.

Because of the addition of the slope compensation ramp to the inductor current, the ARG81801 delivers more current at lower duty cycles and less current at higher duty cycles. Also, the slope compensation is not a perfectly linear function of switching frequency. For a given duty cycle, this results in a little more current being available at lower switching frequencies than higher frequencies. Figure 8 shows the typical and worst case min/max pulse-by-pulse current limits versus duty cycle at f_{OSC} = 250 kHz and 2.45 MHz.

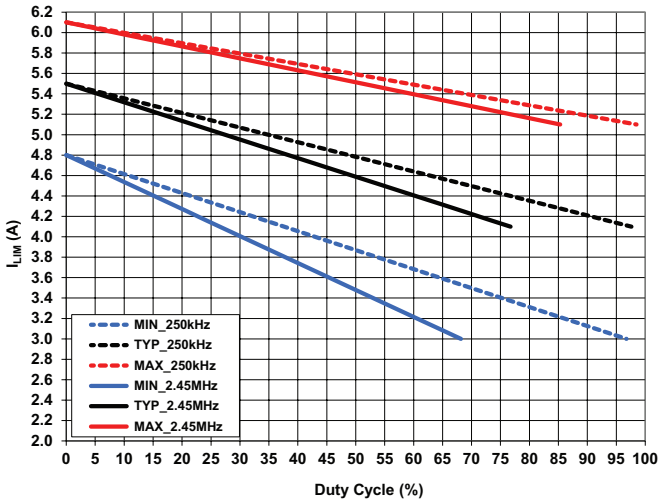


Figure 8: Pulse-by-Pulse Current Limit versus Duty Cycle

At f_{OSC} = 250 kHz (dashed lines) and f_{OSC} = 2.45 MHz (solid lines)

If the synchronization input (SYNC) is used to increase the switching frequency, the on-time and the current ripple will decrease. This will allow slightly more current than at the base switching frequency (f_{OSC}).

The exact current the buck regulators can support is heavily dependent on: duty cycle (V_{IN}, V_{OUT}, V_F), ambient temperature, thermal resistance of the PCB, airflow, component selection, and nearby heat sources.

OVERCURRENT PROTECTION (OCP) AND HICCUP MODE

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. When the voltage at the soft start pin is below the hiccup OCP threshold ($V_{HIC(EN)}$), the hiccup mode counter is disabled. Two conditions must be met for the OCP counter to be enabled and begin counting:

- $V_{SS} > V_{HIC(EN)}$ (2.3 V (typ)) and
- V_{COMP} is clamped at its maximum voltage (OCL = 1)

As long as these two conditions are met, the OCP counter remains enabled and will count pulses from the overcurrent comparator. If the COMP pin voltage decreases (OCL = 0) the OCP counter is cleared.

If the OCP counter reaches OCP_{LIM} counts (120), a hiccup latch is set and the COMP pin is quickly pulled down by a relatively low resistance (1 kΩ). The hiccup latch also enables a small current sink connected to the soft start pin ($I_{SS(HIC)}$). This causes the voltage at the soft start pin to slowly ramp downward. When the voltage at the soft start pin decays to a low enough level ($V_{SS(RST)}$, 200 mV (typ)), the hiccup latch is cleared and the small current sink turned off. At that instant, the soft start pin will begin to source current ($I_{SS(SU)}$) and the voltage at the soft start pin will ramp upward. This marks the beginning of a new, normal soft start cycle as described earlier. (Note: OCP is the only fault that results in hiccup mode that is ignored when V_{SS} < 2.3 V.)

When the voltage at the soft start pin exceeds the soft start offset (typically 400 mV), the error amplifier forces the voltage at the COMP pin to quickly slew upward and PWM switching will resume. If the short circuit at the regulator output remains, another hiccup cycle will occur. Hiccups will repeat until the short circuit is removed or the regulator is disabled. If the short circuit is removed, the ARG81801 will soft start normally and the output voltage will automatically recover to the target level, as shown in Figure 9.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

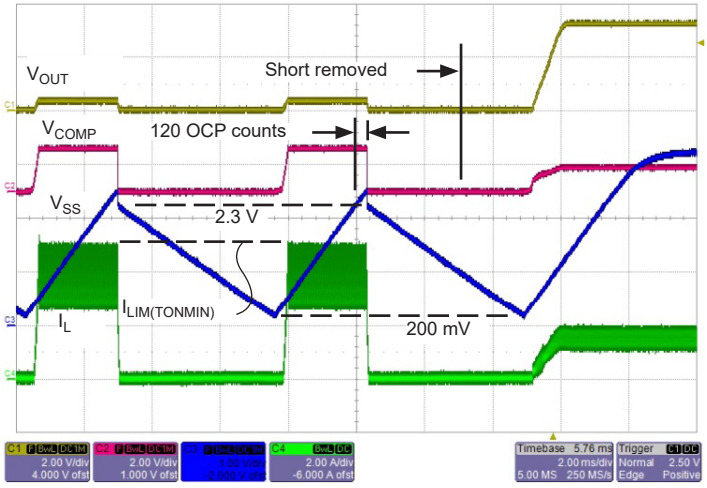


Figure 9: Hiccup Mode Operation and Recovery to V_{OUT} = 3.3 V, I_{OUT} = 1.6 A

BOOT CAPACITOR PROTECTION

The ARG81801 monitors the voltage across the BOOT capacitor to detect if the capacitor is missing or short-circuited. If the BOOT capacitor is missing, the regulator will enter hiccup mode after 7 PWM cycles. If the BOOT capacitor is short-circuited, the regulator will enter hiccup mode after 120 PWM cycles, provided there is no V_{OUT} overvoltage detection. At no load or very light loads, the boot charging circuit will increase the output voltage (via the output inductor) and cause an overvoltage condition to be detected if $V_{IN} > V_{OUT} + 5.7$ V.

For a boot fault, hiccup mode will operate virtually the same as described previously for an output short circuit fault (OCP) with the soft start pin ramping up and down as a timer to initiate repeated soft start attempts. Boot faults are a non-latched condition, so the ARG81801 will automatically recover when the fault is corrected.

ASYNCHRONOUS DIODE PROTECTION

If the asynchronous diode (D1 in the Typical Applications schematics) is missing or damaged (open), the SW pin will be subject to unusually high negative voltages. These negative voltages may cause the ARG81801 to malfunction and could lead to damage.

The ARG81801 includes protection circuitry to detect when the asynchronous diode is missing. If the SW pin is below typically −1.25 V for more than 50 ns, the ARG81801 will enter hiccup mode after detecting one missing diode fault. Also, if the asynchronous diode is short-circuited, the ARG81801 will experience extremely high currents in the high-side MOSFET. If this occurs, the ARG81801 will enter hiccup mode after detecting one short-circuited diode fault.

OVERVOLTAGE PROTECTION (OVP)

The ARG81801 provides a basic level of overvoltage protection by monitoring the voltage level at the FB pin. Two overvoltage conditions can be detected:

- The FB pin is disconnected from its feedback resistor divider. In this case, a tiny internal current source forces the voltage at the FB pin to rise. When the voltage at the FB pin exceeds the overvoltage threshold ($V_{OUT(OV)}$, 880 mV (typ)), PWM switching will stop and POK will be pulled low.
- A higher, external voltage supply is accidently shorted to the ARG81801's output. V_{FB} will probably rise above the overvoltage threshold and be detected as an overvoltage condition. In this case, the low-side MOSFET will continue to operate and can correct the OVP condition, provided that only a few milliamperes of pull-down current are required.

In either case, if the condition causing the overvoltage is corrected, the regulator will automatically recover.

PIN-TO-GROUND AND PIN-TO-PIN SHORT PROTECTIONS

The ARG81801 is designed to satisfy the most demanding automotive applications. For example, the ARG81801 has been carefully designed from the very beginning to withstand a short circuit to ground at each pin without suffering damage.

In addition, care was taken when defining the ARG81801 pin-out to optimize protection against pin-to-pin adjacent short circuits. For example, logic pins and high voltage pins are separated as much as possible. Inevitably, some low voltage pins are located adjacent to high voltage pins, but in these instances the low voltage pins are designed to withstand increased voltages, with clamps and/or series input resistance, to prevent damage to the ARG81801.

THERMAL SHUTDOWN (TSD)

The ARG81801 monitors junction temperature and will stop PWM switching and pull POK low if it becomes too hot. Also, to prepare for a restart, the soft start and COMP pins will be pulled low until $V_{SS} < V_{SS(RST)}$. TSD is a non-latched fault, so the ARG81801 will automatically recover if the junction temperature decreases by approximately 20°C.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 1: Summary of ARG81801 Fault Modes and Operation

Fault Mode	V_{SS}	During Fault Counting, before Hiccup Mode			BOOT Charging	POK State	Latched?	Reset Condition
		V_{COMP}	High-Side MOFSET	Low-Side MOFSET				
Output overcurrent, V_{FB}< 200 mV	Hiccup, after 120 OCP faults	Clamped for I_{LIM}, then pulled low for hiccup	f_{OSC} / 4 due to V_{FB} < 200 mV, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after remove the short
Output overcurrent, V_{FB} > 400 mV	Hiccup, after 120 OCP faults	Clamped for I_{LIM}, then pulled low for hiccup	f_{OSC} / 4 due to V_{FB} > 400 mV, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after decrease load current
Boot capacitor open/missing ($BOOT_{OV}$)	Hiccup, after 7 $BOOT_{OV}$ faults	Pulled low for hiccup	Forced off when $BOOT_{OV}$ fault occurs	Forced off when BOOT fault occurs	Off after BOOT fault occurs	Depends on V_{OUT}	No	Automatic, after replace capacitor
Boot capacitor shorted ($BOOT_{UV}$)	Hiccup, after 120 $BOOT_{UV}$ faults	Not affected, pulled low for hiccup	Forced off when $BOOT_{UV}$ fault occurs	Forced off only during hiccup	Off only during hiccup	Depends on V_{OUT}	No	Automatic, after unshort capacitor
Asynchronous diode missing	Hiccup after 1 fault	Pulled low for hiccup	Forced off after 1 fault	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after install diode
Asynchronous diode (or SW) hard short to ground	Hiccup after 1 fault	Pulled low for hiccup	Forced off after 1 fault	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after remove the short
Asynchronous diode (or SW) soft short to ground	Hiccup, after 120 OCP faults	Clamped for I_{LIM}, then pulled low for hiccup	Active, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Depends on V_{OUT}	No	Automatic, after remove the short
FB pin open (FB floats high)	Begins to ramp up for soft start	Transitions low via loop response	Forced off by low V_{COMP}	Active during $t_{OFF(MIN)}$	Off when V_{FB} is too high	Pulled low when V_{FB} is too high	No	Automatic, after connect FB pin
Output overvoltage (V_{FB} > 880 mV)	Not affected	Transitions low via loop response	Forced off by low V_{COMP}	Active during $t_{OFF(MIN)}$	Off when V_{FB} is too high	Pulled low when V_{FB} is too high	No	Automatic, after V_{FB} returns to normal range
Output undervoltage (V_{FB} < 740 mV)	Not affected	Transitions high via loop response	Active, responds to V_{COMP}	Can be activated if V_{BOOT} is too low	Not affected	Pulled low when V_{FB} is too low	No	Automatic, after V_{FB} returns to normal range
Thermal shutdown	Pulled low and latched until V_{SS} < $V_{SS(RST)}$	Pulled low and latched until V_{SS} < $V_{SS(RST)}$	Forced off by low V_{COMP}	Disabled	Off	Pulled low	No	Automatic, after part cools down

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

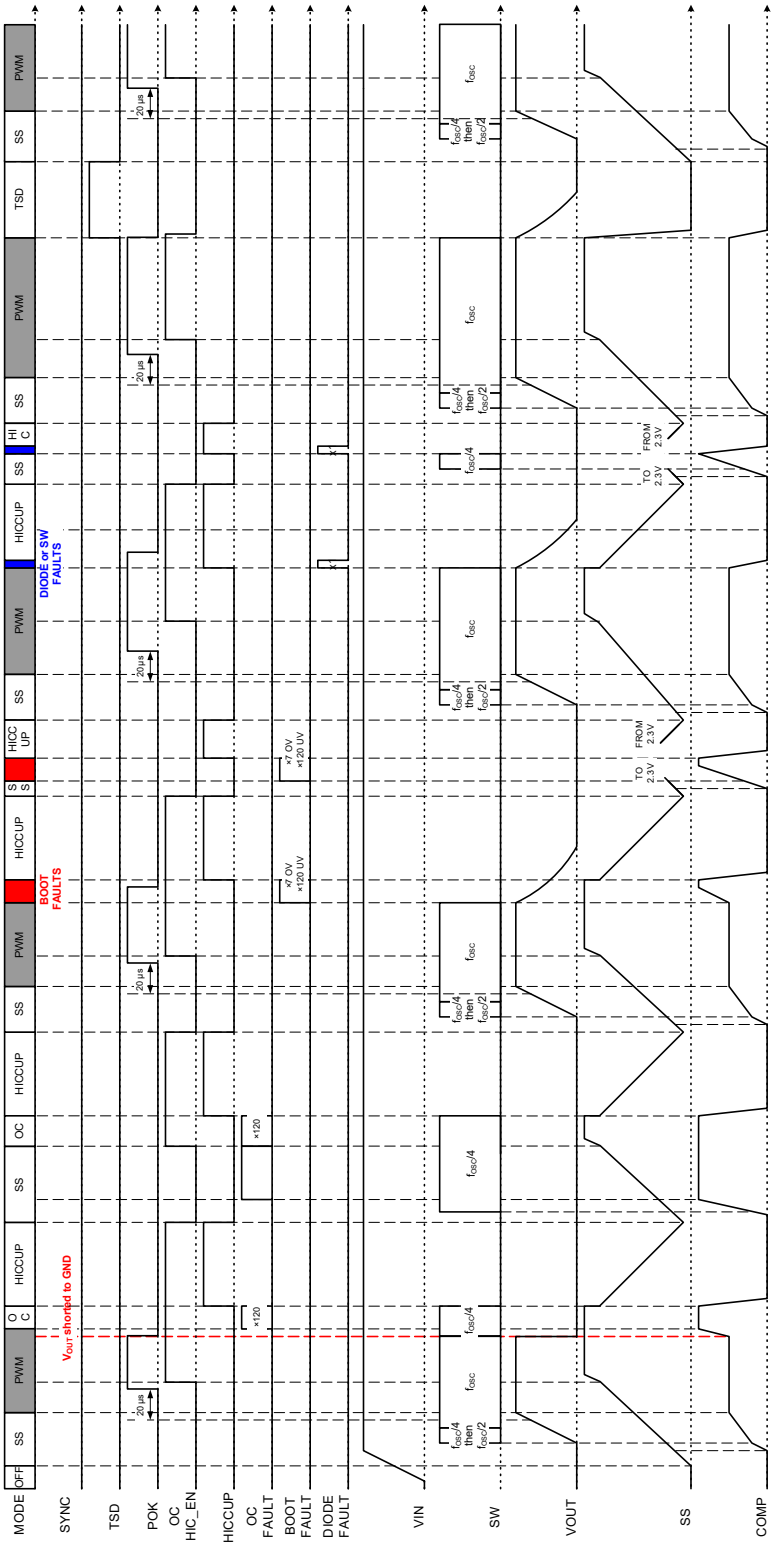


Figure 10: Operation with $\overline{\text{SLEEP}}$ = 1

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION INFORMATION

Design and Component Selection

SETTING THE OUTPUT VOLTAGE (V_{OUT})

The output voltage of the regulator is determined by connecting a resistor divider from the output node (V_{OUT}) to the FB pin as shown in Figure 11. If the parallel combination (R_{FB1} // R_{FB2}) is too high, then the regulator may be susceptible to noise coupling onto the FB pin. Allegro recommends a parallel combination in the range 1 to 4 kΩ.

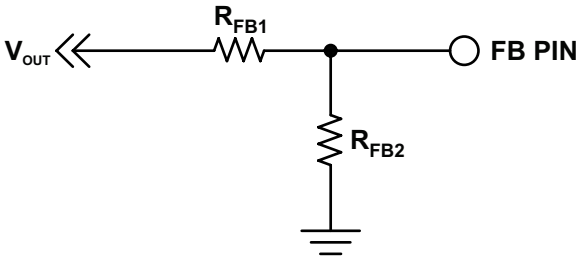


Figure 11: Connecting a Feedback Resistor Divider to Set the Output Voltage

The feedback resistors must satisfy the ratio shown in the following equation to produce the target output voltage, V_{OUT}:

$$\frac{R_{FB1}}{R_{FB2}} = \left(\frac{V_{OUT}}{0.8\ (V)} - 1\right) \quad (1)$$

PWM BASE SWITCHING FREQUENCY (f_{OSC}, R_{FSET})

The PWM base switching frequency, f_{OSC}, is set by connecting a resistor from the FSET pin to ground. Figure 12 is a graph showing the relationship between the typical switching frequency and the FSET resistor.

For a given base frequency (f_{OSC}), the FSET resistor can be calculated as follows:

$$R_{FSET} = \left(\frac{26385}{f_{OSC}} - 2.75\right) \quad (2)$$

where f_{OSC} is in kHz and R_{FSET} is in kΩ.

When the PWM base switching frequency is chosen, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$ of the ARG81801. If the system required on-time is less than the ARG81801 minimum controllable on-time, switch node jitter occurs and the output voltage will have increased ripple or oscillations.

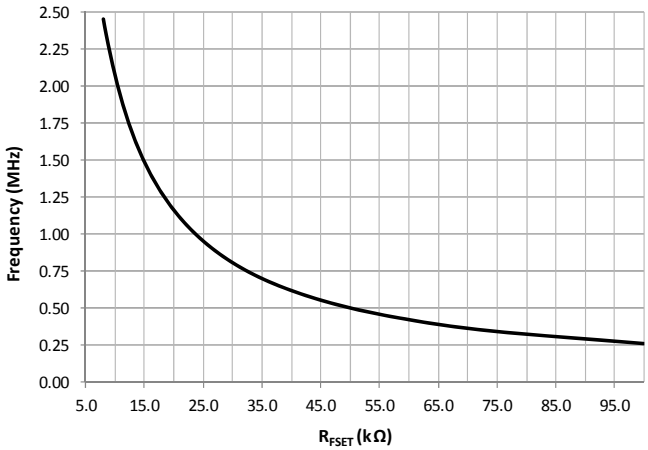


Figure 12: PWM Switching Frequency versus R_{FSET}

The PWM base switching frequency required should be calculated as follows:

$$f_{OSC} < \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \quad (3)$$

where

V_{OUT} is the output voltage,

$t_{ON(MIN)}$ is the minimum controllable on-time, and

$V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage, i.e. load dump voltage).

If the ARG81801 synchronization function is employed, then the base switching frequency should be chosen such that jitter will not result at the maximum synchronized switching frequency, determined from equation 4:

$$f_{OSC} < 0.66 \times \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}} \quad (4)$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OUTPUT INDUCTOR (L_O)

For a peak current mode regulator, it is common knowledge that without adequate slope compensation, the system will become unstable when the duty cycle is near or above 50%. However, the slope compensation in the ARG81801 is a fixed value (S_E). Therefore, it is important to calculate an inductor value such that the falling slope of the inductor current (S_F) will work well with the ARG81801 slope compensation. The following equation can be used to calculate a range of values for the output inductor based on the well-known approach of providing slope compensation that matches 50% to 100% of the falling slope of the inductor current:

$$\left(\frac{V_{OUT}+V_F}{2\times S_E}\right) \le L_O \le \left(\frac{V_{OUT}+V_F}{S_E}\right) \quad (5)$$

where V_F is the forward voltage of the asynchronous diode, and L_O is in µH.

In equation 5, the slope compensation (S_E) is a function of switching frequency according the following:

$$S_E = 0.253\times f^2_{OSC} + 0.726\times f_{OSC} + 0.021 \quad (6)$$

where S_E is in A/µs and f_{OSC} is in MHz.

More recently, Dr. Raymond Ridley presented a formula to calculate the amount of slope compensation required to critically damp the double poles at half the PWM switching frequency:

$$L_O \ge \frac{V_{OUT}+V_F}{S_E}\left(1-\frac{0.18}{D}\right) = \frac{V_{OUT}+V_F}{S_E}\left(1-0.18\times\frac{(V_{IN(MIN)}+V_F)}{V_{OUT}+V_F}\right) \quad (7)$$

This formula allows the inclusion of the duty cycle (D), which should be calculated at the minimum input voltage to ensure optimal stability. Also, to avoid dropout (that is, saturation of the buck regulator), $V_{IN(MIN)}$ must be approximately 1 to 1.5 V above V_{OUT} when calculating the inductor value.

If equations 5 or 7 yield an inductor value that is not a standard value, then the next highest available value should be used. The final inductor value should allow for 10% to 20% of initial tolerance and 20% to 30% of inductor saturation.

The saturation current of the inductor should be higher than the peak current capability of the ARG81801. Ideally, for output short circuit conditions, the inductor should not saturate given the highest pulse-by-pulse current limit at minimum duty cycle ($I_{LIM(TON,MIN)}$), 6.1 A_{MAX}. This may be too costly. At the very least, the inductor should not saturate at the peak operating current according to the following equation:

$$I_{PEAK} = 6.1 - \frac{S_E\times(V_{OUT}+V_F)}{1.15\times f_{OSC}\times(V_{IN(max)}+V_F)} \quad (8)$$

where $V_{IN(MAX)}$ is the maximum continuous input voltage, such as 18 V (not a surge voltage, such as 40 V).

Starting with equation 8, and subtracting half of the inductor ripple current, provides an interesting equation to predict the typical DC load capability of the regulator at a given duty cycle (D):

$$I_{OUT(DC)} = 6.1 - \frac{S_E\times D}{f_{OSC}} - \frac{V_{OUT}\times(1-D)}{2\times f_{OSC}\times L_O} \quad (9)$$

After an inductor is chosen, it should be tested during output short circuit conditions. The inductor current should be monitored using a current probe. A good design would ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

OUTPUT CAPACITORS

The output capacitors filter the output voltage to provide an acceptable level of ripple voltage and they store energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_{OUT}, ESR_{COUT}, and ESL_{COUT}:

$$\Delta V_{OUT} = \Delta I_L\times ESR_{COUT} + \frac{V_{IN}-V_{OUT}}{L_O}\times ESL_{COUT} + \frac{\Delta I_L}{8\times f_{SW}\times C_{OUT}} \quad (10)$$

The type of output capacitors will determine which terms of equation 10 are dominant. For ceramic output capacitors, the ESR_{COUT} and ESL_{COUT} are virtually zero, so the output voltage ripple will be dominated by the third term of equation 11:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8\times f_{SW}\times C_{OUT}} \quad (11)$$

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

To reduce the voltage ripple of a design using ceramic output capacitors, simply increase the total capacitance, reduce the inductor current ripple (that is, increase the inductor value), or increase the switching frequency.

For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in equation 10 will be very small. The output voltage ripple will be determined primarily by the first two terms of equation 10:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{COUT} \quad (12)$$

To reduce the voltage ripple of a design using electrolytic output capacitors, simply decrease the equivalent ESR_{CO} and ESL_{CO} by using a high(er) quality capacitor, or add more capacitors in parallel, or reduce the inductor current ripple (that is, increase the inductor value).

The ESR of some electrolytic capacitors can be quite high so Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambients, as much as 10×, which increases the output voltage ripple and, in most cases, reduces the stability of the system.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (di/dt), the output voltage will change by the amount:

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR_{COUT} + \frac{di}{dt} \times ESL_{COUT} \quad (13)$$

After the load transient occurs, the output voltage will deviate from its nominal value for a short time. This time will depend on the system bandwidth, the output inductor value, and output capacitance. Eventually, the error amplifier will bring the output voltage back to its nominal value.

The speed at which the error amplifier brings the output voltage back to its setpoint depends mainly on the closed-loop bandwidth of the system. A higher bandwidth usually results in a shorter time to return to the nominal voltage. However, with a higher bandwidth system, it may be more difficult to obtain acceptable gain and phase margins. Selection of the compensation components (R_Z, C_Z, and C_P) are discussed in more detail in the Compensation Components section of this datasheet.

INPUT CAPACITORS

Three factors should be considered when choosing the input capacitors. First, they must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor rms current rating must be higher than the expected rms input current to the regulator. Third, they must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to something much less than the hysteresis of the VIN pin UVLO circuitry ($V_{INUV(HYS)}$, nominally 400 mV for the ARG81801), at maximum loading and minimum input voltage.

The input capacitors must deliver the rms current according to:

$$I_{rms} = I_{OUT} \sqrt{D \times (1 - D)} \quad (14)$$

where the duty cycle is:

$$D \approx (V_{OUT} + V_F) / (V_{IN} + V_F) \quad (15)$$

and V_F is the forward voltage of the asynchronous diode, D1.

Figure 13 shows the normalized input capacitor rms current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 3.0 A of steady-state load current, the input capacitor(s) must support 0.40 × 3.0 A, or 1.2 A_{rms}.

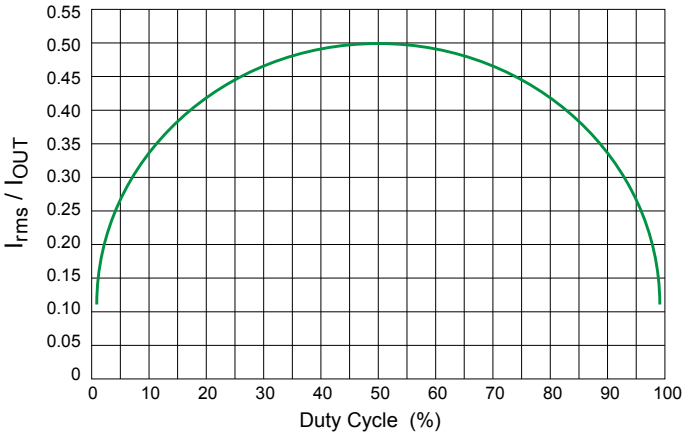


Figure 13: Input Capacitor Ripple versus Duty Cycle

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

The input capacitor(s) must limit the voltage deviations at the VIN pin to something significantly less than the ARG81801 UVLO hysteresis during maximum load and minimum input voltage. The minimum input capacitance can be calculated as follows:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1-D)}{0.85 \times f_{OSC} \times \Delta V_{IN(MIN)}} \quad (16)$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN pin UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended).

The D × (1-D) term in equation 16 has an absolute maximum value of 0.25 at 50% duty cycle. So, for example, a very conservative design, based on: I_{OUT} = 3.0 A, f_{OSC} = 85% of 425 kHz, D × (1-D) = 0.25, and ΔV_{IN} = 150 mV, yields:

$$C_{IN} \geq \frac{3.0\ (A) \times 0.25}{361\ (kHz) \times 150\ (mV)} = 13.8\ \mu F$$

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction) so these types should be avoided. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

For all ceramic capacitors, the DC bias effect is even more pronounced on smaller sizes of device case, so a good design uses the largest affordable case size (such as 1206 or 1210). Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst case transient input voltage (such as a load dump as high as 40 V for automotive applications).

ASYNCHRONOUS DIODE (D1)

There are three requirements for the asynchronous diode. First, the asynchronous diode must be able to withstand the regulator input voltage when the high-side MOSFET is on. Therefore, one should choose a diode with a reverse voltage rating (V_R) higher than the maximum expected input voltage (that is, the surge voltage).

Second, the forward voltage of the diode (V_F) should be minimized or the regulator efficiency suffers. Also if V_F is too high, the ARG81801 missing diode protection function could be falsely activated. A Schottky-type diode that can maintain a very low V_F when the regulator output is shorted to ground—at the coldest ambient temperature—is highly recommended.

Third, the asynchronous diode must conduct the output current when the high-side MOSFET is turned off. Therefore, the average forward current rating of this diode ($I_{F(AVG)}$) must be high enough to deliver the load current according to:

$$I_{F(AVG)} \geq I_{OUT(MAX)} \left(1 - D_{MIN} \right) \quad (17)$$

where $D_{MIN} = (V_{OUT} + V_F) / (V_{IN(MAX)} + V_F)$, $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage), and $I_{OUT(MAX)}$ is the maximum continuous ouput current of the regulator.

BOOTSTRAP CAPACITOR

A bootstrap capacitor must be connected between the BOOT and SW pins to provide the floating gate drive to the high-side MOSFET. Usually, 47 nF is an adequate value. This capacitor should be a high-quality ceramic capacitor, such as an X5R or X7R, with a voltage rating of at least 16 V.

The ARG81801 incorporates a 10 Ω low-side MOSFET to ensure that the bootstrap capacitor is always charged, even when the regulator is lightly loaded or pre-biased.

SOFT START AND HICCUP MODE TIMING (C_{SS})

The soft start time of the ARG81801 is determined by the value of the capacitance at the soft start pin, C_{SS}. When the ARG81801 is enabled, the voltage at the soft start pin starts from 0 V and is charged by the soft start current, $I_{SS(SU)}$. However, PWM switching does not begin instantly because the voltage at the soft start pin must rise above 400 mV. The soft start delay ($t_{d(SS)}$) can be calculated as:

$$t_{d(SS)} = C_{SS} \times \left(\frac{400\ (mV)}{I_{SS(SU)}} \right) \quad (18)$$

If the ARG81801 is starting with a very heavy load, a very fast soft start time may cause the regulator to exceed the pulse-by-pulse overcurrent threshold. This occurs because the total of the full load current, the inductor ripple current, and the additional current required to charge the output capacitors,

$$I_{CO} = C_{OUT} \times V_{OUT} / t_{SS} \quad (19)$$

is higher than the pulse-by-pulse current threshold, as shown in Figure 14. This phenomenon is more pronounced when using high value electrolytic-type output capacitors.

To avoid prematurely triggering hiccup mode, the soft start capacitor, C_{SS}, should be calculated according to:

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

$$C_{SS} \geq \frac{I_{SS(SU)} \times V_{OUT} \times C_{OUT}}{0.8\ (V) \times I_{CO}} \quad (20)$$

where V_{OUT} is the output voltage, C_{OUT} is the output capacitance, I_{CO} is the amount of current allowed to charge the output capacitance during soft start (recommended: 0.1 A < I_{CO} < 0.3 A). Higher values of I_{CO} result in faster soft start times. However, lower values of I_{CO} ensure that hiccup mode is not falsely triggered. Allegro recommends starting the design with an I_{CO} of 0.1 A and increasing it only if the soft start time is too slow. If a non-standard capacitor value for C_{SS} is calculated, the next larger value should be used.

The output voltage ramp time, t_{SS}, can be calculated by using either of the following methods:

$$t_{SS} = V_{OUT} \times \frac{C_{OUT}}{I_{CO}}$$

or

$$t_{SS} = 0.8\ (V) \times \frac{C_{SS}}{I_{SS(SU)}} \quad (21)$$

When the ARG81801 is in hiccup mode, the soft start capacitor is used as a timing capacitor and sets the hiccup period. The soft start pin charges the soft start capacitor with $I_{SS(SU)}$ during a startup attempt and discharges the same capacitor with $I_{SS(HIC)}$ between startup attempts. Because the ratio $I_{SS(SU)}$ / $I_{SS(HIC)}$ is approximately 4:1, the time between hiccups will be about four times as long as the startup time. Therefore, the effective duty cycle of the ARG81801 will be very low and the junction temperature will be kept low.

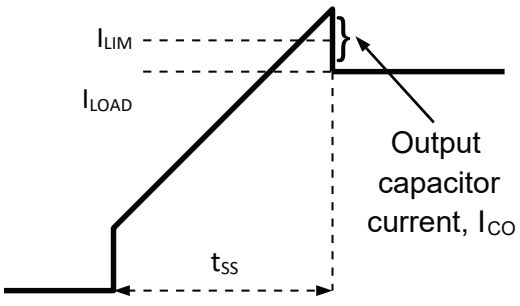


Figure 14: Output Capacitor Current (I_{CO}) During Startup

COMPENSATION COMPONENTS (R_Z, C_Z, AND C_P)

The ARG81801 employs current-mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero pair to control the characteristics of the control system. The DC voltage gain, A_{VDC}, of the complete feedback loop is given by:

$$A_{VDC} = R_L \times gm_{POWER} \times A_{VOL} \times \frac{V_{FB}}{V_{OUT}} \quad (22)$$

where R_L is the load resistance in Ω (V_{OUT}/I_{OUT}), gm_{POWER} is the COMP to SW current gain (4.0 A/V), and A_{VOL} is the error amplifier voltage gain (65 dB, or 1778 V/V).

The system has two noteworthy poles at low frequency. One is due to the compensation capacitor (C_Z) and the error amplifier output resistance, the other is due to the output capacitor (C_{OUT}) and the load resistance. These poles are located at:

$$f_{P1} = \frac{1}{2\pi \times C_Z \times R_O} = \frac{gm}{2\pi \times C_Z \times A_{VOL}} \quad (23)$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_L} \quad (24)$$

where gm is the error amplifier transconductance, 750 µA/V.

The system has one noteworthy zero. This is due to the compensation capacitor (C_Z) and the compensation resistor (R_Z). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times R_Z \times C_Z} \quad (25)$$

A third, high frequency pole is set by the compensation capacitor (C_P) and the compensation resistor (R_Z). This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C_P \times R_Z} \quad (26)$$

With ceramic output capacitors, f_{P3} should be set to limit the high frequency gain of the loop by placing a pole 5× to 10× higher than the 0 dB crossover frequency. Limiting the high frequency gain of the loop usually helps reduce pulse width jitter.

The goal of compensation design is to shape the converter transfer function to obtain a desired loop gain. The system crossover frequency (f_C) where the feedback loop has unity gain is important. Lower crossover frequencies result in slower load and line transient responses, while higher crossover frequencies could

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

cause the system to be unstable. A good rule of thumb is to set the crossover frequency of a 2 MHz regulator below 100 kHz. For a 400 kHz regulator, the crossover frequency should be set below 50 kHz.

The following procedure can be used to calculate the compensation components.

1. Calculate the compensation resistor (R_Z) to set the desired crossover frequency (f_C) using the following formula:

$$R_Z = \frac{2\pi \times C_{OUT} \times f_C}{gm \times gm_{POWER}} \times \frac{V_{OUT}}{V_{FB}} \quad (27)$$

2. Choose the compensation capacitor (C_Z) to achieve the desired phase margin. For most applications, setting the compensation zero (f_{Z1}) below one-fourth of the crossover frequency provides sufficient phase margin. Determine the C_Z value by the following equation:

$$C_Z \geq \frac{4}{2\pi \times R_Z \times f_C} \quad (28)$$

To maximize stability (that is, to have the greatest phase margin), use a higher value of C_Z. To optimize transient recovery time, although at the expense of some phase margin, use a lower value of C_Z.

Figure 15 compares the output voltage recovery time due to a 1 A load transient for a system with f_{Z2} at 4.5 kHz with 63° phase margin versus 15 kHz with 51° phase margin. The system with the higher frequency zero has less phase margin but recovers about 3 times faster than the other system.

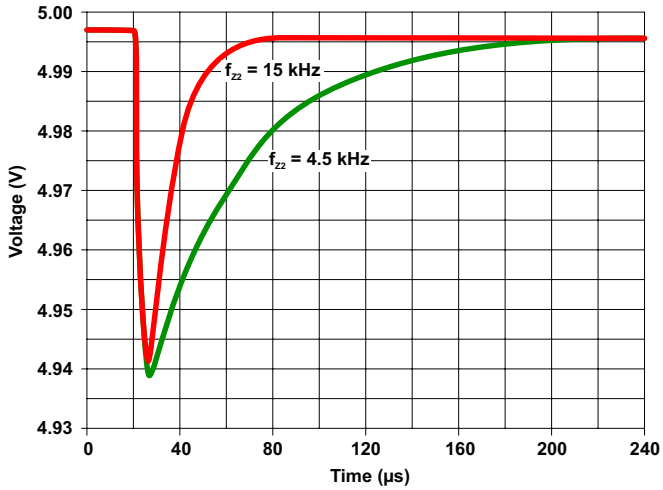


Figure 15: Transient Recovery Comparison

3. Lastly, set the high frequency pole at 5 × f_C using the following equation:

$$C_P = \frac{1}{2\pi \times R_Z \times 5 \times f_C} \quad (29)$$

This should be a good starting value for C_P. Decreasing C_P will improve phase margin slightly, but may result in increased pulse width jitter.

Table 2 lists typical values of compensation components for a high frequency, high output voltage and a low frequency, low output voltage design with recommended output ceramic capacitors and inductors. The output capacitances and bandwidths were chosen to support 0.5 to 3 A load transients at approximately 125 mA/µs. As shown in Figure 16a and Figure 16b, the output voltage deviates about ±4% during the load transients and fully recovers in less than 65 µs. For reduced load transients, the output capacitance can be decreased, but the compensation components must be recalculated to maintain good stability margins.

Table 2: Typical Component Values for 2.5 A Load Steps

V_{OUT} / f_{OSC} (V / kHz)	L_{OUT} (µH)	C_{OUT} (µF)	R_Z (kΩ)	C_Z (nF)	C_P (pF)
5.0 / 2100	3.3	20	20	1.0	15
1.25 / 410	10	188	30.1	0.68	15

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

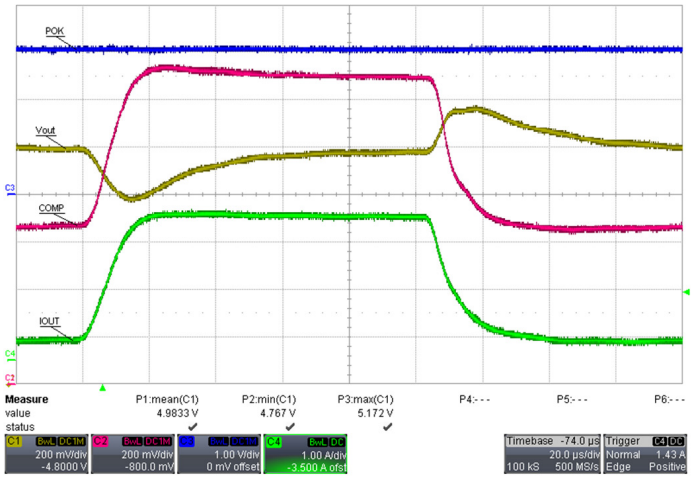


Figure 16a: 0.5 to 3 A Load Transient – 12 V_{IN}, 5 V_{OUT}, 2.1 MHz

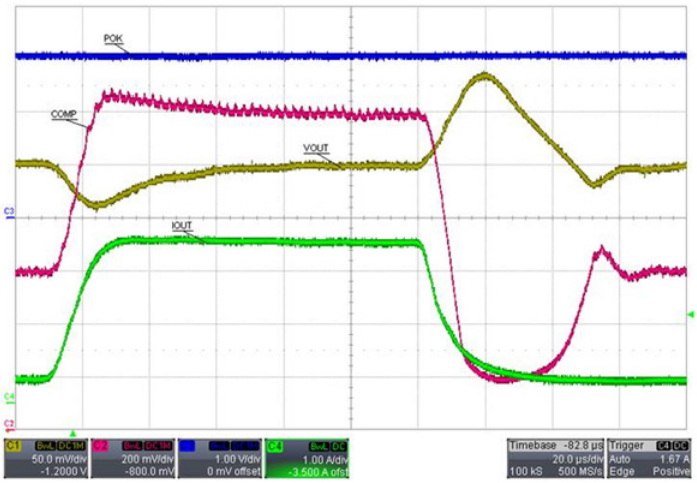


Figure 16b: 0.5 to 3 A Transient – 12 V_{IN}, 1.25 V_{OUT}, 410 kHz

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

POWER DISSIPATION AND THERMAL CALCULATIONS

The power dissipated in the ARG81801 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SW}), the power dissipated due to the rms current being conducted by the internal MOSFET (P_{COND}), and the power dissipated by the internal gate driver ($P_{DRIVERS}$).

The power dissipated from the V_{IN} supply current can be calculated using equation 30, where V_{IN} is the input voltage, I_Q is the input quiesent current drawn by the ARG81801 (nominally 2.5 mA), V_{GS} is the MOSFET gate drive voltage (typically 5 V), Q_G is the internal MOSFET gate charge (approximately 2.5 nC), and f_{OSC} is the PWM switching frequency.

$$P_{IN} = V_{IN} \times I_Q + (V_{IN} - V_{GS}) \times Q_G \times f_{OSC} \qquad (30)$$

The power dissipated by the internal high-side MOSFET during PWM switching can be calculated using Equation 31, where V_{IN} is the input voltage, I_{OUT} is the regulator output current, f_{OSC} is the PWM switching frequency, and t_r and t_f are the rise and fall times measured at the SW node. The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load. Approximate values for both t_r and t_f range from 5 to 10 ns.

$$P_{SW} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2} \qquad (31)$$

The power dissipated by the internal high-side MOSFET while it is conducting can be calculated using equation 32, where I_{OUT} is the regulator output current, ΔI_L is the peak-to-peak inductor ripple current, $R_{DS(on)}$ is the on resistance of the high-side MOSFET, and V_F is the forward voltage of the asynchronous diode,

$$P_{COND} = I_{rms(FET)}^2 \times R_{DS(on)} = \left(\frac{V_{OUT}+V_F}{V_{IN}+V_F}\right) \times \left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right) \times R_{DS(on)} \qquad (32)$$

The $R_{DS(on)}$ of the high-side MOSFET will have some initial tolerance plus an increase from self-heating and elevated ambient temperatures. A conservative design should accommodate an $R_{DS(on)}$ with at least a 15% initial tolerance plus 0.39%/°C increase due to temperature.

The power dissipated by the internal gate driver can be calculated using equation 33, where V_{GS} is the gate drive voltage (typically 5 V), Q_G is the gate charge to drive the internal MOSFET to V_{GS} = 5 V (about 2.5 nC), and f_{OSC} is the PWM switching frequency:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_{OSC} \qquad (33)$$

Finally, the total power dissipated by the ARG81801 (P_{TOTAL}) is the sum of the previous equations,

$$P_{TOTAL} = P_{IN} + P_{SW} + P_{COND} + P_{DRIVER} \qquad (34)$$

The average junction temperature can be calculated with the equation 35, where P_{TOTAL} is the total power dissipated from equation 34, $R_{\theta JA}$ is the junction-to-ambient thermal resistance (37°C/W on a 4-layer PCB), and T_A is the ambient temperature,

$$T_J = P_{TOTAL} + R_{\theta JA} + T_A \qquad (35)$$

The maximum junction temperature will be dependent on how efficiently heat can be transferred from the PCB to ambient air. It is critical that the thermal pad on the bottom of the IC should be connected to a at least one ground plane using multiple vias.

As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow will reduce the junction temperature considerably.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PCB COMPONENT PLACEMENT AND ROUTING

A good PCB layout is critical if the ARG81801 is to provide clean, stable output voltages. Follow these guidelines to insure a good PCB layout. Figure 17 shows a typical buck converter schematic with the critical power paths/loops. Figure 18 shows an example PCB component placement and routing with the same critical power paths/loops as shown in the schematic.

1. By far, the highest di/dt in the asynchronous buck regulator occurs at the instant the high-side MOSFET turns on and the capacitance of the asynchronous Schottky diode is quickly charged to V_{IN}. The ceramic input capacitors must deliver this fast, short pulse of current. Therefore the loop, from the ceramic input capacitors through the high-side MOSFET and into the asynchronous diode to ground, must be minimized. Ideally these components are all connected using only the top metal layer (that is, do not use vias to other power/signal layers).
2. When the upper FET is off, free-wheeling current flows from ground, through the asynchronous diode, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.
3. When the high-side MOSFET is on, current flows from the input supply and capacitors, through the high-side MOSFET, into the load via the output inductor, and back to ground. This loop should be minimized and have relatively wide traces.
4. The voltage on the SW node transitions from 0 V to V_{IN} very quickly and is the root cause of many noise issues. It is best to place the asynchronous diode and output inductor close to the ARG81801 to minimize the size of the SW polygon. Also, keep low-level analog signals (like FB and COMP) away from the SW polygon.
5. Place the feedback resistor divider (R_{FB1} and R_{FB2}) very close to the FB pin. Ground this resistor divider as close as possible to the ARG81801.
6. To have the highest output voltage accuracy, the output voltage sense trace (from V_{OUT} to R_{FB1}) should be connected as close as possible to the load.
7. Place the compensation components (R_Z, C_Z, and C_P) as close as possible to the COMP pin. Place vias to the GND plane as close as possible to these components.
8. Place the bootstrap capacitor (CBOOT) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible.
9. When connecting the input and output ceramic capacitors, use multiple vias to GND and place the vias as close as possible to the pads of the components.
10. To minimize PCB losses and improve system efficiency, the input and output traces should be as wide as possible and be duplicated on multiple layers, if possible.
11. The thermal pad under the ARG81801 must connect to the GND plane using multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.
12. EMI/EMC issues are always a concern. Allegro strongly recommends having component locations for an RC snubber from SW to ground. The resistor should be 1206 size and connect directly to the ground plane to aid thermal dissipation.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

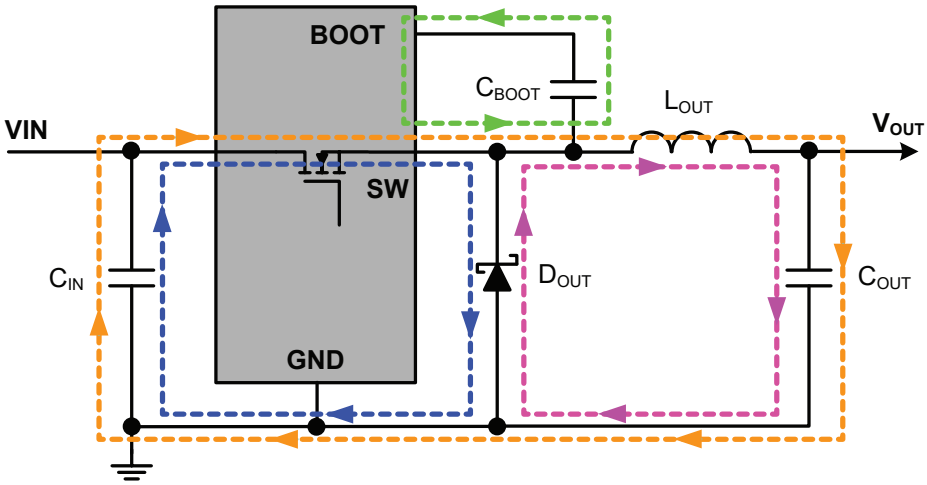


Figure 17: Buck Regulator Circuit with Critical Paths/Loops Shown

"Hot Loop" (Blue): To minimize radiated emissions (RE), the loop area from C_{IN}, through the high-side MOSFET (M1), asynchronous diode (D_{OUT}), to ground directly at C_{IN} must be minimized. These components should be placed on the same side of the PCB—this loop should not use vias to make the connections.

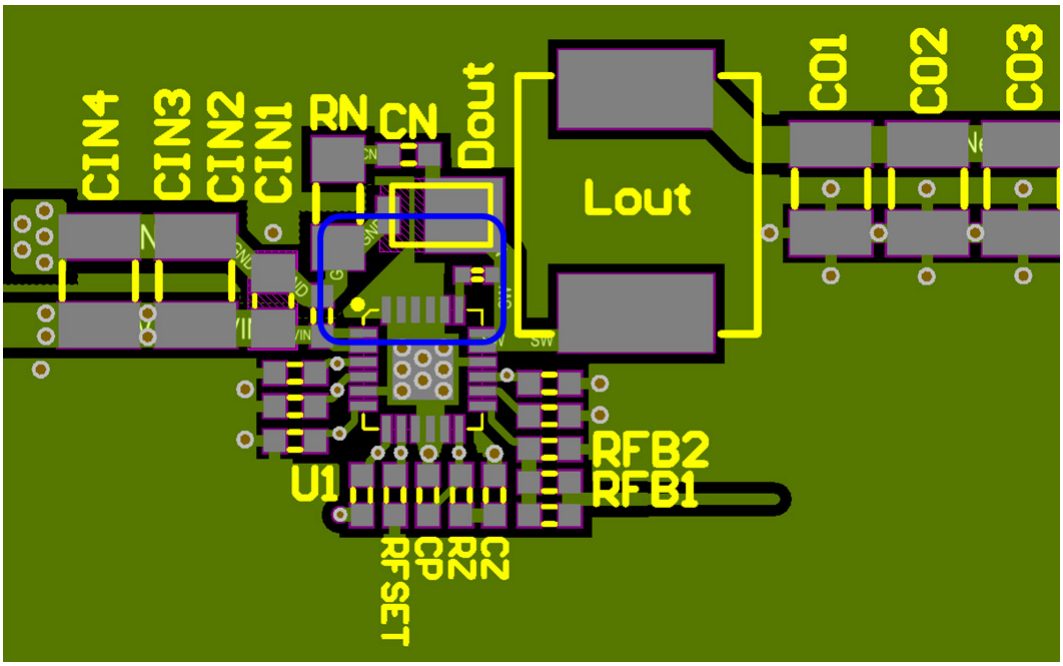


Figure 18: Recommended Component Placement and Routing

The area of the Hot Loop, shown in blue, must be minimized.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-220WGGD)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

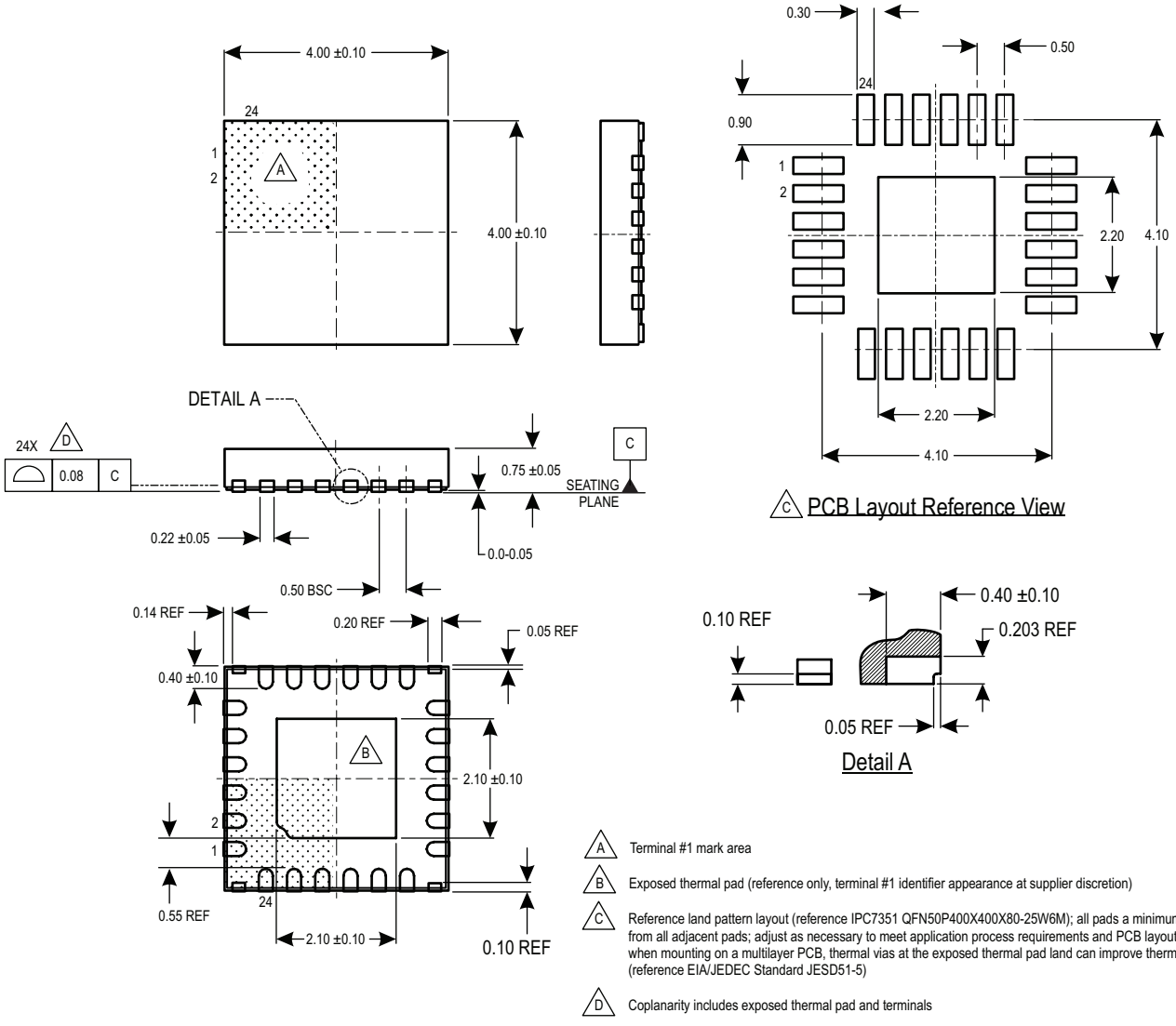


Figure 19: Package ES, 24-pin wettable flank QFN with exposed thermal pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	February 2, 2018	Initial release
1	March 20, 2018	Minor editorial updates
2	February 11, 2019	Minor editorial updates
3	February 20, 2020	Minor editorial updates

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com