SILEGO

APL Power Sequencer

General Description

Silego SLG7NT4850 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

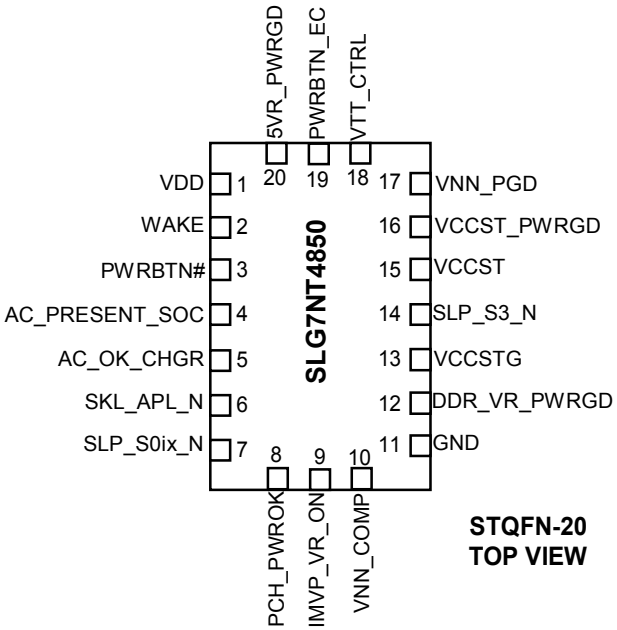
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

- 8 Outputs — Open Drain NMOS 1X

Pin Configuration



STQFN-20
TOP VIEW

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	WAKE	Digital Input	Digital Input without Schmitt trigger
3	PWRBTN#	Digital Input	Digital Input with Schmitt trigger
4	AC_PRESENT_SOC	Digital Output	Open Drain NMOS 1X
5	AC_OK_CHGR	Digital Input	Digital Input without Schmitt trigger
6	SKL_APL_N	Analog Input/Output	Analog Input/Output
7	SLP_S0ix_N	Digital Input	Low Voltage Digital Input
8	PCH_PWROK	Digital Output	Open Drain NMOS 1X
9	IMVP_VR_ON	Digital Output	Open Drain NMOS 1X
10	VNN_COMP	Analog Input/Output	Analog Input/Output
11	GND	GND	Ground
12	DDR_VR_PWRGD	Digital Input	Low Voltage Digital Input
13	VCCSTG	Analog Input/Output	Analog Input/Output
14	SLP_S3_N	Digital Input	Low Voltage Digital Input
15	VCCST	Analog Input/Output	Analog Input/Output
16	VCCST_PWRGD	Digital Output	Open Drain NMOS 1X
17	VNN_PGD	Digital Output	Open Drain NMOS 1X
18	VTT_CTRL	Digital Output	Open Drain NMOS 1X
19	PWRBTN_EC	Digital Output	Open Drain NMOS 1X
20	5VR_PWRGD	Digital Output	Open Drain NMOS 1X

Ordering Information

Part Number	Package Type
SLG7NT4850V	V=STQFN-20
SLG7NT4850VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

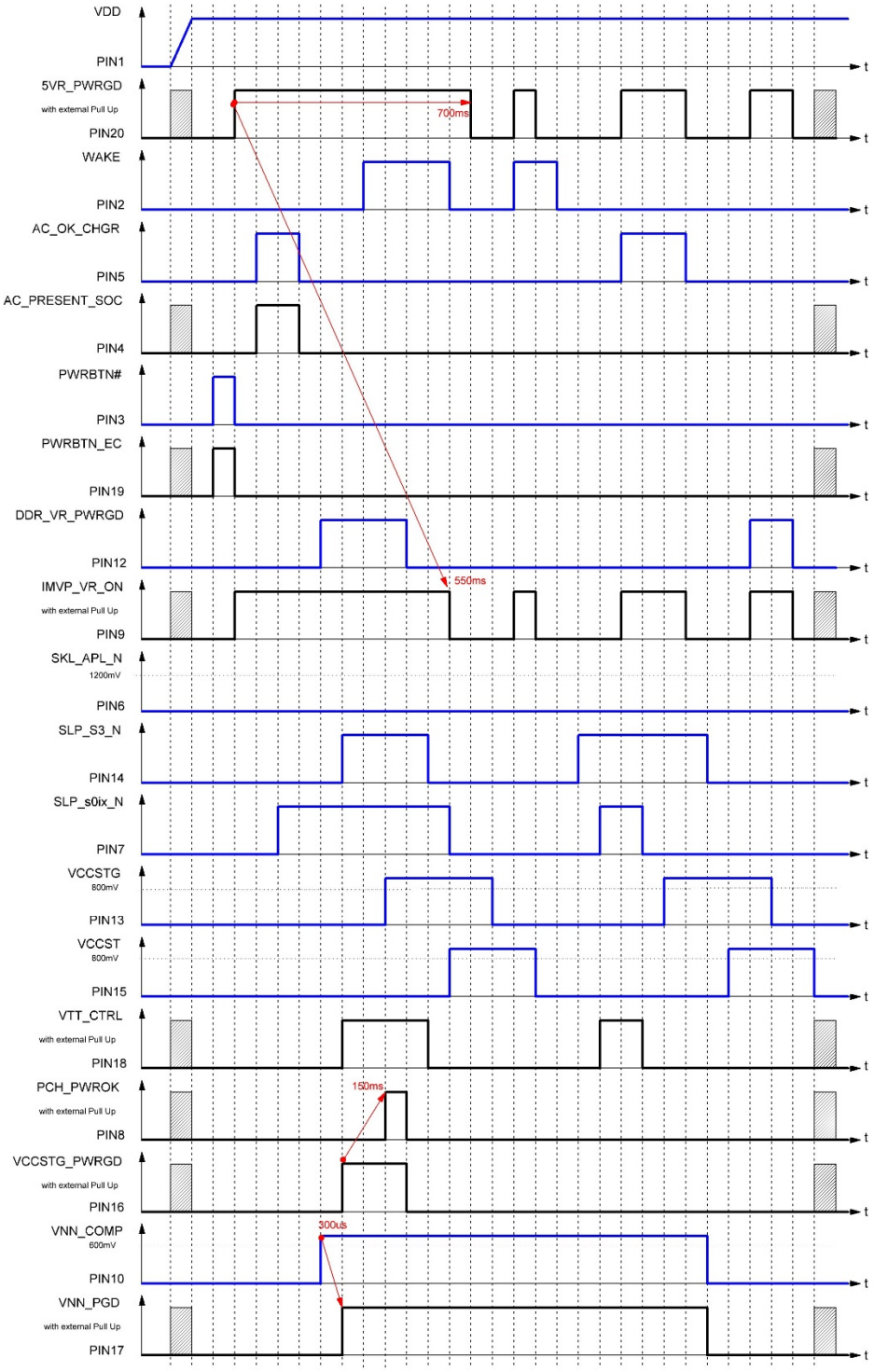
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.659	3.3	5.665	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs @VDD=5.665V	--	80	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.10	--	VDD	V
		Logic Input with Schmitt Trigger, at VDD=1.8V	1.27	--	VDD	
		Low-Level Logic Input, at VDD=1.8V	0.98	--	VDD	
		Logic Input, at VDD=3.3V	1.78	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=3.3V	2.13	--	VDD	
		Low-Level Logic Input, at VDD=3.3V	1.13	--	VDD	
		Logic Input, at VDD=5.0V	2.64	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=5.0V	3.16	--	VDD	
		Low-Level Logic Input, at VDD=5.0V	1.23	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	--	--	0.69	V
		Logic Input with Schmitt Trigger, at VDD=1.8V	--	--	0.44	
		Low-Level Logic Input, at VDD=1.8V	--	--	0.52	
		Logic Input, at VDD=3.3V	--	--	1.21	
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.95	
		Low-Level Logic Input, at VDD=3.3V	--	--	0.69	
		Logic Input, at VDD=5.0V	--	--	1.84	

		Logic Input with Schmitt Trigger, at VDD=5.0V	--	--	1.51	
		Low-Level Logic Input, at VDD=5.0V	--	--	0.78	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OL}	LOW-Level Output Voltage	Open Drain, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	0.005	0.020	V
		Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.080	0.147	
		Open Drain, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.102	0.180	
I_{OL}	LOW-Level Output Current	Open Drain, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V	1.375	2.534	--	mA
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	7.313	12.37	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V	10.82	17.38	--	
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis.	1034	--	1342	mV
V_{ACMP1}	Analog Comparator Threshold Voltage	ACMP1 threshold including input offset, reference voltage variation and hysteresis.	522	--	682	mV
V_{ACMP2}	Analog Comparator Threshold Voltage	ACMP2 threshold including input offset, reference voltage variation and hysteresis.	735	--	848	mV
V_{ACMP3}	Analog Comparator Threshold Voltage	ACMP3 threshold including input offset, reference voltage variation and hysteresis.	735	--	848	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (note 1)	ACMP 2, 3	--	25	--	mV
		ACMP 1	--	50	--	
T_{DLY0}	Delay0 Time	At temperature 25°C	135.47	150.02	156.73	ms
		At temperature -40°C +85°C (note 1)	122.72	150.02	185.55	
T_{DLY1}	Delay1 Time	At temperature 25°C	632.22	700.08	731.32	ms
		At temperature -40°C +85°C (note 1)	572.74	700.08	865.85	
T_{DLY4}	Delay4 Time	At temperature 25°C	497.1	551.68	577.57	ms
		At temperature -40°C +85°C (note 1)	450.34	551.68	683.82	
T_{DLY5}	Delay5 Time	At temperature 25°C	252.88	300	334.25	µs
		At temperature -40°C +85°C (note 1)	229.09	300	395.73	
T_{SU}	Start up Time	From VDD rising past 1.35V	--	0.3	--	ms

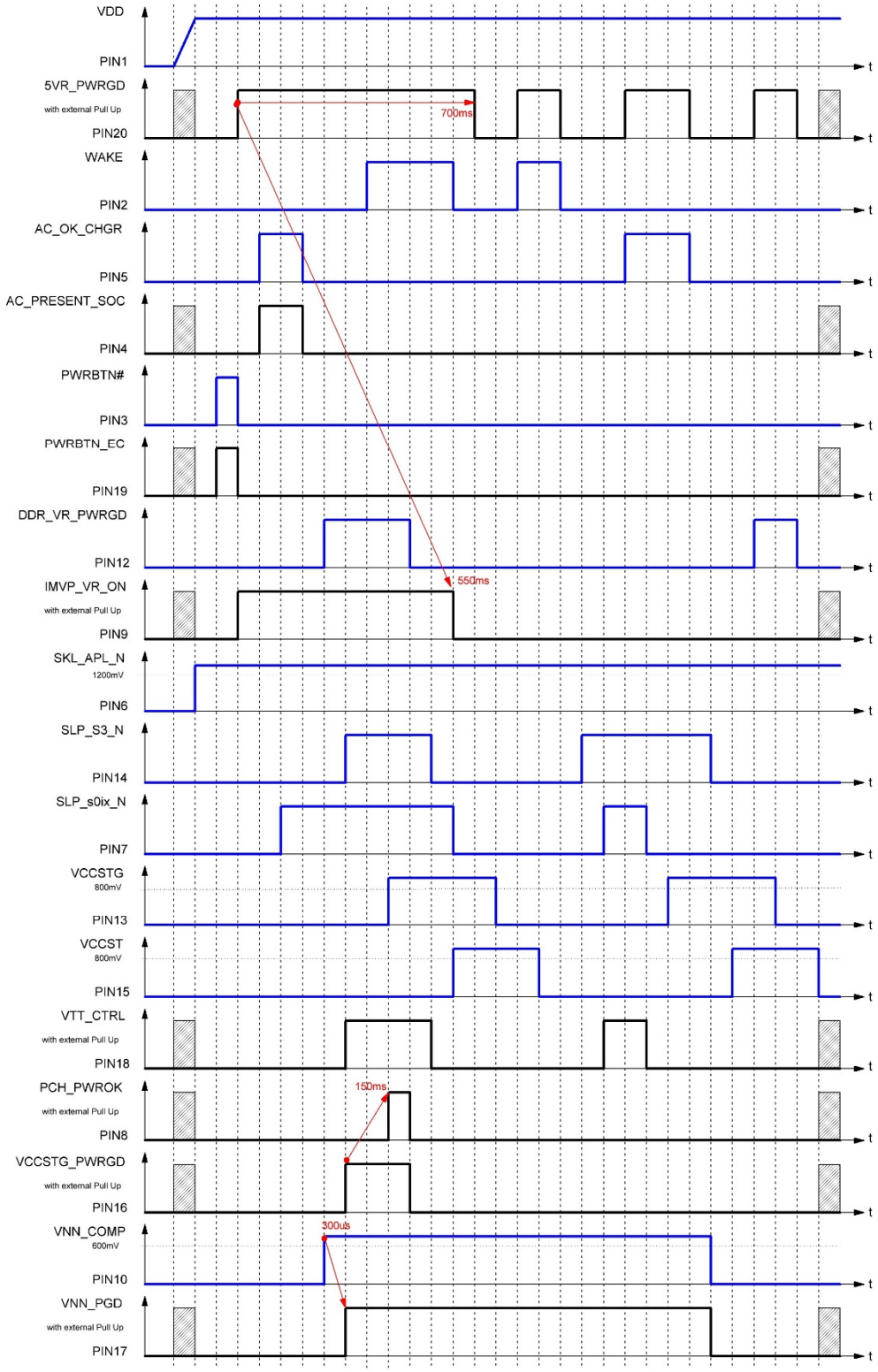
1. Guaranteed by Design.

Timing Diagram

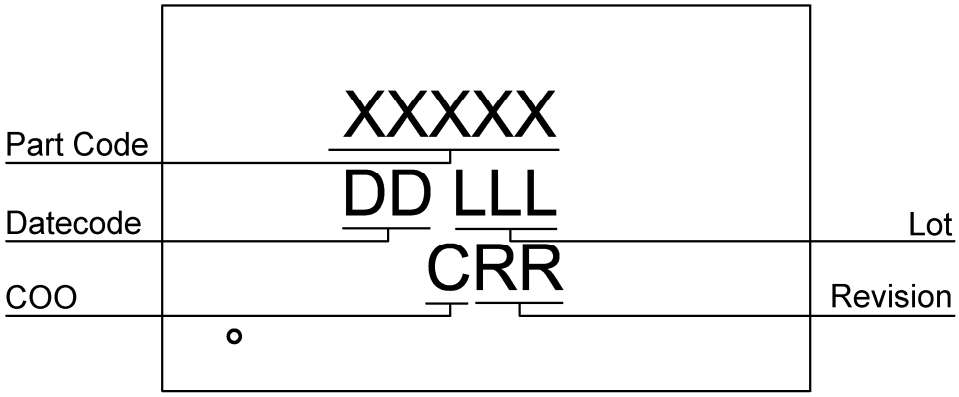
1. Case 1: PIN#6(SKL_APL_N) - LOW



2. Case 2: PIN#6(SKL_APL_N) - HIGH



Package Top Marking



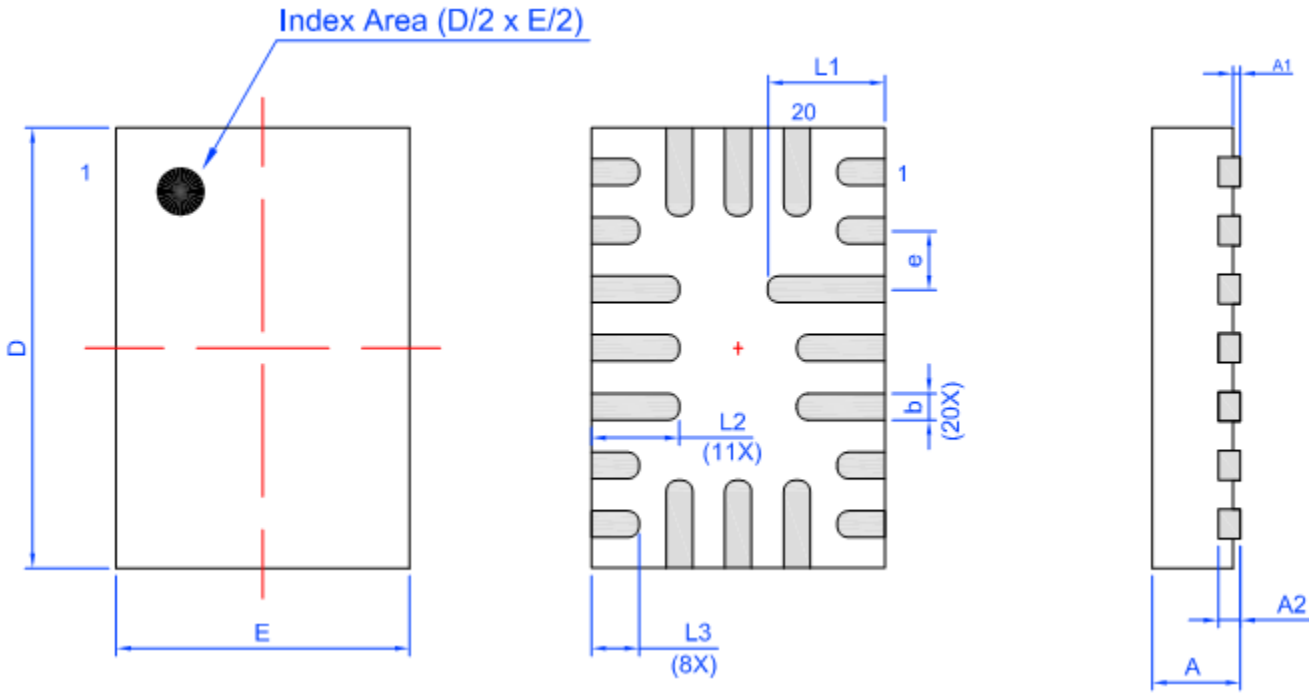
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.02	003	U	4850V	AA	03/11/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

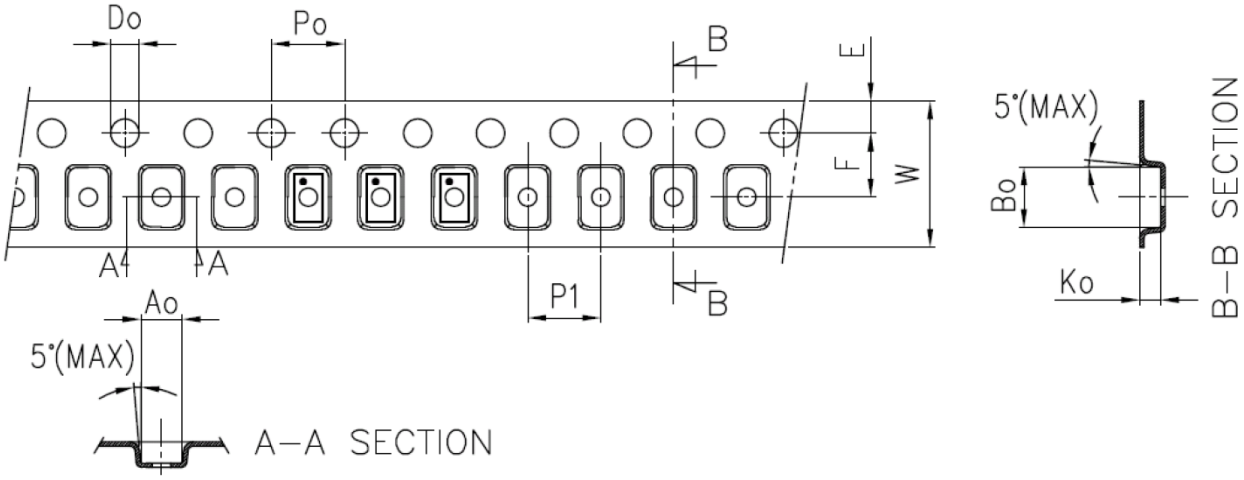
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal). More information can be found at www.jedec.org.

Silego Website & Support

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Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

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