

**ULTRA-SMALL PACKAGE HIGH-PRECISION VOLTAGE DETECTOR
WITH DELAY CIRCUIT (INTERNAL DELAY TIME SETTING)**www.ablic.com

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Rev.4.2_01

The S-801 Series is a series of high-precision voltage detectors with a built-in delay time generator of fixed time developed using CMOS process. The detection voltage is fixed internally, with an accuracy of $\pm 2.0\%$. Internal oscillator and counter timer can delay the release signal without external parts. Three delay times 50 ms, 100 ms, and 200 ms are available. Two output forms, Nch open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption 1.3 μA typ. (at $V_{\text{DD}}=3.5\text{ V}$)
- High-precision detection voltage $\pm 2.0\%$
- Operating voltage range 0.95 V to 10.0 V
- Hysteresis characteristics 60 mV typ.
- Detection voltage 2.2 V to 6.0 V (0.1 V step)
- Three delay times
 - A type 50 ms typ.
 - B type 100 ms typ.
 - C type 200 ms typ.
- ON/OFF switching function of delay time (DS pin)
- Output forms
 - Nch open-drain output (Active Low)
 - CMOS output (Active Low)
- Lead-free, Sn 100%, halogen-free*1

*1. Refer to “**■ Product Name Structure**” for details.

■ Applications

- Power monitor for portable equipment such as notebook computers, digital still cameras, PDA, and cellular phones.
- Constant voltage power monitor for cameras, video equipment and communication devices.
- Power monitor for microcomputers and reset for CPUs.

■ Packages

- SOT-23-5
- SNT-4A

■ **Block Diagrams**

1. Nch Open-drain Output Products



*1. Parasitic diode

Figure 1

2. CMOS Output Products



*1. Parasitic diode

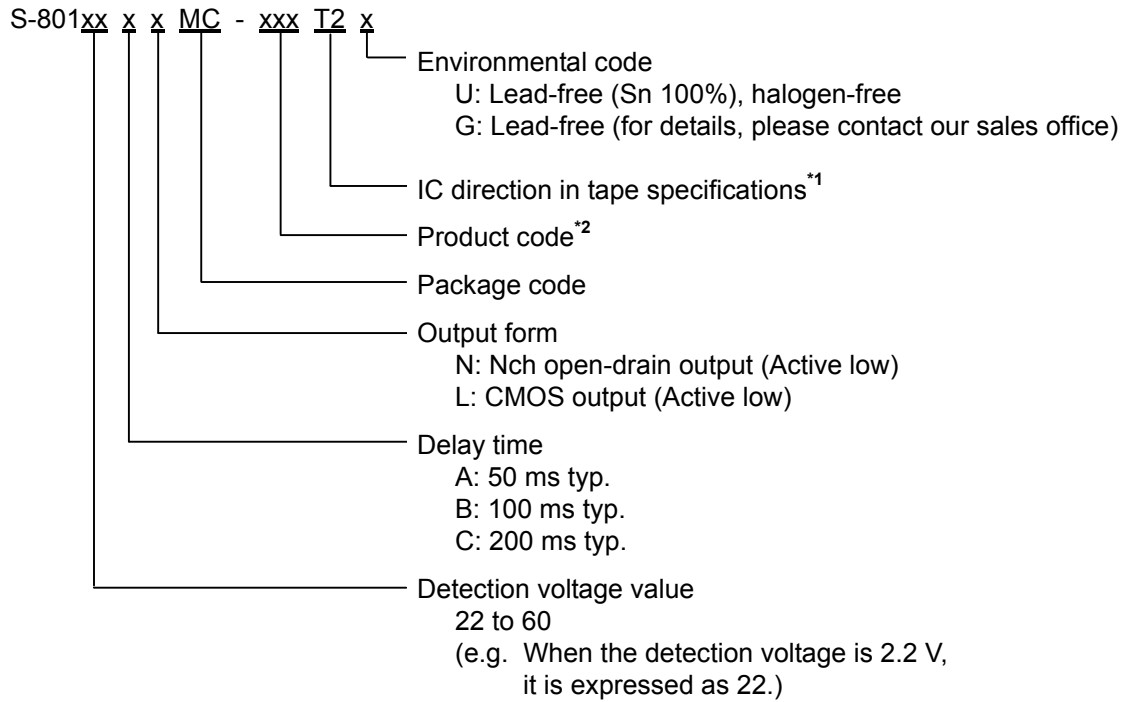
Figure 2

■ **Product Name Structure**

The detection voltage, delay time, output form and packages for S-801 Series can be selected at the user's request. Refer to the "1. **Product name**" for the construction of the product name, "2. **Packages**" regarding the package drawings and "3. **Product Name List**" for the full product names.

1. Product Name

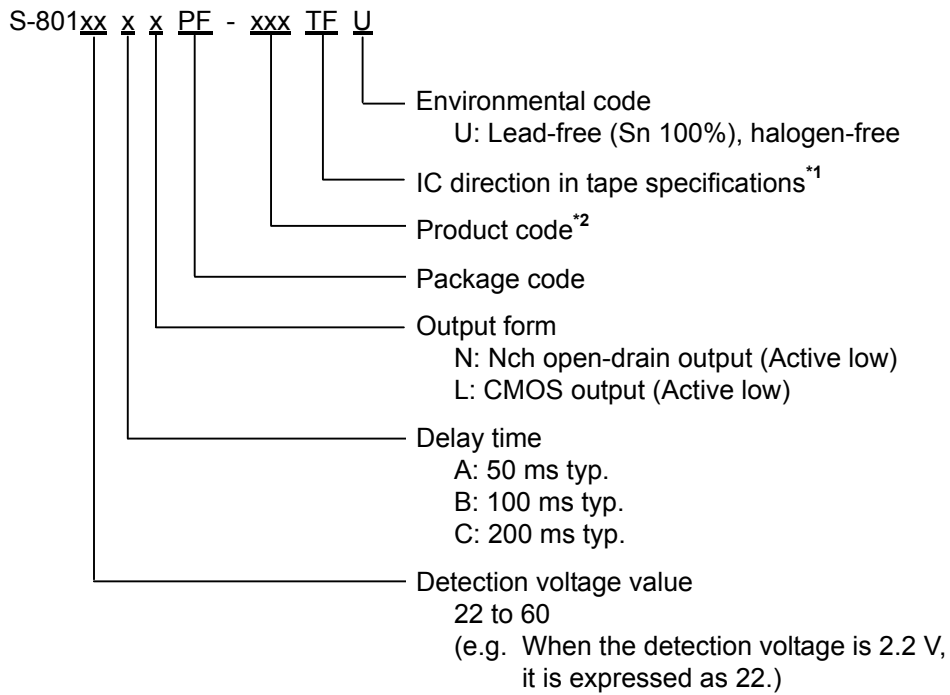
1-1. SOT-23-5



*1. Refer to the tape drawing.

*2. Refer to **Table 2** in "3. **Product name list**".

1-2. SNT-4A



*1. Refer to the tape drawing.

*2. Refer to **Table 2** in “**3. Product name list**”.

2. Packages

| Package name | Drawing code | | | |
|--------------|--------------|--------------|--------------|--------------|
| | Package | Tape | Reel | Land |
| SOT-23-5 | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD | — |
| SNT-4A | PF004-A-P-SD | PF004-A-C-SD | PF004-A-R-SD | PF004-A-L-SD |

3. Product Name List

3-1. SOT-23-5

Table 1 (1/3)

| Detection voltage range | Delay time | Nch open-drain output products | CMOS output products |
|-------------------------|-------------|--------------------------------|----------------------|
| 2.2 V ±2.0% | 50 ms typ. | S-80122ANMC-JCHT2x | S-80122ALMC-JAHT2x |
| | 100 ms typ. | S-80122BNMC-JGHT2x | S-80122BLMC-JEHT2x |
| | 200 ms typ. | S-80122CNMC-JKHT2x | S-80122CLMC-JIHT2x |
| 2.3 V ±2.0% | 50 ms typ. | S-80123ANMC-JCIT2x | S-80123ALMC-JAIT2x |
| | 100 ms typ. | S-80123BNMC-JGIT2x | S-80123BLMC-JEIT2x |
| | 200 ms typ. | S-80123CNMC-JKIT2x | S-80123CLMC-JIIT2x |
| 2.4 V ±2.0% | 50 ms typ. | S-80124ANMC-JCJT2x | S-80124ALMC-JAJT2x |
| | 100 ms typ. | S-80124BNMC-JGJT2x | S-80124BLMC-JEJT2x |
| | 200 ms typ. | S-80124CNMC-JKJT2x | S-80124CLMC-JIJT2x |
| 2.5 V ±2.0% | 50 ms typ. | S-80125ANMC-JCKT2x | S-80125ALMC-JAKT2x |
| | 100 ms typ. | S-80125BNMC-JGKT2x | S-80125BLMC-JEKT2x |
| | 200 ms typ. | S-80125CNMC-JKKT2x | S-80125CLMC-JIKT2x |
| 2.6 V ±2.0% | 50 ms typ. | S-80126ANMC-JCLT2x | S-80126ALMC-JALT2x |
| | 100 ms typ. | S-80126BNMC-JGLT2x | S-80126BLMC-JELT2x |
| | 200 ms typ. | S-80126CNMC-JKLT2x | S-80126CLMC-JILT2x |
| 2.7 V ±2.0% | 50 ms typ. | S-80127ANMC-JCMT2x | S-80127ALMC-JAMT2x |
| | 100 ms typ. | S-80127BNMC-JGMT2x | S-80127BLMC-JEMT2x |
| | 200 ms typ. | S-80127CNMC-JKMT2x | S-80127CLMC-JIMT2x |
| 2.8 V ±2.0% | 50 ms typ. | S-80128ANMC-JCNT2x | S-80128ALMC-JANT2x |
| | 100 ms typ. | S-80128BNMC-JGNT2x | S-80128BLMC-JENT2x |
| | 200 ms typ. | S-80128CNMC-JKNT2x | S-80128CLMC-JINT2x |
| 2.9 V ±2.0% | 50 ms typ. | S-80129ANMC-JCOT2x | S-80129ALMC-JAOT2x |
| | 100 ms typ. | S-80129BNMC-JGOT2x | S-80129BLMC-JEOT2x |
| | 200 ms typ. | S-80129CNMC-JKOT2x | S-80129CLMC-JIOT2x |
| 3.0 V ±2.0% | 50 ms typ. | S-80130ANMC-JCPT2x | S-80130ALMC-JAPT2x |
| | 100 ms typ. | S-80130BNMC-JGPT2x | S-80130BLMC-JEPT2x |
| | 200 ms typ. | S-80130CNMC-JKPT2x | S-80130CLMC-JIPT2x |
| 3.1 V ±2.0% | 50 ms typ. | S-80131ANMC-JCQT2x | S-80131ALMC-JAQT2x |
| | 100 ms typ. | S-80131BNMC-JGQT2x | S-80131BLMC-JEQT2x |
| | 200 ms typ. | S-80131CNMC-JKQT2x | S-80131CLMC-JIQT2x |
| 3.2 V ±2.0% | 50 ms typ. | S-80132ANMC-JCRT2x | S-80132ALMC-JART2x |
| | 100 ms typ. | S-80132BNMC-JGRT2x | S-80132BLMC-JERT2x |
| | 200 ms typ. | S-80132CNMC-JKRT2x | S-80132CLMC-JIRT2x |
| 3.3 V ±2.0% | 50 ms typ. | S-80133ANMC-JCST2x | S-80133ALMC-JAST2x |
| | 100 ms typ. | S-80133BNMC-JGST2x | S-80133BLMC-JEST2x |
| | 200 ms typ. | S-80133CNMC-JKST2x | S-80133CLMC-JIST2x |
| 3.4 V ±2.0% | 50 ms typ. | S-80134ANMC-JCTT2x | S-80134ALMC-JATT2x |
| | 100 ms typ. | S-80134BNMC-JGTT2x | S-80134BLMC-JETT2x |
| | 200 ms typ. | S-80134CNMC-JKTT2x | S-80134CLMC-JITT2x |

Table 1 (2/3)

| Detection voltage range | Delay time | Nch open-drain output products | CMOS output products |
|-------------------------|-------------|--------------------------------|----------------------|
| 3.5 V ±2.0% | 50 ms typ. | S-80135ANMC-JCUT2x | S-80135ALMC-JAUT2x |
| | 100 ms typ. | S-80135BNMC-JGUT2x | S-80135BLMC-JEUT2x |
| | 200 ms typ. | S-80135CNMC-JKUT2x | S-80135CLMC-JIUT2x |
| 3.6 V ±2.0% | 50 ms typ. | S-80136ANMC-JCVT2x | S-80136ALMC-JAVT2x |
| | 100 ms typ. | S-80136BNMC-JGVT2x | S-80136BLMC-JEVT2x |
| | 200 ms typ. | S-80136CNMC-JKVT2x | S-80136CLMC-JIVT2x |
| 3.7 V ±2.0% | 50 ms typ. | S-80137ANMC-JCWT2x | S-80137ALMC-JAWT2x |
| | 100 ms typ. | S-80137BNMC-JGWT2x | S-80137BLMC-JEWT2x |
| | 200 ms typ. | S-80137CNMC-JKWT2x | S-80137CLMC-JIWT2x |
| 3.8 V ±2.0% | 50 ms typ. | S-80138ANMC-JCXT2x | S-80138ALMC-JAXT2x |
| | 100 ms typ. | S-80138BNMC-JGXT2x | S-80138BLMC-JEXT2x |
| | 200 ms typ. | S-80138CNMC-JKXT2x | S-80138CLMC-JIXT2x |
| 3.9 V ±2.0% | 50 ms typ. | S-80139ANMC-JCYT2x | S-80139ALMC-JAYT2x |
| | 100 ms typ. | S-80139BNMC-JGYT2x | S-80139BLMC-JEYT2x |
| | 200 ms typ. | S-80139CNMC-JKYT2x | S-80139CLMC-JIYT2x |
| 4.0 V ±2.0% | 50 ms typ. | S-80140ANMC-JCZT2x | S-80140ALMC-JAZT2x |
| | 100 ms typ. | S-80140BNMC-JGZT2x | S-80140BLMC-JEZT2x |
| | 200 ms typ. | S-80140CNMC-JKZT2x | S-80140CLMC-JIZT2x |
| 4.1 V ±2.0% | 50 ms typ. | S-80141ANMC-JC2T2x | S-80141ALMC-JA2T2x |
| | 100 ms typ. | S-80141BNMC-JG2T2x | S-80141BLMC-JE2T2x |
| | 200 ms typ. | S-80141CNMC-JK2T2x | S-80141CLMC-JI2T2x |
| 4.2 V ±2.0% | 50 ms typ. | S-80142ANMC-JC3T2x | S-80142ALMC-JA3T2x |
| | 100 ms typ. | S-80142BNMC-JG3T2x | S-80142BLMC-JE3T2x |
| | 200 ms typ. | S-80142CNMC-JK3T2x | S-80142CLMC-JI3T2x |
| 4.3 V ±2.0% | 50 ms typ. | S-80143ANMC-JC4T2x | S-80143ALMC-JA4T2x |
| | 100 ms typ. | S-80143BNMC-JG4T2x | S-80143BLMC-JE4T2x |
| | 200 ms typ. | S-80143CNMC-JK4T2x | S-80143CLMC-JI4T2x |
| 4.4 V ±2.0% | 50 ms typ. | S-80144ANMC-JC5T2x | S-80144ALMC-JA5T2x |
| | 100 ms typ. | S-80144BNMC-JG5T2x | S-80144BLMC-JE5T2x |
| | 200 ms typ. | S-80144CNMC-JK5T2x | S-80144CLMC-JI5T2x |
| 4.5 V ±2.0% | 50 ms typ. | S-80145ANMC-JC6T2x | S-80145ALMC-JA6T2x |
| | 100 ms typ. | S-80145BNMC-JG6T2x | S-80145BLMC-JE6T2x |
| | 200 ms typ. | S-80145CNMC-JK6T2x | S-80145CLMC-JI6T2x |
| 4.6 V ±2.0% | 50 ms typ. | S-80146ANMC-JC7T2x | S-80146ALMC-JA7T2x |
| | 100 ms typ. | S-80146BNMC-JG7T2x | S-80146BLMC-JE7T2x |
| | 200 ms typ. | S-80146CNMC-JK7T2x | S-80146CLMC-JI7T2x |
| 4.7 V ±2.0% | 50 ms typ. | S-80147ANMC-JC8T2x | S-80147ALMC-JA8T2x |
| | 100 ms typ. | S-80147BNMC-JG8T2x | S-80147BLMC-JE8T2x |
| | 200 ms typ. | S-80147CNMC-JK8T2x | S-80147CLMC-JI8T2x |
| 4.8 V ±2.0% | 50 ms typ. | S-80148ANMC-JC9T2x | S-80148ALMC-JA9T2x |
| | 100 ms typ. | S-80148BNMC-JG9T2x | S-80148BLMC-JE9T2x |
| | 200 ms typ. | S-80148CNMC-JK9T2x | S-80148CLMC-JI9T2x |
| 4.9 V ±2.0% | 50 ms typ. | S-80149ANMC-JDAT2x | S-80149ALMC-JBAT2x |
| | 100 ms typ. | S-80149BNMC-JHAT2x | S-80149BLMC-JFAT2x |
| | 200 ms typ. | S-80149CNMC-JLAT2x | S-80149CLMC-JJAT2x |

Table 1 (3/3)

| Detection voltage range | Delay time | Nch open-drain output products | CMOS output products |
|-------------------------|-------------|--------------------------------|----------------------|
| 5.0 V \pm 2.0% | 50 ms typ. | S-80150ANMC-JDBT2x | S-80150ALMC-JBBT2x |
| | 100 ms typ. | S-80150BNMC-JHBT2x | S-80150BLMC-JFBT2x |
| | 200 ms typ. | S-80150CNMC-JLBT2x | S-80150CLMC-JJBT2x |
| 5.1 V \pm 2.0% | 50 ms typ. | S-80151ANMC-JDCT2x | S-80151ALMC-JBCT2x |
| | 100 ms typ. | S-80151BNMC-JHCT2x | S-80151BLMC-JFCT2x |
| | 200 ms typ. | S-80151CNMC-JLCT2x | S-80151CLMC-JJCT2x |
| 5.2 V \pm 2.0% | 50 ms typ. | S-80152ANMC-JDDT2x | S-80152ALMC-JBDT2x |
| | 100 ms typ. | S-80152BNMC-JHDT2x | S-80152BLMC-JFDT2x |
| | 200 ms typ. | S-80152CNMC-JLDT2x | S-80152CLMC-JJDT2x |
| 5.3 V \pm 2.0% | 50 ms typ. | S-80153ANMC-JDET2x | S-80153ALMC-JBET2x |
| | 100 ms typ. | S-80153BNMC-JHET2x | S-80153BLMC-JFET2x |
| | 200 ms typ. | S-80153CNMC-JLET2x | S-80153CLMC-JJET2x |
| 5.4 V \pm 2.0% | 50 ms typ. | S-80154ANMC-JDFT2x | S-80154ALMC-JBFT2x |
| | 100 ms typ. | S-80154BNMC-JHFT2x | S-80154BLMC-JFFT2x |
| | 200 ms typ. | S-80154CNMC-JLFT2x | S-80154CLMC-JJFT2x |
| 5.5 V \pm 2.0% | 50 ms typ. | S-80155ANMC-JDGT2x | S-80155ALMC-JBGT2x |
| | 100 ms typ. | S-80155BNMC-JHGT2x | S-80155BLMC-JFGT2x |
| | 200 ms typ. | S-80155CNMC-JLGT2x | S-80155CLMC-JJGT2x |
| 5.6 V \pm 2.0% | 50 ms typ. | S-80156ANMC-JDHT2x | S-80156ALMC-JBHT2x |
| | 100 ms typ. | S-80156BNMC-JHHT2x | S-80156BLMC-JFHT2x |
| | 200 ms typ. | S-80156CNMC-JLHT2x | S-80156CLMC-JJHT2x |
| 5.7 V \pm 2.0% | 50 ms typ. | S-80157ANMC-JDIT2x | S-80157ALMC-JBIT2x |
| | 100 ms typ. | S-80157BNMC-JHIT2x | S-80157BLMC-JFIT2x |
| | 200 ms typ. | S-80157CNMC-JLIT2x | S-80157CLMC-JJIT2x |
| 5.8 V \pm 2.0% | 50 ms typ. | S-80158ANMC-JDJT2x | S-80158ALMC-JBJT2x |
| | 100 ms typ. | S-80158BNMC-JHJT2x | S-80158BLMC-JFJT2x |
| | 200 ms typ. | S-80158CNMC-JLJT2x | S-80158CLMC-JJJT2x |
| 5.9 V \pm 2.0% | 50 ms typ. | S-80159ANMC-JDKT2x | S-80159ALMC-JBKT2x |
| | 100 ms typ. | S-80159BNMC-JHKT2x | S-80159BLMC-JFKT2x |
| | 200 ms typ. | S-80159CNMC-JLKT2x | S-80159CLMC-JJKT2x |
| 6.0 V \pm 2.0% | 50 ms typ. | S-80160ANMC-JDLT2x | S-80160ALMC-JBLT2x |
| | 100 ms typ. | S-80160BNMC-JHLT2x | S-80160BLMC-JFLT2x |
| | 200 ms typ. | S-80160CNMC-JLLT2x | S-80160CLMC-JJLT2x |

Remark 1. x: G or U

2. Please select products of environmental code = U for Sn 100%, halogen-free products.

3-2. SNT-4A

Table 2 (1/3)

| Detection voltage range | Delay time | Nch open-drain output products | CMOS output products |
|-------------------------|-------------|--------------------------------|----------------------|
| 2.2 V ±2.0% | 50 ms typ. | S-80122ANPF-JCHTFU | S-80122ALPF-JAHTFU |
| | 100 ms typ. | S-80122BNPF-JGHTFU | S-80122BLPF-JEHTFU |
| | 200 ms typ. | S-80122CNPF-JKHTFU | S-80122CLPF-JIHTFU |
| 2.3 V ±2.0% | 50 ms typ. | S-80123ANPF-JCITFU | S-80123ALPF-JAITFU |
| | 100 ms typ. | S-80123BNPF-JGITFU | S-80123BLPF-JEITFU |
| | 200 ms typ. | S-80123CNPF-JKITFU | S-80123CLPF-JIITFU |
| 2.4 V ±2.0% | 50 ms typ. | S-80124ANPF-JCJTFU | S-80124ALPF-JAJTFU |
| | 100 ms typ. | S-80124BNPF-JGJTFU | S-80124BLPF-JEJTFU |
| | 200 ms typ. | S-80124CNPF-JKJTFU | S-80124CLPF-JIJTFU |
| 2.5 V ±2.0% | 50 ms typ. | S-80125ANPF-JCKTFU | S-80125ALPF-JAKTFU |
| | 100 ms typ. | S-80125BNPF-JGKTFU | S-80125BLPF-JEKTFU |
| | 200 ms typ. | S-80125CNPF-JKKTFU | S-80125CLPF-JIKTFU |
| 2.6 V ±2.0% | 50 ms typ. | S-80126ANPF-JCLTFU | S-80126ALPF-JALTFU |
| | 100 ms typ. | S-80126BNPF-JGLTFU | S-80126BLPF-JELTFU |
| | 200 ms typ. | S-80126CNPF-JKLTUFU | S-80126CLPF-JILTFU |
| 2.7 V ±2.0% | 50 ms typ. | S-80127ANPF-JCMTFU | S-80127ALPF-JAMTFU |
| | 100 ms typ. | S-80127BNPF-JGMTFU | S-80127BLPF-JEMTFU |
| | 200 ms typ. | S-80127CNPF-JKMTFU | S-80127CLPF-JIMTFU |
| 2.8 V ±2.0% | 50 ms typ. | S-80128ANPF-JCNTFU | S-80128ALPF-JANTFU |
| | 100 ms typ. | S-80128BNPF-JGNTFU | S-80128BLPF-JENTFU |
| | 200 ms typ. | S-80128CNPF-JKNTFU | S-80128CLPF-JINTFU |
| 2.9 V ±2.0% | 50 ms typ. | S-80129ANPF-JCOTFU | S-80129ALPF-JAOTFU |
| | 100 ms typ. | S-80129BNPF-JGOTFU | S-80129BLPF-JEOTFU |
| | 200 ms typ. | S-80129CNPF-JKOTFU | S-80129CLPF-JIOTFU |
| 3.0 V ±2.0% | 50 ms typ. | S-80130ANPF-JCPTFU | S-80130ALPF-JAPTUFU |
| | 100 ms typ. | S-80130BNPF-JGPTFU | S-80130BLPF-JEPTFU |
| | 200 ms typ. | S-80130CNPF-JKPTFU | S-80130CLPF-JIPTFU |
| 3.1 V ±2.0% | 50 ms typ. | S-80131ANPF-JCQTFU | S-80131ALPF-JAQTFU |
| | 100 ms typ. | S-80131BNPF-JGQTFU | S-80131BLPF-JEQTFU |
| | 200 ms typ. | S-80131CNPF-JKQTFU | S-80131CLPF-JIQTFU |
| 3.2 V ±2.0% | 50 ms typ. | S-80132ANPF-JCRTFU | S-80132ALPF-JARTFU |
| | 100 ms typ. | S-80132BNPF-JGRTFU | S-80132BLPF-JERTFU |
| | 200 ms typ. | S-80132CNPF-JKRTFU | S-80132CLPF-JIRTFU |
| 3.3 V ±2.0% | 50 ms typ. | S-80133ANPF-JCSTFU | S-80133ALPF-JASTFU |
| | 100 ms typ. | S-80133BNPF-JGSTFU | S-80133BLPF-JESTFU |
| | 200 ms typ. | S-80133CNPF-JKSTFU | S-80133CLPF-JISTFU |
| 3.4 V ±2.0% | 50 ms typ. | S-80134ANPF-JCTTFU | S-80134ALPF-JATTFU |
| | 100 ms typ. | S-80134BNPF-JGTTFU | S-80134BLPF-JETTFU |
| | 200 ms typ. | S-80134CNPF-JKTTFU | S-80134CLPF-JITTFU |
| 3.5 V ±2.0% | 50 ms typ. | S-80135ANPF-JCUTFU | S-80135ALPF-JAUTFU |
| | 100 ms typ. | S-80135BNPF-JGUTFU | S-80135BLPF-JEUTFU |
| | 200 ms typ. | S-80135CNPF-JKUTFU | S-80135CLPF-JIUTFU |
| 3.6 V ±2.0% | 50 ms typ. | S-80136ANPF-JCVTFU | S-80136ALPF-JAVTFU |
| | 100 ms typ. | S-80136BNPF-JGVTFU | S-80136BLPF-JEVTFU |
| | 200 ms typ. | S-80136CNPF-JKVTFU | S-80136CLPF-JIVTFU |
| 3.7 V ±2.0% | 50 ms typ. | S-80137ANPF-JCWTFU | S-80137ALPF-JAWTFU |
| | 100 ms typ. | S-80137BNPF-JGWTFU | S-80137BLPF-JEWTFU |
| | 200 ms typ. | S-80137CNPF-JKWTFU | S-80137CLPF-JIWTFU |

Table 2 (2/3)

| Detection voltage range | Delay time | Nch open-drain output products | CMOS output products |
|-------------------------|-------------|--------------------------------|----------------------|
| 3.8 V \pm 2.0% | 50 ms typ. | S-80138ANPF-JCXTFU | S-80138ALPF-JAXTFU |
| | 100 ms typ. | S-80138BNPF-JGXTFU | S-80138BLPF-JEXTFU |
| | 200 ms typ. | S-80138CNPF-JKXTFU | S-80138CLPF-JIXTFU |
| 3.9 V \pm 2.0% | 50 ms typ. | S-80139ANPF-JCYTFU | S-80139ALPF-JAYTFU |
| | 100 ms typ. | S-80139BNPF-JGYTFU | S-80139BLPF-JEYTFU |
| | 200 ms typ. | S-80139CNPF-JKYTFU | S-80139CLPF-JIYTFU |
| 4.0 V \pm 2.0% | 50 ms typ. | S-80140ANPF-JCZTFU | S-80140ALPF-JAZTFU |
| | 100 ms typ. | S-80140BNPF-JGZTFU | S-80140BLPF-JEZTFU |
| | 200 ms typ. | S-80140CNPF-JKZTFU | S-80140CLPF-JIZTFU |
| 4.1 V \pm 2.0% | 50 ms typ. | S-80141ANPF-JC2TFU | S-80141ALPF-JA2TFU |
| | 100 ms typ. | S-80141BNPF-JG2TFU | S-80141BLPF-JE2TFU |
| | 200 ms typ. | S-80141CNPF-JK2TFU | S-80141CLPF-JI2TFU |
| 4.2 V \pm 2.0% | 50 ms typ. | S-80142ANPF-JC3TFU | S-80142ALPF-JA3TFU |
| | 100 ms typ. | S-80142BNPF-JG3TFU | S-80142BLPF-JE3TFU |
| | 200 ms typ. | S-80142CNPF-JK3TFU | S-80142CLPF-JI3TFU |
| 4.3 V \pm 2.0% | 50 ms typ. | S-80143ANPF-JC4TFU | S-80143ALPF-JA4TFU |
| | 100 ms typ. | S-80143BNPF-JG4TFU | S-80143BLPF-JE4TFU |
| | 200 ms typ. | S-80143CNPF-JK4TFU | S-80143CLPF-JI4TFU |
| 4.4 V \pm 2.0% | 50 ms typ. | S-80144ANPF-JC5TFU | S-80144ALPF-JA5TFU |
| | 100 ms typ. | S-80144BNPF-JG5TFU | S-80144BLPF-JE5TFU |
| | 200 ms typ. | S-80144CNPF-JK5TFU | S-80144CLPF-JI5TFU |
| 4.5 V \pm 2.0% | 50 ms typ. | S-80145ANPF-JC6TFU | S-80145ALPF-JA6TFU |
| | 100 ms typ. | S-80145BNPF-JG6TFU | S-80145BLPF-JE6TFU |
| | 200 ms typ. | S-80145CNPF-JK6TFU | S-80145CLPF-JI6TFU |
| 4.6 V \pm 2.0% | 50 ms typ. | S-80146ANPF-JC7TFU | S-80146ALPF-JA7TFU |
| | 100 ms typ. | S-80146BNPF-JG7TFU | S-80146BLPF-JE7TFU |
| | 200 ms typ. | S-80146CNPF-JK7TFU | S-80146CLPF-JI7TFU |
| 4.7 V \pm 2.0% | 50 ms typ. | S-80147ANPF-JC8TFU | S-80147ALPF-JA8TFU |
| | 100 ms typ. | S-80147BNPF-JG8TFU | S-80147BLPF-JE8TFU |
| | 200 ms typ. | S-80147CNPF-JK8TFU | S-80147CLPF-JI8TFU |
| 4.8 V \pm 2.0% | 50 ms typ. | S-80148ANPF-JC9TFU | S-80148ALPF-JA9TFU |
| | 100 ms typ. | S-80148BNPF-JG9TFU | S-80148BLPF-JE9TFU |
| | 200 ms typ. | S-80148CNPF-JK9TFU | S-80148CLPF-JI9TFU |
| 4.9 V \pm 2.0% | 50 ms typ. | S-80149ANPF-JDATFU | S-80149ALPF-JBATFU |
| | 100 ms typ. | S-80149BNPF-JHATFU | S-80149BLPF-JFATFU |
| | 200 ms typ. | S-80149CNPF-JLATFU | S-80149CLPF-JJATFU |
| 5.0 V \pm 2.0% | 50 ms typ. | S-80150ANPF-JDBTFU | S-80150ALPF-JBBTFU |
| | 100 ms typ. | S-80150BNPF-JHBTFU | S-80150BLPF-JFBTFU |
| | 200 ms typ. | S-80150CNPF-JLBTFU | S-80150CLPF-JJBTFU |
| 5.1 V \pm 2.0% | 50 ms typ. | S-80151ANPF-JDCTFU | S-80151ALPF-JBCTFU |
| | 100 ms typ. | S-80151BNPF-JHCTFU | S-80151BLPF-JFCTFU |
| | 200 ms typ. | S-80151CNPF-JLCTFU | S-80151CLPF-JJCTFU |
| 5.2 V \pm 2.0% | 50 ms typ. | S-80152ANPF-JDDTFU | S-80152ALPF-JBDTFU |
| | 100 ms typ. | S-80152BNPF-JHDTFU | S-80152BLPF-JFDTFU |
| | 200 ms typ. | S-80152CNPF-JLDTFU | S-80152CLPF-JJDTFU |
| 5.3 V \pm 2.0% | 50 ms typ. | S-80153ANPF-JDETFU | S-80153ALPF-JBETFU |
| | 100 ms typ. | S-80153BNPF-JHETFU | S-80153BLPF-JFETFU |
| | 200 ms typ. | S-80153CNPF-JLETFU | S-80153CLPF-JJETFU |

Table 2 (3/3)

| Detection voltage range | Delay time | Nch open-drain output products | CMOS output products |
|-------------------------|-------------|--------------------------------|----------------------|
| 5.4 V \pm 2.0% | 50 ms typ. | S-80154ANPF-JDFTFU | S-80154ALPF-JBFTFU |
| | 100 ms typ. | S-80154BNPF-JHFTFU | S-80154BLPF-JFFTFU |
| | 200 ms typ. | S-80154CNPF-JLFTFU | S-80154CLPF-JJFTFU |
| 5.5 V \pm 2.0% | 50 ms typ. | S-80155ANPF-JDGTFU | S-80155ALPF-JBGTFU |
| | 100 ms typ. | S-80155BNPF-JHGTFU | S-80155BLPF-JFUTFU |
| | 200 ms typ. | S-80155CNPF-JLGTFU | S-80155CLPF-JJGTFU |
| 5.6 V \pm 2.0% | 50 ms typ. | S-80156ANPF-JDHTFU | S-80156ALPF-JBHTFU |
| | 100 ms typ. | S-80156BNPF-JHHTFU | S-80156BLPF-JFHHTFU |
| | 200 ms typ. | S-80156CNPF-JLHTFU | S-80156CLPF-JJHTFU |
| 5.7 V \pm 2.0% | 50 ms typ. | S-80157ANPF-JDITFU | S-80157ALPF-JBITFU |
| | 100 ms typ. | S-80157BNPF-JHITFU | S-80157BLPF-JFITFU |
| | 200 ms typ. | S-80157CNPF-JLITFU | S-80157CLPF-JJITFU |
| 5.8 V \pm 2.0% | 50 ms typ. | S-80158ANPF-JDJTFU | S-80158ALPF-JBJTFU |
| | 100 ms typ. | S-80158BNPF-JHJTFU | S-80158BLPF-JFJTFU |
| | 200 ms typ. | S-80158CNPF-JLJTFU | S-80158CLPF-JJJTFU |
| 5.9 V \pm 2.0% | 50 ms typ. | S-80159ANPF-JDKTFU | S-80159ALPF-JBKTFU |
| | 100 ms typ. | S-80159BNPF-JHKTFU | S-80159BLPF-JFKTFU |
| | 200 ms typ. | S-80159CNPF-JLKTFU | S-80159CLPF-JJKTFU |
| 6.0 V \pm 2.0% | 50 ms typ. | S-80160ANPF-JDLTFU | S-80160ALPF-JBLTFU |
| | 100 ms typ. | S-80160BNPF-JHLTFU | S-80160BLPF-JFLTUFU |
| | 200 ms typ. | S-80160CNPF-JLLTFU | S-80160CLPF-JJLTFU |

■ Pin Configurations

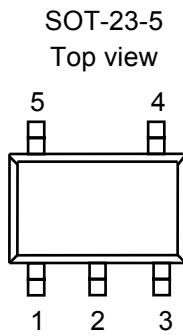


Figure 3

- *1. Refer to “2. Delay Circuit” in “■ Operation” for operation.
- *2. The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

Table 3

| Pin No. | Pin name | Pin description |
|---------|----------|------------------------------|
| 1 | DS*1 | ON/OFF switch for delay time |
| 2 | VSS | GND pin |
| 3 | NC*2 | No connection |
| 4 | OUT | Voltage detection output pin |
| 5 | VDD | Voltage input pin |

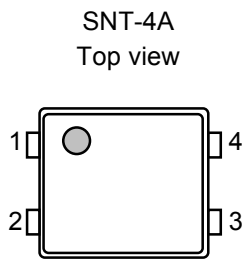


Figure 4

- *1. Refer to “2. Delay Circuit” in “■ Operation” for operation.

Table 4

| Pin No. | Pin name | Pin description |
|---------|----------|------------------------------|
| 1 | VSS | GND pin |
| 2 | DS*1 | ON/OFF switch for delay time |
| 3 | VDD | Voltage input pin |
| 4 | OUT | Voltage detection output pin |

■ Absolute Maximum Ratings

Table 5

(Ta=25°C unless otherwise specified)

| Item | Symbol | Absolute maximum ratings | Unit |
|-------------------------------|--|--------------------------|---------------------------------|
| Power supply voltage | $V_{DD}-V_{SS}$ | 12 | V |
| Output voltage | Nch open-drain output products CMOS output products | V_{OUT} | $V_{SS}-0.3$ to $V_{SS}+12$ |
| | | | $V_{SS}-0.3$ to $V_{DD}+0.3$ |
| Output current | I_{OUT} | 50 | mA |
| Power dissipation | SOT-23-5 | P_D | 250 (When not mounted on board) |
| | | | 600*1 |
| | SNT-4A | | 140 (When not mounted on board) |
| | | | 300*1 |
| Operating ambient temperature | T_{opr} | -40 to +85 | °C |
| Storage temperature | T_{stg} | -40 to +125 | |

*1. When mounted on board

[Mounted board]

- (1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
- (2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

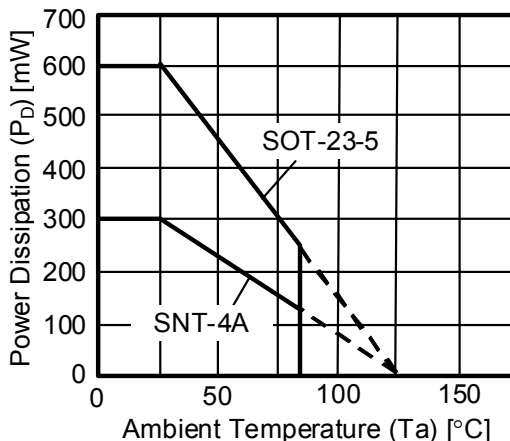


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 6

(Ta=25 °C Unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test circuit | |
|---|---|---|--|---------------|---------------------------|-----------------------|---------------|---|
| Detection voltage*1 | $-V_{DET}$ | — | $-V_{DET(S)} \times 0.98$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.02$ | V | 1 | |
| Hysteresis width | V_{HYS} | — | 30 | 60 | 100 | mV | | |
| Current consumption | I_{SS} | $V_{DD}=3.5\text{ V}$ | S-80122 to 26 | — | 1.3 | 3.3 | μA | |
| | | $V_{DD}=4.5\text{ V}$ | S-80127 to 39 | — | 1.5 | 3.5 | | |
| | | $V_{DD}=6.5\text{ V}$ | S-80140 to 60 | — | 1.8 | 4.0 | | |
| Operating voltage | V_{DD} | — | 0.95 | — | 10.0 | V | | |
| Output current | I_{OUT} | Output transistor, Nch, $V_{OUT}=0.5\text{ V}$ | $V_{DD}=1.2\text{ V}$ S-80122 to 60 | 0.75 | 1.5 | — | mA | 2 |
| | | | $V_{DD}=2.4\text{ V}$ S-80127 to 60 | 3.0 | 6.0 | — | | |
| | | Only for CMOS output products, Output transistor, Pch, $V_{DD}-V_{OUT}=0.5\text{ V}$ | $V_{DD}=4.8\text{ V}$ S-80122 to 39 | 1.0 | 2.0 | — | | |
| | | | $V_{DD}=6.0\text{ V}$ S-80140 to 54 | 1.25 | 2.5 | — | | |
| Leakage current | I_{LEAK} | Only for Nch open-drain output products, Output transistor, Nch, $V_{DD}=10.0\text{ V}$, $V_{OUT}=10.0\text{ V}$ | — | — | 0.1 | μA | | |
| | | | — | — | 0.1 | μA | | |
| Detection voltage temperature coefficient*2 | $\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$ | $Ta=-40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$ | — | ± 120 | ± 360 | ppm/ $^\circ\text{C}$ | 1 | |
| Delay time 1 | t_{D1} | $V_{DD}=-V_{DET}+1\text{ V}$, DS pin Low | S-801xxAx | 32.5 | 50 | 72.5 | ms | |
| | | | S-801xxBx | 65 | 100 | 145 | | |
| | | | S-801xxCx | 130 | 200 | 290 | | |
| Delay time 2 | t_{D2} | $V_{DD}=-V_{DET}+1\text{ V}$, DS pin High | 110 | 220 | 330 | μs | 3 | |
| Input voltage | V_{SH} | DS pin, $V_{DD}=6.0\text{ V}$ | 1.0 | — | — | V | 4 | |
| | V_{SL} | DS pin, $V_{DD}=6.0\text{ V}$ | — | — | 0.3 | | | |

*1. $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Specified detection voltage value (The center value of the detection voltage range in **Table 1 to 2**.)

*2. Temperature change ratio for the detection voltage [mV/ $^\circ\text{C}$] is calculated using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta} [\text{mV}/^\circ\text{C}]^{*1} = -V_{DET(S)}(\text{Typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}} [\text{ppm}/^\circ\text{C}]^{*3} \div 1000$$

*1. Temperature change ratio of the detection voltage

*2. Specified detection voltage value

*3. Detection voltage temperature coefficient

■ Test Circuits

1.



*1. R is unnecessary for CMOS output products.

Figure 6

2.



Figure 7

3.



*1. R is unnecessary for CMOS output products.

Figure 8

4.



*1. R is unnecessary for CMOS output products.

Figure 9

■ Operation

1. Basic Operation: CMOS Output (Active Low)

- 1-1. When the power supply voltage (V_{DD}) is higher than the release voltage ($+V_{DET}$), the Nch transistor is OFF and the Pch transistor is ON to provide V_{DD} (high) at the output. Since the Nch transistor N1 in **Figure 10** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \cdot V_{DD}}{R_A + R_B + R_C}$.
- 1-2. When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as V_{DD} remains above the detection voltage ($-V_{DET}$). When the V_{DD} falls below $-V_{DET}$ (point A in **Figure 11**), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the V_{SS} level appears at the output. At this time the Nch transistor N1 in **Figure 10** becomes ON, the comparator input voltage is changed to $\frac{R_B \cdot V_{DD}}{R_A + R_B}$.
- 1-3. When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to V_{DD} when the output is pulled up to V_{DD} .
- 1-4. The V_{SS} level appears when V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when V_{DD} surpasses the $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.
- 1-5. When V_{DD} rises above $+V_{DET}$ (point B in **Figure 11**), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide V_{DD} at the output. The V_{DD} at the OUT pin is delayed for t_d due to the delay circuit.



*1. Paracitic diode

Figure 10 Operation 1

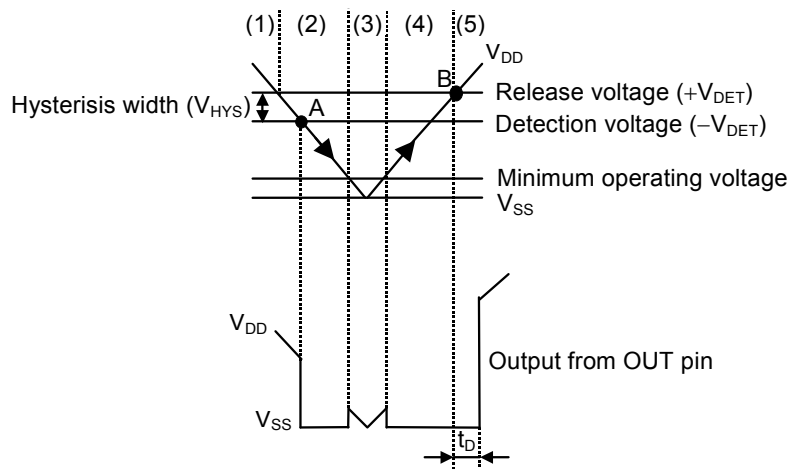


Figure 11 Operation 2

2. Delay Circuit

2-1. Delay Time

The delay circuit delays the output signal from the time at which the power voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when the V_{DD} goes below the detection voltage ($-V_{DET}$). (Refer to **Figure 11**.)

The delay time (t_D) is a fixed value that is determined by a built-in oscillation circuit and counter.

2-2. DS Pin (ON/OFF Switch Pin for Delay Time)

The DS pin should be connected to Low or High. When the DS pin is High, the output delay time becomes short since the output signal is taken from the middle of counter circuit (Refer to **Figure 16**).

3. Other Characteristics

3-1. Temperature Characteristics of Detection Voltage

The shaded area in **Figure 12** shows the temperature characteristics of the detection voltage.



Figure 12 Temperature Characteristics of Detection Voltage (Example for S-80122xxxx)

3-2. Temperature Characteristics of Release Voltage

The temperature coefficient $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by the temperature coefficient $\frac{\Delta - V_{DET}}{\Delta Ta}$ for the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature coefficients for the release voltage and the detection voltage have the same sign consequently.

3-3. Temperature Characteristics of Hysteresis Voltage

The temperature characteristics for the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

■ Standard Circuit



*1. R is unnecessary for CMOS output products.

Figure 13

Caution The above connection diagram and constant will not guarantees successful operation. Perform through using the actual application to set the constant.

■ Technical Terms

1. Detection Voltage ($-V_{DET}$), Release Voltage ($+V_{DET}$)

The detection voltage ($-V_{DET}$) is a voltage at which the output turns to low. The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$) Min. and the maximum ($-V_{DET}$) Max. is called the detection voltage range (Refer to **Figure 14**).

e.g. For the S-80122AN, the detection voltage lies in the range of $2.156 \leq -V_{DET} \leq 2.244$.
 This means that some S-80122ANs have 2.156 V for $-V_{DET}$ and some have 2.244 V.

The release voltage ($+V_{DET}$) is a voltage at which the output turns to high. The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$) Min. and the maximum ($+V_{DET}$) Max. is called the release voltage range (Refer to **Figure 15**).

e.g. For the S-80122AN, the release voltage lies in the range of $2.186 \leq +V_{DET} \leq 2.344$.
 This means that some S-80122ANs have 2.186 V for $+V_{DET}$ and some have 2.344 V.



Figure 14 Detection Voltage



Figure 15 Release Voltage

Remark Although the detection voltage and release voltage overlap in the range of 2.186 V to 2.244 V, $+V_{DET}$ is always larger than $-V_{DET}$.

2. Hysteresis Width (V_{HYS})

Hysteresis width is the voltage difference between the detection voltage and the release voltage (The voltage at point B–The voltage at point A= V_{HYS} in **Figure 11**). The existence of the hysteresis width prevents malfunction caused by noise on input signal.

3. Delay Time (t_D)

Delay time is a time internally measured from the instant at which input voltage to the VDD pin exceeds the release voltage ($+V_{DET}$) to the point at which the output of the OUT pin inverts. The delay time is fixed in each series distinguished by A, B and C.

S-801xxAx series: typ. 50 ms

S-801xxBx series: typ. 100 ms

S-801xxCx series: typ. 200 ms

The output of the OUT pin can be inverted in a short delay time (t_{D2}) by setting the DS pin High (Refer to **Figure 16**).



Figure 16

4. Through-type Current

The through-type current refers to the current that flows instantaneously at the time of detection and release of a voltage detector. The through-type current flows at a frequency of 20 kHz during release delay time since the internal logic circuit operates.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 17**), taking a CMOS active low products for example, the through-type current which is generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the through-type current stops and its resultant voltage drop disappears, and the output goes from low to high. The through-type current is again generated, a voltage drop appears, and repeating the process finally induces oscillation.



Figure 17 Example for Bad Implementation of Input Voltage Divider

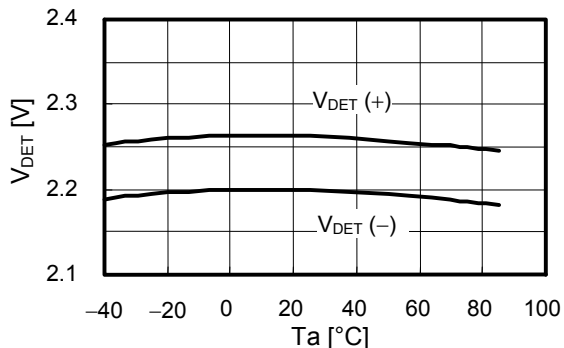
■ Precautions

- In the S-801 series products, the through-type current flows at a frequency of 20 kHz approximately during the delay time since the internal oscillator circuit and counter timer operate at voltage release. High impedance in the input may cause oscillation by the through-type current. When the input impedance is high, insert a capacitor between VDD pin and VSS pin to prevent oscillation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output products of the S-801 Series, the through-type current flows at detection and release. If the impedance is high, oscillation may occur due to the voltage drop by the through-type current during releasing.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for the patents on the circuits described herein.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned a third party.

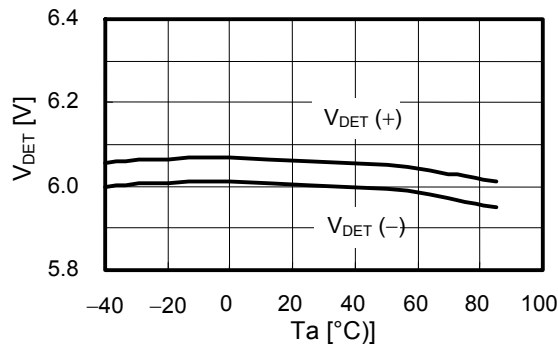
■ Typical Characteristics (Typical Data)

1. Detection Voltage (V_{DET}) - Temperature (T_a)

S-80122AL

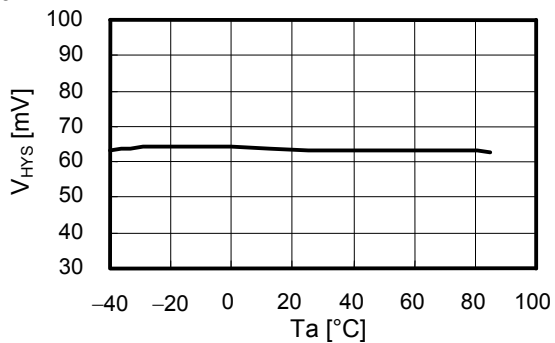


S-80160AL

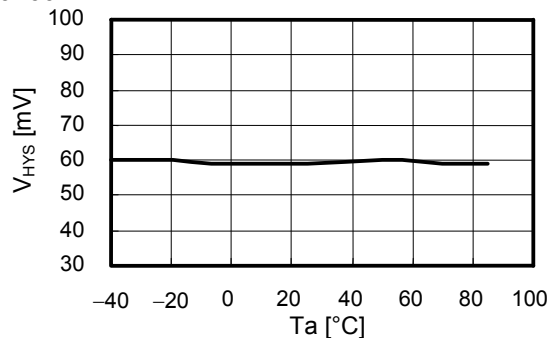


2. Hysteresis Voltage Width (V_{HYS}) - Temperature (T_a)

S-80122AL

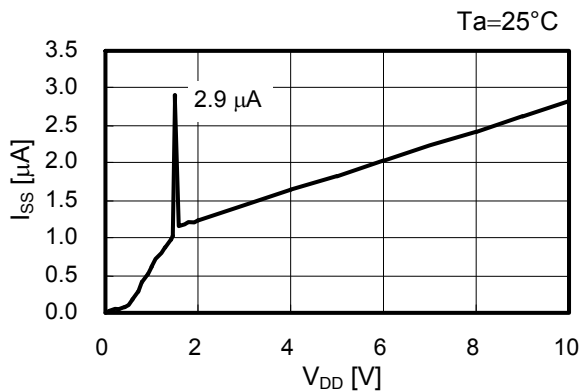


S-80160AL

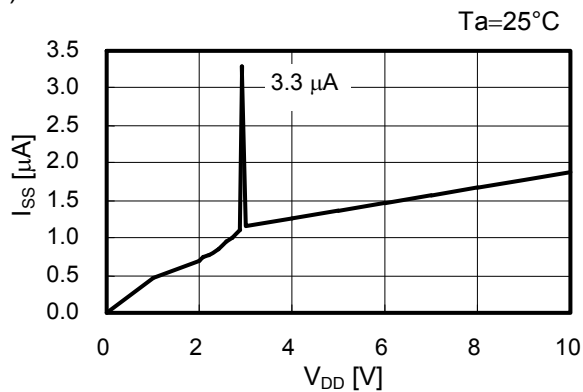


3. Current Consumption (I_{SS}) - Input Voltage (V_{DD})

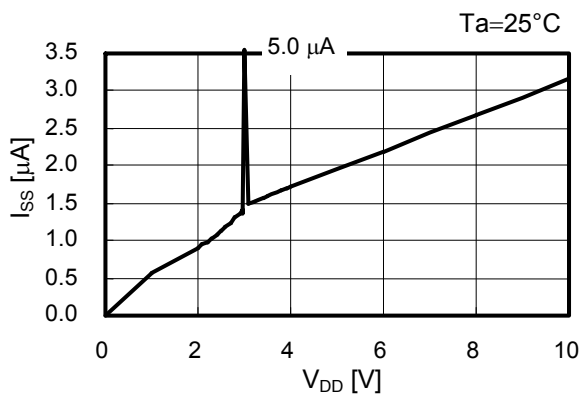
(a) S-80122AL



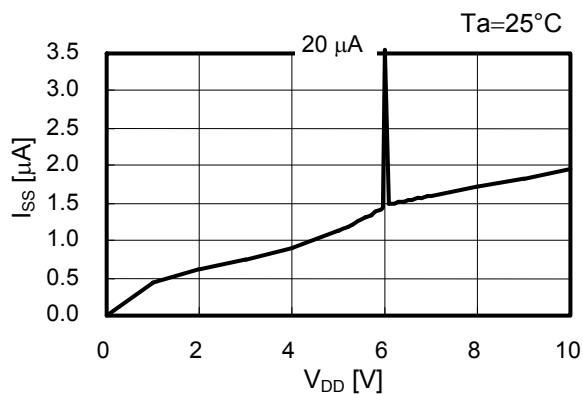
(b) S-80129AL



(c) S-80130AL

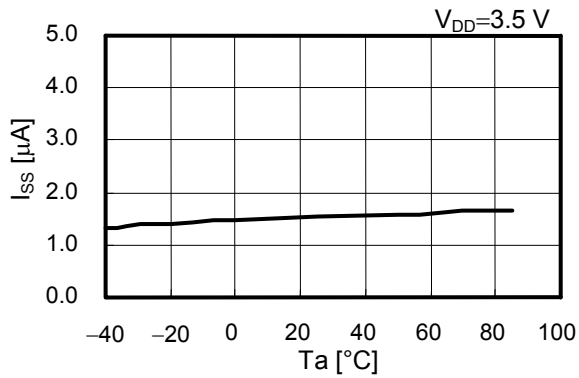


(d) S-80160AL

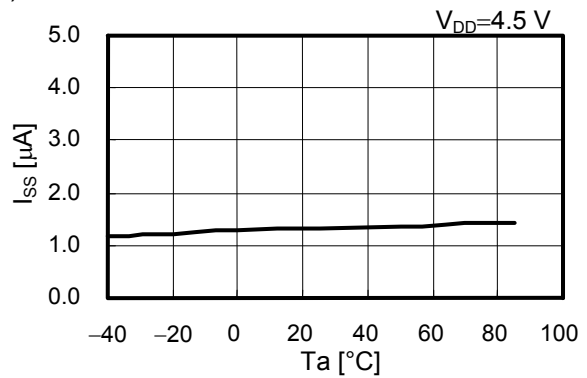


4. Current Consumption (I_{SS}) - Temperature (T_a)

(a) S-80122AL



(b) S-80129AL



(c) S-80130AL



(d) S-80160AL



5. Nch Transistor Output Current (I_{OUT}) - V_{OUT}
S-80160AL



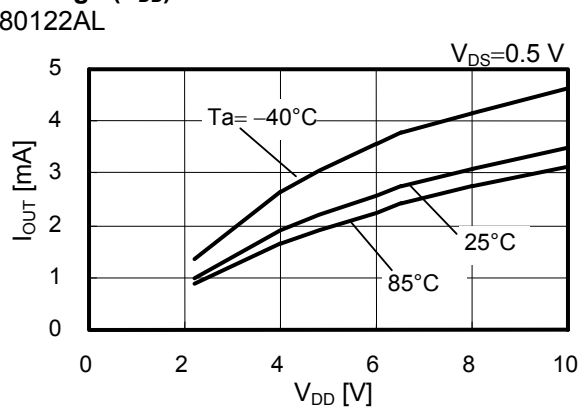
6. Pch Transistor Output Current (I_{OUT}) - ($V_{DD}-V_{OUT}$)
S-80122AL



7. Nch Transistor Output Current (I_{OUT}) - Input Voltage (V_{DD})
S-80160AL

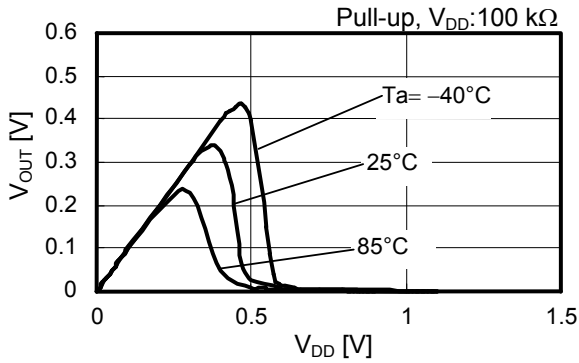


8. Pch transistor Output Current (I_{OUT}) - Input Voltage (V_{DD})
S-80122AL



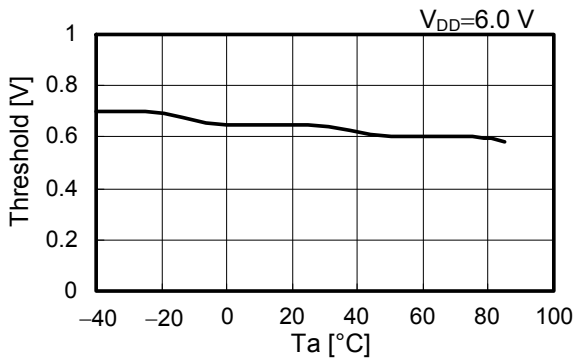
9. Minimum Operating Voltage - Input Voltage (V_{DD})

S-80122AN



10. Threshold Voltage of DS Pin - Temperature (T_a)

S-80122AL



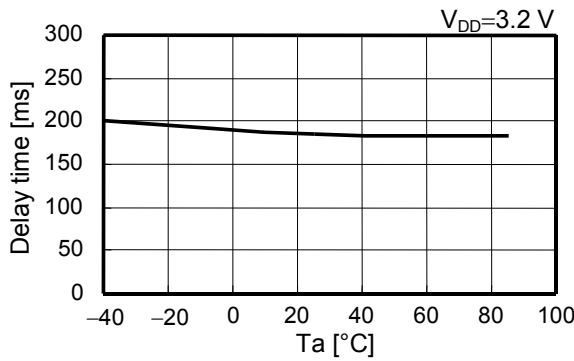
11. Threshold Voltage of DS Pin - Input Voltage (V_{DD})

S-80122AL



12. Delay Time 1 - Temperature (T_a)

S-80122CL

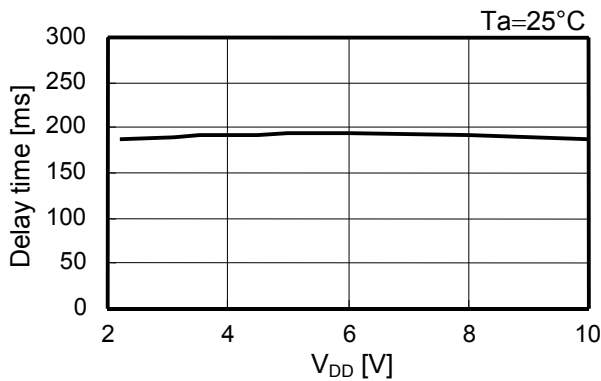


S-80160CL



13. Delay Time 1 - Input Voltage (V_{DD})

S-80122CL



14. Delay Time 2 - Temperature (Ta)

S-80122AL



S-80160AL

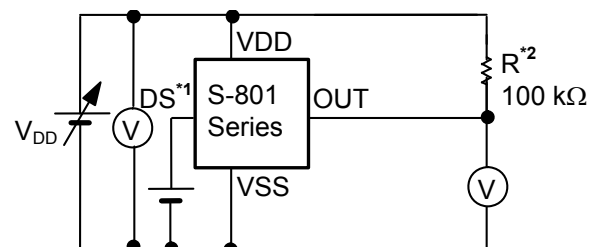


15. Delay Time 2 - Input Voltage (VDD)

S-80122AN



Figure 18 Measurement Condition for Delay Time



*1. Set to VDD or VSS.

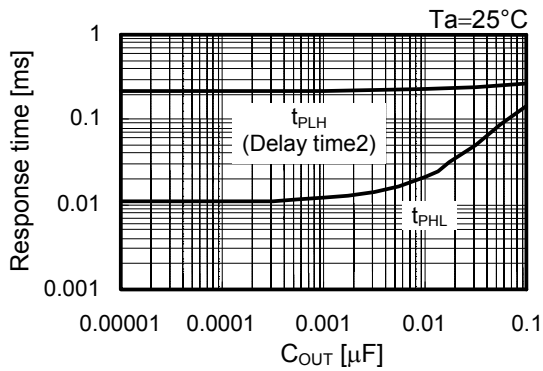
*2. R is not necessary for CMOS output products.

Figure 19 Measurement Circuit for Delay Time

Caution The above connection diagram will not guarantees successful operation. Perform through using the actual application to set the constant.

16. Response Time - Load Capacitor (C_{OUT})

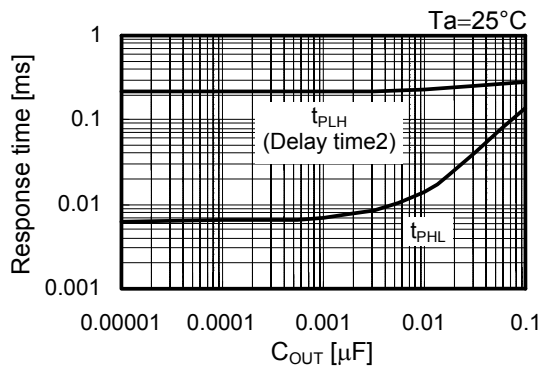
S-80122AL



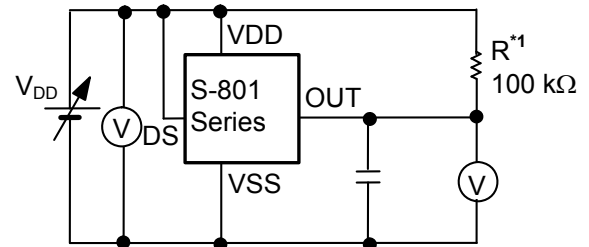
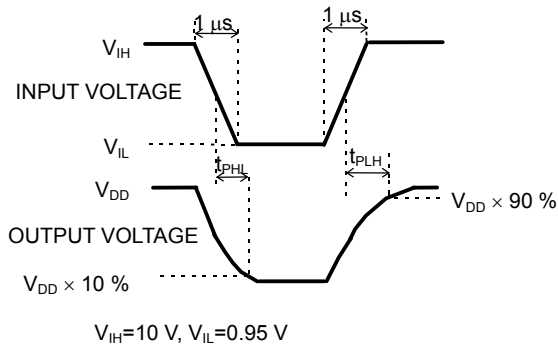
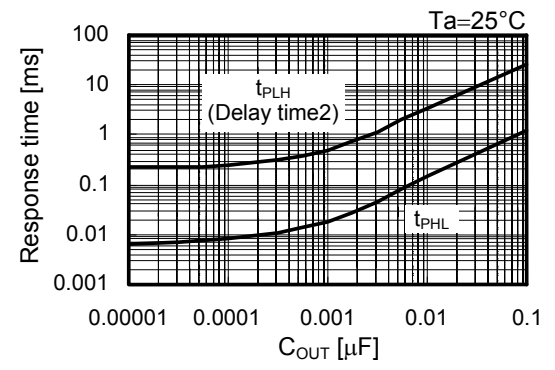
S-80122AN



S-80160AL



S-80160AN



*1. R is not necessary for CMOS output products.

Figure 20 Measurement Condition for Response Time

Figure 21 Measurement Circuit for Response Time

Caution The above connection diagram will not guarantees successful operation. Perform through using the actual application to set the constant.

■ Application Circuit Examples

Microcomputer Reset Circuits

If the power supply voltage to a microcomputer falls below the specified level, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to normal, the microcomputer needs to be initialized before normal operations can be done. Reset circuits protect microcomputers in the event of current being momentarily switched off or lowered.

Reset circuits shown in **Figures 22 to 23** can be easily constructed with the help of the S-801 series that has low operating voltage, a high-precision detection voltage, hysteresis, and a built-in delay circuit.



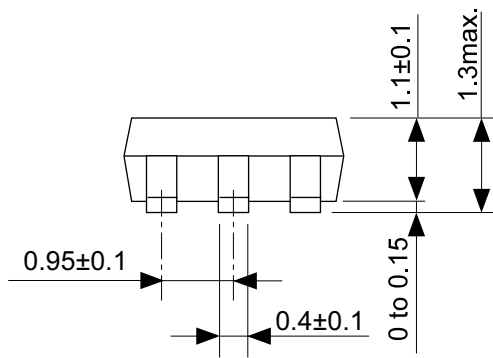
Figure 22 Ret Circuit (S-801xxAL)



(Nch open-drain output products only.)

Figure 23 Reset Circuit (S-801xxAN)

Caution The above connection diagram will not guarantees successful operation. Perform through using the actual application to set the constant.



No. MP005-A-P-SD-1.3

| | |
|-------------------|-------------------------|
| TITLE | SOT235-A-PKG Dimensions |
| No. | MP005-A-P-SD-1.3 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



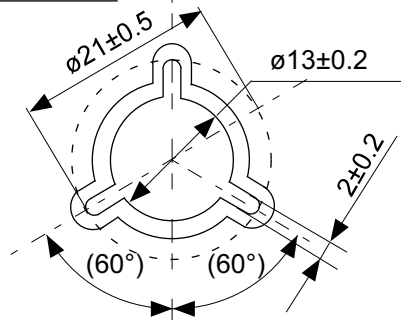
Feed direction →

No. MP005-A-C-SD-2.1

| | |
|-------------------|-----------------------|
| TITLE | SOT235-A-Carrier Tape |
| No. | MP005-A-C-SD-2.1 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

| | | | |
|-------------------|------------------|------|-------|
| TITLE | SOT235-A-Reel | | |
| No. | MP005-A-R-SD-1.1 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |



No. PF004-A-P-SD-6.0

| | |
|-------------------|-------------------------|
| TITLE | SNT-4A-A-PKG Dimensions |
| No. | PF004-A-P-SD-6.0 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



Feed direction

No. PF004-A-C-SD-2.0

| | |
|-------------------|-----------------------|
| TITLE | SNT-4A-A-Carrier Tape |
| No. | PF004-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| ABLIC Inc. | |



Enlarged drawing in the central part



No. PF004-A-R-SD-1.0

| | | | |
|-------------------|------------------|------|-------|
| TITLE | SNT-4A-A-Reel | | |
| No. | PF004-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.).

※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

- 注意
1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
 2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm以下にしてください。
 3. マスク開口サイズと開口位置はランドパターンと合わせてください。
 4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).

※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.

2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.

3. Match the mask aperture size and aperture position with the land pattern.

4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.).

※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。

2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。

3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。

4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PF004-A-L-SD-4.1

| | |
|-------------------|----------------------------------|
| TITLE | SNT-4A-A -Land Recommendation |
| No. | PF004-A-L-SD-4.1 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |

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