# HIGH-SPEED 3.3V 16/8K X 9 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

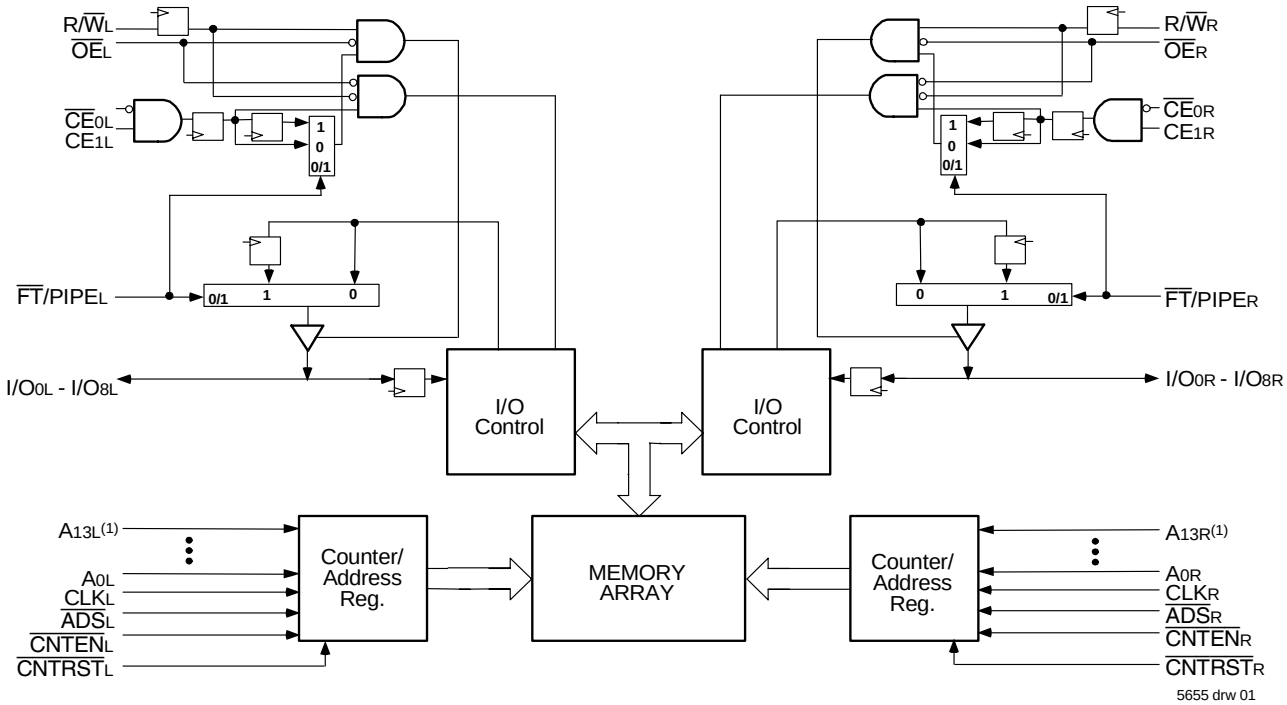
**IDT70V9169/59L**

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

## Features:

- **True Dual-Ported memory cells which allow simultaneous access of the same memory location**
- **High-speed clock to data access**
  - *Commercial: 6.5/7.5/9ns (max.)*
  - *Industrial: 7.5ns (max.)*
- **Low-power operation**
  - *IDT70V916/59L/59L*
    *Active: 450mW (typ.)*
    *Standby: 1.5mW (typ.)*
- **Flow-Through or Pipelined output mode on either port via the $\overline{FT}$/PIPE pins**
- **Counter enable and reset features**
- **Dual chip enables allow for depth expansion without additional logic**
- **Full synchronous operation on both ports**
  - *3.5ns setup to clock and 0ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 6.5ns clock to data out in the Pipelined output mode*
  - *Self-timed write allows fast cycle time*
  - *10ns cycle time, 100MHz operation in Pipelined output mode*
- **Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility**
- **LVTTL- compatible, single 3.3V (±0.3V) power supply**
- **Industrial temperature range (–40°C to +85°C) is available for 83 MHz**
- **Available in a 100-pin Thin Quad Flatpack (TQFP) and 100-pin fine pitch Ball Grid Array (fpBGA) packages.**

## Functional Block Diagram




**NOTE:**

1. $A_{13}$ is a NC for IDT70V9159.

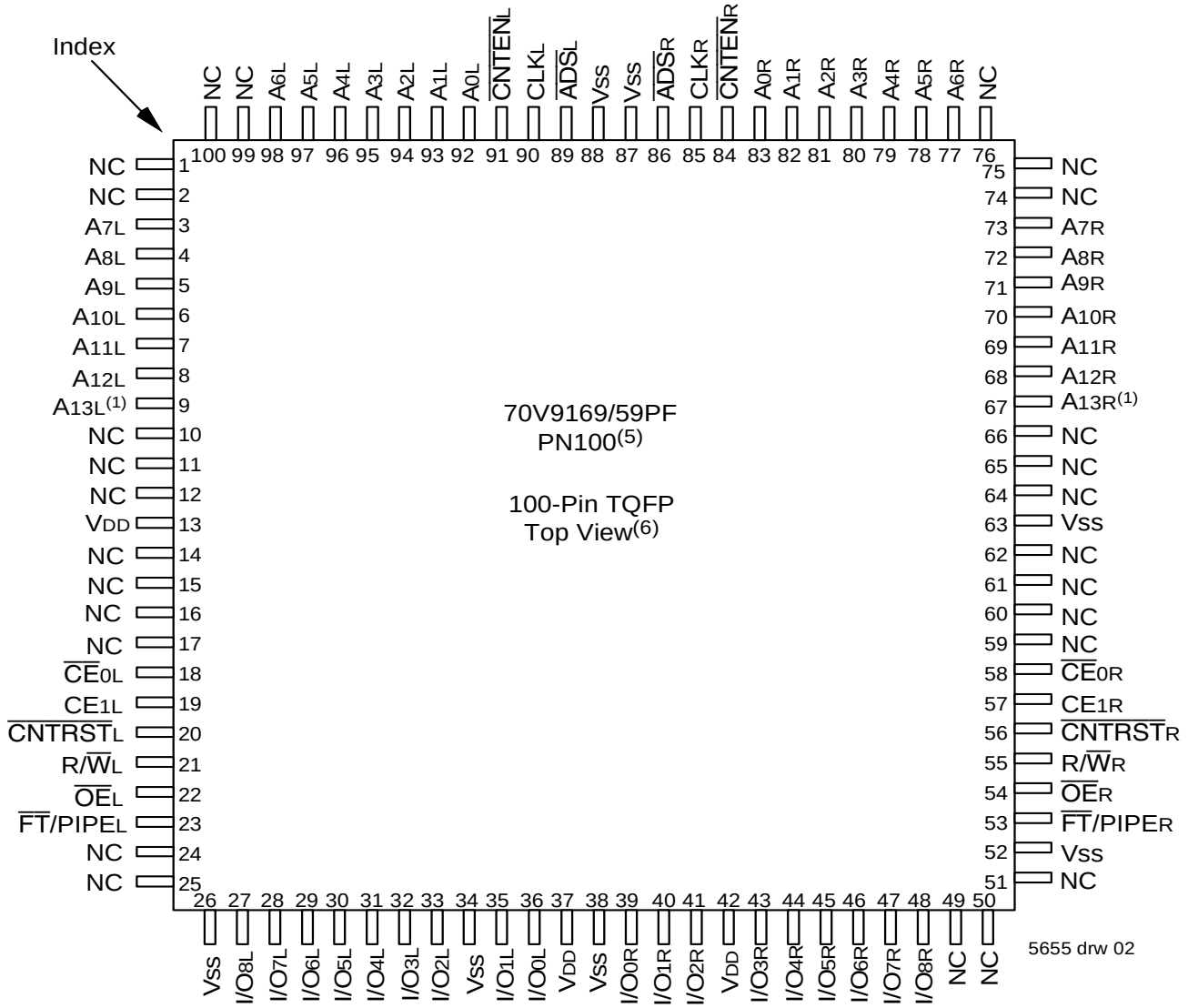
FEBRUARY 2018

## Description:

The IDT70V9169/59 is a high-speed 16/8K x 9 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9169/59 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and $CE_1$, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 450mW of power.

## Pin Configurations[1,2,3,4]




**NOTES:**

1. $A_{13}$ is a NC for IDT70V9159.
2. All $V_{DD}$ pins must be connected to power supply.
3. All $V_{SS}$ pins must be connected to ground supply.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Configurations(cont'd)[1,2,3,4]

70V9169/59PF
BF100[5]

100-Pin fpBGA
Top View[6]

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A1 $A_{6R}$ | A2 $A_{9R}$ | A3 $A_{12R}$ | A4 NC | A5 $V_{SS}$ | A6 $V_{SS}$ | A7 NC | A8 $R/\overline{W}_R$ | A9 $V_{SS}$ | A10 NC |
| B1 $A_{4R}$ | B2 $A_{5R}$ | B3 $A_{8R}$ | B4 $A_{10R}$ | B5 NC | B6 NC | B7 NC | B8 $\overline{OE}_R$ | B9 NC | B10 $I/O_{6R}$ |
| C1 $A_{3R}$ | C2 NC | C3 NC | C4 $A_{7R}$ | C5 NC | C6 $\overline{CE}_{0R}$ | C7 $CE_{1R}$ | C8 $PL/\overline{FT}_R$ | C9 $I/O_{7R}$ | C10 $I/O_{3R}$ |
| D1 $A_{0R}$ | D2 $CLK_R$ | D3 $A_{1R}$ | D4 $A_{2R}$ | D5 $A_{11R}$ | D6 $A_{13R}$[1] | D7 $\overline{CNTRST}_R$ | D8 $I/O_{8R}$ | D9 $I/O_{5R}$ | D10 $I/O_{1R}$ |
| E1 $V_{SS}$ | E2 $\overline{ADS}_R$ | E3 $\overline{CNTEN}_R$ | E4 $A_{1L}$ | E5 $\overline{ADS}_L$ | E6 $V_{SS}$ | E7 $I/O_{4R}$ | E8 $I/O_{2R}$ | E9 $I/O_{0R}$ | E10 $V_{DD}$ |
| F1 $V_{SS}$ | F2 $CLK_L$ | F3 $A_{0L}$ | F4 $A_{3L}$ | F5 $V_{DD}$ | F6 $V_{SS}$ | F7 $V_{DD}$ | F8 $I/O_{2L}$ | F9 $I/O_{1L}$ | F10 $I/O_{0L}$ |
| G1 $\overline{CNTEN}_L$ | G2 NC | G3 $A_{5L}$ | G4 $A_{12L}$ | G5 NC | G6 $R/\overline{W}_L$ | G7 NC | G8 $I/O_{4L}$ | G9 $V_{SS}$ | G10 $I/O_{3L}$ |
| H1 $A_{2L}$ | H2 $A_{4L}$ | H3 $A_{9L}$ | H4 $A_{13L}$[1] | H5 NC | H6 $CE_{1L}$ | H7 NC | H8 $I/O_{7L}$ | H9 $I/O_{6L}$ | H10 $I/O_{5L}$ |
| J1 NC | J2 $A_{7L}$ | J3 $A_{10L}$ | J4 NC | J5 NC | J6 NC | J7 $\overline{OE}_L$ | J8 $V_{SS}$ | J9 $V_{SS}$ | J10 $I/O_{8L}$ |
| K1 $A_{6L}$ | K2 $A_{8L}$ | K3 $A_{11L}$ | K4 NC | K5 $V_{DD}$ | K6 $V_{DD}$ | K7 $\overline{CE}_{0L}$ | K8 $\overline{CNTRST}_L$ | K9 $PL/\overline{FT}_L$ | K10 NC |

5655 drw 03

**NOTES:**
1. $A_{13}$ is a NC for IDT70V9159.
2. All $V_{DD}$ pins must be connected to power supply.
3. All $V_{SS}$ pins must be connected to ground supply.
4. Package body is approximately 10mm x 10mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Names

| Left Port | Right Port | Names |
|---|---|---|
| $\overline{CE}_{0L}$, $CE_{1L}$ | $\overline{CE}_{0R}$, $CE_{1R}$ | Chip Enables |
| R/$\overline{W}_L$ | R/$\overline{W}_R$ | Read/Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $A_{0L}$ - $A_{13L}$(1) | $A_{0R}$ - $A_{13R}$(1) | Address |
| $I/O_{0L}$ - $I/O_{8L}$ | $I/O_{0R}$ - $I/O_{8R}$ | Data Input/Output |
| $CLK_L$ | $CLK_R$ | Clock |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | Address Strobe |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | Counter Enable |
| $\overline{CNTRST}_L$ | $\overline{CNTRST}_R$ | Counter Reset |
| $\overline{FT}$/$PIPE_L$ | $\overline{FT}$/$PIPE_R$ | Flow-Through/Pipeline |
| $V_{DD}$ | | Power (3.3V) |
| $V_{SS}$ | | Ground (0V) |

5655 tbl 01

**NOTE:**
1. $A_{13}$ is a NC for IDT70V9159.

## Truth Table I—Read/Write and Enable Control(1,2,3)

| $\overline{OE}$ | CLK | $\overline{CE}_0$ | $CE_1$ | R/$\overline{W}$ | $I/O_{0-8}$ | Mode |
|---|---|---|---|---|---|---|
| X | ↑ | H | X | X | High-Z | Deselected—Power Down |
| X | ↑ | X | L | X | High-Z | Deselected—Power Down |
| X | ↑ | L | H | L | $DATA_{IN}$ | Write |
| L | ↑ | L | H | H | $DATA_{OUT}$ | Read |
| H | X | L | H | X | High-Z | Outputs Disabled |

5655 tbl 02

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = X.
3. $\overline{OE}$ is an asynchronous input signal.

## Truth Table II—Address Counter Control(1,2)

| External Address | Previous Internal Address | Internal Address Used | CLK | $\overline{ADS}$ | $\overline{CNTEN}$ | $\overline{CNTRST}$ | I/O(3) | MODE |
|---|---|---|---|---|---|---|---|---|
| An | X | An | ↑ | L(4) | X | H | DI/O (n) | External Address Used |
| X | An | An + 1 | ↑ | H | L(5) | H | DI/O(n+1) | Counter Enabled—Internal Address generation |
| X | An + 1 | An + 1 | ↑ | H | H | H | DI/O(n+1) | External Address Blocked—Counter disabled (An + 1 reused) |
| X | X | A0 | ↑ | X | X | L(4) | DI/O(0) | Counter Reset to Address 0 |

5655 tbl 03

**NOTES:**
1. "H" = $V_{IH}$, "L" = $V_{IL}$, "X" = Don't Care.
2. $\overline{CE_0}$, $\overline{LB}$, $\overline{UB}$, and $\overline{OE}$ = $V_{IL}$; $CE_1$ and R/$\overline{W}$ = $V_{IH}$.
3. Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. $\overline{ADS}$ and $\overline{CNTRST}$ are independent of all other signals including $\overline{CE_0}$, $CE_1$, $\overline{UB}$ and $\overline{LB}$.
5. The address counter advances if $\overline{CNTEN}$ = $V_{IL}$ on the rising edge of CLK, regardless of all other signals including $\overline{CE_0}$, $CE_1$, $\overline{UB}$ and $\overline{LB}$.

## Recommended Operating Temperature and Supply Voltage

| Grade | Ambient Temperature(1) | GND | $V_{DD}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C | 0V | 3.3V ± 0.3V |

5655 tbl 04

**NOTES:**
1. This is the parameter $T_A$. This is the "instant on" case temperature.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| $V_{SS}$ | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | — | $V_{DD}$+0.3V(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.3(1) | — | 0.8 | V |

5655 tbl 05

**NOTES:**
1. $V_{IL}$ ≥ -1.5V for pulse width less than 10 ns.
2. $V_{TERM}$ must not exceed $V_{DD}$+0.3V.

## Absolute Maximum Ratings(1)

| Symbol | Rating | Commercial & Industrial | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | 50 | mA |

5655 tbl 06

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed $V_{DD}$ +0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM}$ ≥ $V_{DD}$ + 0.3V.

## Capacitance(1)
($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter | Conditions(2) | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 9 | pF |
| $C_{OUT}$(3) | Output Capacitance | $V_{OUT}$ = 3dV | 10 | pF |

5655 tbl 07

**NOTES:**
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. $C_{OUT}$ also references $C_{I/O}$.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD}$= 3.3V ± 0.3V)

| Symbol | Parameter | Test Conditions | 70V9169/59L | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current[1] | $V_{DD}$ = 3.6V, $V_{IN}$ = 0V to $V_{DD}$ | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{CE}$ = $V_{IH}$ or $CE_1$ = $V_{IL}$, $V_{OUT}$ = 0V to $V_{DD}$ | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = +4mA | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA | 2.4 | — | V |

5655 tbl 08

**NOTE:**
1. At $V_{DD}$ ≤ 2.0V input leakages are undefined.

## DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[3] ($V_{DD}$ = 3.3V ± 0.3V)

| Symbol | Parameter | Test Condition | Version | | 70V9169/59L6 Com'l Only | | 70V9169/59L7 Com'l & Ind | | 70V9169/59L9 Com'l Only | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Typ.[4] | Max. | Typ.[4] | Max. | Typ.[4] | Max. | |
| $I_{DD}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$= $V_{IL}$, Outputs Disabled, f = $f_{MAX}$[1] | COM'L | L | 175 | 330 | 155 | 280 | 135 | 230 | mA |
| | | | IND | L | — | — | 155 | 330 | — | — | |
| $I_{SB1}$ | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ = $\overline{CE}_R$ = $V_{IH}$ f = $f_{MAX}$[1] | COM'L | L | 50 | 80 | 40 | 70 | 30 | 60 | mA |
| | | | IND | L | — | — | 40 | 80 | — | — | |
| $I_{SB2}$ | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$[5] Active Port Outputs Disabled, f=$f_{MAX}$[1] | COM'L | L | 115 | 185 | 105 | 170 | 95 | 155 | mA |
| | | | IND | L | — | — | 105 | 180 | — | — | |
| $I_{SB3}$ | Full Standby Current (Both Ports - CMOS Level Inputs) | Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ $V_{DD}$ - 0.2V, $V_{IN}$ ≥ $V_{DD}$- 0.2V or $V_{IN}$ ≤ 0.2V, f = 0[2] | COM'L | L | 0.5 | 3.0 | 0.5 | 3.0 | 0.5 | 3.0 | mA |
| | | | IND | L | — | — | 0.5 | 3.0 | — | — | |
| $I_{SB4}$ | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ $V_{DD}$ - 0.2V[5] $V_{IN}$ ≥ $V_{DD}$- 0.2V or $V_{IN}$ ≤ 0.2V, Active Port, Outputs Disabled, f = $f_{MAX}$[1] | COM'L | L | 105 | 175 | 95 | 160 | 85 | 145 | mA |
| | | | IND | L | — | — | 95 | 175 | — | — | |

5655 tbl 09

**NOTES:**
1. At f = $f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/$t_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. $V_{DD}$ = 3.3V, $T_A$ = 25°C for Typ, and are not production tested. $I_{CC\,DC}$(f=0) = 90mA (Typ).
5. $\overline{CE}_X$ = $V_{IL}$ means $\overline{CE}_{0X}$ = $V_{IL}$ and $CE_{1X}$ = $V_{IH}$
   $\overline{CE}_X$ = $V_{IH}$ means $\overline{CE}_{0X}$ = $V_{IH}$ or $CE_{1X}$ = $V_{IL}$
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and $CE_{1X}$ ≥ $V_{DD}$ - 0.2V
   $\overline{CE}_X$ ≥ $V_{DD}$ - 0.2V means $\overline{CE}_{0X}$ ≥ $V_{DD}$ - 0.2V or $CE_{1X}$ ≤ 0.2V
   "X" represents "L" for left port or "R" for right port.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 2ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1, 2 & 3 |

5655 tbl 10

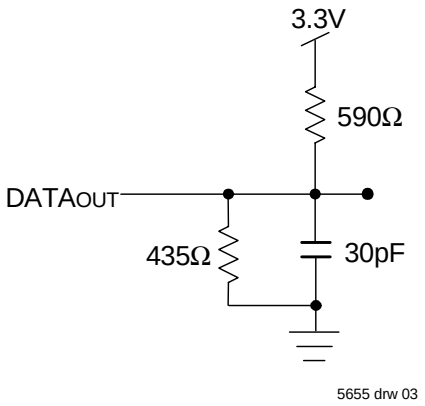



**Figure 1. AC Output Test load.**

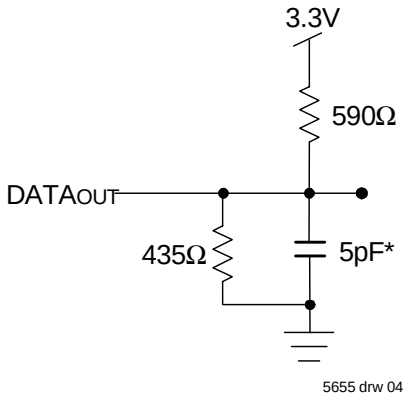



**Figure 2. Output Test Load (For $t_{CKLZ}$, $t_{CKHZ}$, $t_{OLZ}$, and $t_{OHZ}$).**
*Including scope and jig.

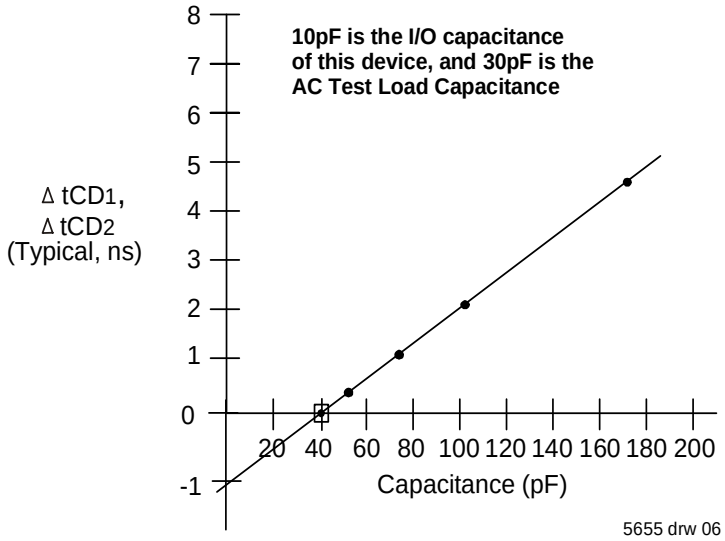



**Figure 3. Typical Output Derating (Lumped Capacitive Load).**

# AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3] ( $V_{DD}$= 3.3V ± 0.3V, $T_A$ = 0°C to +70°C)

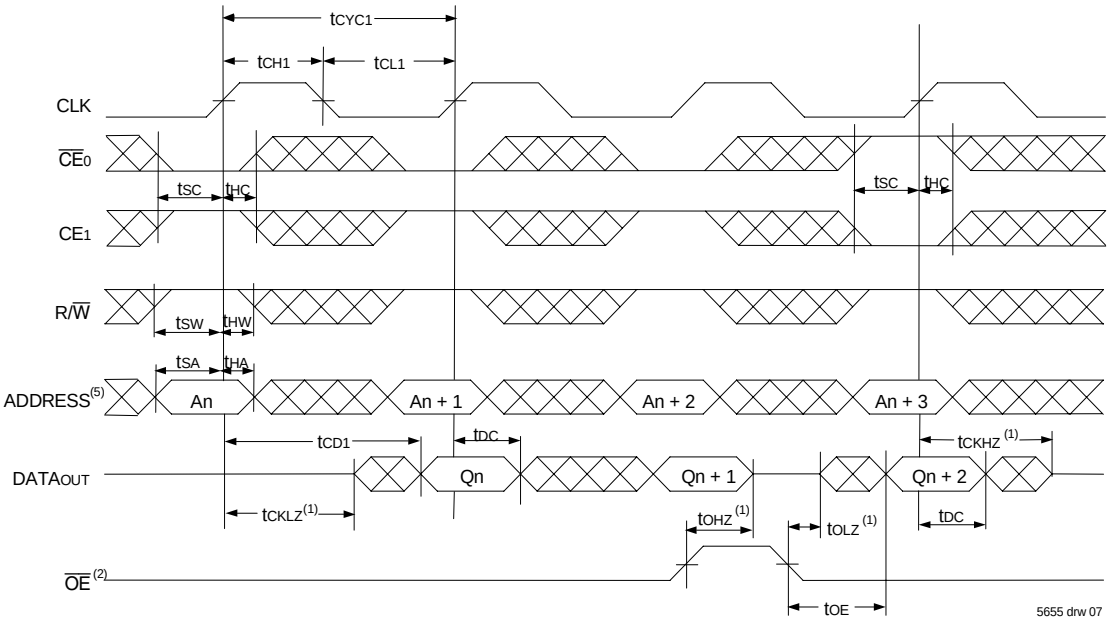
| | | 70V9169/59L6 Com'l Only | | 70V9169/59L7 Com'l & Ind | | 70V9169/59L9 Com'l Only | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Unit** |
| $t_{CYC1}$ | Clock Cycle Time (Flow-Through)[2] | 19 | — | 22 | — | 25 | — | ns |
| $t_{CYC2}$ | Clock Cycle Time (Pipelined)[2] | 10 | — | 12 | — | 15 | — | ns |
| $t_{CH1}$ | Clock High Time (Flow-Through)[2] | 6.5 | — | 7.5 | — | 12 | — | ns |
| $t_{CL1}$ | Clock Low Time (Flow-Through)[2] | 6.5 | — | 7.5 | — | 12 | — | ns |
| $t_{CH2}$ | Clock High Time (Pipelined)[2] | 4 | — | 5 | — | 6 | — | ns |
| $t_{CL2}$ | Clock Low Time (Pipelined)[2] | 4 | — | 5 | — | 6 | — | ns |
| $t_R$ | Clock Rise Time | — | 3 | — | 3 | — | 3 | ns |
| $t_F$ | Clock Fall Time | — | 3 | — | 3 | — | 3 | ns |
| $t_{SA}$ | Address Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HA}$ | Address Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SC}$ | Chip Enable Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HC}$ | Chip Enable Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SB}$ | Byte Enable Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HB}$ | Byte Enable Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SW}$ | R/$\overline{W}$ Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HW}$ | R/$\overline{W}$ Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SD}$ | Input Data Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HD}$ | Input Data Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SAD}$ | $\overline{ADS}$ Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HAD}$ | $\overline{ADS}$ Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SCN}$ | $\overline{CNTEN}$ Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HCN}$ | $\overline{CNTEN}$ Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{SRST}$ | $\overline{CNTRST}$ Setup Time | 3.5 | — | 4 | — | 4 | — | ns |
| $t_{HRST}$ | $\overline{CNTRST}$ Hold Time | 0 | — | 0 | — | 1 | — | ns |
| $t_{OE}$ | Output Enable to Data Valid | — | 6.5 | — | 7.5 | — | 9 | ns |
| $t_{OLZ}$ | Output Enable to Output Low-Z[1] | 2 | — | 2 | — | 2 | — | ns |
| $t_{OHZ}$ | Output Enable to Output High-Z[1] | 1 | 7 | 1 | 7 | 1 | 7 | ns |
| $t_{CD1}$ | Clock to Data Valid (Flow-Through)[2] | — | 15 | — | 18 | — | 20 | ns |
| $t_{CD2}$ | Clock to Data Valid (Pipelined)[2] | — | 6.5 | — | 7.5 | — | 9 | ns |
| $t_{DC}$ | Data Output Hold After Clock High | 2 | — | 2 | — | 2 | — | ns |
| $t_{CKHZ}$ | Clock High to Output High-Z[1] | 2 | 9 | 2 | 9 | 2 | 9 | ns |
| $t_{CKLZ}$ | Clock High to Output Low-Z[1] | 2 | — | 2 | — | 2 | — | ns |
| **Port-to-Port Delay** | | | | | | | | |
| $t_{CWDD}$ | Write Port Clock High to Read Data Delay | — | 24 | — | 28 | — | 35 | ns |
| $t_{CCS}$ | Clock-to-Clock Setup Time | — | 9 | — | 10 | — | 15 | ns |

5655 tbl 11

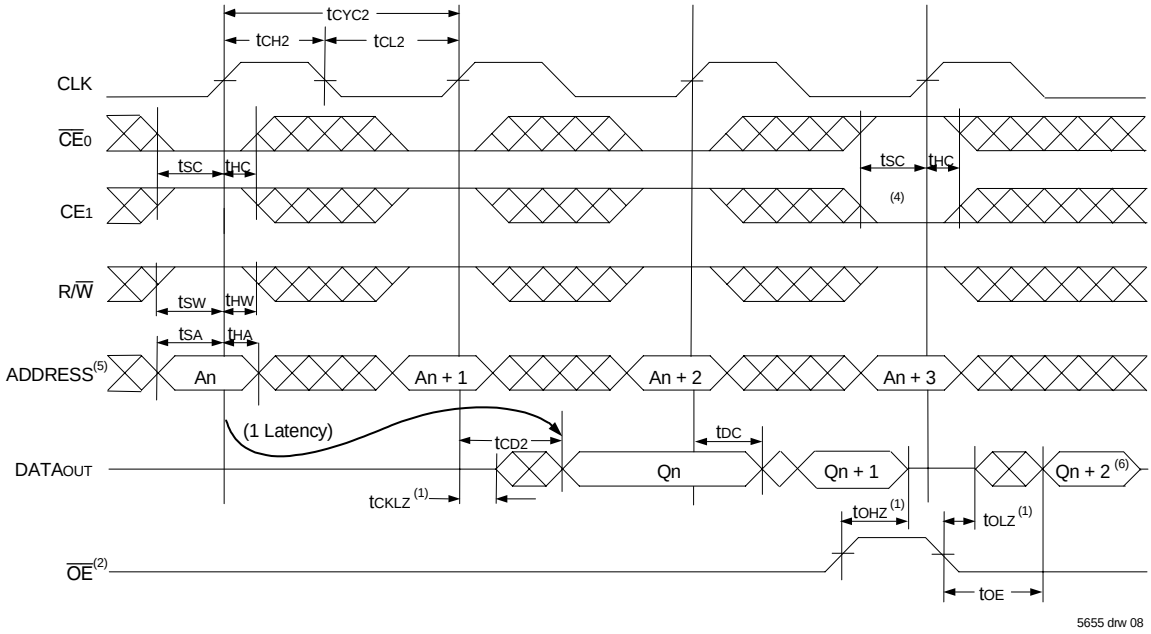
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters ($t_{CYC2}$, $t_{CD2}$) apply to either or both the Left and Right ports when $\overline{FT}$/PIPE = $V_{IH}$. Flow-through parameters ($t_{CYC1}$, $t_{CD1}$) apply when $\overline{FT}$/PIPE = $V_{IL}$ for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$), $\overline{FT}$/PIPE$_R$, and $\overline{FT}$/PIPE$_L$.

## Timing Waveform of Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE"X" = $V_{IL}$)(3,6)



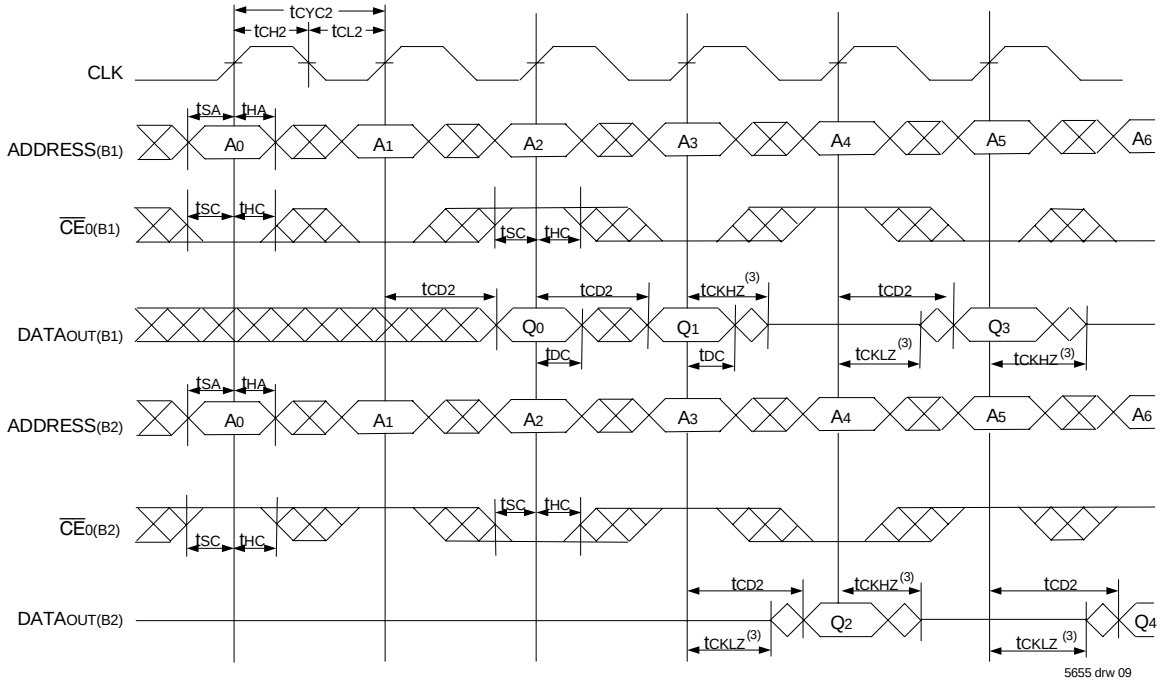

## Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE"X" = $V_{IH}$)(3,6)



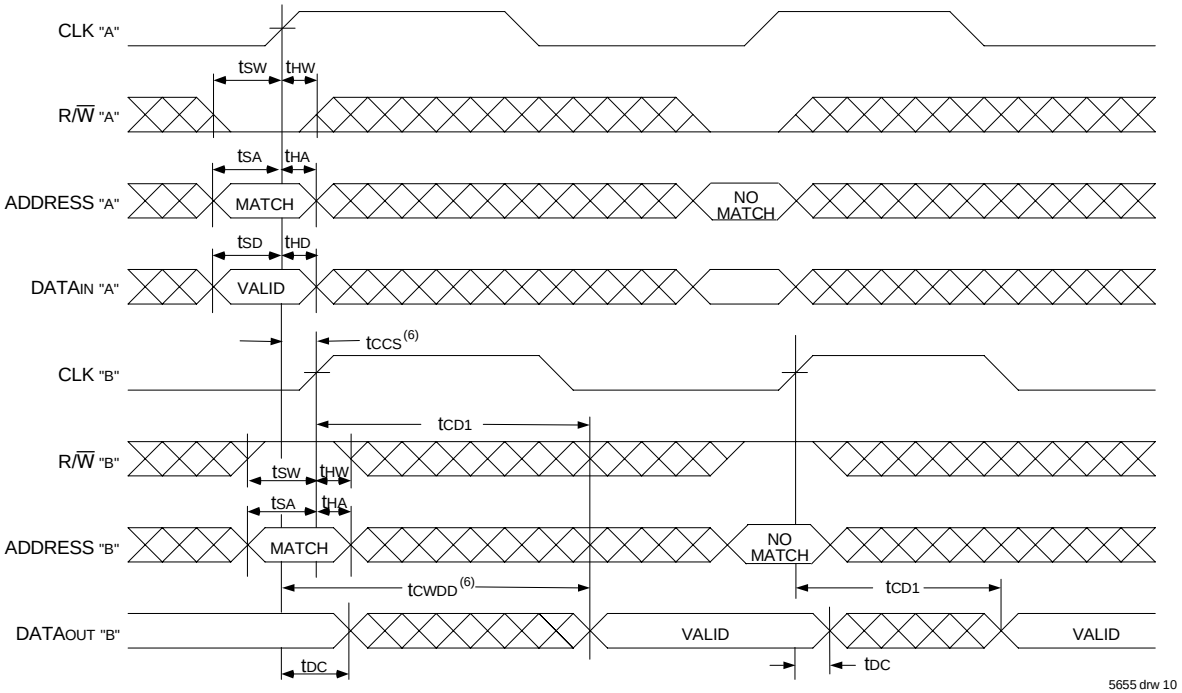

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $\overline{ADS}$ = $V_{IL}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = $V_{IH}$.
4. The output is disabled (High-Impedance state) by $\overline{CE}_0$ = $V_{IH}$, $CE_1$ = $V_{IL}$ following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since ADS = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. "X' here denotes Left or Right port. The diagram is with respect to that port.

## Timing Waveform of a Bank Select Pipelined Read(1,2)



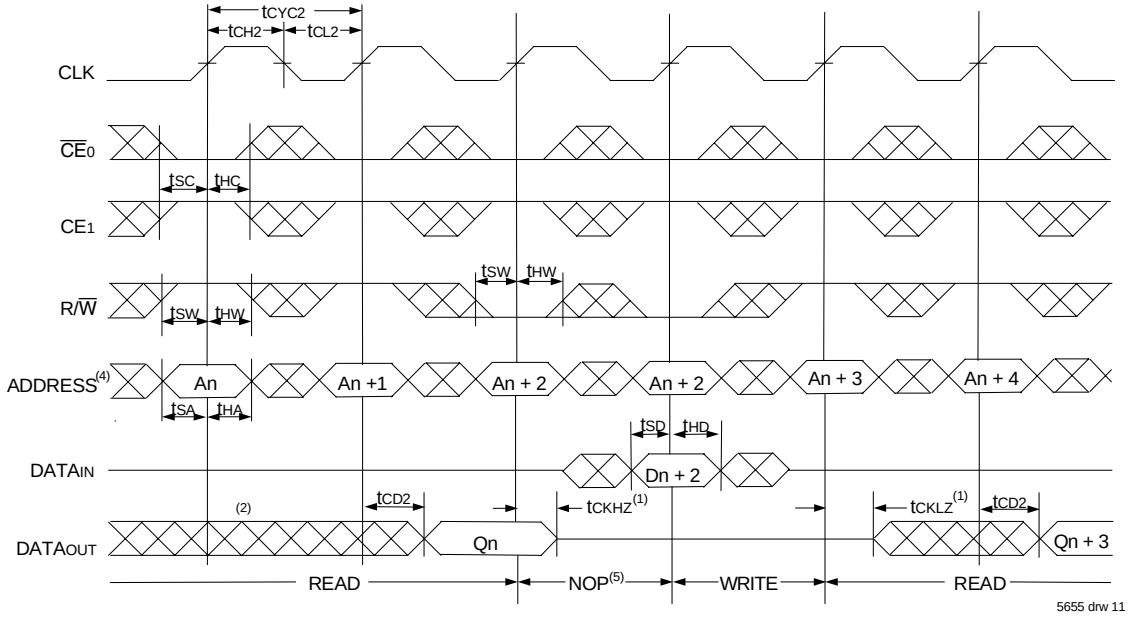

## Timing Waveform with Port-to-Port Flow-Through Read(4,5,7)



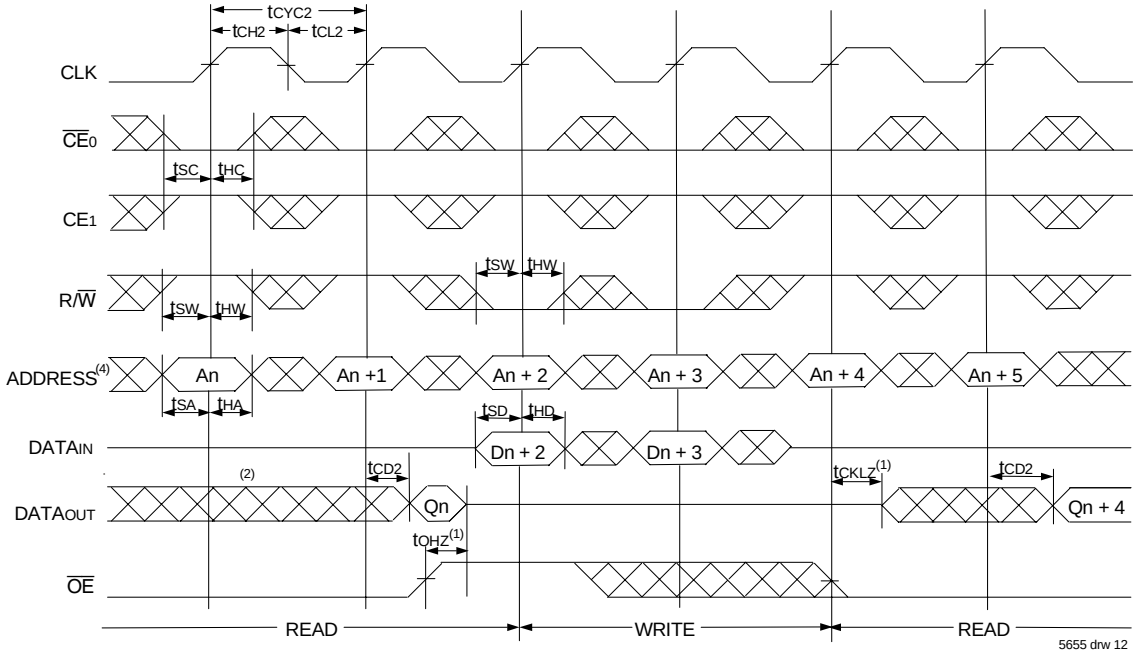

**NOTES:**

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V916/59L for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{OE}$ and $\overline{ADS}$ = $V_{IL}$; $CE_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = $V_{IH}$.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. $\overline{CE}_0$ and $\overline{ADS}$ = $V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{CNTRST}$ = $V_{IH}$.
5. $\overline{OE}$ = $V_{IL}$ for the Right Port, which is being read from. $\overline{OE}$ = $V_{IH}$ for the Left Port, which is being written to.
6. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for $t_{CWDD}$.
   If $t_{CCS}$ > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD1}$. $t_{CWDD}$ does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



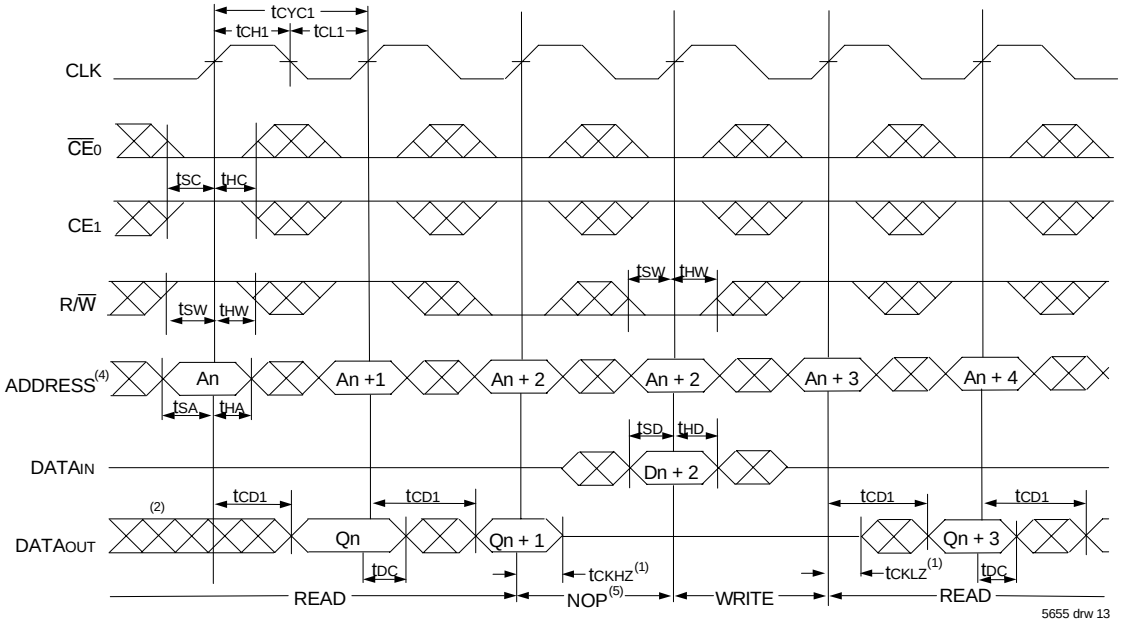

## Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)



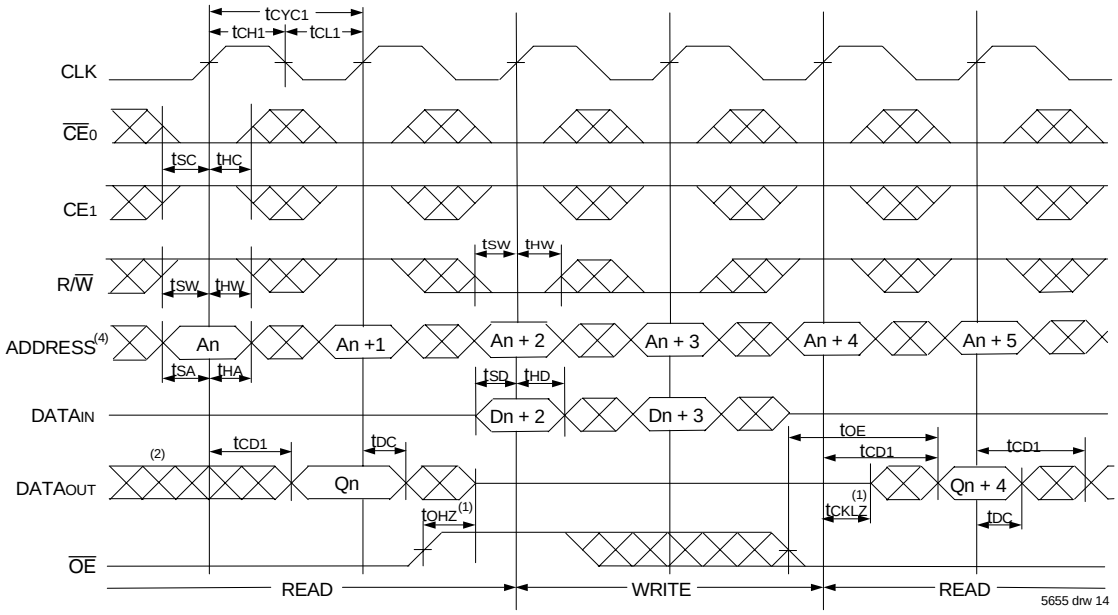

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$ and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since ADS = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = VIL)(3)



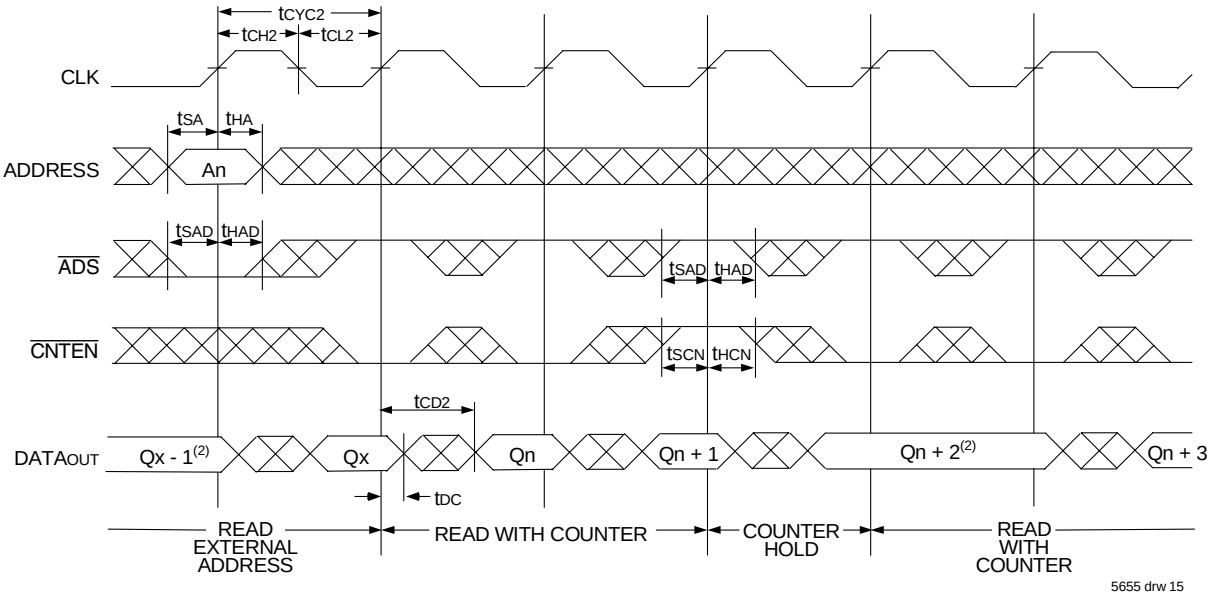

## Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)




**NOTES:**

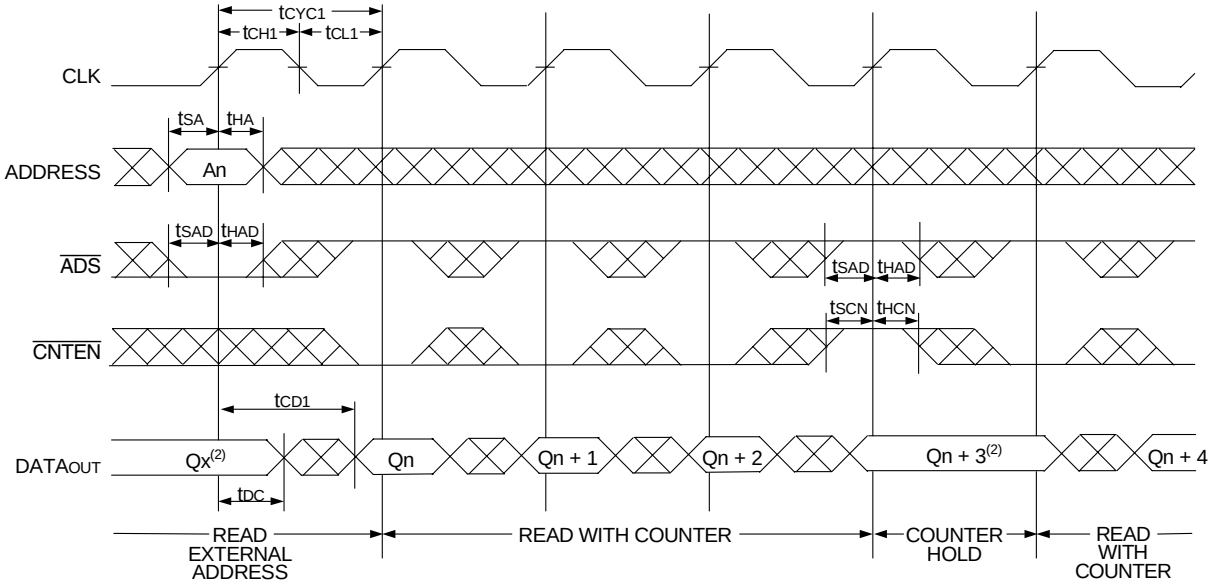
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$ and $\overline{ADS}$ = VIL; CE1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = VIH. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = VIL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

## Timing Waveform of Pipelined Read with Address Counter Advance(1)




5655 drw 15

## Timing Waveform of Flow-Through Read with Address Counter Advance(1)

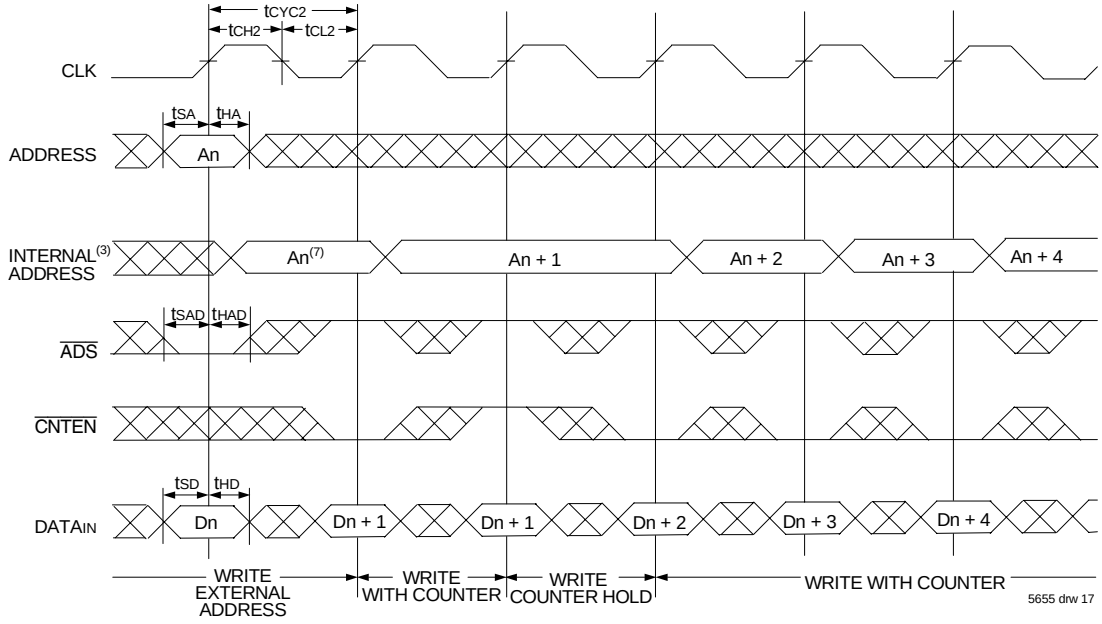



5655 drw 16

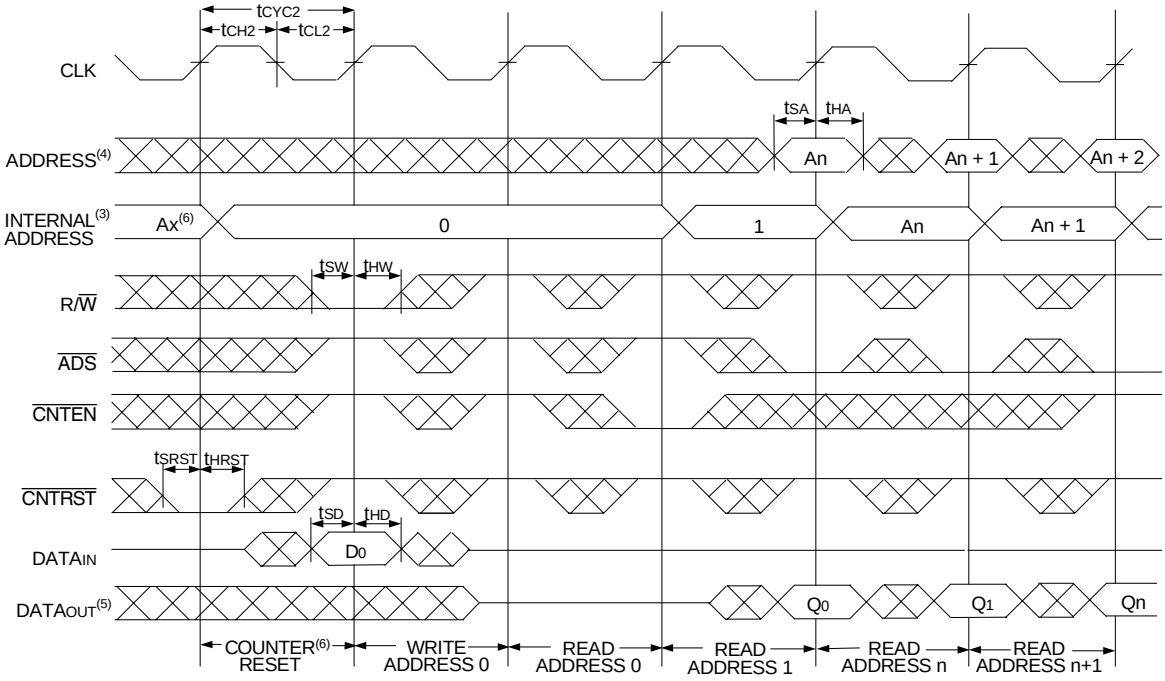
**NOTES:**

1. $\overline{CE_0}$ and $\overline{OE}$ = $V_{IL}$; $CE_1$, R/$\overline{W}$, and $\overline{CNTRST}$ = $V_{IH}$.
2. If there is no address change via $\overline{ADS}$ = $V_{IL}$ (loading a new address) or $\overline{CNTEN}$ = $V_{IL}$ (advancing the address), i.e. $\overline{ADS}$ = $V_{IH}$ and $\overline{CNTEN}$ = $V_{IH}$, then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)(1)




## Timing Waveform of Counter Reset (Pipelined Outputs)(2)




**NOTES:**

1. $\overline{CE_0}$ and R/$\overline{W}$ = $V_{IL}$; $CE_1$ and $\overline{CNTRST}$ = $V_{IH}$.
2. $\overline{CE_0}$ = $V_{IL}$; $CE_1$ = $V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = $V_{IL}$ and equals the counter output when $\overline{ADS}$ = $V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle. $ADDR_0$ will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN}$ = $V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

## Functional Description

The IDT70V9169/59 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

$\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9169/59's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$ to re-activate the outputs.

## Depth and Width Expansion

The IDT70V9169/59 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9169/59 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.

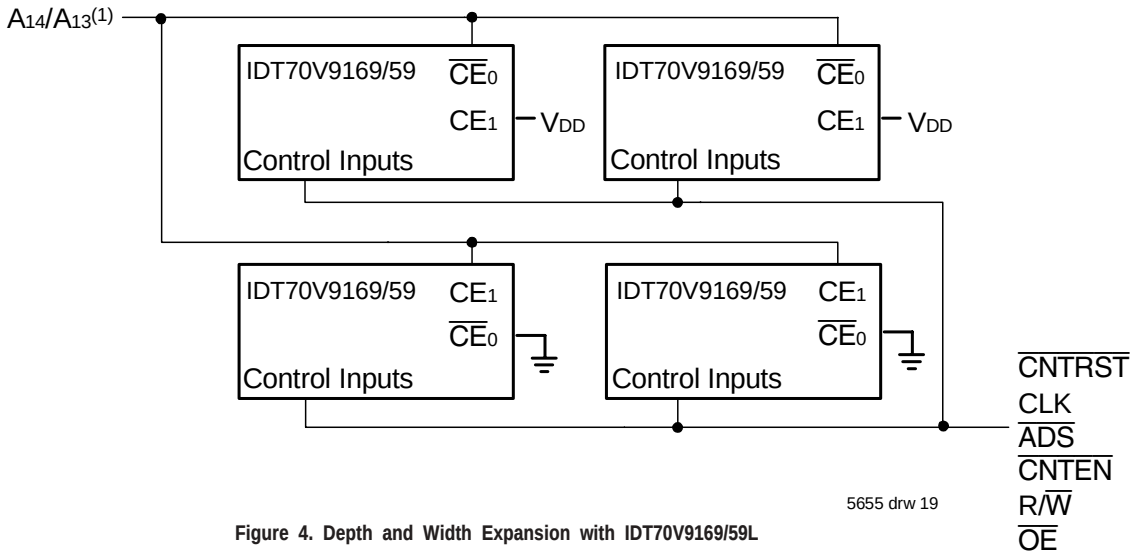
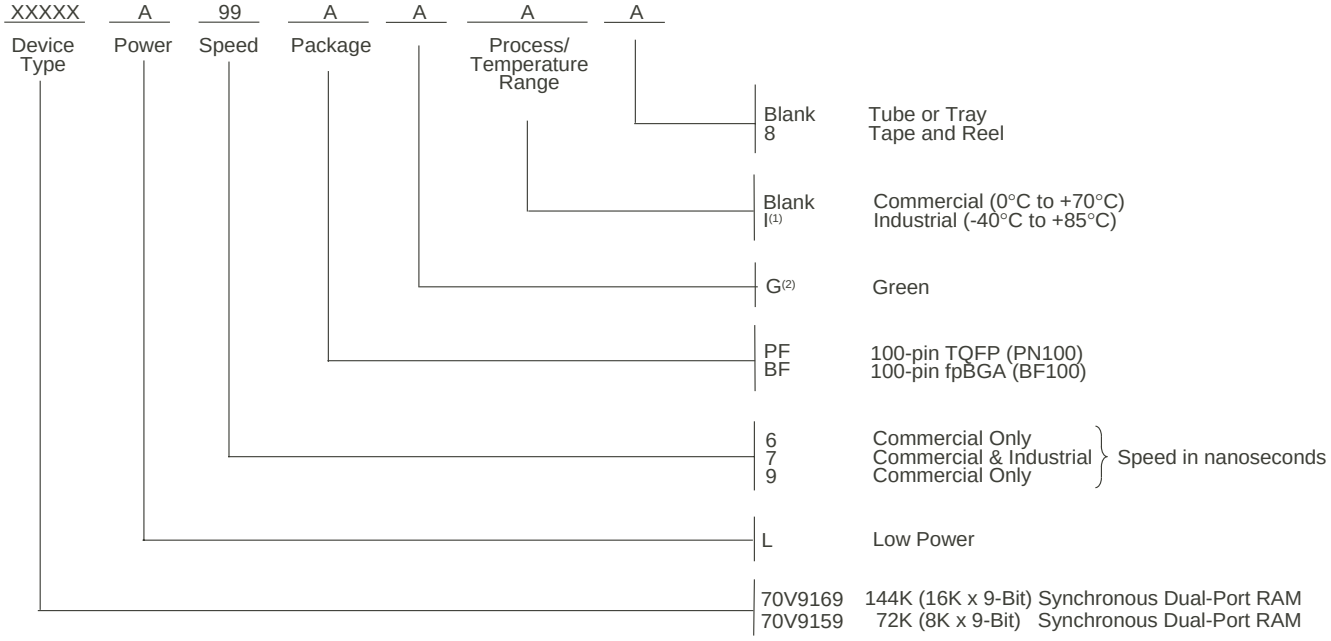



**Figure 4. Depth and Width Expansion with IDT70V9169/59L**

**NOTE:**
1. A14 is for IDT70V9169, $A_{13}$ is for IDT70V9159.

## Ordering Information




5655 drw 20

**NOTES:**

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers see your sales office.
   LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

## IDT Clock Solution for IDT70V9169/59 Dual-Port

| IDT Dual-Port Part Number | Dual-Port I/O Specitications | | Clock Specifications | | | | IDT PLL Clock Device | IDT Non-PLL Clock Device |
|---|---|---|---|---|---|---|---|---|
| | Voltage | I/O | Input Capacitance | Input Duty Cycle Requirement | Maximum Frequency | Jitter Tolerance | | |
| 70V9169/59 | 3.3 | LVTTL | 9pF | 40% | 100 | 150ps | IDT2305<br>IDT2308<br>IDT2309 | FCT3805<br>FCT3805D/E<br>FCT3807<br>FCT3807D/E |

5638 tbl 12

## Datasheet Document History

| | |
|---|---|
| 07/08/02: | Initial Public Release |
| 08/15/03: | Removed Preliminary status |
| | Page 16 Added IDT Clock Solution Table |
| 01/29/09: | Page 16 Removed "IDT" from orderable part number |
| 06/18/15: | Page 2 Removed IDT with reference to fabrication |
| | Page 2 Removed date from 100-pin TQFP configuration |
| | Page 2 & 16 The package code PN100-1 changed to PN100 to match standard package codes |
| | Page 3 Removed date from 100-pin fpBGA configuration |
| | Page 6 Corrected typo in the Typical Output Derating drawing |
| | Page 16 Added Tape and Reel and Green indicators and updated the footnotes to the Ordering Information |
| 02/21/18: | Product Discontinuation Notice - PDN# SP-17-02 |
| | Last time buy expires June 15, 2018 |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/


### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.