

Features

- ◆ 256K x 16 advanced high-speed CMOS Static RAM
- ◆ JEDEC Center Power / GND pinout for reduced noise.
- ◆ Equal access and cycle times
 - Commercial and Industrial: 10/12/15ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional data inputs and outputs directly LVTTTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Upper and Lower Byte Enable Pins
- ◆ Single 3.3V power supply
- ◆ Available in 44-pin, 400 mil plastic SOJ package and a 44-pin, 400 mil TSOP Type II package and a 48 ball grid array, 9mm x 9mm package.
- ◆ Green parts available, see ordering information

Description

The IDT71V416 is a 4,194,304-bit high-speed Static RAM organized as 256K x 16. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71V416 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71V416 are LVTTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V416 is packaged in a 44-pin, 400 mil Plastic SOJ and a 44-pin, 400 mil TSOP Type II package and a 48 ball grid array, 9mm x 9mm package.

Functional Block Diagram



3624 drw 01

Pin Configurations - SOJ/TSOP



3624 drw 02

*Pin 28 can either be a NC or connected to Vss

Top View

Pin Descriptions

| | | |
|--------------|-------------------|-------|
| A0 - A17 | Address Inputs | Input |
| CS | Chip Select | Input |
| WE | Write Enable | Input |
| OE | Output Enable | Input |
| BHE | High Byte Enable | Input |
| BLE | Low Byte Enable | Input |
| I/O0 - I/O15 | Data Input/Output | I/O |
| VDD | 3.3V Power | Pwr |
| VSS | Ground | Gnd |

3624 tbl 01

Pin Configurations - 48 BGA

71V416BE
BE48
48- BGA



3624 tbl 11

Top View

SOJ Capacitance

(TA = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|--------|--------------------------|------------|------|------|
| CIN | Input Capacitance | VIN = 3dV | 7 | pF |
| CIO | I/O Capacitance | VOUT = 3dV | 8 | pF |

3624 tbl 02

48 BGA Capacitance

(TA = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|--------|--------------------------|------------|------|------|
| CIN | Input Capacitance | VIN = 3dV | 6 | pF |
| CIO | I/O Capacitance | VOUT = 3dV | 7 | pF |

3624 tbl 02b

NOTE:

1. This parameter is guaranteed by device characterization, but not production tested.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Value | Unit |
|------------------------------------|--|------------------------------|------|
| V _{DD} | Supply Voltage Relative to V _{SS} | -0.5 to +4.6 | V |
| V _{IN} , V _{OUT} | Terminal Voltage Relative to V _{SS} | -0.5 to V _{DD} +0.5 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -55 to +125 | °C |
| P _T | Power Dissipation | 1 | W |
| I _{OUT} | DC Output Current | 50 | mA |

3624 tbl 04

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | V _{SS} | V _{DD} |
|------------|----------------|-----------------|-----------------|
| Commercial | 0°C to +70°C | 0V | See Below |
| Industrial | -40°C to +85°C | 0V | See Below |

3624 tbl 05

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|-------------------------------------|------|
| V _{DD} | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{SS} | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.0 | — | V _{DD} +0.3 ⁽¹⁾ | V |
| V _{IL} | Input Low Voltage | -0.3 ⁽²⁾ | — | 0.8 | V |

3624 tbl 06

NOTES:

1. V_{IH} (max.) = V_{DD}+2V for pulse width less than 5ns, once per cycle.
2. V_{IL} (min.) = -2V for pulse width less than 5ns, once per cycle.

Truth Table⁽¹⁾

| \overline{CS} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Function |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------|
| H | X | X | X | X | High-Z | High-Z | Deselected - Standby |
| L | L | H | L | H | DATA _{OUT} | High-Z | Low Byte Read |
| L | L | H | H | L | High-Z | DATA _{OUT} | High Byte Read |
| L | L | H | L | L | DATA _{OUT} | DATA _{OUT} | Word Read |
| L | X | L | L | L | DATA _{IN} | DATA _{IN} | Word Write |
| L | X | L | L | H | DATA _{IN} | High-Z | Low Byte Write |
| L | X | L | H | L | High-Z | DATA _{IN} | High Byte Write |
| L | H | H | X | X | High-Z | High-Z | Outputs Disabled |
| L | X | X | H | H | High-Z | High-Z | Outputs Disabled |

3624 tbl 03

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't care.

DC Electrical Characteristics

(VDD = Min. to Max., Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | Test Conditions | IDT71V416 | | Unit |
|-----------------|------------------------|---|-----------|------|------|
| | | | Min. | Max. | |
| I _{LI} | Input Leakage Current | V _{CC} = Max., V _{IN} = V _{SS} to V _{DD} | — | 5 | μA |
| I _{LO} | Output Leakage Current | V _{DD} = Max., \overline{CS} = V _{IH} , V _{OUT} = V _{SS} to V _{DD} | — | 5 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 8mA, V _{DD} = Min. | — | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -4mA, V _{DD} = Min. | 2.4 | — | V |

3624 tbl 07

DC Electrical Characteristics^(1, 2, 3)

(VDD = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} - 0.2V)

| Symbol | Parameter | | 71V416S/L10 | | 71V416S/L12 | | 71V416S/L15 | | Unit |
|------------------|---|---|-------------|------|-------------|------|-------------|------|------|
| | | | Com'l. | Ind. | Com'l. | Ind. | Com'l. | Ind. | |
| I _{CC} | Dynamic Operating Current $\overline{CS} \leq V_{LC}$, Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽⁴⁾ | S | 200 | 200 | 180 | 180 | 170 | 170 | mA |
| | | L | 180 | 180 | 170 | 170 | 160 | 160 | |
| I _{SB} | Dynamic Standby Power Supply Current $\overline{CS} \geq V_{HC}$, Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽⁴⁾ | S | 70 | 70 | 60 | 60 | 50 | 50 | mA |
| | | L | 50 | 50 | 45 | 45 | 40 | 40 | |
| I _{SB1} | Full Standby Power Supply Current (static) $\overline{CS} \geq V_{HC}$, Outputs Open, V _{DD} = Max., f = 0 ⁽⁴⁾ | S | 20 | 20 | 20 | 20 | 20 | 20 | mA |
| | | L | 10 | 10 | 10 | 10 | 10 | 10 | |

3624 tbl 08

NOTES:

1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V_{DD} - 0.2V (High).
3. Power specifications are preliminary.
4. f_{MAX} = 1/t_{rc} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC Test Loads



3624 drw 03

Figure 1. AC Test Load



3624 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{ow}, and t_{whz})



3624 drw 05

Figure 3. Output Capacitive Derating

AC Test Conditions

| | |
|-------------------------------|-------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 1.5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | Figures 1,2 and 3 |

3624 tbl 09

AC Electrical Characteristics

(VDD = Min. to Max., Commercial and Industrial Temperature Ranges)

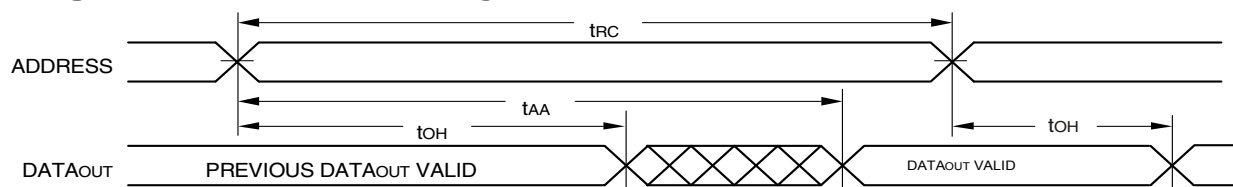
| Symbol | Parameter | 71V416S/L10 | | 71V416S/L12 | | 71V416S/L15 | | Unit |
|---------------------------------|--|-------------|------|-------------|------|-------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 10 | — | 12 | — | 15 | — | ns |
| t _{AA} | Address Access Time | — | 10 | — | 12 | — | 15 | ns |
| t _{ACS} | Chip Select Access Time | — | 10 | — | 12 | — | 15 | ns |
| t _{CLZ} ⁽¹⁾ | Chip Select Low to Output in Low-Z | 4 | — | 4 | — | 4 | — | ns |
| t _{CHZ} ⁽¹⁾ | Chip Select High to Output in High-Z | — | 5 | — | 6 | — | 7 | ns |
| t _{OE} | Output Enable Low to Output Valid | — | 5 | — | 6 | — | 7 | ns |
| t _{OLZ} ⁽¹⁾ | Output Enable Low to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽¹⁾ | Output Enable High to Output in High-Z | — | 5 | — | 6 | — | 7 | ns |
| t _{OH} | Output Hold from Address Change | 4 | — | 4 | — | 4 | — | ns |
| t _{BE} | Byte Enable Low to Output Valid | — | 5 | — | 6 | — | 7 | ns |
| t _{BLZ} ⁽¹⁾ | Byte Enable Low to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{BHZ} ⁽¹⁾ | Byte Enable High to Output in High-Z | — | 5 | — | 6 | — | 7 | ns |
| WRITE CYCLE | | | | | | | | |
| t _{WC} | Write Cycle Time | 10 | — | 12 | — | 15 | — | ns |
| t _{AW} | Address Valid to End of Write | 8 | — | 8 | — | 10 | — | ns |
| t _{CW} | Chip Select Low to End of Write | 8 | — | 8 | — | 10 | — | ns |
| t _{BW} | Byte Enable Low to End of Write | 8 | — | 8 | — | 10 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{WR} | Address Hold from End of Write | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 8 | — | 8 | — | 10 | — | ns |
| t _{DW} | Data Valid to End of Write | 5 | — | 6 | — | 7 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ⁽¹⁾ | Write Enable High to Output in Low-Z | 3 | — | 3 | — | 3 | — | ns |
| t _{WHZ} ⁽¹⁾ | Write Enable Low to Output in High-Z | — | 6 | — | 7 | — | 7 | ns |

3624 tbl 10

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1^(1,2,3)



NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. \overline{OE} , \overline{BHE} , and \overline{BLE} are LOW.

3624 drw 06

Timing Waveform of Read Cycle No. 2⁽¹⁾



3624 drw 07

NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of \overline{CS} , \overline{BHE} , or \overline{BLE} transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,4)



3624 drw 08

NOTES:

1. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CS LOW or BHE and BLE LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled Timing)^(1,3)



3624 drw 09

Timing Waveform of Write Cycle No. 3 ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ Controlled Timing)^(1,3)

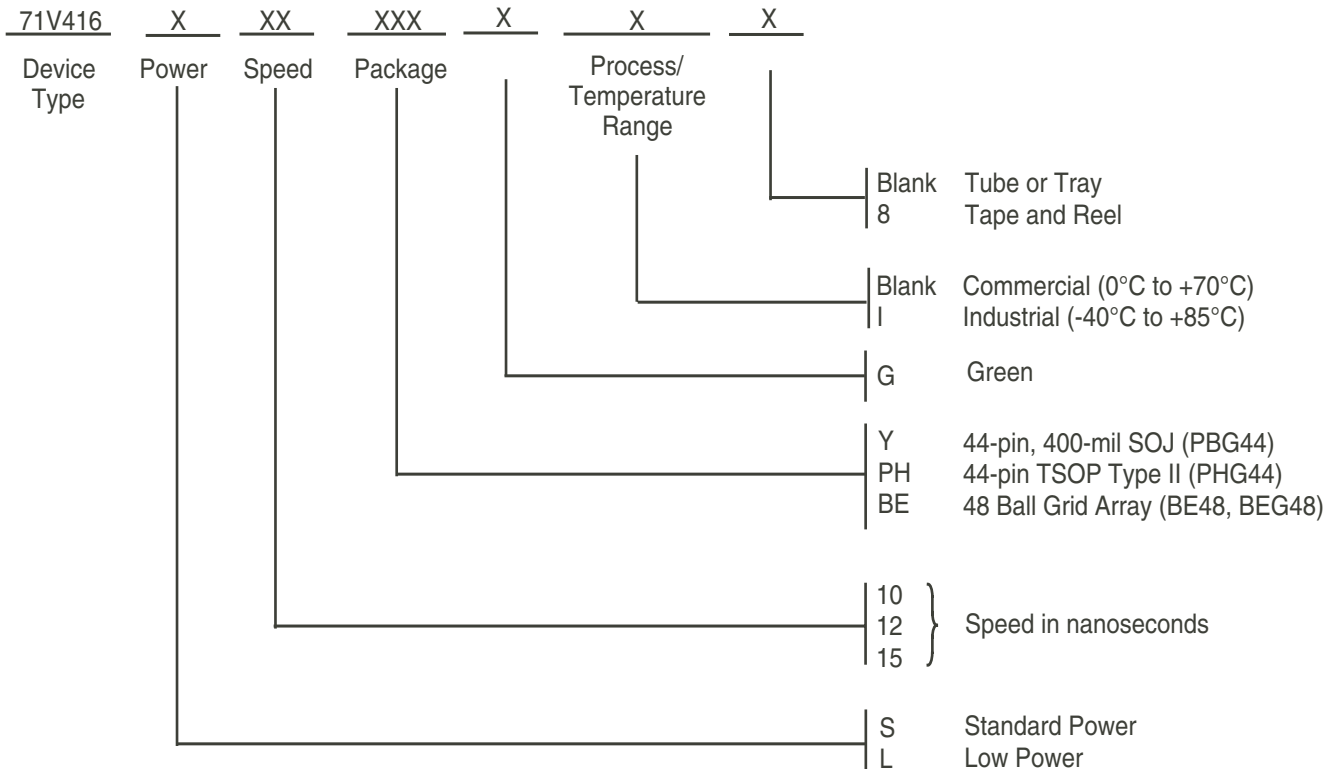


3624 drw 10

NOTES:

1. A write occurs during the overlap of a LOW $\overline{\text{CS}}$, LOW $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$, and a LOW $\overline{\text{WE}}$.
2. During this period, I/O pins are in the output state, and input signals must not be applied.
3. If the $\overline{\text{CS}}$ LOW or $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high-impedance state.

Ordering Information



Orderable Part Information

3624 drw 11a

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 10 | 71V416L10BE | BE48 | CABGA | C |
| | 71V416L10BEG | BEG48 | CABGA | C |
| | 71V416L10BEG8 | BEG48 | CABGA | C |
| | 71V416L10PHG | PHG44 | TSOP | C |
| | 71V416L10PHG8 | PHG44 | TSOP | C |
| | 71V416L10PHGI | PHG44 | TSOP | I |
| | 71V416L10PHGI8 | PHG44 | TSOP | I |
| | 71V416L10YG | PBG44 | SOJ | C |
| | 71V416L10YG8 | PBG44 | SOJ | C |
| 12 | 71V416L12BE | BE48 | CABGA | C |
| | 71V416L12BE8 | BE48 | CABGA | C |
| | 71V416L12BEG | BEG48 | CABGA | C |
| | 71V416L12BEG8 | BEG48 | CABGA | C |
| | 71V416L12BEGI | BEG48 | CABGA | I |
| | 71V416L12BEGI8 | BEG48 | CABGA | I |
| | 71V416L12BEI | BE48 | CABGA | I |
| | 71V416L12BEI8 | BE48 | CABGA | I |
| | 71V416L12PHG | PHG44 | TSOP | C |
| | 71V416L12PHG8 | PHG44 | TSOP | C |
| | 71V416L12PHGI | PHG44 | TSOP | I |
| | 71V416L12PHGI8 | PHG44 | TSOP | I |
| | 71V416L12YG | PBG44 | SOJ | C |
| | 71V416L12YG8 | PBG44 | SOJ | C |
| | 71V416L12YGI | PBG44 | SOJ | I |
| | 71V416L12YGI8 | PBG44 | SOJ | I |

3624 tbl 12a

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade | |
|----------------|-------------------|--------------|-----------|-------------|---|
| 10 | 71V416S10BE | BE48 | CABGA | C | |
| | 71V416S10BE8 | BE48 | CABGA | C | |
| | 71V416S10BEG | BEG48 | CABGA | C | |
| | 71V416S10BEG8 | BEG48 | CABGA | C | |
| | 71V416S10PHG | PHG44 | TSOP | C | |
| | 71V416S10PHG8 | PHG44 | TSOP | C | |
| | 71V416S10PHGI | PHG44 | TSOP | I | |
| | 71V416S10PHGI8 | PHG44 | TSOP | I | |
| | 71V416S10YG | PBG44 | SOJ | C | |
| | 71V416S10YG8 | PBG44 | SOJ | C | |
| | 12 | 71V416S12BE | BE48 | CABGA | C |
| | | 71V416S12BE8 | BE48 | CABGA | C |
| 71V416S12BEG | | BEG48 | CABGA | C | |
| 71V416S12BEG8 | | BEG48 | CABGA | C | |
| 71V416S12BEI | | BE48 | CABGA | I | |
| 71V416S12BEI8 | | BE48 | CABGA | I | |
| 71V416S12PHG | | PHG44 | TSOP | C | |
| 71V416S12PHG8 | | PHG44 | TSOP | C | |
| 71V416S12PHGI | | PHG44 | TSOP | I | |
| 71V416S12PHGI8 | | PHG44 | TSOP | I | |
| 71V416S12YG | | PBG44 | SOJ | C | |
| 71V416S12YG8 | | PBG44 | SOJ | C | |
| 71V416S12YGI | PBG44 | SOJ | I | | |
| 71V416S12YGI8 | PBG44 | SOJ | I | | |

3624 tbl 12b

Orderable Part Information (con't)

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 15 | 71V416L15BE | BE48 | CABGA | C |
| | 71V416L15BE8 | BE48 | CABGA | C |
| | 71V416L15BEG | BEG48 | CABGA | C |
| | 71V416L15BEG8 | BEG48 | CABGA | C |
| | 71V416L15BEGI | BEG48 | CABGA | I |
| | 71V416L15BEGI8 | BEG48 | CABGA | I |
| | 71V416L15BEI | BE48 | CABGA | I |
| | 71V416L15BEI8 | BE48 | CABGA | I |
| | 71V416L15PHG | PHG44 | TSOP | C |
| | 71V416L15PHG8 | PHG44 | TSOP | C |
| | 71V416L15PHGI | PHG44 | TSOP | I |
| | 71V416L15PHGI8 | PHG44 | TSOP | I |
| | 71V416L15YGI | PBG44 | SOJ | I |
| | 71V416L15YGI8 | PBG44 | SOJ | I |

3624 tbl 12c

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 15 | 71V416S15BE | BE48 | CABGA | C |
| | 71V416S15BE8 | BE48 | CABGA | C |
| | 71V416S15BEG | BEG48 | CABGA | C |
| | 71V416S15BEG8 | BEG48 | CABGA | C |
| | 71V416S15BEGI | BEG48 | CABGA | I |
| | 71V416S15BEGI8 | BEG48 | CABGA | I |
| | 71V416S15BEI | BE48 | CABGA | I |
| | 71V416S15BEI8 | BE48 | CABGA | I |
| | 71V416S15PHG | PHG44 | TSOP | C |
| | 71V416S15PHG8 | PHG44 | TSOP | C |
| | 71V416S15PHGI | PHG44 | TSOP | I |
| | 71V416S15PHGI8 | PHG44 | TSOP | I |
| | 71V416S15YG | PBG44 | SOJ | C |
| | 71V416S15YG8 | PBG44 | SOJ | C |
| | 71V416S15YGI | PBG44 | SOJ | I |
| | 71V416S15YGI8 | PBG44 | SOJ | I |

3624 tbl 12d

Datasheet Document History

| | | |
|-----------|---------|--|
| 08/5/99 | | Updated to new format |
| | Pg 6 | Revised footnote for tcw on Write Cycle No. 1 diagram |
| 08/31/99 | Pg. 1-9 | Added Industrial temperature range offering |
| | Pg. 9 | Added Datasheet Document History |
| 03/24/00 | Pg. 6 | Changed note to Write cycle No. 1 according to footnotes |
| 08/10/00 | | Add 48 ball grid array package offering |
| | Pg. 1 | Correct TTL to LVTTTL |
| 09/11/02 | Pg. 2 | Updated TBD information for the 48 BGA Capacitance table |
| 11/26/02 | Pg. 8 | Added "Die Revision" to ordering information |
| 07/31/03 | Pg. 8 | Updated note, L10 speed grade commercial temperature only and updated die stepping from YF to Y. |
| 10/13/03 | Pg. 8 | Updated ordering information. Refer to 71V416YS and 71V416YL datasheet for latest generation die step. |
| 01/30/04 | Pg. 8 | Added "Restricted hazardous substance device" to ordering information |
| 02/01/13: | Pg. 1 | Removed IDT reference to fabrication |
| | Pg. 8 | Removed die revision information from the Ordering Information |
| 11/18/16: | Pg. 2 | Updated the orderable part numbers for all pin configurations |
| | | Added the corrected configuration title for the 48 BGA pin configuration |
| | | Reformatted SOJ/TSOP pins & labels. No change in functionality. It remains the same |
| | Pg.4 | Updated the Industrial values and the footnote references in the DC Electrical table |
| | Pg. 5 | Updated the footnote references in the AC Electrical table |
| | Pg. 8 | Updated the orderable part numbers in the Ordering Information |
| | Pg. 8-9 | Added orderable part information tables |

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