

Serial EEPROM Series Standard EEPROM

WLCSP EEPROM

BU9897GUL-W (128Kbit)

● General Description

BU9897GUL-W is a serial EEPROM of I²C BUS interface method.
Memory density is 128Kbit (16,384 × 8bit) , compact package VCSP50L2.

● Features

- Completely conforming to the world standard I²C BUS.
All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
- Other devices than EEPROM can be connected to the same port, saving microcontroller port.
- 1.7V to 5.5V single power source action most suitable for battery use.
- FAST MODE :400kHz at 1.7V to 5.5V
- Page write mode useful for initial value write at factory shipment.
- Auto erase and auto end function at data rewrite.
- Low current consumption
 - At write operation (5.0V) : 0.5mA (Typ.)
 - At read operation (5.0V) : 0.2mA (Typ.)
 - At standby operation (5.0V) : 0.1μA (Typ.)
- Write mistake prevention function
 - Write (write protect) function added
 - Write mistake prevention function at low voltage
- Compact package
 - W(Typ.) x D(Typ.) x H(Max.) : 2.44mm x 1.99mm x 0.55mm
- Data rewrite up to 1,000,000 times
- Data kept for 40 years
- Noise filter built in SCL / SDA terminal
- Shipment data all address FFh

● Page write

Product number	Number of pages
BU9897GUL-W	64Byte

● Absolute Maximum Ratings (Ta=25°C)

Parameter	symbol	Ratings	Unit	Remarks
Impressed voltage	V _{CC}	-0.3 to 6.5	V	
Permissible dissipation	P _d	220	mW	When using at Ta=25°C or higher, 2.2mW to be reduced per 1°C
Storage temperature range	T _{stg}	-65 to 125	°C	
Action temperature range	T _{opr}	-40 to 85	°C	
Terminal voltage	—	-0.3 to V _{CC} +1.0	V	The Max value of Terminal Voltage is not over 6.5V.

● Memory cell characteristics (Ta=25°C, V_{CC}=1.7V to 5.5V)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Number of data rewrite times *1	1,000,000	—	—	Times
Data hold years *1	40	—	—	Years

*1 Not 100% TESTED

● Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Power source voltage	V _{CC}	1.7 to 5.5	V
Input voltage	V _{IN}	0 to V _{CC}	

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

● **Electrical Characteristics** (Unless otherwise specified Ta=-40°C to 85°C, V_{CC}=1.7V to 5.5V)

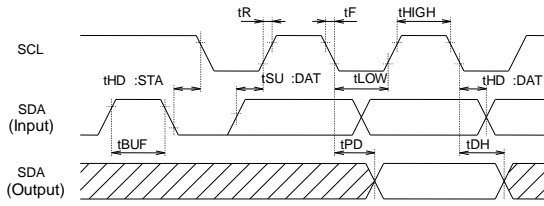
Parameter	Symbol	Limits			Unit	Condition
		Min	Typ.	Max.		
"H" Input Voltage1	V _{IH1}	0.7V _{CC}	—	V _{CC} +1.0	V	
"L" Input Voltage1	V _{IL1}	-0.3	—	0.3V _{CC}	V	
"L" Output Voltage1	V _{OL1}	—	—	0.4	V	I _{OL} =3.0mA, 2.5V ≤ V _{CC} ≤ 5.5V(SDA)
"L" Output Voltage2	V _{OL2}	—	—	0.2	V	I _{OL} =0.7mA, 1.7V ≤ V _{CC} < 2.5V(SDA)
Input Leakage Current	I _{LI}	-1	—	1	μA	V _{IN} =0V to V _{CC}
Output Leakage Current	I _{LO}	-1	—	1	μA	V _{OUT} =0V to V _{CC} (SDA)
Current consumption at action	I _{CC1}	—	—	2.5	mA	V _{CC} =5.5V, f _{SCL} =400kHz, t _{WR} =5ms Byte Write, Page Write
	I _{CC2}	—	—	0.5	mA	V _{CC} =5.5V, f _{SCL} =400kHz Random read, Current read, Sequential read
Standby Current	I _{SB}	—	—	2.0	μA	V _{CC} =5.5V, SDA · SCL=V _{CC} , WP=GND

● **Action timing characteristics** (Unless otherwise specified Ta=-40°C to 85°C, V_{CC}=1.7V to 5.5V)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SCL Frequency	f _{SCL}	—	—	400	kHz
Data clock "High" time	t _{HIGH}	0.6	—	—	μs
Data clock "Low" time	t _{LOW}	1.2	—	—	μs
SDA, SCL rise time *1	t _R	—	—	0.3	μs
SDA, SCL fall time *1	t _F	—	—	0.3	μs
Start condition hold time	t _{HD:STA}	0.6	—	—	μs
Start condition setup time	t _{SU:STA}	0.6	—	—	μs
Input data hold time	t _{HD:DAT}	0	—	—	ns
Input data setup time	t _{SU:DAT}	100	—	—	ns
Output data delay time	t _{PD}	0.1	—	0.9	μs
Output data hold time	t _{DH}	0.1	—	—	μs
Stop condition data setup time	t _{SU:STO}	0.6	—	—	μs
Bus release time before transfer start	t _{BUF}	1.2	—	—	μs
Internal write cycle time	t _{WR}	—	—	5	ms
Noise removal valid period (SDA,SCL terminal)	t _l	—	—	0.1	μs
WP hold time	t _{HD:WP}	0	—	—	ns
WP setup time	t _{SU:WP}	0.1	—	—	μs
WP valid time	t _{HIGH:WP}	1.0	—	—	μs

*1 : Not 100% TESTED

● Sync Data Input / Output Timing



- Input read at the rise edge of SCL
- Data output in sync with the fall of SCL

Figure 1-(a) Sync data input / output timing

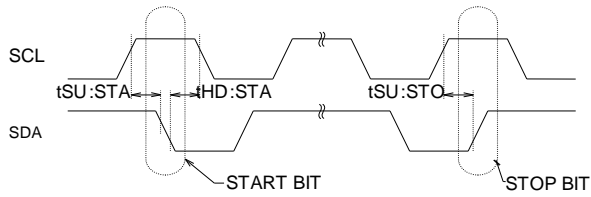


Figure 1-(b) Start - stop bit timing

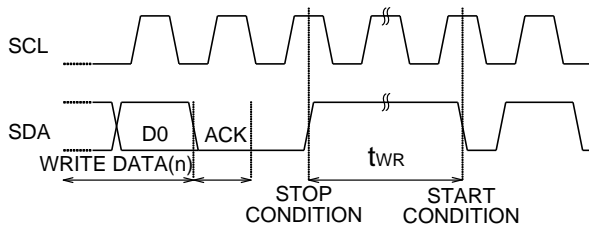


Figure 1-(c) Write cycle timing

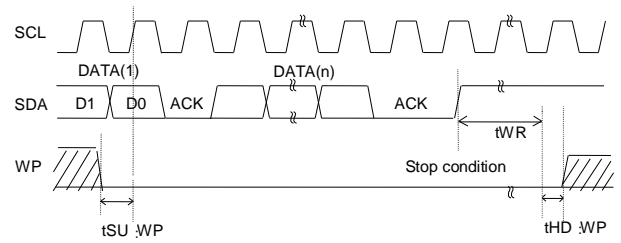
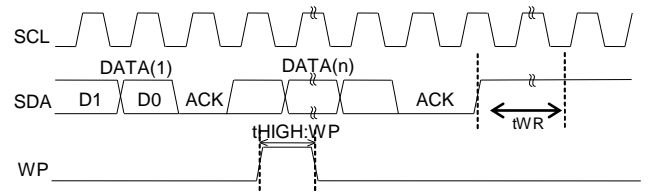


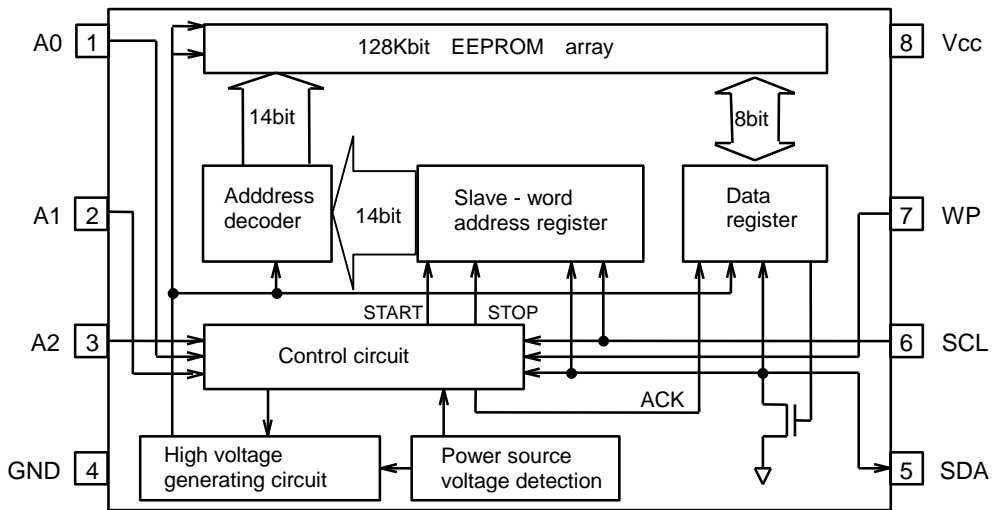
Figure 1-(d) WP timing at write execution



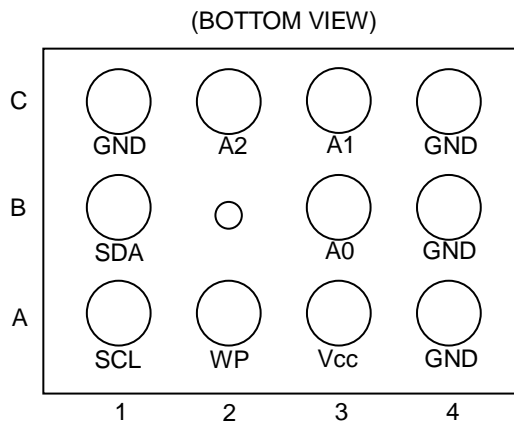
- At write execution, in the area from the D0 taken clock rise of the first DATA(1), to t_{WR} , set WP = 'LOW'.
- By setting WP "HIGH" in the area, write can be cancelled. When it is set WP = 'HIGH' during t_{WR} , write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

Figure 1-(e) WP timing at write cancel

●Block Diagram



●Pin Configuration



●Pin Descriptions

Land No.	Terminal name	Input / output	Function
C4	GND	-	Reference voltage of all input / output
C3	A1	Input	Slave address
C2	A2	input	Slave address
C1	GND	-	Reference voltage of all input / output
B4	GND	-	Reference voltage of all input / output
B3	A0	input	Slave address
B1	SDA	Input / output	Slave and word address, Serial data input serial data output
A4	GND	-	Reference voltage of all input / output
A3	Vcc	-	Power Supply
A2	WP	input	Write protect terminal
A1	SCL	input	Serial clock input

● Typical Performance Curves

(The following values are Typ. ones.)

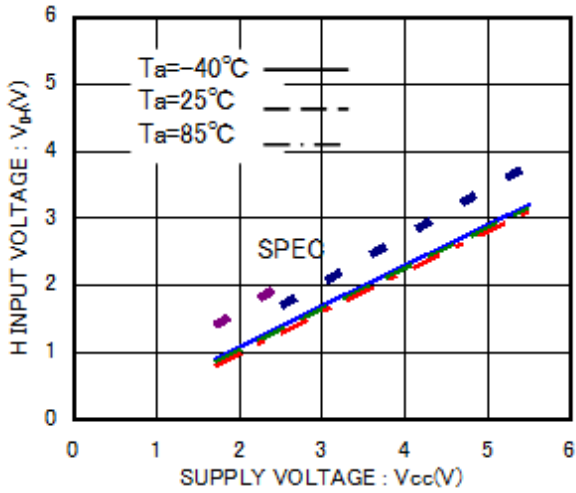


Figure 2. 'H' input voltage V_{IH}
(AO, A1, A2, SCL, SDA, WP)

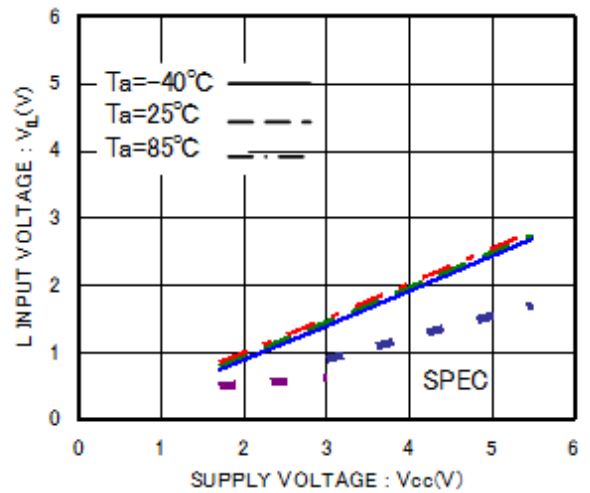


Figure 3. 'L' input voltage V_{IL}
(AO, A1, A2, SCL, SDA, WP)

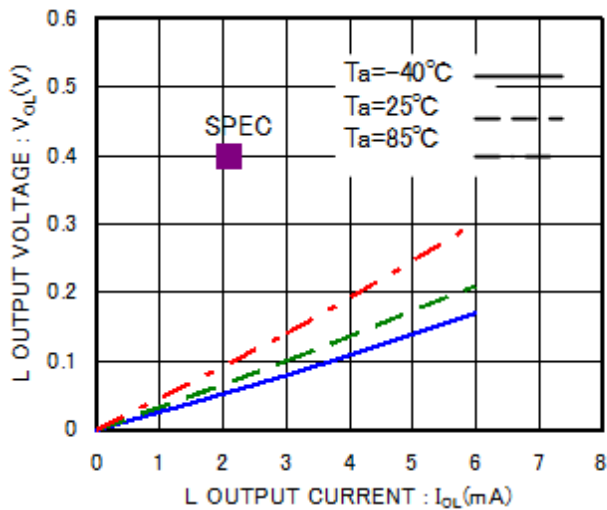


Figure 4. 'L' output voltage $V_{OL} - I_{OL}$ ($V_{CC}=1.7$)

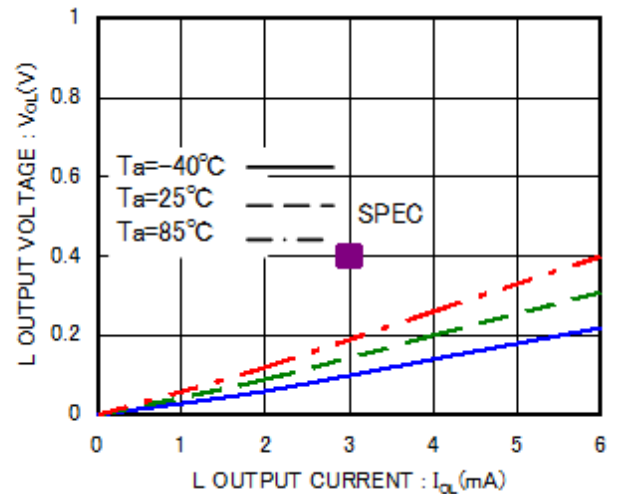


Figure 5. 'L' output voltage $V_{OL} - I_{OL}$ ($V_{CC}=2.5$)

● Typical Performance Curves - Continued

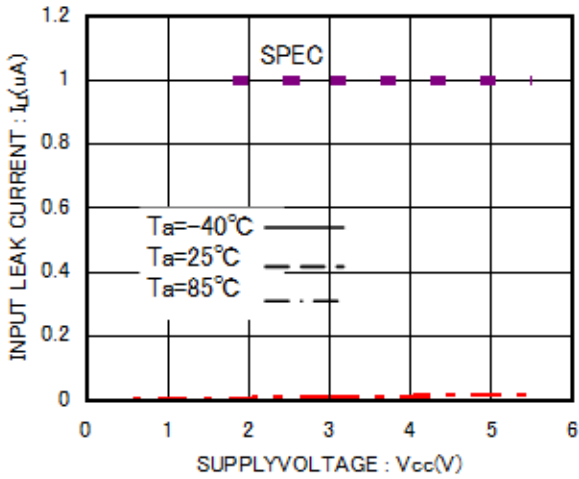


Figure 6. Input leak current I_{LI} (AO, A1, A2, SCL, WP)

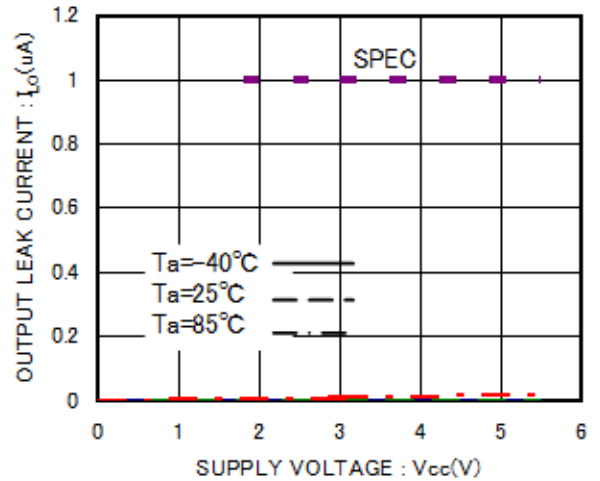


Figure 7. Output leak current I_{LO} (SDA)

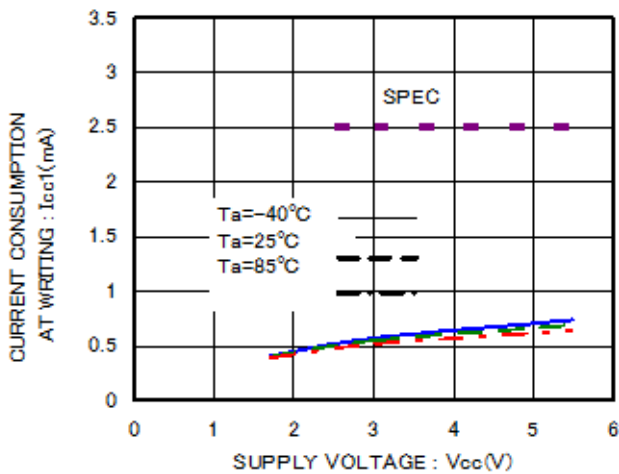


Figure 8. Current consumption at WRITE operation I_{cc1} (fsc1 = 400kHz)

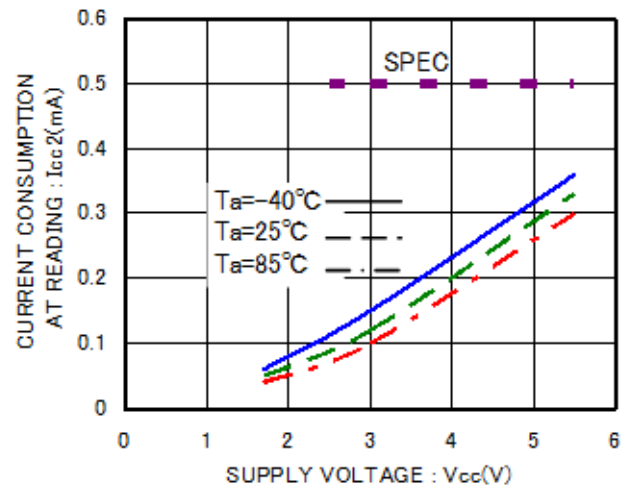


Figure 9. Current consumption at READ operation I_{cc2} (fsc2 = 400kHz)

● Typical Performance Curves - Continued

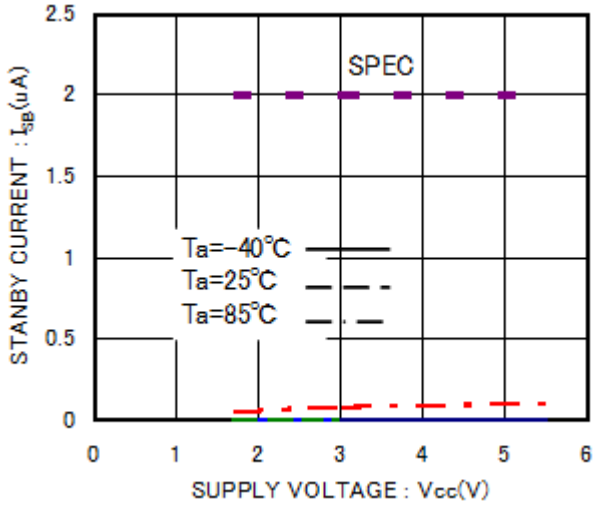


Figure 10. Standby operation I_{SB}

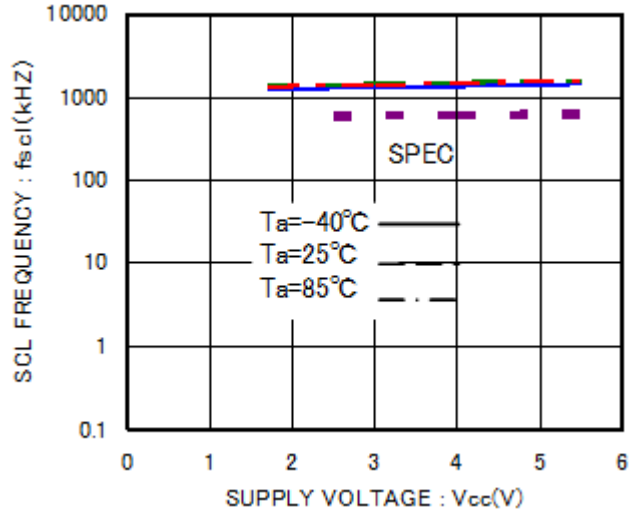


Figure 11. SCL frequency f_{SCL}

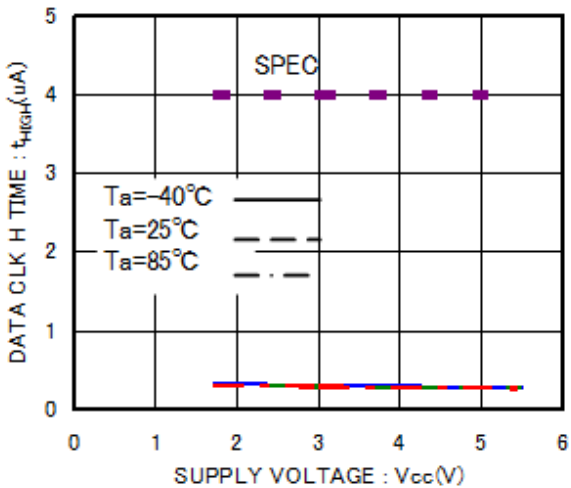


Figure 12. Data clock High Period t_{HIGH}

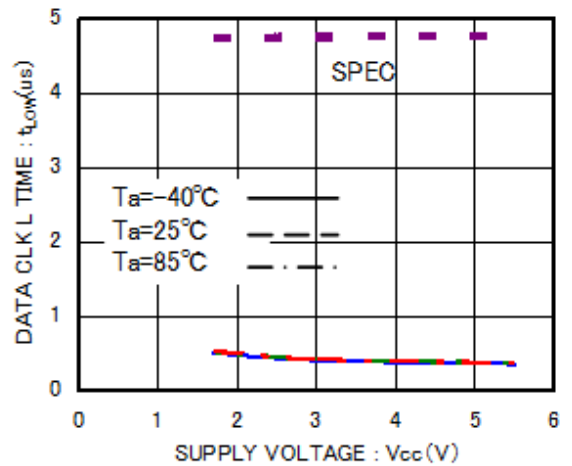


Figure 13. Data clock Low Period t_{LOW}

● Typical Performance Curves - Continued

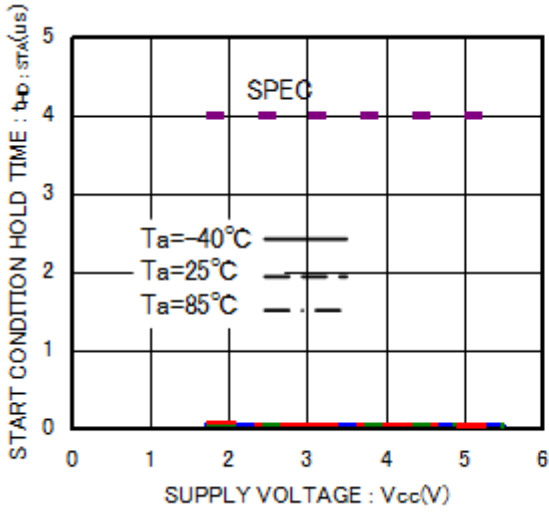


Figure 14. Start Condition Hold Time $t_{HD:STA}$

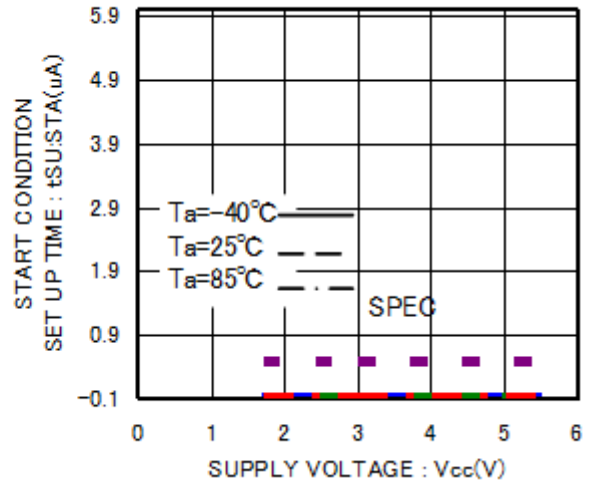


Figure 15. Start Condition Setup Time $t_{SU:STA}$

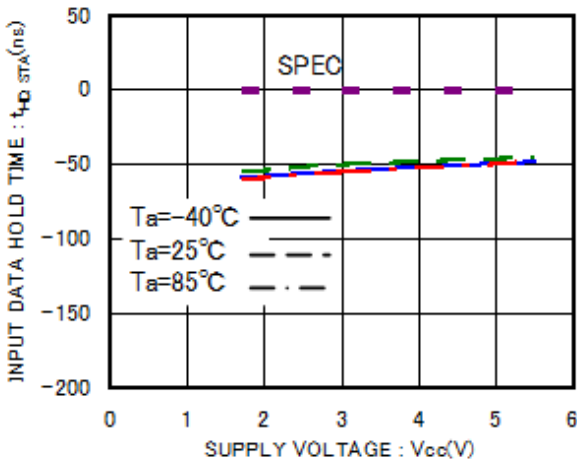


Figure 16. Input Data Hold Time $t_{HD:DAT}$ (HIGH)

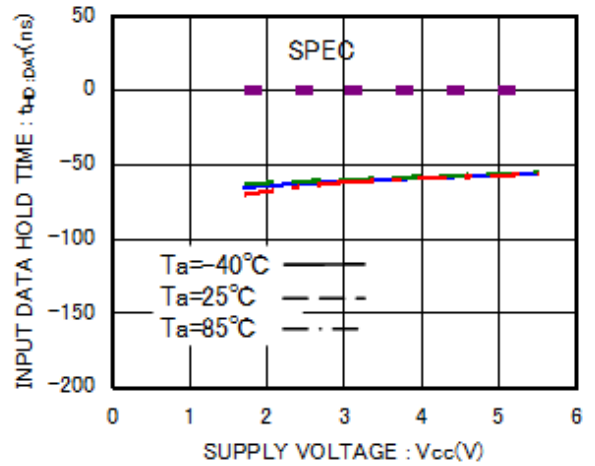


Figure 17. Input Data Hold Time $t_{HD:DAT}$ (LOW)

● Typical Performance Curves - Continued

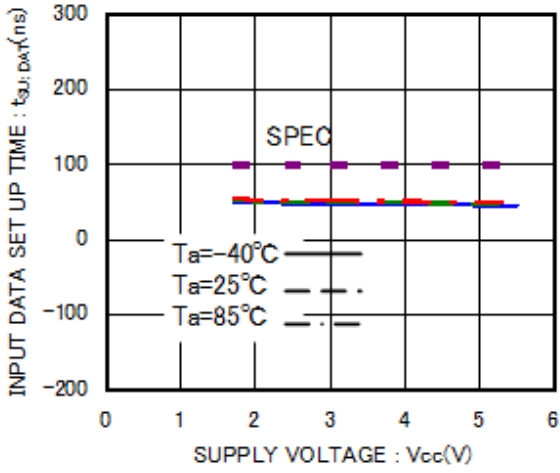


Figure 18. Input Data Setup Time $t_{SU:DAT}$ (HIGH)

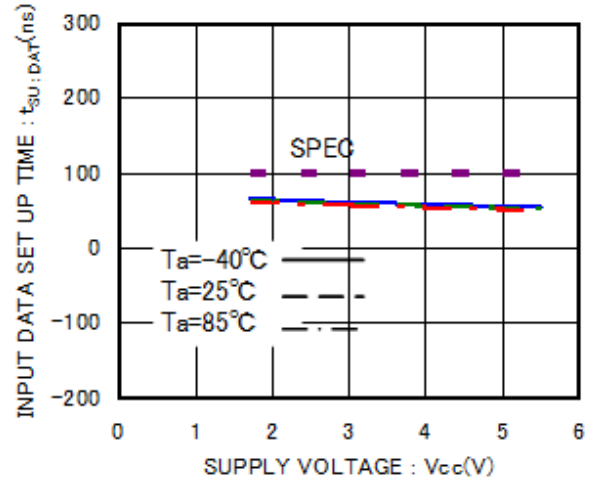


Figure 19. Input Data Setup Time $t_{SU:DAT}$ (LOW)

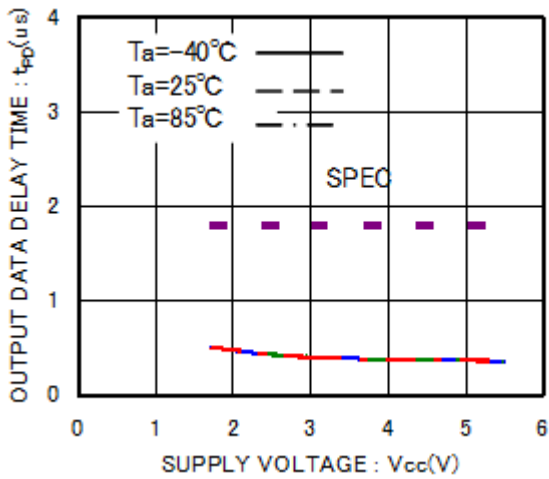


Figure 20. "L" Data output delay time t_{PD0}

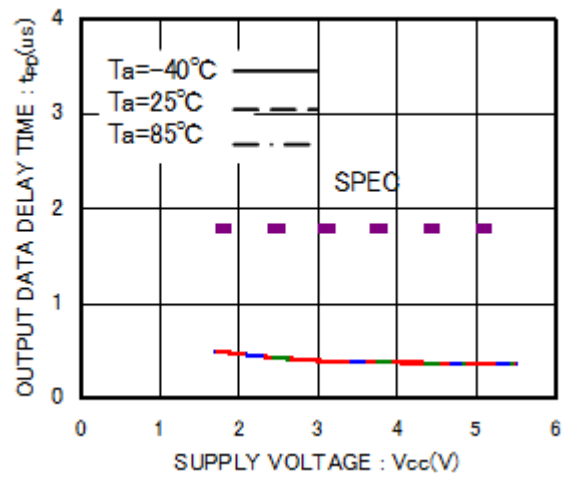


Figure 21. 'H' Data output delay time t_{PD1}

● Typical Performance Curves - Continued

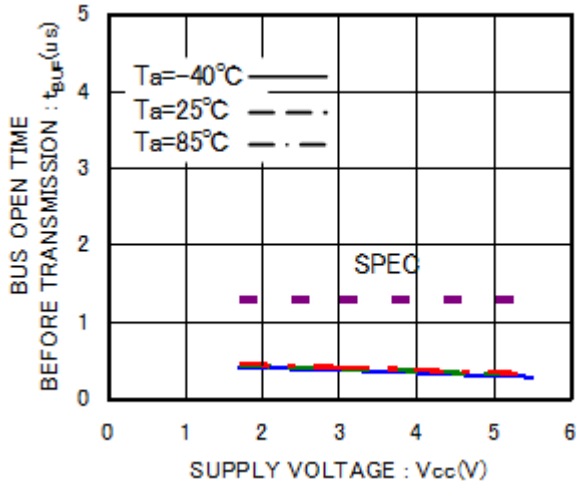


Figure 22. BUS open time before transmission t_{BUF}

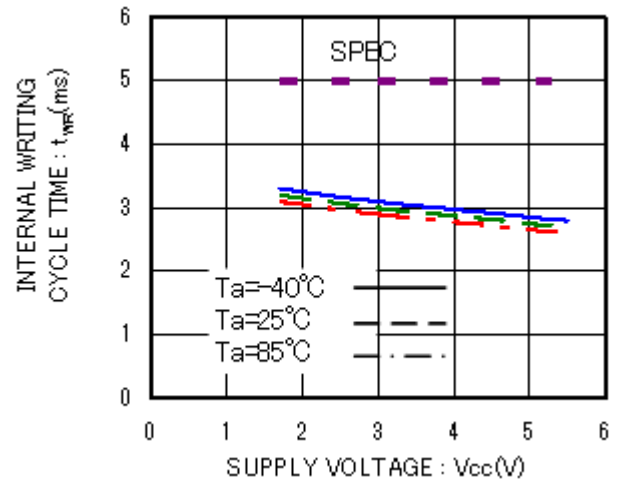


Figure 23. Internal writing cycle time t_{WR}

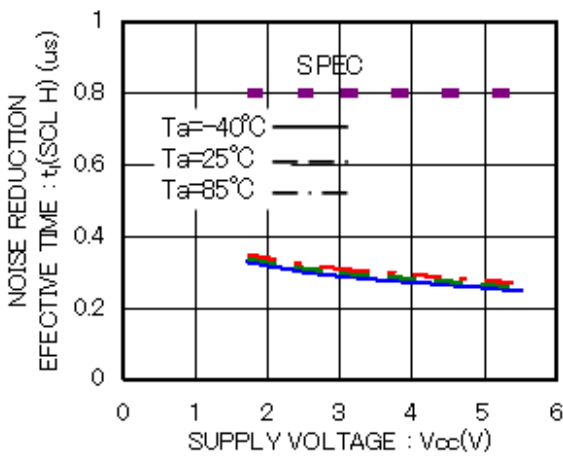


Figure 24. Noise reduction effective time t_I (SCL H)

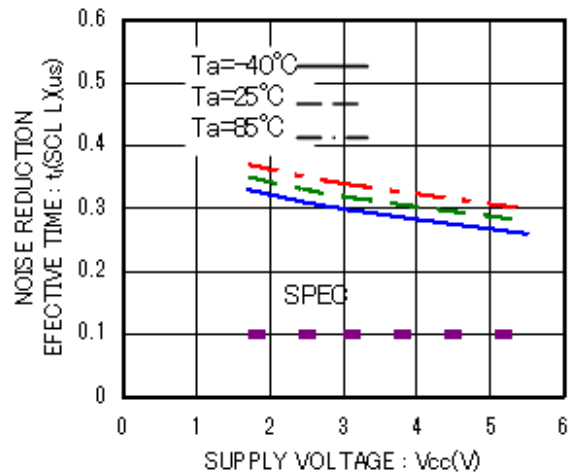


Figure 25. Noise reduction effective time t_I (SCL L)

● Typical Performance Curves - Continued

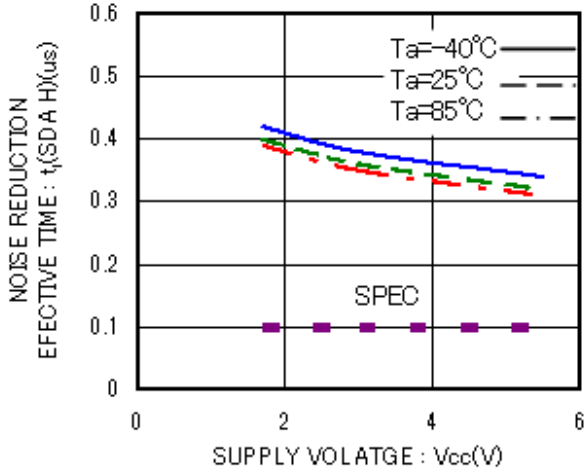


Figure 26. Noise reduction effective time t_i (SDA H)

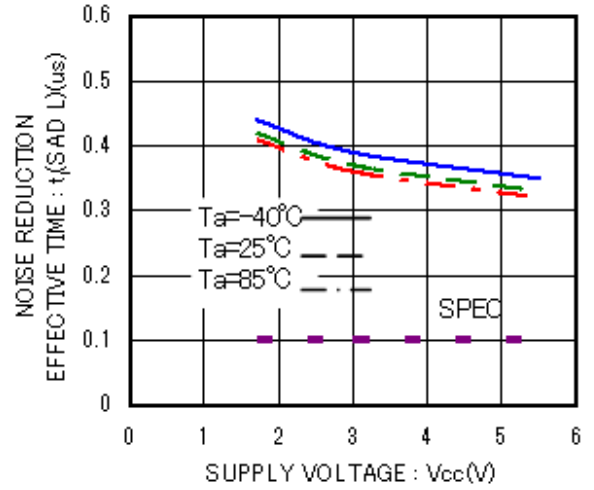


Figure 27. Noise reduction effective time t_i (SDA L)

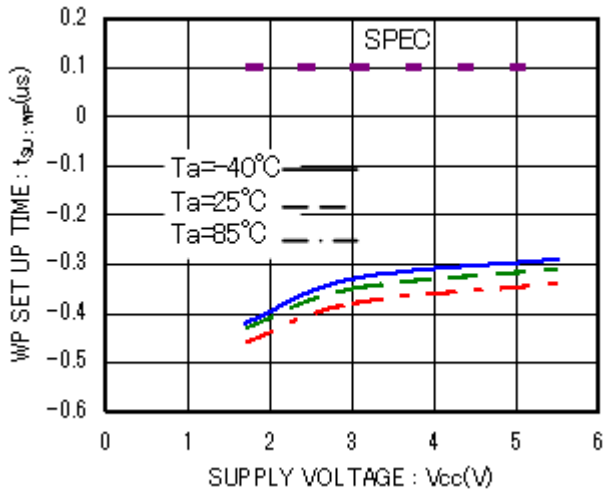


Figure 28. WP Setup time $t_{SU:WP}$

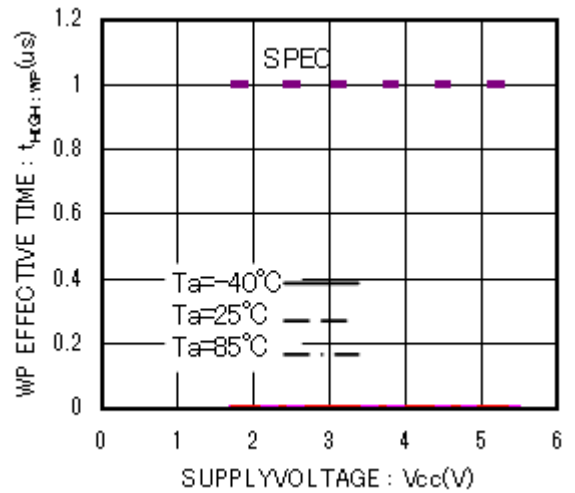


Figure 29. WP effective time $t_{HIGH:WP}$

● I²C BUS communication

○ I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte.

I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).

Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by addresses peculiar to devices.

EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

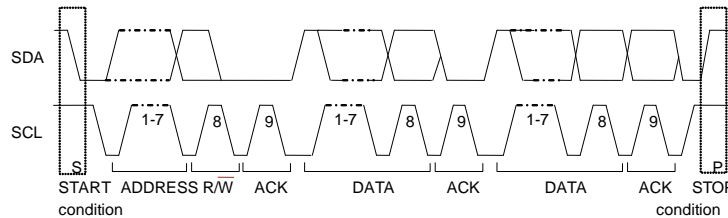


Figure 30. Data transfer timing

○ Start condition (start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command is executed.

○ Stop condition (stop bit recognition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

○ Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action. And this IC gets in standby status.

○ Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
- The most insignificant bit (R / \overline{W} --- READ / WRITE) of slave address is used for designating write or read action, and is as shown below.

Setting R / \overline{W} to 0 --- write (setting 0 to word address setting of random read)

Setting R / \overline{W} to 1 --- read

Type	Slave address							
BU9897GUL-W	1	0	1	0	0	0	0	R / \overline{W}

●Write Command

○Write cycle

- Arbitrary data is written to EEPROM. When to write only 1 byte, byte write normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity. Up to 64 arbitrary bytes can be written.

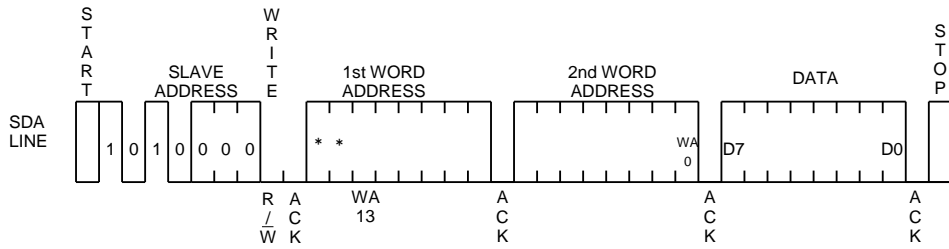


Figure 31. Byte write cycle

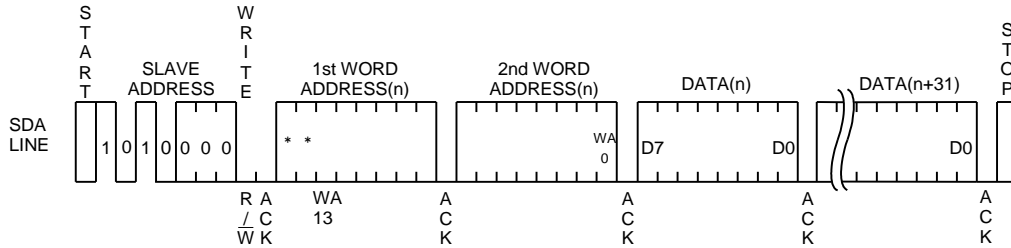


Figure 32. Page write cycle

- Data is written to the address designated by word address (n-th address).
- By issuing stop bit after 8bit data input, write to memory cell inside starts.
- When internal write is started, command is not accepted for tWR (5ms at maximum).
- By page write cycle, the following can be written in bulk: Up to 64 bytes. (Refer to "Internal address increment " in Page 14.)
- As for page write cycle of BU9897GUL-W , after the significant 7 bits of word address, are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 6 bits is incremented internally, and data up to 64 bytes can be written.

Notes on write cycle continuous input

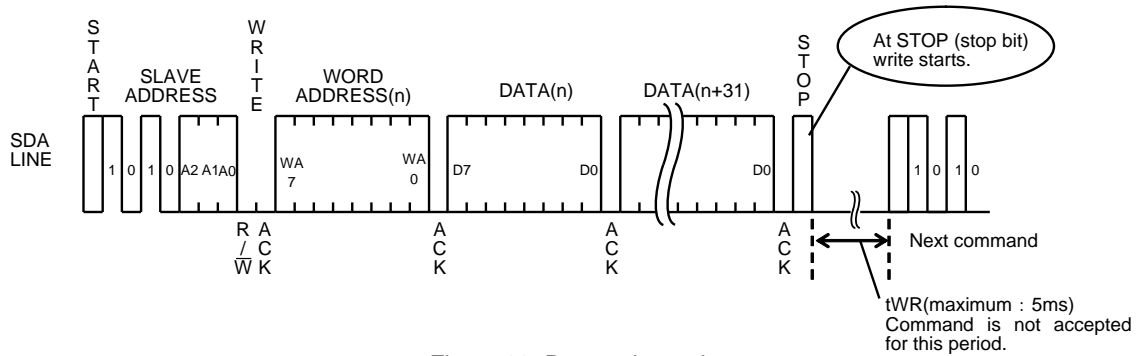


Figure 33. Page write cycle

Notes on page write cycle

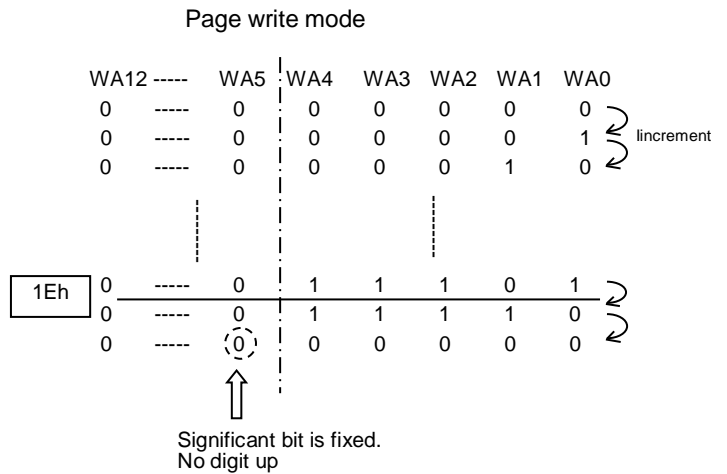
List of numbers of page write

Product number	Number of pages
BU9897GUL-W	64Byte

The above numbers are maximum bytes for respective types. Any bytes below these can be written.

In the case of BU9897GUL-W, 1 page = 64bytes, but the page write cycle write time is 5ms at maximum for 64byte bulk write. It does not stand 5ms at maximum × 64byte = 320ms(Max.).

Internal address increment



For example, when it is started from address 1Eh, therefore, increment is made as below, 1Eh→1Fh→00h→01h...

* 1Eh...16 in hexadecimal, therefore, 00011110 becomes a binary number.

Write protect (WP) terminal

- Write protect (WP) function

When WP terminal is set Vcc (H level), data rewrite of all address is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open. At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', mistake write can be prevented. During tWR, set the WP terminal always to 'L'. If it is set 'H', write is forcibly terminated.

●Read Command

○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.

Random read cycle is a command to read data by designating address, and is used generally.

Current read cycle is a command to read data of internal addressing register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

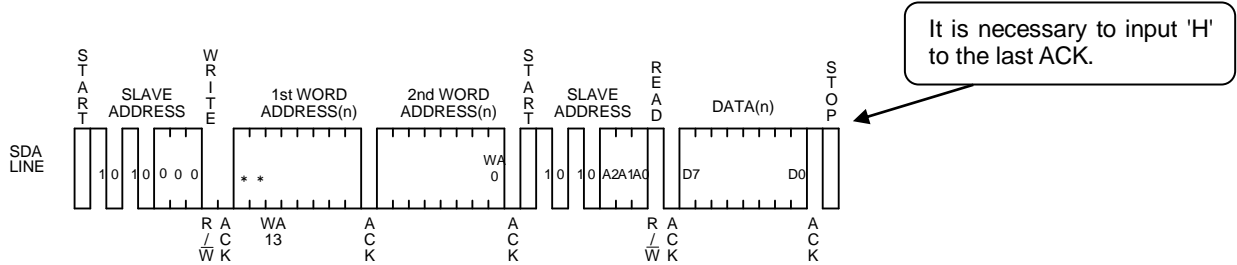


Figure 34. Random read cycle

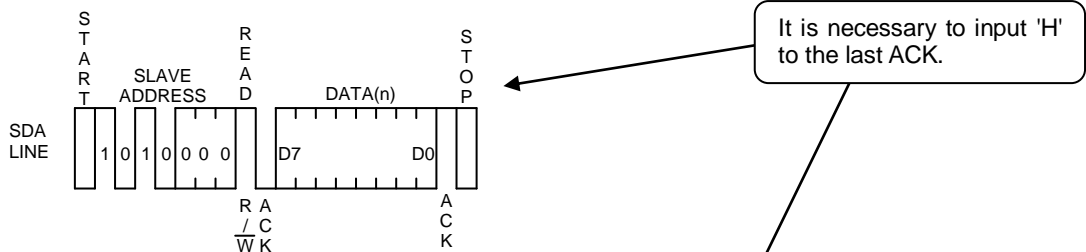


Figure 35. Current read cycle

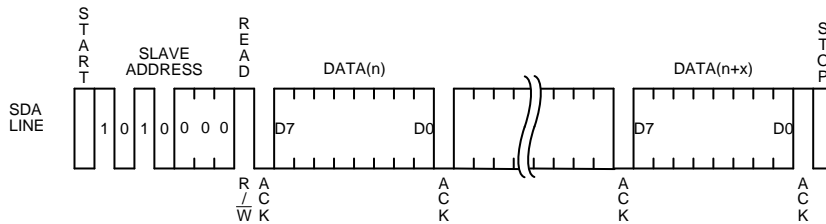


Figure 36. Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ -COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H'.
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output. Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

● Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 37-(a), Figure 37-(b), Figure 37-(c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

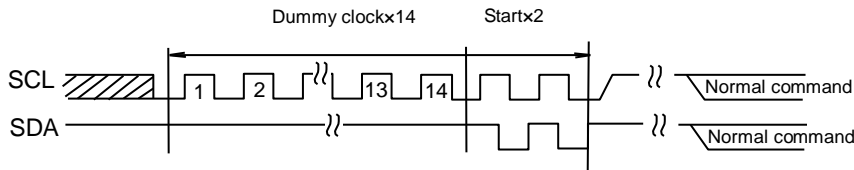


Figure 37-(a) The case of 14 Dummy clock + START + START+ command input

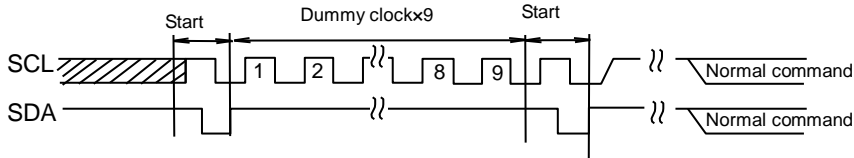


Figure 37-(b) The case of START+9 Dummy clock + START + command input

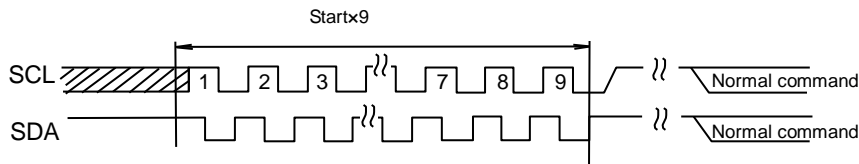


Figure 37-(c) START x 9 + command input * Start command from START input.

● Acknowledge polling

During internal write, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for $t_{WR} = 5ms$.

When to write continuously, $R/\bar{W} = 0$, when to carry out current read cycle after write, slave address $R/\bar{W} = 1$ is sent, and if ACK signal sends back 'L', then execute word address input and data so forth.

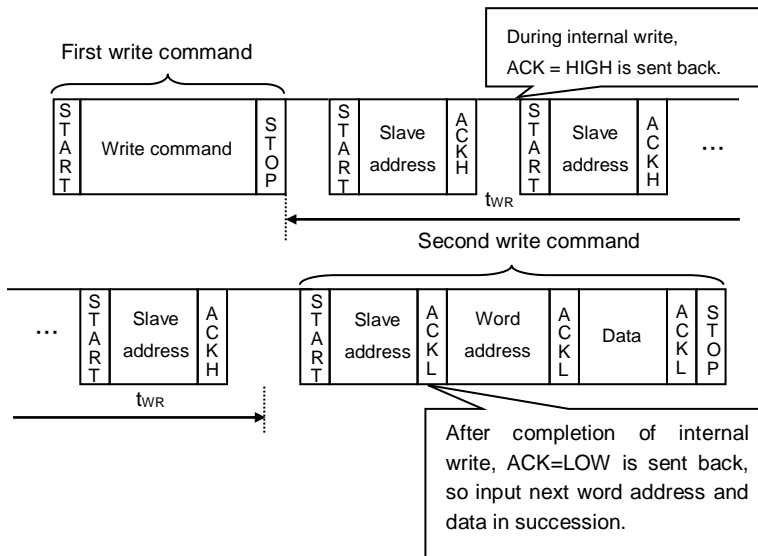


Figure 38. Case to continuously write by acknowledge polling

●WP valid timing (write cancel)

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes Don't care. Set the setup time to rise of D0 taken 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP='H' during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again.(Refer to Figure 39.) After execution of forced end by WP standby status gets in, so there is no need to wait for tWR (5ms at maximum).

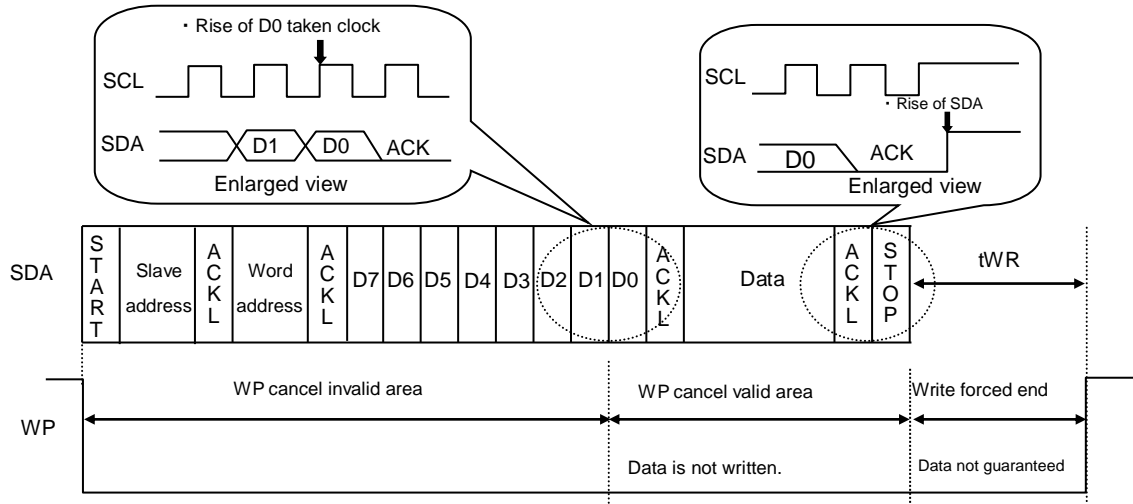


Figure 39. WP valid timing

●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Figure 40.) However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

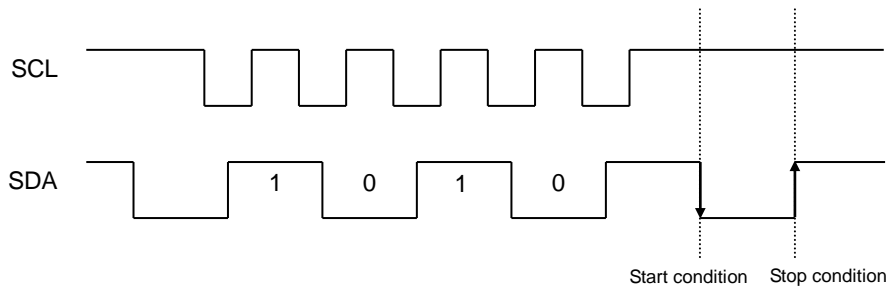


Figure 40. Case of cancel by start, stop condition during slave address input

●Cautions on microcontroller connection

○Rs

In I²C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

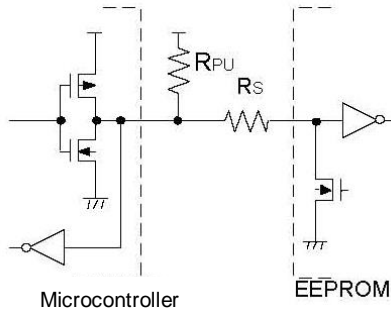


Figure 41. I/O circuit diagram

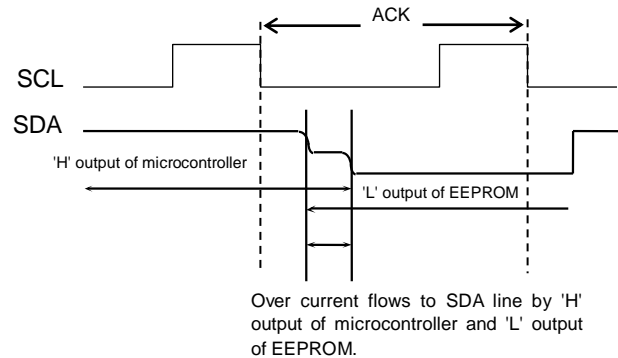


Figure 42. Input/output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by following relations.

- (1) SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tr or below. And AC timing should be satisfied even when SDA rise time is late.
- (2) The bus electric potential (A) to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (VIL) of microcontroller including recommended noise margin 0.1Vcc.

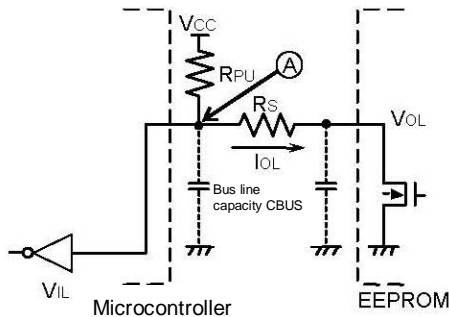


Figure 43. I/O circuit diagram

$$\frac{(V_{CC}-V_{OL}) \times R_S}{R_{PU}+R_S} + V_{OL} + 0.1V_{CC} \leq V_{IL}$$

$$\therefore R_S \leq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When VCC=3V, VIL=0.3VCC, VOL=0.4V, RPU=10kΩ,

$$\text{from(2), } R_S \leq \frac{0.3 \times 3 - 0.4 - 0.1 \times 3}{1.1 \times 3 - 0.3 \times 3} \times 10 \times 10^3$$

$$\leq 0.835[\text{k}\Omega]$$

○Maximum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

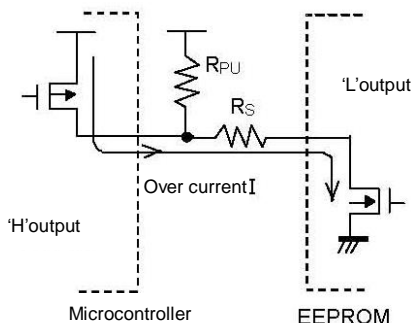


Figure 44. I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leq I$$

$$\therefore R_S \geq \frac{V_{CC}}{I}$$

Example) When VCC=3V, I=10mA

$$R_S \geq \frac{3}{10 \times 10^{-3}}$$

$$\geq 300[\Omega]$$

● I²C BUS input / output circuit

○ Input (A0, A1, A2, SCL, SDA)

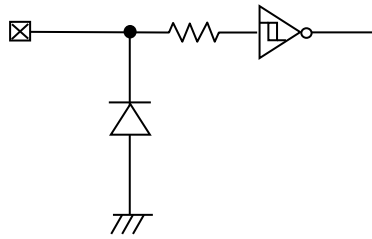


Figure 45. Input pin circuit diagram

○ Input/Output (SDA)

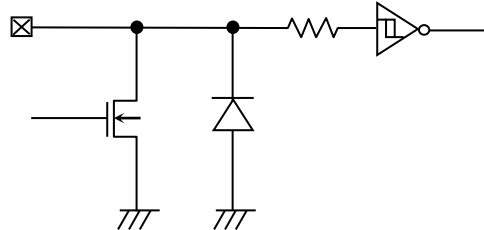


Figure 46. Input/output pin circuit diagram

● Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following condition at power on.

1. Set SDA = 'H' and SCL = 'L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R , t_{OFF} , and V_{bot} for operating POR circuit.

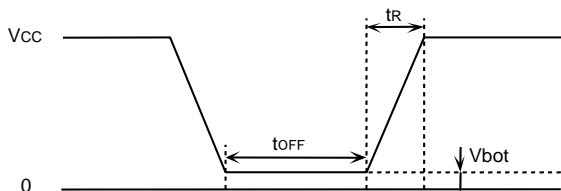


Figure 47. Rise waveform diagram

Recommended conditions of t_R , t_{OFF} , V_{bot}

t_R	t_{OFF}	V_{bot}
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

- a) In the case when the above conditions 1 cannot be observed. When SDA becomes 'L' at power on .
→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

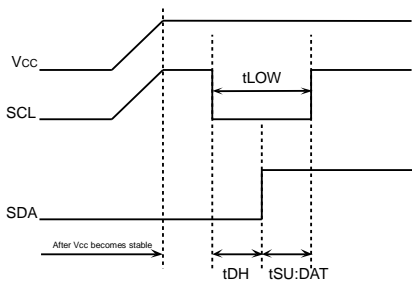


Figure 48. When SCL='H' and SDA='L'

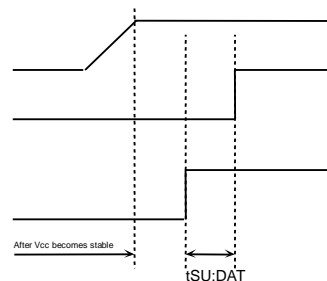


Figure 49. When SCL='H' and SDA='L'

- b) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(Page 16).
- c) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out a), and then carry out b).

●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●V_{CC} noise countermeasures**○Bypass capacitor**

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC V_{CC} and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board V_{CC} and GND.

●Notes for use

- (1) Described numeric values and data are design representative values, and the values are not guaranteed.
- (2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.
- (3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
- (4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.
- (5) Terminal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.
- (6) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.
- (7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

●Ordering Information

B U 9 8 9 7 G U L - W

E 2

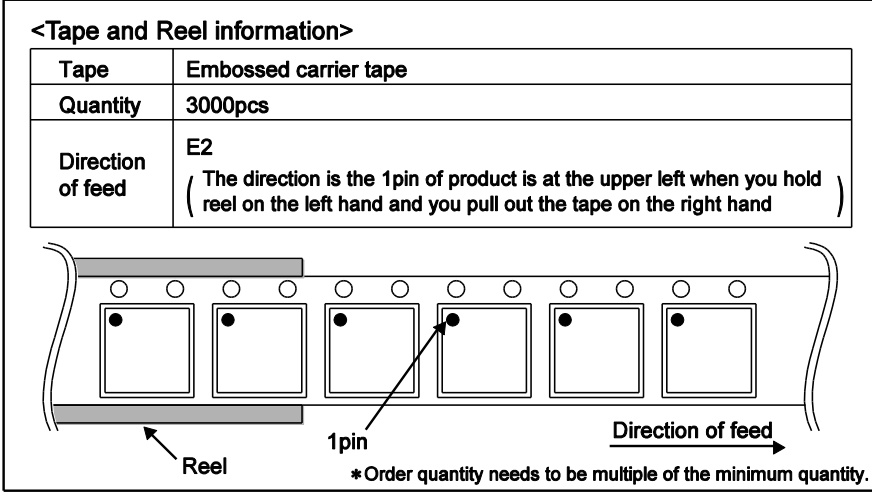
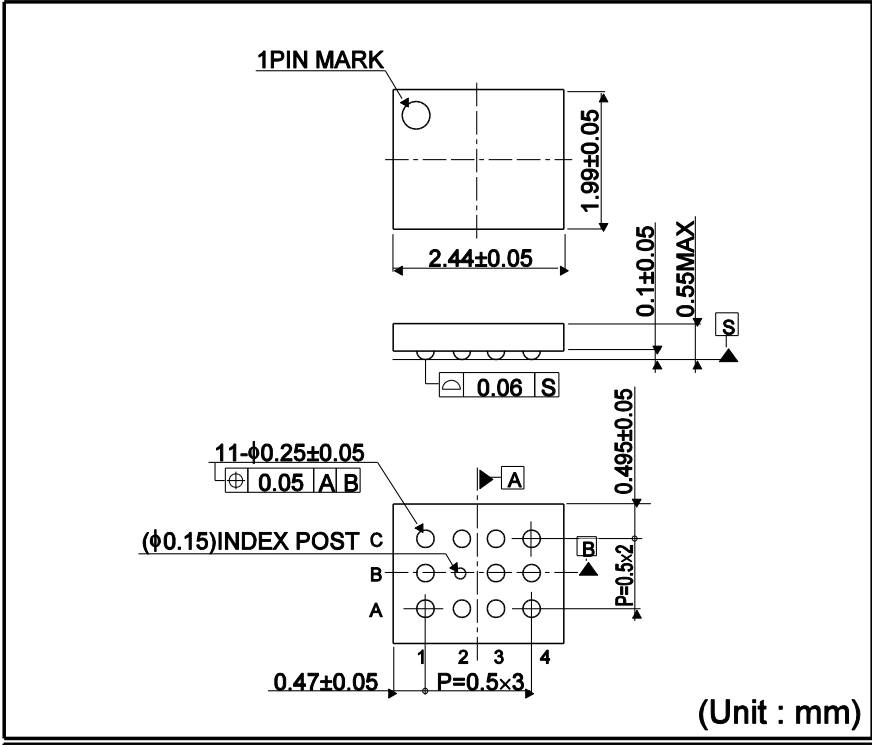
Part Number

Package
GUL: VCSP50L2(BU9897GUL-W)

Packaging and forming specification
E2: Embossed tape and reel

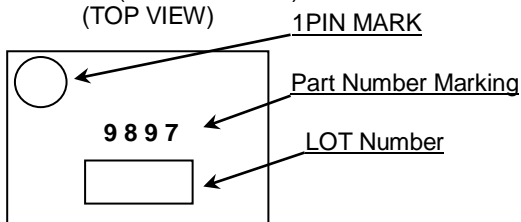
●Physical Dimension Tape and Reel Information

VCSP50L2 (BU9897GUL-W)



●Marking Diagram

VCSP50L2(BU9897GUL-W)
(TOP VIEW)



●Revision History

Date	Revision	Changes
4.Sep.2012	001	New Release
21.Dec.2017	002	P4 Pin Configuration Change A4,B4,C1,C4 Terminal Name from VSS to GND Pin Descriptions Change A4,B4,C4 Function.

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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