

Features

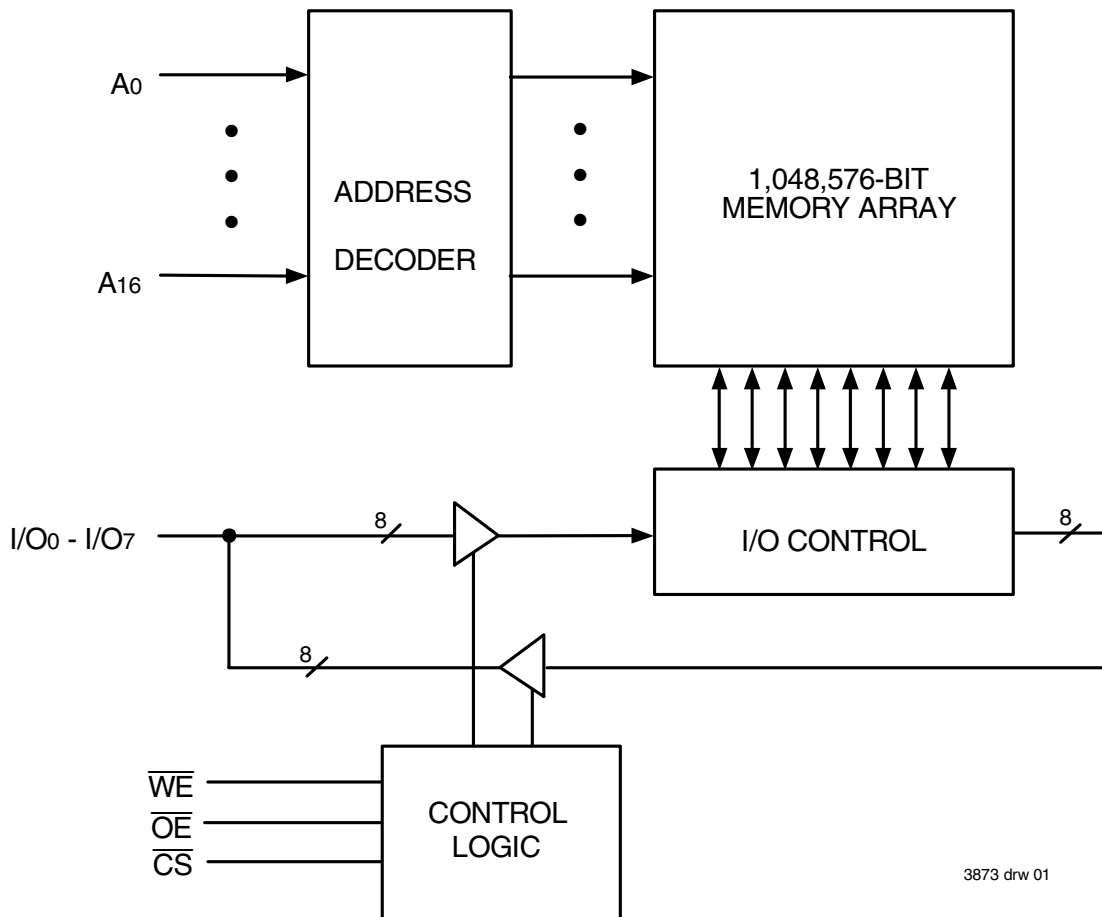
- ◆ 128K x 8 advanced high-speed CMOS static RAM
- ◆ JEDEC revolutionary pinout (center power/GND) for reduced noise
- ◆ Equal access and cycle times
 - Commercial: 10/12/15ns
 - Industrial: 10/12/15ns
- ◆ One Chip Select plus one Output Enable pin
- ◆ Inputs and outputs are LVTTTL-compatible
- ◆ Single 3.3V supply
- ◆ Low power consumption via chip deselect
- ◆ Available in a 32-pin 300- and 400-mil Plastic SOJ, and 32-pin Type II TSOP packages
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Green parts available, see ordering information

Description

The IDT71V124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center power/GND pinout reduces noise generation and improves system performance.

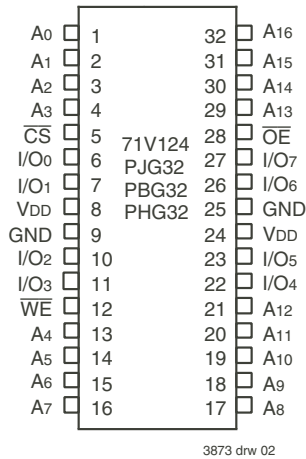
The IDT71V124 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns available. All bidirectional inputs and outputs of the IDT71V124 are LVTTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

Functional Block Diagram



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Pin Configurations⁽¹⁾



SOJ and TSOP Top View

NOTE:

- This text does not indicate orientation of actual part-marking.

Truth Table⁽¹⁾

| \overline{CS} | \overline{OE} | \overline{WE} | I/O | Function |
|-----------------|-----------------|-----------------|---------|----------------------|
| L | L | H | DATAOUT | Read Data |
| L | X | L | DATAIN | Write Data |
| L | H | H | High-Z | Output Disabled |
| H | X | X | High-Z | Deselected – Standby |

NOTE:

- H = V_{IH} , L = V_{IL} , X = Don't care.

Capacitance

($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$, SOJ package)

| Symbol | Parameter ⁽¹⁾ | Conditions | Max. | Unit |
|-----------|--------------------------|------------------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 3\text{dV}$ | 6 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT} = 3\text{dV}$ | 7 | pF |

NOTE:

- This parameter is guaranteed by device characterization, but is not production tested.

DC Electrical Characteristics

($V_{DD} = \text{Min. to Max.}$, Commercial and Industrial Temperature Ranges)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|------------|------------------------|---|------|------|---------------|
| $ I_{L} $ | Input Leakage Current | $V_{DD} = \text{Max.}, V_{IN} = \text{GND to } V_{DD}$ | — | 5 | μA |
| $ I_{LO} $ | Output Leakage Current | $V_{DD} = \text{Max.}, \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{DD}$ | — | 5 | μA |
| V_{OL} | Output Low Voltage | $I_{OL} = 8\text{mA}, V_{DD} = \text{Min.}$ | — | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -4\text{mA}, V_{DD} = \text{Min.}$ | 2.4 | — | V |

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Value | Unit |
|-------------------|----------------------------------|----------------------|------------------|
| V_{DD} | Supply Voltage Relative to GND | -0.5 to +4.6 | V |
| V_{IN}, V_{OUT} | Terminal Voltage Relative to GND | -0.5 to $V_{DD}+0.5$ | V |
| T_A | Commercial Operating Temperature | -0 to +70 | $^\circ\text{C}$ |
| | Industrial Operating Temperature | -40 to +85 | |
| T_{BIAS} | Temperature Under Bias | -55 to +125 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | -55 to +125 | $^\circ\text{C}$ |
| P_T | Power Dissipation | 1.25 | W |
| I_{OUT} | DC Output Current | 50 | mA |

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | V_{DD} |
|------------|---|-----|-----------|
| Commercial | $0^\circ\text{C to } +70^\circ\text{C}$ | 0V | See Below |
| Industrial | $-40^\circ\text{C to } +85^\circ\text{C}$ | 0V | See Below |

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------|--------------------|---------------------|------|--------------------|------|
| $V_{DD}^{(1)}$ | Supply Voltage | 3.15 | 3.3 | 3.6 | V |
| $V_{DD}^{(2)}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V_{SS} | Ground | 0 | 0 | 0 | V |
| V_{IH} | Input High Voltage | 2.0 | — | $V_{DD}+0.3^{(3)}$ | V |
| V_{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

NOTES:

- For 71V124SA10 only.
- For all speed grades except 71V124SA10.
- $V_{IH}(\text{max.}) = V_{DD}+2\text{V}$ for pulse width less than 5ns, once per cycle.
- $V_{IL}(\text{min.}) = -2\text{V}$ for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics^(1, 2)

(V_{DD} = Min. to Max., V_{LC} = 0.2V, V_{HC} = V_{DD} - 0.2V)

| Symbol | Parameter | 71V124SA10 | 71V124SA12 | | 71V124SA15 | | Unit |
|------------------|--|------------|------------|-----|------------|-----|------|
| | | Commercial | Com'l | Ind | Com'l | Ind | |
| I _{CC} | Dynamic Operating Current CS ≤ V _{LC} , Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽³⁾ | 145 | 130 | 140 | 100 | 120 | mA |
| I _{SB} | Dynamic Standby Power Supply Current CS ≥ V _{HC} , Outputs Open, V _{DD} = Max., f = f _{MAX} ⁽³⁾ | 45 | 40 | 40 | 35 | 40 | mA |
| I _{SB1} | Full Standby Power Supply Current (static) CS ≥ V _{HC} , Outputs Open, V _{DD} = Max., f = 0 ⁽³⁾ | 10 | 10 | 10 | 10 | 10 | mA |

NOTES:

- All values are maximum guaranteed values.
- All inputs switch between 0.2V (Low) and V_{DD}-0.2V (High).
- f_{MAX} = 1/TRC (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

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AC Test Conditions

| | |
|-------------------------------|--------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figure 1 and 2 |

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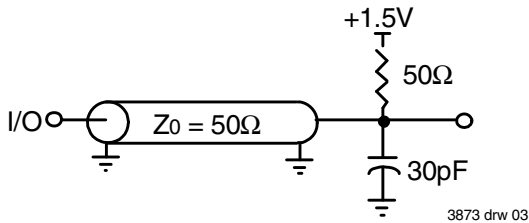
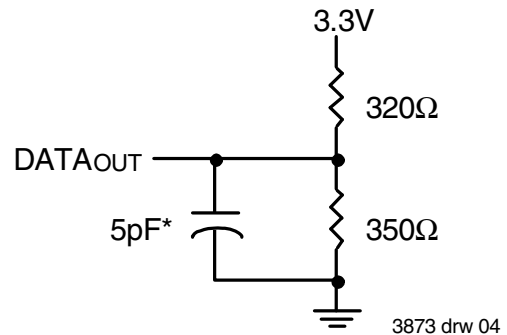


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC Electrical Characteristics

(VDD = Min. to Max., Commercial and Industrial Temperature Ranges)

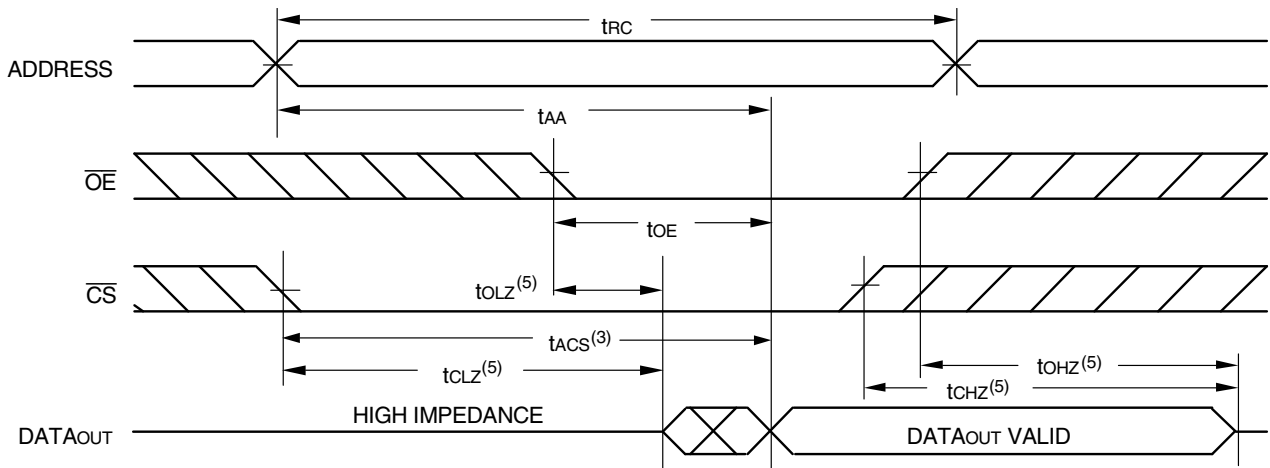
| Symbol | Parameter | 71V124SA10 | | 71V124SA12 | | 71V124SA15 | | Unit |
|---------------------------------|------------------------------------|------------|------|------------|------|------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 10 | — | 12 | — | 15 | — | ns |
| t _{AA} | Address Access Time | — | 10 | — | 12 | — | 15 | ns |
| t _{ACS} | Chip Select Access Time | — | 10 | — | 12 | — | 15 | ns |
| t _{CLZ} ⁽¹⁾ | Chip Select to Output in Low-Z | 4 | — | 4 | — | 4 | — | ns |
| t _{CHZ} ⁽¹⁾ | Chip Deselect to Output in High-Z | 0 | 5 | 0 | 6 | 0 | 7 | ns |
| t _{OE} | Output Enable to Output Valid | — | 5 | — | 6 | — | 7 | ns |
| t _{OLZ} ⁽¹⁾ | Output Enable to Output in Low-Z | 0 | — | 0 | — | 0 | — | ns |
| t _{OHZ} ⁽¹⁾ | Output Disable to Output in High-Z | 0 | 5 | 0 | 5 | 0 | 5 | ns |
| t _{OH} | Output Hold from Address Change | 4 | — | 4 | — | 4 | — | ns |
| WRITE CYCLE | | | | | | | | |
| t _{WC} | Write Cycle Time | 10 | — | 12 | — | 15 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 7 | — | 8 | — | 10 | — | ns |
| t _{CW} | Chip Select to End-of-Write | 7 | — | 8 | — | 10 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width | 7 | — | 8 | — | 10 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| t _{DW} | Data Valid to End-of-Write | 5 | — | 6 | — | 7 | — | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| t _{OW} ⁽²⁾ | Output Active from End-of-Write | 3 | — | 3 | — | 3 | — | ns |
| t _{WHZ} ⁽²⁾ | Write Enable to Output in High-Z | 0 | 5 | 0 | 5 | 0 | 5 | ns |

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NOTES:

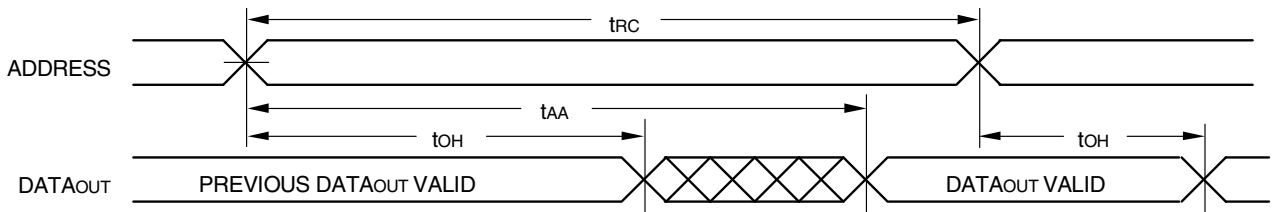
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1⁽¹⁾



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Timing Waveform of Read Cycle No. 2^(1, 2, 4)

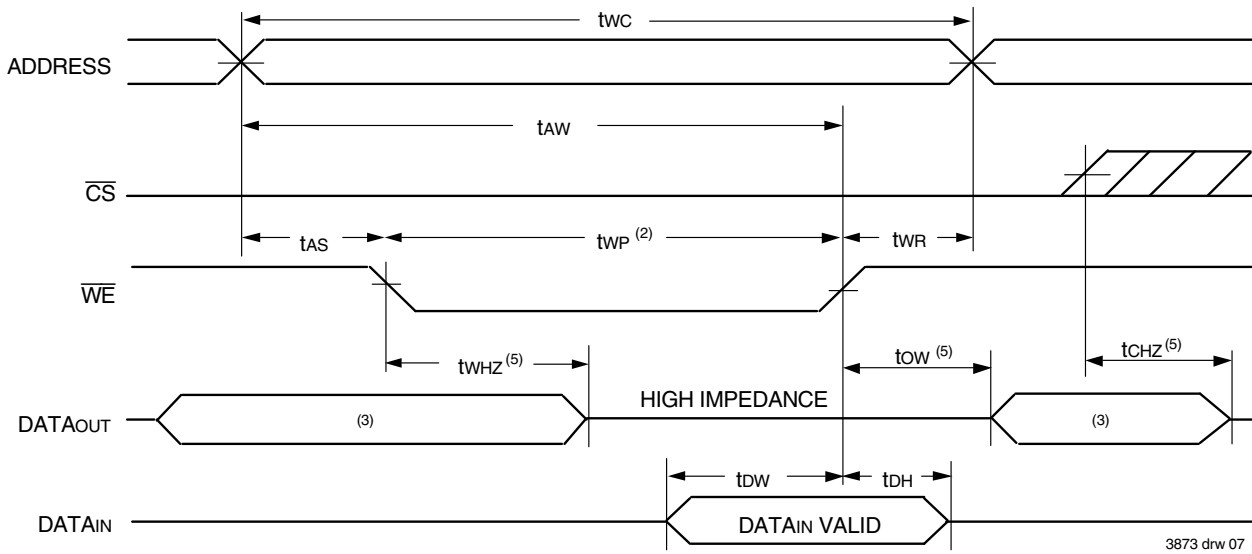


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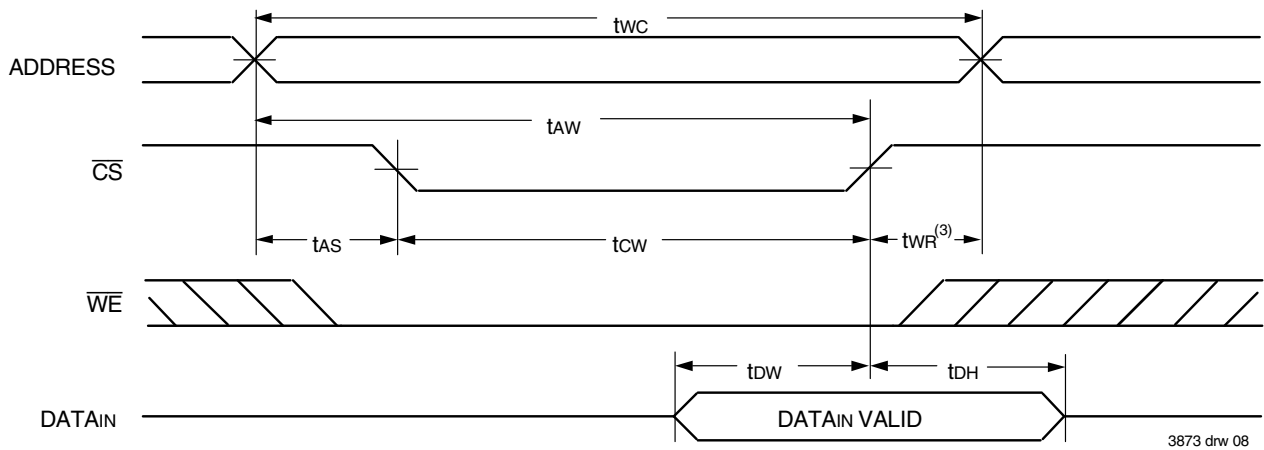
NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. Address must be valid prior to or coincident with the later of \overline{CS} transition LOW; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,4)



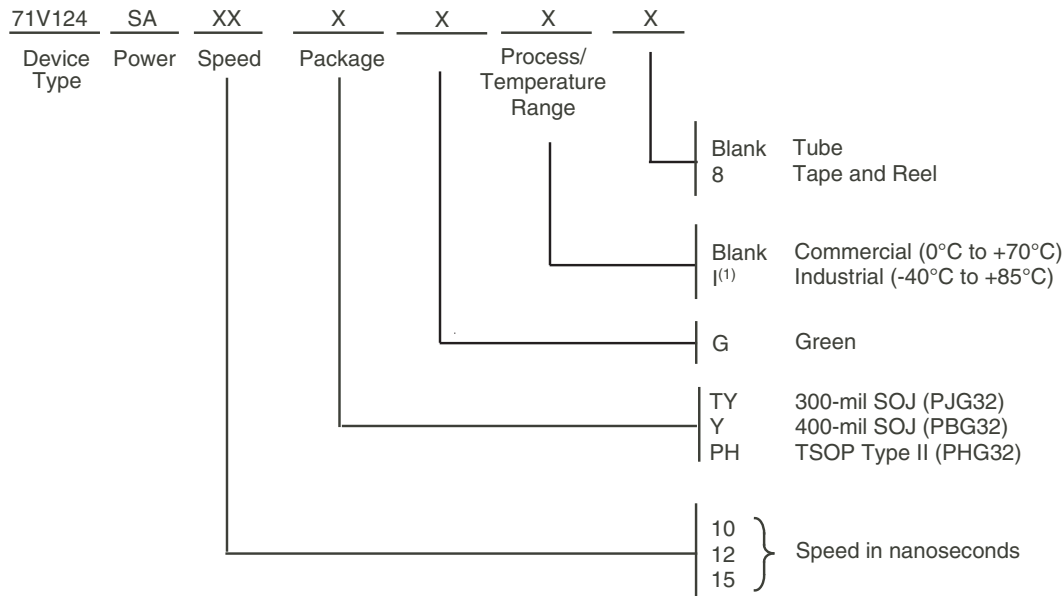
Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)^(1, 4)



NOTES:

1. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
2. \overline{OE} is continuously HIGH. During a \overline{WE} controlled write cycle with \overline{OE} LOW, t_{WP} must be greater than or equal to t_{WHZ} + t_{OW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high impedance state. \overline{CS} must be active during the t_{OW} write period.
5. Transition is measured ± 200 mV from steady state.

Ordering Information



NOTE:

1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.

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Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 10 | 71V124SA10PHG | PHG32 | TSOP | C |
| | 71V124SA10PHG8 | PHG32 | TSOP | C |
| | 71V124SA10PHGI | PHG32 | TSOP | I |
| | 71V124SA10PHG8I | PHG32 | TSOP | I |
| | 71V124SA10TYG | PJG32 | SOJ | C |
| | 71V124SA10TYG8 | PJG32 | SOJ | C |
| | 71V124SA10YG | PBG32 | SOJ | C |
| | 71V124SA10YG8 | PBG32 | SOJ | C |
| 12 | 71V124SA12PHG | PHG32 | TSOP | C |
| | 71V124SA12PHG8 | PHG32 | TSOP | C |
| | 71V124SA12PHGI | PHG32 | TSOP | I |
| | 71V124SA12PHG8I | PHG32 | TSOP | I |
| | 71V124SA12TYG | PJG32 | SOJ | C |
| | 71V124SA12TYG8 | PJG32 | SOJ | C |
| | 71V124SA12TYGI | PJG32 | SOJ | I |
| | 71V124SA12TYG8I | PJG32 | SOJ | I |
| | 71V124SA12YG | PBG32 | SOJ | C |
| | 71V124SA12YG8 | PBG32 | SOJ | C |
| | 71V124SA12YGI | PBG32 | SOJ | I |
| | 71V124SA12YG8I | PBG32 | SOJ | I |

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 15 | 71V124SA15PHG | PHG32 | TSOP | C |
| | 71V124SA15PHG8 | PHG32 | TSOP | C |
| | 71V124SA15PHGI | PHG32 | TSOP | I |
| | 71V124SA15PHG8I | PHG32 | TSOP | I |
| | 71V124SA15TYG | PJG32 | SOJ | C |
| | 71V124SA15TYG8 | PJG32 | SOJ | C |
| | 71V124SA15TYGI | PJG32 | SOJ | I |
| | 71V124SA15TYG8I | PJG32 | SOJ | I |
| | 71V124SA15YG | PBG32 | SOJ | C |
| | 71V124SA15YG8 | PBG32 | SOJ | C |
| | 71V124SA15YGI | PBG32 | SOJ | I |
| | 71V124SA15YG8I | PBG32 | SOJ | I |

Datasheet Document History

| | | |
|----------|-------------|---|
| 11/22/99 | | Updated to new format |
| | Pg. 1-4, 7 | Added Industrial Temperature range offerings |
| | Pg. 2 | Added Recommended Operating Temperature and Supply Voltage table |
| | Pg. 6 | Revised footnotes on Write Cycle No. 1 diagram |
| | Pg. 8 | Added Datasheet Document History |
| 08/30/00 | Pg. 3 | Tighten Icc and Isb |
| | Pg. 4 | Tighten AC Characteristics toHZ, tow and tWHZ |
| 08/22/01 | Pg. 7 | Removed footnote "400-mil SOJ package only offered in 10ns and 12ns speed grade" |
| 11/30/03 | Pg. 1,3,7 | Added Industrial temperature offering 10ns speed grade |
| 01/30/04 | Pg. 7 | Added "Restricted hazardous substance device" to ordering information |
| 2/14/07 | Pg. 7 | Added H generation die step to data sheet ordering information |
| 10/13/08 | Pg. 7 | Removed "IDT" from the orderable part number |
| 11/15/10 | Pg. 1,3,4,7 | Removed 20ns commercial, 10ns & 20ns industrial and also removed HSA offering |
| 03/29/12 | Pg. 7 | Removed die step indicator from the ordering information Added tape and reel and green to the ordering information |
| 02/19/13 | Pg. 1 | Removed IDT reference to fabrication and changed fastest access address time from 9ns to 10ns |
| 03/10/17 | Pg. 2 | Updated pin configurations with correct package codes and with new IDT logo |
| 06/30/20 | Pg. 1 - 9 | Rebranded as Renesas datasheet |
| | Pg. 2 & 7 | Updated package codes |
| | Pg. 1 & 7 | Updated Industrial temp range and green availability |
| | Pg. 7 | Added Orderable Part Information table |

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