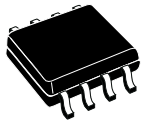
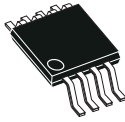


## Low-power, rail-to-rail output, 36 V operational amplifiers



SO8



MiniSO8



SOT23-5

### Features

- Low offset voltage: 1 mV max
- Low current consumption: 125  $\mu$ A max. per amplifier at 36 V
- Wide supply voltage: 2.7 to 36 V
- Gain bandwidth product: 560 kHz typ
- Unity gain stable
- Rail-to-rail output
- Input common mode voltage includes ground
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive qualification

### Applications

- Industrial
- Power supplies
- Automotive

### Description

The **TSB611**, **TSB612** operational amplifiers (op amps) offer an extended supply voltage operating range and rail-to-rail output. They also offer an excellent speed/power consumption ratio with 560 kHz gain bandwidth product while consuming less than 125  $\mu$ A per amplifier at 36 V supply voltage.

The **TSB611**, **TSB612** operate over a wide temperature range from -40 °C to 125°C making this device ideal for industrial and automotive applications.

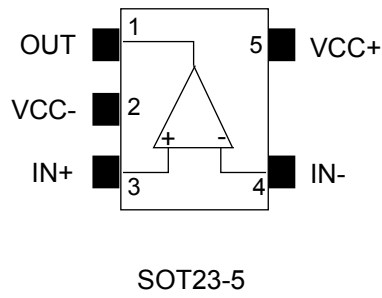
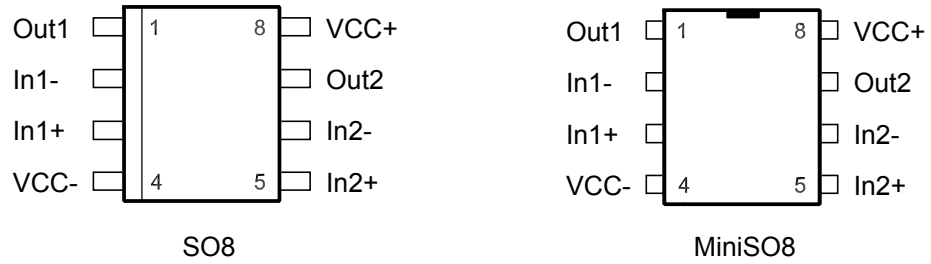
Thanks to their small package size, the **TSB611**, **TSB612** can be used in applications where space on the board is limited. They can thus reduce the overall cost of the PCB.

Maturity status link

[TSB611, TSB612](#)

# 1 Pin connection

Figure 1. Pin connection (top view)



## 2 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage <sup>(1)</sup>	40	V	
$V_{id}$	Differential input voltage <sup>(2)</sup>	$\pm V_{CC}$		
$V_{in}$	Input voltage	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$		
$I_{in}$	Input current <sup>(3)</sup>	10	mA	
$T_{stg}$	Storage temperature	-65 to 150	°C	
$R_{thja}$	Thermal resistance junction to ambient <sup>(4)</sup> <sup>(5)</sup>	SOT23-5	250	°C/W
		MiniSO8	190	
		SO-8	125	
$T_j$	Maximum junction temperature	150	°C	
ESD	HBM: human body model <sup>(6)</sup>	4000	V	
	CDM: charged device model <sup>(7)</sup>	1500		
	Latch-up immunity	200	mA	

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Input current must be limited by a resistor in series with the inputs.
4.  $R_{th}$  are typical values.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. According to JEDEC standard JESD22-A114F.
7. According to ANSI/ESD STM5.3.1.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	2.7 to 36	V
$V_{icm}$	Common mode input voltage range	$(V_{CC-}) - 0.1$ to $(V_{CC+}) - 1$	
$T_{oper}$	Operating free air temperature range	-40 to 125	°C

### 3 Electrical characteristics

**Table 3. Electrical characteristics at  $V_{CC+} = 2.7\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Input offset voltage		-1		1	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1.8	6	$\mu\text{V}/^{\circ}\text{C}$
$I_{io}$	Input offset current			1	5	nA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			10	
$I_{ib}$	Input bias current	$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		5	10	
CMR	Common mode rejection ratio: $20 \log(\Delta V_{icm}/\Delta V_{io})$	$V_{icm} = 0\text{ V}$ to $V_{CC+} - 1\text{ V}$ , $V_{out} = V_{CC}/2$	90	115		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	85			
$A_{vd}$	Large signal voltage gain	$V_{out} = 0.5\text{ V}$ to $(V_{CC+} - 0.5\text{ V})$				
		TSB611	98	102		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	94			
		TSB612	96	102		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	93			
$V_{OH}$	High level output voltage (voltage drop from $V_{CC+}$ )			13	25	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			30	
$V_{OL}$	Low level output voltage			26	30	
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			35	
$I_{out}$	$I_{sink}$	$V_{out} = V_{CC}$	13	20		mA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	10			
	$I_{source}$	$V_{out} = 0\text{ V}$	20	28		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	7			
$I_{CC}$	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$		92	110	$\mu\text{A}$
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			125	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		480		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		430		
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		60		Degrees
$G_m$	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		18		dB
SR+	Positive slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$	0.13	0.18		V/ $\mu\text{s}$
SR-	Negative slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$	0.10	0.14		
$e_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$		37		nV/ $\sqrt{\text{Hz}}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$e_n$	Equivalent input noise voltage	$f = 10 \text{ kHz}$		32		$\text{nV}/\sqrt{\text{Hz}}$
THD+N	Total harmonic distortion + noise	$f_{in} = 1 \text{ kHz}$ , Gain = 1, $R_L = 100 \text{ k}\Omega$ , $V_{icm} = (V_{cc} - 1 \text{ V})/2$ , BW = 22 kHz, $V_{out} = 1 \text{ V}_{pp}$		0.005		%
$t_{rec}$	Overload recovery time			2		$\mu\text{s}$

**Table 4. Electrical characteristics at  $V_{CC+} = 12\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{ICM} = V_{CC}/2$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Input offset voltage		-1		1	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1.6	6	$\mu\text{V}/^{\circ}\text{C}$
$I_{io}$	Input offset current			1	5	nA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			15	
$I_{ib}$	Input bias current			5	10	nA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			15	
CMR	Common mode rejection ratio: $20\log(\Delta V_{icm}/\Delta V_{io})$	$V_{icm} = 0\text{ V to } V_{CC+} - 1\text{ V}, V_{out} = V_{CC}/2$	95	126		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	90			
SVR	Supply voltage rejection ratio: $20\log(\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 2.8\text{ to } 12\text{ V}$	95	124		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	90			
$A_{vd}$	Large signal voltage gain	$V_{out} = 0.5\text{ V to } (V_{CC+} - 0.5\text{ V})$	105	115		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	100			
$V_{OH}$	High level output voltage drop from $V_{CC+}$			37	60	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			65	
$V_{OL}$	Low level output voltage			56	65	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			75	
$I_{out}$	$I_{sink}$	$V_{out} = V_{CC}$	24	35		mA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	10			
	$I_{source}$	$V_{out} = 0\text{ V}$	28	40		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	10			
$I_{CC}$	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$		97	115	$\mu\text{A}$
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			130	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$		510		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$		460		
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$		60		Degrees
$G_m$	Gain margin	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}$		18		dB
SR+	Positive slew rate	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}, V_{out} = 0.5\text{ V to } V_{CC} - 0.5\text{ V}$	0.13	0.19		V/ $\mu\text{s}$
SR-	Negative slew rate	$R_L = 10\text{ k}\Omega, C_L = 100\text{ pF}, V_{out} = 0.5\text{ V to } V_{CC} - 0.5\text{ V}$	0.11	0.15		
$e_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$		31		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		30		
THD+N	Total harmonic distortion + noise	$f_{in} = 1\text{ kHz}, \text{Gain} = 1, R_L = 100\text{ k}\Omega, V_{icm} = (V_{CC} - 1\text{ V})/2, \text{BW} = 22\text{ kHz}, V_{out} = 2\text{ V}_{pp}$		0.004		%

---

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{rec}$	Overload recovery time			2		$\mu s$

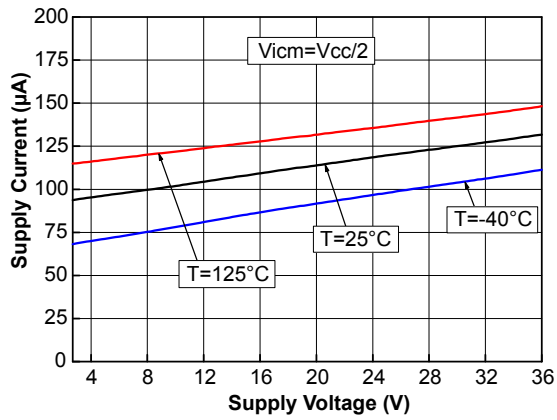
**Table 5. Electrical characteristics at  $V_{CC+} = 36\text{ V}$  with  $V_{CC-} = 0\text{ V}$ ,  $V_{ICM} = V_{CC}/2$ ,  $T_{amb} = 25\text{ }^{\circ}\text{C}$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Input offset voltage		-1		1	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$		1.3	6	$\mu\text{V}/^{\circ}\text{C}$
$I_{io}$	Input offset current			1	5	nA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			20	
$I_{ib}$	Input bias current			5	10	nA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			20	
CMR	Common mode rejection ratio: 20 log ( $\Delta V_{icm}/\Delta V_{io}$ )	$V_{icm} = 0\text{ V to } V_{CC+} - 1\text{ V}$ , $V_{out} = V_{CC}/2$	105	130		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	100			
SVR	Supply voltage rejection ratio 20 log ( $\Delta V_{CC}/\Delta V_{io}$ )	$V_{CC} = 12\text{ to } 36\text{ V}$	100	124		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	95			
$A_{vd}$	Large signal voltage gain	$V_{out} = 0.5\text{ V to } (V_{CC+} - 0.5\text{ V})$	110	120		dB
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	105			
$V_{OH}$	High level output voltage drop from $V_{CC+}$			80	110	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			150	
$V_{OL}$	Low level output voltage			90	110	mV
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			150	
$I_{out}$	$I_{sink}$	$V_{out} = V_{CC}$	40	60		mA
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	10			
	$I_{source}$	$V_{out} = 0\text{ V}$	40	70		
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$	20			
$I_{CC}$	Supply current (per channel)	No load, $V_{out} = V_{CC}/2$		103	125	$\mu\text{A}$
		$-40\text{ }^{\circ}\text{C} < T < 125\text{ }^{\circ}\text{C}$			140	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		560		kHz
$F_u$	Unity gain frequency	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		500		
$\phi_m$	Phase margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		58		Degrees
$G_m$	Gain margin	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$		18		dB
SR+	Positive slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$	0.15	0.20		V/ $\mu\text{s}$
SR-	Negative slew rate	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $V_{out} = 0.5\text{ V}$ to $V_{CC} - 0.5\text{ V}$	0.12	0.16		
$e_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$		29		nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		28		
THD+N	Total harmonic distortion + noise	$f_{in} = 1\text{ kHz}$ , Gain = 1, $R_L = 100\text{ k}\Omega$ , $V_{icm} = (V_{CC} - 1\text{ V})/2$ , BW = 22 kHz, $V_{out} = 2\text{ V}_{pp}$		0.004		%

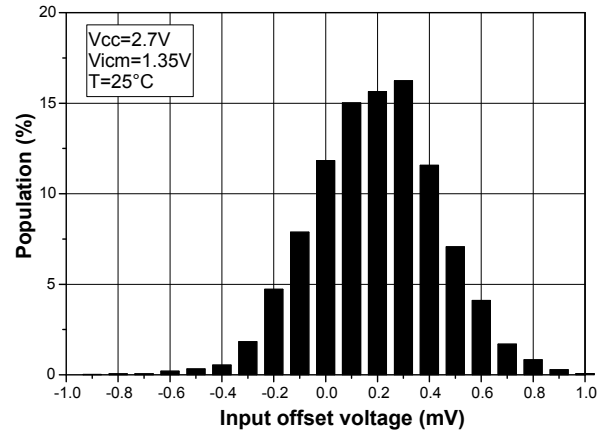


Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{rec}$	Overload recovery time	$R_L = 10\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , Gain = 1		2		$\mu\text{s}$

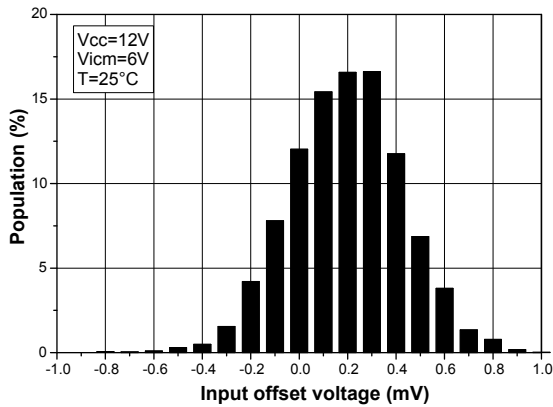
**Figure 2. Supply current vs. supply voltage at  $V_{icm} = V_{CC}/2$**



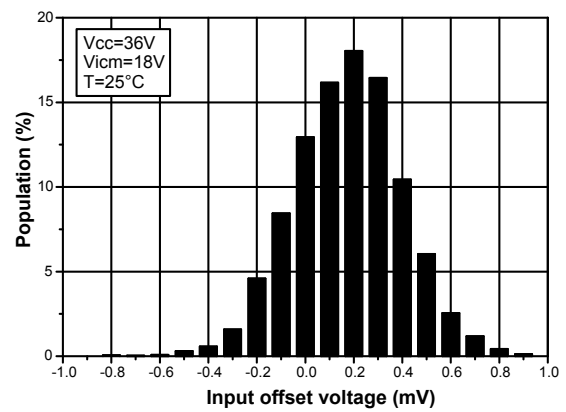
**Figure 3. Input offset voltage distribution at  $V_{CC} = 2.7\text{ V}$**



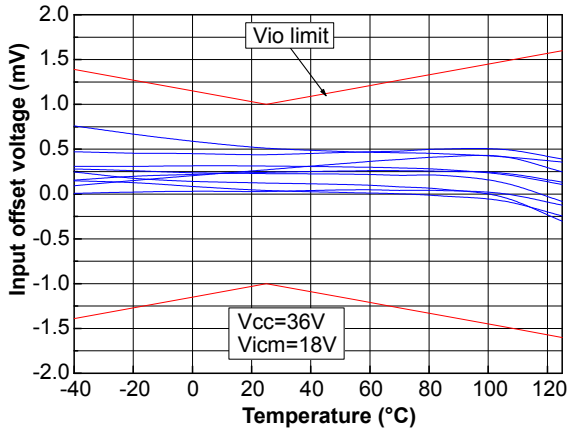
**Figure 4. Input offset voltage distribution at  $V_{CC} = 12\text{ V}$**



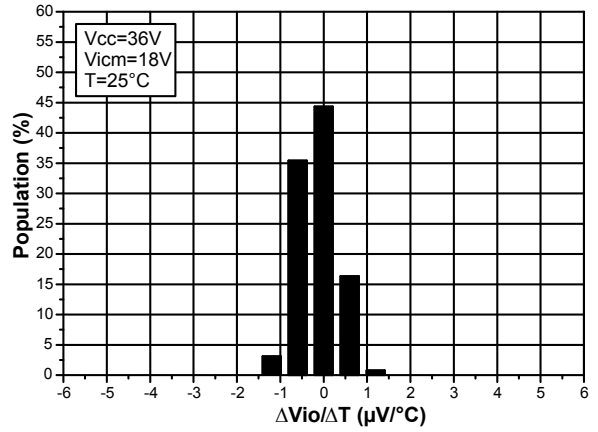
**Figure 5. Input offset voltage distribution at  $V_{CC} = 36\text{ V}$**



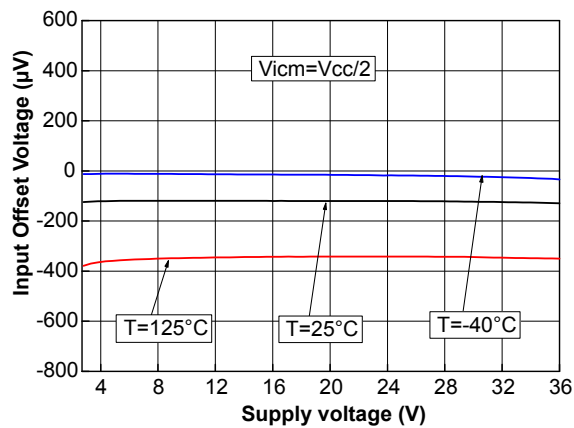
**Figure 6. Input offset voltage vs. Temperature at  $V_{CC} = 36$  V**



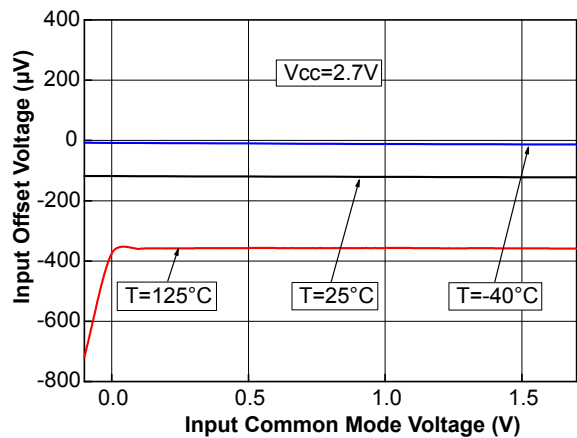
**Figure 7. Input offset voltage temperature variation distribution at  $V_{CC} = 36$  V**



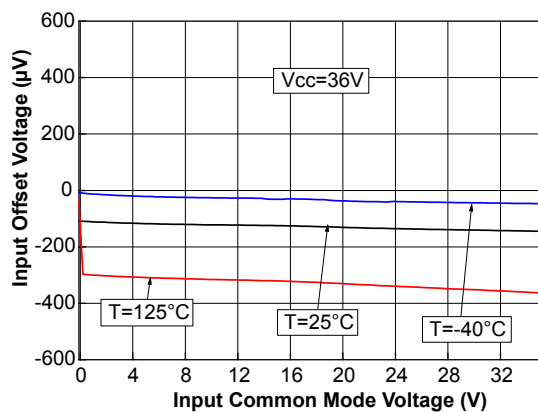
**Figure 8. Input offset voltage vs. supply voltage**



**Figure 9. Input offset voltage vs. common-mode voltage at  $V_{CC} = 2.7$  V**



**Figure 10. Input offset voltage vs. common-mode voltage at  $V_{CC} = 36$  V**



**Figure 11. Input bias current vs common mode voltage at  $V_{CC} = 4$  V**

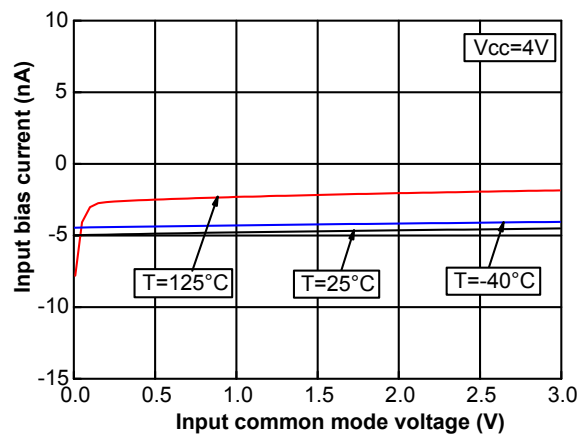


Figure 12. Input bias current vs common mode voltage at  $V_{CC} = 36\text{ V}$

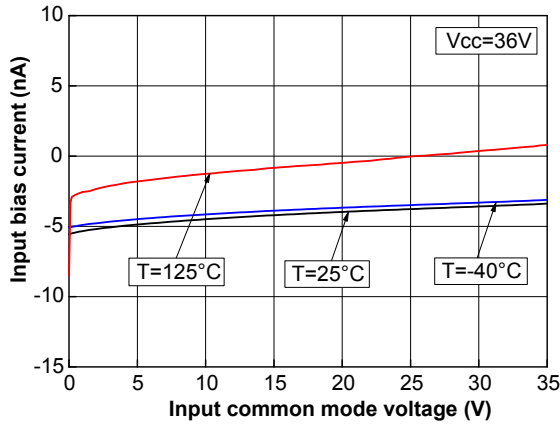


Figure 13. Output current vs. output voltage at  $V_{CC} = 2.7\text{ V}$

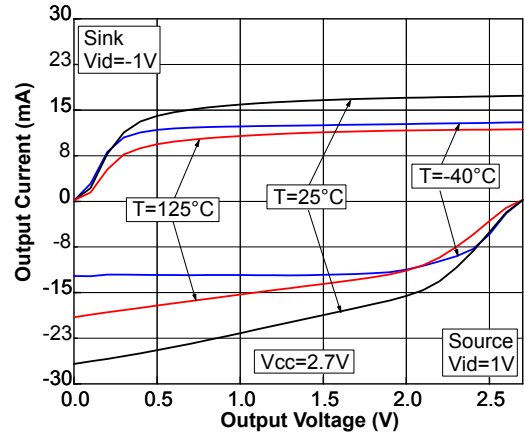


Figure 14. Output current vs. output voltage at  $V_{CC} = 36\text{ V}$

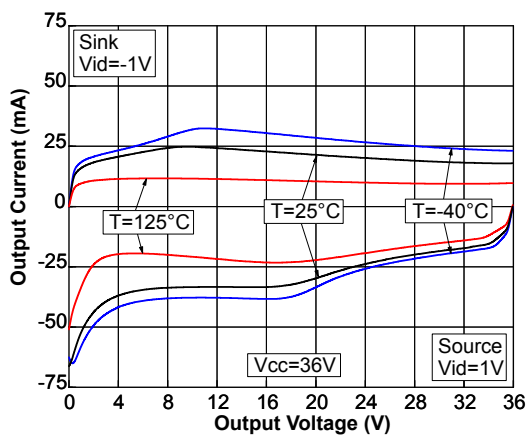


Figure 15. Output voltage (Voh) vs. supply voltage

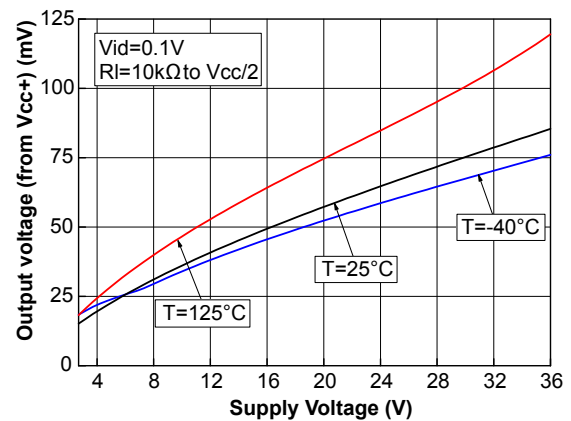


Figure 16. Output voltage (Vol) vs. supply voltage

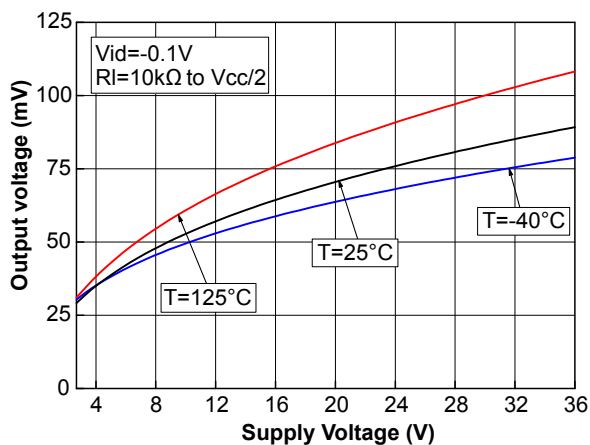


Figure 17. Amplifier behavior close to negative rail at  $V_{CC} = 5\text{ V}$

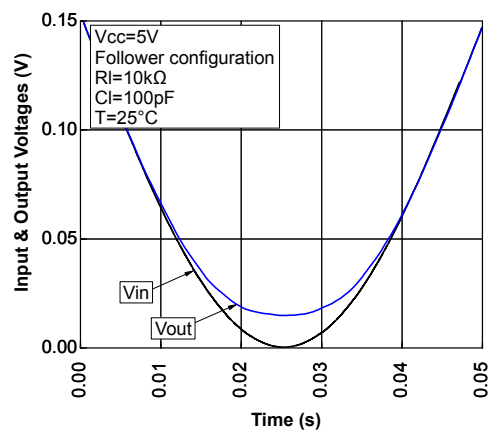


Figure 18. Amplifier behavior close to positive rail at  $V_{CC} = 5\text{ V}$

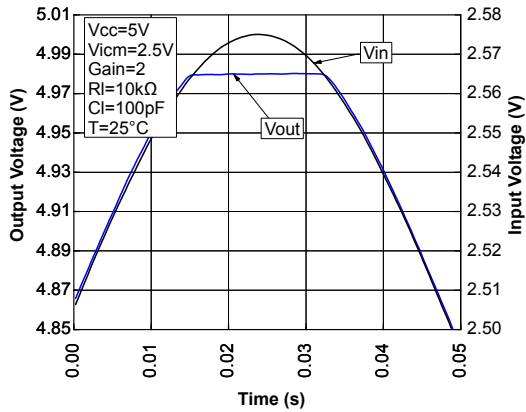


Figure 19. Slew rate vs. supply voltage

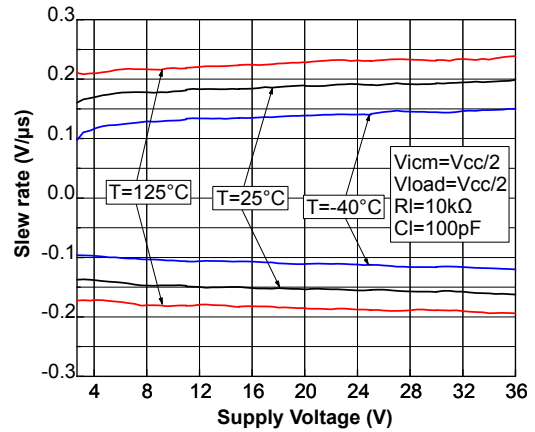


Figure 20. Negative slew rate behavior vs. temperature at  $V_{CC} = 36\text{ V}$

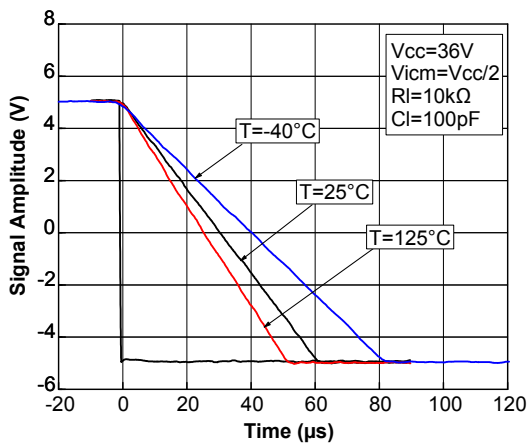


Figure 21. Positive slew rate behavior vs. temperature at  $V_{CC} = 36\text{ V}$

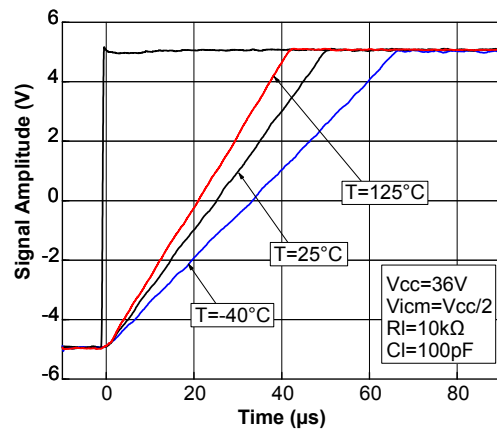


Figure 22. Small step response vs. time at  $V_{CC} = 36\text{ V}$

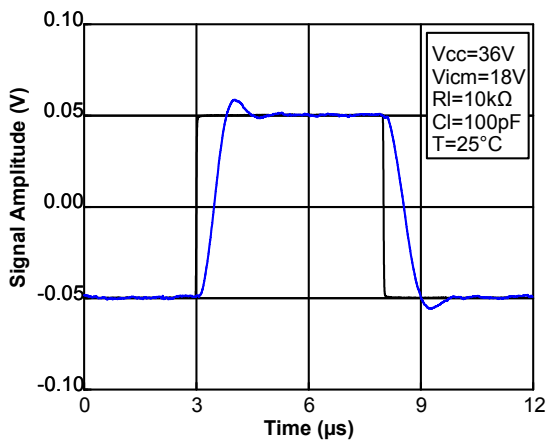


Figure 23. Output desaturation vs. time

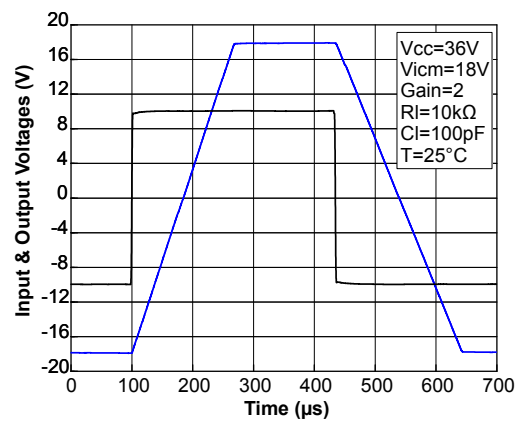


Figure 24. Gain and phase vs. frequency at  $V_{CC} = 2.7\text{ V}$

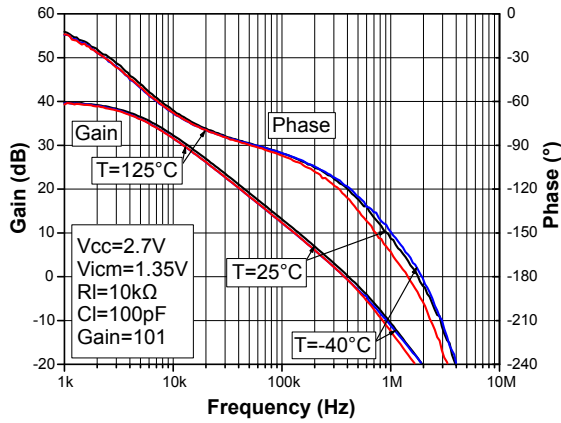


Figure 25. Gain and phase vs. frequency at  $V_{CC} = 36\text{ V}$

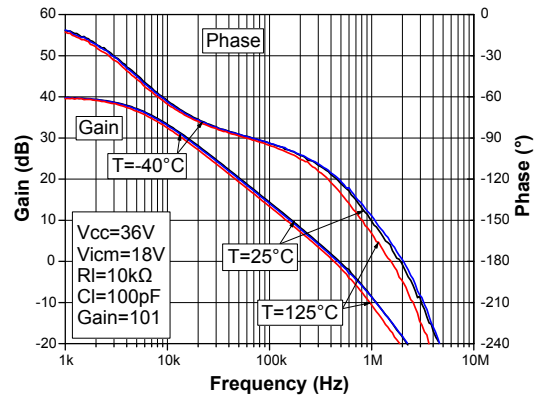


Figure 26. Phase margin vs. output current at  $V_{CC} = 2.7\text{ V}$  and  $36\text{ V}$

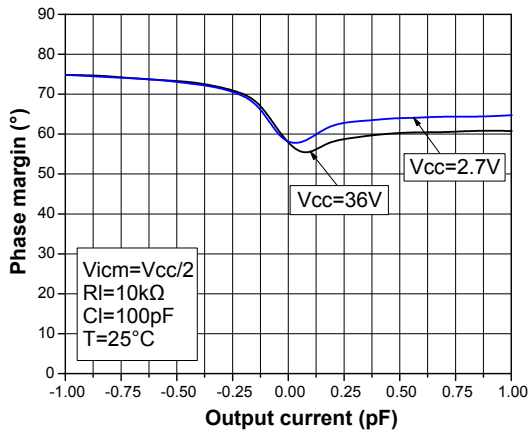


Figure 27. Phase margin vs. capacitive load at  $V_{CC} = 2.7\text{ V}$  and  $36\text{ V}$

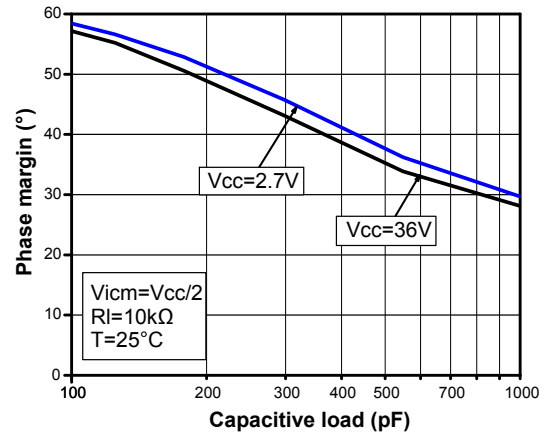


Figure 28. Overshoot vs. capacitive load at  $V_{CC} = 2.7\text{ V}$  and  $36\text{ V}$

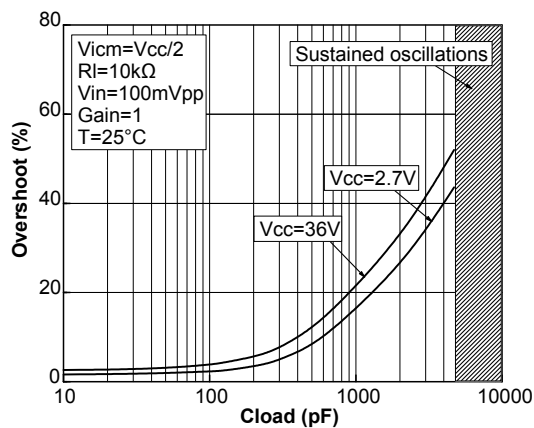
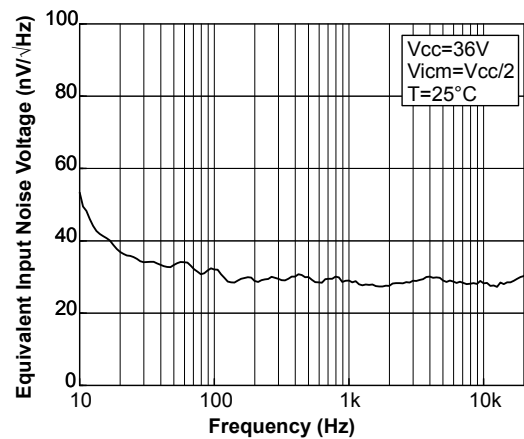
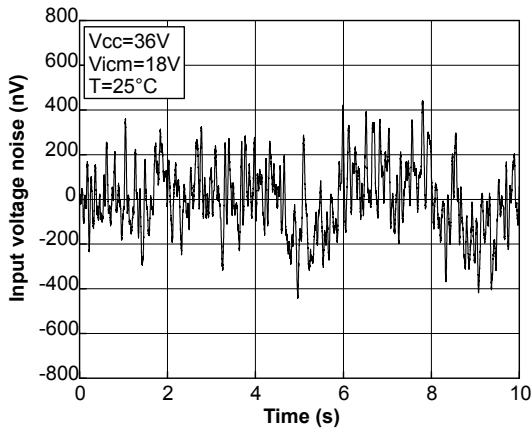


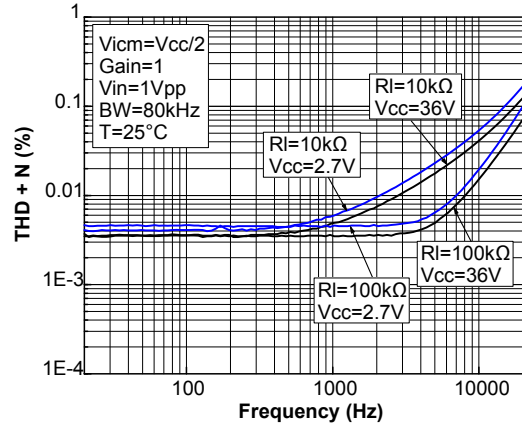
Figure 29. Noise vs. frequency at  $V_{CC} = 36\text{ V}$



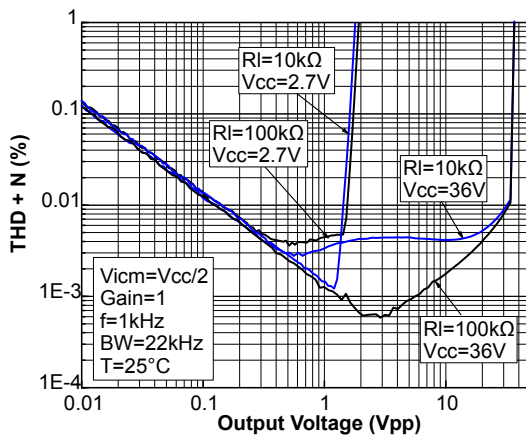
**Figure 30. Noise vs. time at  $V_{CC} = 36\text{ V}$**



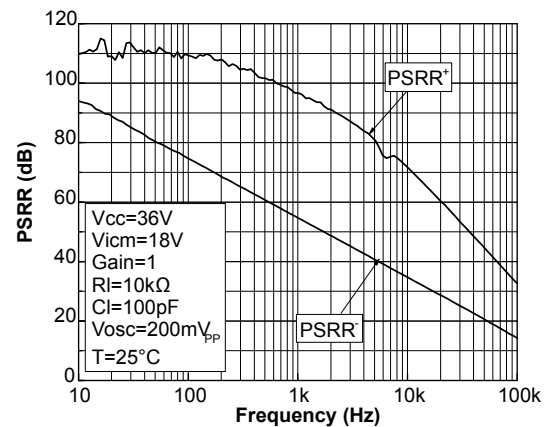
**Figure 31. THD+N vs. frequency**



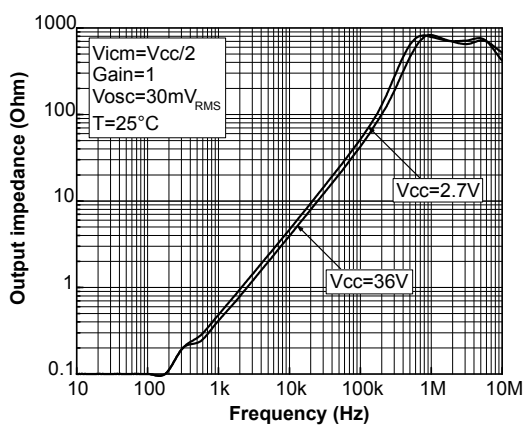
**Figure 32. THD+N vs. output voltage**



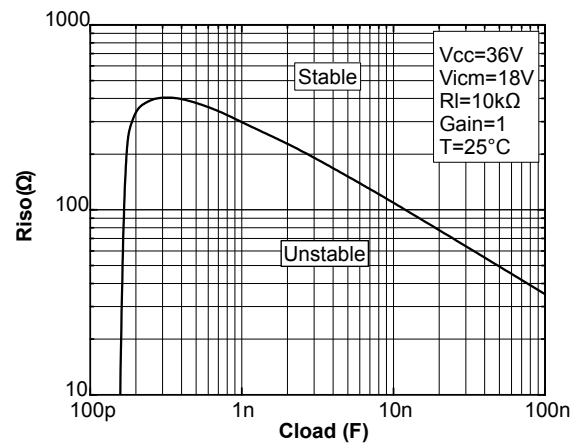
**Figure 33. PSRR vs. frequency at  $V_{CC} = 36\text{ V}$**



**Figure 34. Output impedance vs. frequency at  $V_{CC} = 2.7\text{ V}$  and  $36\text{ V}$**



**Figure 35. Output series resistor recommended for stability vs. capacitive load**



## 4 Application information

### 4.1 Operating voltages

The TSB611, TSB612 operational amplifiers can operate from 2.7 V to 36 V. The parameters are fully specified at 2.7 V, 12 V, and 36 V power supplies. However, parameters are very stable in the full  $V_{CC}$  range. Additionally, main specifications are guaranteed in the extended temperature range from -40 to 125 °C.

### 4.2 Input common-mode range

The TSB611, TSB612 have an input common-mode range that includes ground. The input common-mode range is extended from  $(V_{CC-}) - 0.1$  V to  $(V_{CC+}) - 1$  V.

### 4.3 Rail-to-rail output

The operational amplifier's output levels can go close to the rails: 100 mV maximum below the positive rail and 110 mV maximum above the negative rail when connected to a 10 k $\Omega$  resistive load to  $V_{CC}/2$  for a power supply voltage of 36 V.

### 4.4 Input offset voltage drift over temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using [Equation 1](#).

#### Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25\text{ °C})}{T - 25\text{ °C}} \right|$$

Where T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a  $C_{pk}$  (process capability index) greater than 2.

## 4.5 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using [Equation 2](#).

### Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

$A_{FV}$  is the voltage acceleration factor

$\beta$  is the voltage acceleration constant in  $1/V$ , constant technology parameter ( $\beta = 1$ )

$V_S$  is the stress voltage used for the accelerated test

$V_U$  is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in [Equation 3](#).

### Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left( \frac{1}{T_U} - \frac{1}{T_S} \right)}$$

Where:

$A_{FT}$  is the temperature acceleration factor

$E_a$  is the activation energy of the technology based on the failure rate

$k$  is the Boltzmann constant ( $8.6173 \times 10^{-5} \text{ eV.K}^{-1}$ )

$T_U$  is the temperature of the die when  $V_U$  is used (K)

$T_S$  is the temperature of the die under temperature stress (K)

The final acceleration factor,  $A_F$ , is the multiplication of the voltage acceleration factor and the temperature acceleration factor ([Equation 4](#)).

### Equation 4

$$A_F = A_{FT} \times A_{FV}$$

$A_F$  is calculated using the temperature and voltage defined in the mission profile of the product. The  $A_F$  value can then be used in [Equation 5](#) to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

### Equation 5

$$\text{Months} = A_F \times 1000 \text{ h} \times 12 \text{ months} / (24 \text{ h} \times 365.25 \text{ days})$$

To evaluate the op amp reliability, a follower stress condition is used where  $V_{CC}$  is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The  $V_{io}$  drift (in  $\mu\text{V}$ ) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see [Equation 6](#)).

### Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC} / 2$$

The long term drift parameter ( $\Delta V_{io}$ ), estimating the reliability performance of the product, is obtained using the ratio of the  $V_{io}$  (input offset voltage value) drift over the square root of the calculated number of months ([Equation 7](#)).

### Equation 7



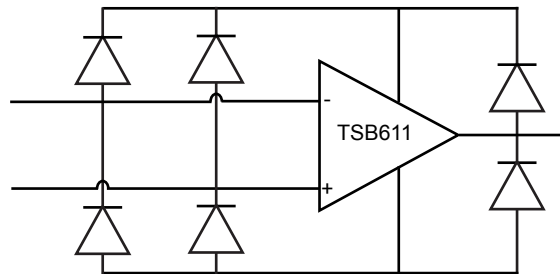
$$\Delta V_{io} = \frac{V_{io\text{ drift}}}{\sqrt{(\text{months})}}$$

Where  $V_{io}$  drift is the measured drift value in the specified test conditions after 1000 h stress duration.

#### 4.6 ESD structure of TSB611, TSB612

The TSB611, TSB612 are protected against electrostatic discharge (ESD) with dedicated diodes (see Figure 36. ESD structure). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails ( $V_{CC+}$  or  $V_{CC-}$ ). Current through the diodes must be limited to a maximum of 10 mA as stated in Table 1. Absolute maximum ratings (AMR). A serial resistor or a Schottky diode can be used on the inputs to improve protection but the 10 mA limit of input current must be strictly observed.

Figure 36. ESD structure



#### 4.7 Initialization time

The TSB611, TSB612 have a good power supply rejection ratio (PSRR), but as with all devices, it is recommended to use a 22 nF bypass capacitor as close as possible to the power supply pins. It prevents the noise present on the power supply impacting the signal conditioning. In addition, this bypass capacitor enhances the initialization time (see Figure 37. Startup behavior without bypass capacitor and Figure 38. Startup behavior with a 22 nF bypass capacitor).

Figure 37. Startup behavior without bypass capacitor

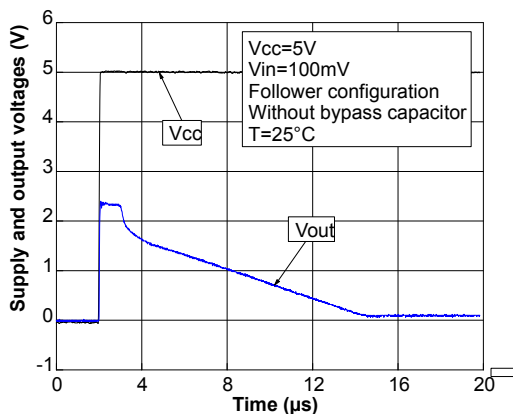
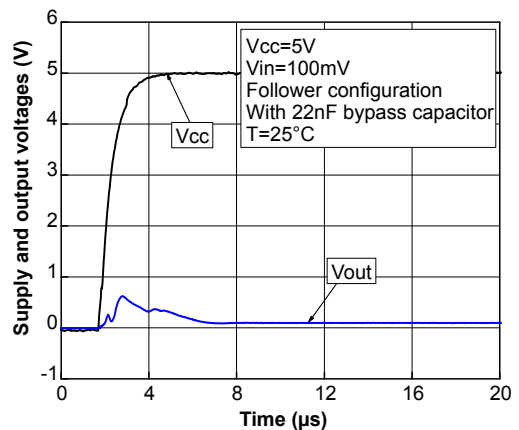


Figure 38. Startup behavior with a 22 nF bypass capacitor

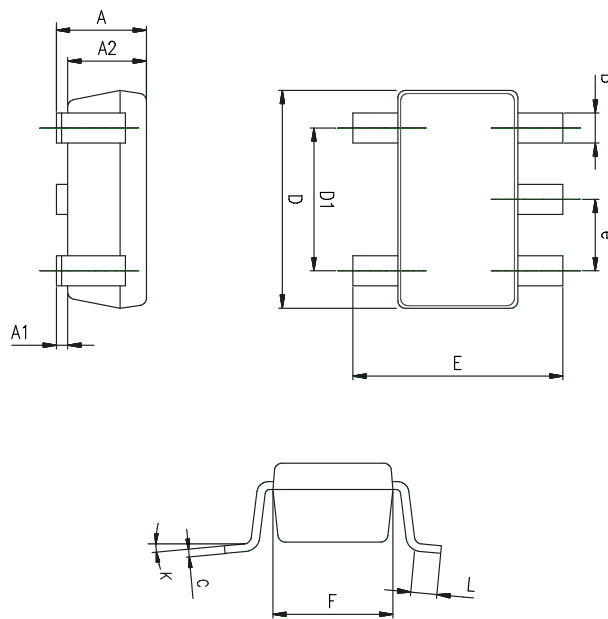


## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 5.1 SOT23-5 package information

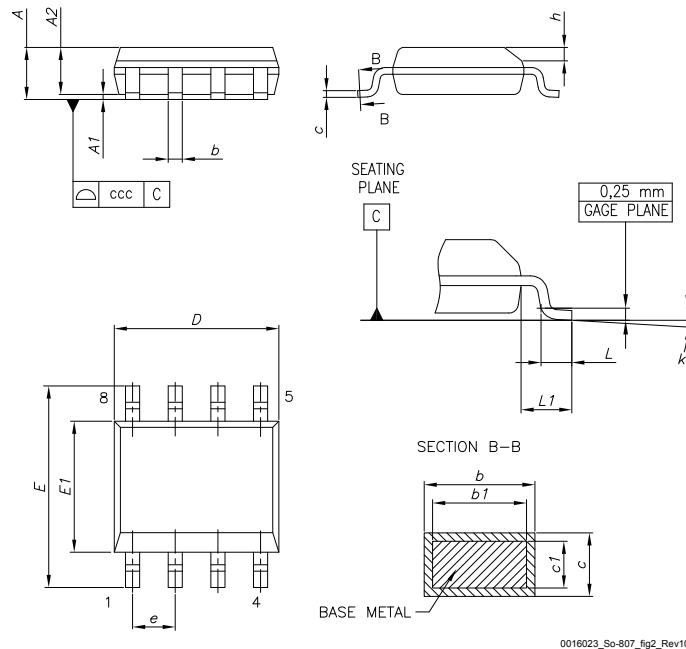
**Figure 39. SOT23-5 package outline**



**Table 6. SOT23-5 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

## 5.2 SO-8 package information

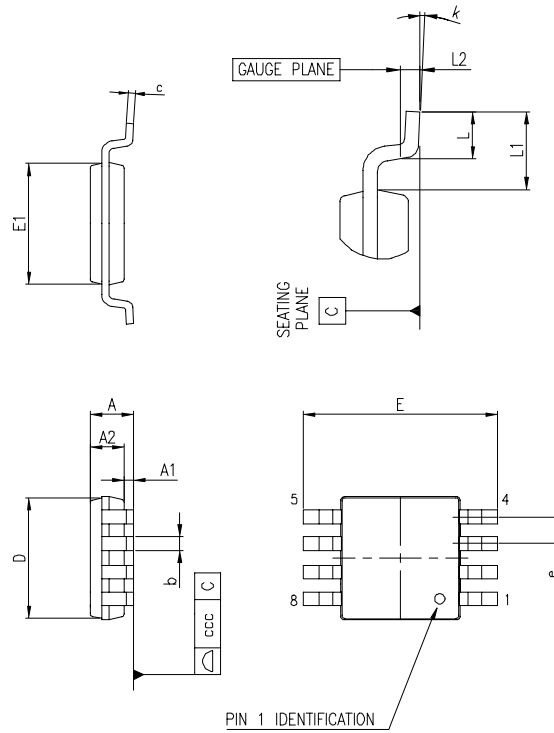
**Figure 40. SO-8 package outline**


0016023\_So-807\_fig2\_Rev10

**Table 7. SO-8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

### 5.3 MiniSO8 package information

**Figure 41. MiniSO8 package outline**

**Table 8. MiniSO8 mechanical data**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

## 6 Ordering information

**Table 9. Order codes**

Order code	Temperature range	Package	Packing	Marking
TSB611ILT	-40 °C to 125 °C	SOT23-5	Tape and reel	K191
TSB611IYLT <sup>(1)</sup>				K194
TSB612IDT		SO8		TSB612I
TSB612IYDT <sup>(1)</sup>				TSB612IY
TSB612IST		MiniSO8		K191
TSB612IYST <sup>(1)</sup>				K194

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
17-Aug-2015	1	Initial release
15-May-2017	2	Updated automotive footnote in Table 11. Order codes
12-Nov-2020	3	Added new part number TSB612, new <a href="#">Section 1 Pin connection</a> Updated <a href="#">Section 6 Ordering information</a> Minor text changes

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved