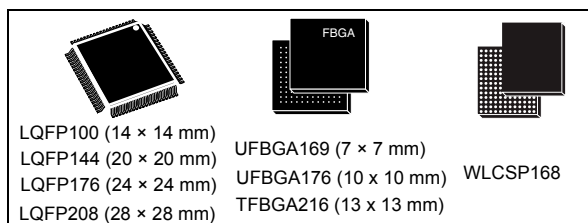


Arm[®]Cortex[®]-M4 32b MCU+FPU, 225DMIPS, up to 2MB Flash/384+4KB RAM, USB OTG HS/FS, Ethernet, FMC, dual Quad-SPI, Crypto, Graphical accelerator, Camera IF, LCD-TFT & MIPI DSI

Datasheet - production data

Features

- Core: Arm[®] 32-bit Cortex[®]-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator[™]) allowing 0-wait state execution from Flash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhystone 2.1), and DSP instructions
- Memories
 - Up to 2 MB of Flash memory organized into two banks allowing read-while-write
 - Up to 384+4 KB of SRAM including 64 KB of CCM (core coupled memory) data RAM
 - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSPDR, SDRAM, Flash NOR/NAND memories
 - Dual-flash mode Quad-SPI interface
- Graphics:
 - Chrom-ART Accelerator[™] (DMA2D), graphical hardware accelerator enabling enhanced graphical user interface with minimum CPU load
 - LCD parallel interface, 8080/6800 modes
 - LCD TFT controller supporting up to XGA resolution
 - MIPI[®] DSI host controller supporting up to 720p 30Hz resolution
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input. 2x watchdogs and SysTick timer



- Debug mode
 - SWD & JTAG interfaces
 - Cortex[®]-M4 Trace Macrocell[™]
- Up to 161 I/O ports with interrupt capability
 - Up to 157 fast I/Os up to 90 MHz
 - Up to 159 5 V-tolerant I/Os
- Up to 21 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs and 4 UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
 - Up to 6 SPIs (45 Mbits/s), 2 with muxed full-duplex I²S for audio class accuracy via internal audio PLL or external clock
 - 1 × SAI (serial audio interface)
 - 2 × CAN (2.0B Active)
 - SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - Dedicated USB power rail enabling on-chip PHYs operation throughout the entire MCU power supply range
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- Cryptographic accelerator
 - HW accelerator for AES 128, 192, 256, Triple DES, HASH (MD5, SHA-1, SHA-2) and HMAC
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM32F479xx	STM32F479AI, STM32F479AG, STM32F479BI, STM32F479BG, STM32F479II, STM32F479IG, STM32F479NI, STM32F479NG, STM32479VG, STM32479VI, STM32479ZG, STM32479ZI

Contents

1	Description	12
1.1	Compatibility throughout the family	15
1.1.1	LQFP176 package	16
1.1.2	LQFP208 package	17
1.1.3	UFPGA176 package	18
1.1.4	TFBGA216 package	19
2	Functional overview	21
2.1	Arm [®] Cortex [®] -M4 with FPU and embedded Flash and SRAM	21
2.2	Adaptive real-time memory accelerator (ART Accelerator [™])	21
2.3	Memory protection unit	21
2.4	Embedded Flash memory	22
2.5	CRC (cyclic redundancy check) calculation unit	22
2.6	Embedded SRAM	22
2.7	Multi-AHB bus matrix	22
2.8	DMA controller (DMA)	23
2.9	Flexible Memory Controller (FMC)	24
2.10	Quad-SPI memory interface (QUADSPI)	25
2.11	LCD-TFT controller	25
2.12	DSI Host (DSIHOST)	25
2.13	Chrom-ART Accelerator [™] (DMA2D)	27
2.14	Nested vectored interrupt controller (NVIC)	27
2.15	External interrupt/event controller (EXTI)	27
2.16	Clocks and startup	28
2.17	Boot modes	28
2.18	Power supply schemes	28
2.19	Power supply supervisor	30
2.19.1	Internal reset ON	30
2.19.2	Internal reset OFF	30
2.20	Voltage regulator	31
2.20.1	Regulator ON	32
2.20.2	Regulator OFF	33

2.20.3	Regulator ON/OFF and internal reset ON/OFF availability	35
2.21	Real-time clock (RTC), backup SRAM and backup registers	35
2.22	Low-power modes	36
2.23	V _{BAT} operation	37
2.24	Timers and watchdogs	37
2.24.1	Advanced-control timers (TIM1, TIM8)	38
2.24.2	General-purpose timers (TIMx)	39
2.24.3	Basic timers TIM6 and TIM7	39
2.24.4	Independent watchdog	39
2.24.5	Window watchdog	39
2.24.6	SysTick timer	40
2.25	Inter-integrated circuit interface (I ² C)	40
2.26	Universal synchronous/asynchronous receiver transmitters (USART)	40
2.27	Serial peripheral interface (SPI)	41
2.28	Inter-integrated sound (I ² S)	41
2.29	Serial Audio interface (SAI1)	42
2.30	Audio PLL (PLLI2S)	42
2.31	Audio and LCD PLL(PLLSAI)	42
2.32	Secure digital input/output interface (SDIO)	42
2.33	Ethernet MAC interface with dedicated DMA and IEEE 1588 support	43
2.34	Controller area network (bxCAN)	43
2.35	Universal serial bus on-the-go full-speed (OTG_FS)	44
2.36	Universal serial bus on-the-go high-speed (OTG_HS)	44
2.37	Digital camera interface (DCMI)	45
2.38	Cryptographic accelerator	45
2.39	Random number generator (RNG)	45
2.40	General-purpose input/outputs (GPIOs)	45
2.41	Analog-to-digital converters (ADCs)	46
2.42	Temperature sensor	46
2.43	Digital-to-analog converter (DAC)	46
2.44	Serial wire JTAG debug port (SWJ-DP)	47
2.45	Embedded Trace Macrocell™	47
3	Pinouts and pin description	48

4	Memory mapping	84
5	Electrical characteristics	89
5.1	Parameter conditions	89
5.1.1	Minimum and maximum values	89
5.1.2	Typical values	89
5.1.3	Typical curves	89
5.1.4	Loading capacitor	89
5.1.5	Pin input voltage	89
5.1.6	Power supply scheme	90
5.1.7	Current consumption measurement	91
5.2	Absolute maximum ratings	91
5.3	Operating conditions	93
5.3.1	General operating conditions	93
5.3.2	VCAP1/VCAP2 external capacitor	95
5.3.3	Operating conditions at power-up / power-down (regulator ON)	96
5.3.4	Operating conditions at power-up / power-down (regulator OFF)	96
5.3.5	Reset and power control block characteristics	96
5.3.6	Over-drive switching characteristics	98
5.3.7	Supply current characteristics	98
5.3.8	Wakeup time from low-power modes	114
5.3.9	External clock source characteristics	115
5.3.10	Internal clock source characteristics	119
5.3.11	PLL characteristics	120
5.3.12	PLL spread spectrum clock generation (SSCG) characteristics	123
5.3.13	MIPI D-PHY characteristics	124
5.3.14	MIPI D-PHY PLL characteristics	127
5.3.15	MIPI D-PHY regulator characteristics	128
5.3.16	Memory characteristics	129
5.3.17	EMC characteristics	131
5.3.18	Absolute maximum ratings (electrical sensitivity)	132
5.3.19	I/O current injection characteristics	133
5.3.20	I/O port characteristics	134
5.3.21	NRST pin characteristics	140
5.3.22	TIM timer characteristics	141
5.3.23	Communications interfaces	141
5.3.24	12-bit ADC characteristics	156

5.3.25	Temperature sensor characteristics	162
5.3.26	V _{BAT} monitoring characteristics	162
5.3.27	Reference voltage	162
5.3.28	DAC electrical characteristics	163
5.3.29	FMC characteristics	165
5.3.30	Quad-SPI interface characteristics	185
5.3.31	Camera interface (DCMI) timing specifications	186
5.3.32	LCD-TFT controller (LTDC) characteristics	187
5.3.33	SD/SDIO MMC card host interface (SDIO) characteristics	189
5.3.34	RTC characteristics	191
6	Package information	192
6.1	LQFP100 package information	192
6.2	LQFP144 package information	195
6.3	WLCSP168 package information	198
6.4	UFBGA169 package information	200
6.5	LQFP176 package information	202
6.6	UFBGA176+25 package information	206
6.7	LQFP208 package information	208
6.8	TFBGA216 package information	212
6.9	Thermal characteristics	214
7	Part numbering	215
	Appendix A Recommendations when using internal reset OFF	216
A.1	Operating conditions	216
	Revision history	217

List of tables

Table 1.	Device summary	1
Table 2.	STM32F479xx features and peripheral counts	13
Table 3.	Voltage regulator configuration mode versus device operating mode	32
Table 4.	Regulator ON/OFF and internal reset ON/OFF availability	35
Table 5.	Voltage regulator modes in stop mode	36
Table 6.	Timer feature comparison	38
Table 7.	Comparison of I2C analog and digital filters	40
Table 8.	USART feature comparison	41
Table 9.	Legend/abbreviations used in the pinout table	56
Table 10.	STM32F479xx pin and ball definitions	57
Table 11.	FMC pin definition	71
Table 12.	Alternate function	74
Table 13.	STM32F479xx register boundary addresses	85
Table 14.	Voltage characteristics	91
Table 15.	Current characteristics	92
Table 16.	Thermal characteristics	92
Table 17.	General operating conditions	93
Table 18.	Limitations depending on the operating power supply range	95
Table 19.	VCAP1/VCAP2 operating conditions	96
Table 20.	Operating conditions at power-up / power-down (regulator ON)	96
Table 21.	Operating conditions at power-up / power-down (regulator OFF)	96
Table 22.	Reset and power control block characteristics	97
Table 23.	Over-drive switching characteristics	98
Table 24.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM, regulator ON	100
Table 25.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled), regulator ON	101
Table 26.	Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch), regulator OFF	102
Table 27.	Typical and maximum current consumption in Sleep mode, regulator ON	103
Table 28.	Typical and maximum current consumption in Sleep mode, regulator OFF	104
Table 29.	Typical and maximum current consumption in Stop mode	105
Table 30.	Typical and maximum current consumption in Standby mode	106
Table 31.	Typical and maximum current consumption in V _{BAT} mode	107
Table 32.	Switching output I/O current consumption	109
Table 33.	Peripheral current consumption	111
Table 34.	Low-power mode wakeup timings	114
Table 35.	High-speed external user clock characteristics	115
Table 36.	Low-speed external user clock characteristics	115
Table 37.	HSE 4-26 MHz oscillator characteristics	117
Table 38.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	118
Table 39.	HSI oscillator characteristics	119
Table 40.	LSI oscillator characteristics	120
Table 41.	Main PLL characteristics	120
Table 42.	PLL12S (audio PLL) characteristics	121
Table 43.	PLLSAI (audio and LCD-TFT PLL) characteristics	122

Table 44.	SSCG parameters constraint	123
Table 45.	MIPI D-PHY characteristics	124
Table 46.	MIPI D-PHY AC characteristics LP mode and HS/LP transitions	126
Table 47.	DSI-PLL characteristics	127
Table 48.	DSI regulator characteristics	128
Table 49.	Flash memory characteristics	129
Table 50.	Flash memory programming	129
Table 51.	Flash memory programming with V_{PP}	130
Table 52.	Flash memory endurance and data retention	131
Table 53.	EMS characteristics	131
Table 54.	EMI characteristics	132
Table 55.	ESD absolute maximum ratings	133
Table 56.	Electrical sensitivities	133
Table 57.	I/O current injection susceptibility	134
Table 58.	I/O static characteristics	134
Table 59.	Output voltage characteristics	137
Table 60.	I/O AC characteristics	138
Table 61.	NRST pin characteristics	140
Table 62.	TIMx characteristics	141
Table 63.	I2C analog filter characteristics	141
Table 64.	SPI dynamic characteristics	142
Table 65.	I ² S dynamic characteristics	146
Table 66.	SAI characteristics	148
Table 67.	USB OTG full speed startup time	150
Table 68.	USB OTG full speed DC electrical characteristics	150
Table 69.	USB OTG full speed electrical characteristics	151
Table 70.	USB HS DC electrical characteristics	151
Table 71.	USB HS clock timing parameters	152
Table 72.	Dynamic characteristics: USB ULPI	153
Table 73.	Dynamics characteristics: Ethernet MAC signals for SMI	154
Table 74.	Dynamics characteristics: Ethernet MAC signals for RMII	155
Table 75.	Dynamics characteristics: Ethernet MAC signals for MII	155
Table 76.	ADC characteristics	156
Table 77.	ADC static accuracy at $f_{ADC} = 18$ MHz	158
Table 78.	ADC static accuracy at $f_{ADC} = 30$ MHz	158
Table 79.	ADC static accuracy at $f_{ADC} = 36$ MHz	158
Table 80.	ADC dynamic accuracy at $f_{ADC} = 18$ MHz - limited test conditions	159
Table 81.	ADC dynamic accuracy at $f_{ADC} = 36$ MHz - limited test conditions	159
Table 82.	Temperature sensor characteristics	162
Table 83.	Temperature sensor calibration values	162
Table 84.	V_{BAT} monitoring characteristics	162
Table 85.	internal reference voltage	162
Table 86.	Internal reference voltage calibration values	163
Table 87.	DAC characteristics	163
Table 88.	Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings	167
Table 89.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings	167
Table 90.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	168
Table 91.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings	169
Table 92.	Asynchronous multiplexed PSRAM/NOR read timings	170
Table 93.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings	170
Table 94.	Asynchronous multiplexed PSRAM/NOR write timings	171
Table 95.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings	172

Table 96.	Synchronous multiplexed NOR/PSRAM read timings	174
Table 97.	Synchronous multiplexed PSRAM write timings	176
Table 98.	Synchronous non-multiplexed NOR/PSRAM read timings	177
Table 99.	Synchronous non-multiplexed PSRAM write timings	178
Table 100.	Switching characteristics for NAND Flash read cycles	181
Table 101.	Switching characteristics for NAND Flash write cycles	181
Table 102.	SDRAM read timings	182
Table 103.	LPSDR SDRAM read timings	183
Table 104.	SDRAM write timings	184
Table 105.	LPSDR SDRAM write timings	184
Table 106.	Quad-SPI characteristics in SDR mode	185
Table 107.	Quad-SPI characteristics in DDR mode	186
Table 108.	DCMI characteristics	187
Table 109.	LTDC characteristics	188
Table 110.	Dynamic characteristics: SD / MMC characteristics, VDD = 2.7 to 3.6 V	190
Table 111.	Dynamic characteristics: SD / MMC characteristics, VDD = 1.71 to 1.9 V	191
Table 112.	RTC characteristics	191
Table 113.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	193
Table 114.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data	196
Table 115.	WLCSP168 - 168-pin, 4.891 x 5.692 mm, 0.4 mm pitch wafer level chip scale package mechanical data	199
Table 116.	UFBGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	200
Table 117.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package mechanical data	202
Table 118.	UFBGA176+25, - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data	206
Table 119.	UFBGA176+25 recommended PCB design rules (0.65 mm pitch BGA)	207
Table 120.	LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package mechanical data	208
Table 121.	TFBGA216 - thin fine pitch ball grid array 13 x 13 x 0.8mm package mechanical data	212
Table 122.	Package thermal characteristics	214
Table 123.	Ordering information scheme	215
Table 124.	Limitations depending on the operating power supply range	216
Table 125.	Document revision history	217

List of figures

Figure 1.	Incompatible board design for LQFP176 package	16
Figure 2.	Incompatible board design for LQFP208 package	17
Figure 3.	UFBGA176 port-to-terminal assignment differences	18
Figure 4.	TFBGA216 port-to-terminal assignment differences.	19
Figure 5.	STM32F479xx block diagram	20
Figure 6.	STM32F479xx Multi-AHB matrix	23
Figure 7.	VDDUSB connected to an external independent power supply	29
Figure 8.	Power supply supervisor interconnection with internal reset OFF	30
Figure 9.	PDR_ON control with internal reset OFF	31
Figure 10.	Regulator OFF	33
Figure 11.	Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1} , V_{CAP_2} stabilization	34
Figure 12.	Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1} , V_{CAP_2} stabilization	35
Figure 13.	STM32F47x LQFP100 pinout	48
Figure 14.	STM32F47x LQFP144 pinout	49
Figure 15.	STM32F47x WLCSP168 pinout	50
Figure 16.	STM32F47x UFBGA169 ballout	51
Figure 17.	STM32F47x UFBGA176 ballout	52
Figure 18.	STM32F47x LQFP176 pinout	53
Figure 19.	STM32F47x LQFP208 pinout	54
Figure 20.	STM32F47x TFBGA216 ballout	55
Figure 21.	Memory map	84
Figure 22.	Pin loading conditions	89
Figure 23.	Pin input voltage	89
Figure 24.	Power supply scheme	90
Figure 25.	Current consumption measurement scheme	91
Figure 26.	External capacitor C_{EXT}	95
Figure 27.	Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in Low drive mode)	107
Figure 28.	Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in High drive mode)	108
Figure 29.	High-speed external clock source AC timing diagram	116
Figure 30.	Low-speed external clock source AC timing diagram	116
Figure 31.	Typical application with an 8 MHz crystal	117
Figure 32.	Typical application with a 32.768 kHz crystal	118
Figure 33.	ACC _{HSI} vs. temperature	119
Figure 34.	ACC _{LSI} versus temperature	120
Figure 35.	PLL output clock waveforms in center spread mode	124
Figure 36.	PLL output clock waveforms in down spread mode	124
Figure 37.	MIPI D-PHY HS/LP clock lane transition timing diagram	127
Figure 38.	MIPI D-PHY HS/LP data lane transition timing diagram	127
Figure 39.	FT I/O input characteristics	136
Figure 40.	I/O AC characteristics definition	139
Figure 41.	Recommended NRST pin protection	140
Figure 42.	SPI timing diagram - slave mode and CPHA = 0	144
Figure 43.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	144
Figure 44.	SPI timing diagram - master mode ⁽¹⁾	145

Figure 45.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	147
Figure 46.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	147
Figure 47.	SAI master timing waveforms	149
Figure 48.	SAI slave timing waveforms	149
Figure 49.	USB OTG full speed timings: definition of data signal rise and fall time	151
Figure 50.	ULPI timing diagram	152
Figure 51.	Ethernet SMI timing diagram	153
Figure 52.	Ethernet RMII timing diagram	154
Figure 53.	Ethernet MII timing diagram	155
Figure 54.	ADC accuracy characteristics	160
Figure 55.	Typical connection diagram using the ADC	160
Figure 56.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	161
Figure 57.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	161
Figure 58.	12-bit buffered/non-buffered DAC	165
Figure 59.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	166
Figure 60.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	168
Figure 61.	Asynchronous multiplexed PSRAM/NOR read waveforms	169
Figure 62.	Asynchronous multiplexed PSRAM/NOR write waveforms	171
Figure 63.	Synchronous multiplexed NOR/PSRAM read timings	173
Figure 64.	Synchronous multiplexed PSRAM write timings	175
Figure 65.	Synchronous non-multiplexed NOR/PSRAM read timings	177
Figure 66.	Synchronous non-multiplexed PSRAM write timings	178
Figure 67.	NAND controller waveforms for read access	179
Figure 68.	NAND controller waveforms for write access	180
Figure 69.	NAND controller waveforms for common memory read access	180
Figure 70.	NAND controller waveforms for common memory write access	181
Figure 71.	SDRAM read access waveforms (CL = 1)	182
Figure 72.	SDRAM write access waveforms	183
Figure 73.	Quad-SPI SDR timing diagram	185
Figure 74.	Quad-SPI DDR timing diagram	186
Figure 75.	DCMI timing diagram	187
Figure 76.	LCD-TFT horizontal timing diagram	188
Figure 77.	LCD-TFT vertical timing diagram	189
Figure 78.	SDIO high-speed mode	189
Figure 79.	SD default mode	190
Figure 80.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	192
Figure 81.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	194
Figure 82.	LQFP100 marking example (package top view)	194
Figure 83.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline	195
Figure 84.	LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package recommended footprint	197
Figure 85.	LQFP144 marking example (package top view)	197
Figure 86.	WLCSP168 - 168-pin, 4.891 x 5.692 mm, 0.4 mm pitch wafer level chip scale package outline	198
Figure 87.	UFBGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	200
Figure 88.	UFBGA169 marking example (package top view)	201
Figure 89.	LQFP176, 24 x 24 mm, 176-pin low-profile quad flat package outline	202
Figure 90.	LQFP176 recommended footprint	204
Figure 91.	LQFP176 marking example (package top view)	205
Figure 92.	UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch,	

	ultra fine pitch ball grid array package outline	206
Figure 93.	UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint	207
Figure 94.	LQFP208, 28 x 28 mm, 208-pin low-profile quad flat package outline	208
Figure 95.	LQFP208 recommended footprint	210
Figure 96.	LQFP208 marking example (package top view)	211
Figure 97.	TFBGA216 - thin fine pitch ball grid array 13 x 13 x 0.8mm, package outline	212
Figure 98.	TFBGA216 marking example (package top view)	213

1 Description

The STM32F479xx devices are based on the high-performance Arm^{®(a)} Cortex[®]-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex[®]-M4 core features a Floating point unit (FPU) single precision which supports all Arm[®] single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F479xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbytes, up to 384 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers, a true random number generator (RNG), and a cryptographic acceleration cell. They also feature standard and advanced communication interfaces:

- Up to three I²Cs
- Six SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
- Two CANs
- One SAI serial audio interface
- An SDMMC host interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™
- DSI Host.

Advanced peripherals include an SDMMC interface, a flexible memory control (FMC) interface, a Quad-SPI Flash memory, camera interface for CMOS sensors and a cryptographic acceleration cell. Refer to [Table 2](#) for the list of peripherals available on each part number.

The STM32F479xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply. A dedicated supply input for USB (OTG_FS and OTG_HS) only in full speed mode, is available on all packages.

The supply voltage can drop to 1.7 V (refer to [Section 2.19.2](#)). A comprehensive set of power-saving mode allows the design of low-power applications.



a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The STM32F479xx devices are offered in eight packages, ranging from 100 to 216 pins. The set of included peripherals changes with the device chosen, according to [Table 2](#).

These features make the STM32F479xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances

[Figure 5](#) shows the general block diagram of the device family.

Table 2. STM32F479xx features and peripheral counts

Peripherals	STM32F479Vx		STM32F479Zx		STM32F479Ax		STM32F479Ix		STM32F479Bx		STM32F479Nx	
	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048
Flash memory in Kbytes	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048	1024	2048
SRAM in Kbytes	System											
	Backup											
FMC memory controller	384(160+32+128+64)											
Quad-SPI	4											
Ethernet	No						Yes					
Timers	General-purpose											
	Advanced-control											
	Basic											
Random number generator	10											
Communication interfaces	Yes											
	SPI / I ² S				4/2(full duplex) ⁽¹⁾				6/2(full duplex) ⁽¹⁾			
	I ² C											
	USART/UART						4/3					
	USB OTG FS											
	USB OTG HS											
	CAN											
	SAI											
SDIO	2											
Camera interface	1											
	Yes											

Table 2. STM32F479xx features and peripheral counts (continued)

Peripherals	STM32F479Vx	STM32F479Zx	STM32F479Ax	STM32F479Ix	STM32F479Bx	STM32F479Nx
MIPI-DSI Host	Yes					
LCD-TFT	Yes					
Chrom-ART Accelerator™ (DMA2D)	Yes					
Cryptography	Yes					
GPIOs	71	131	114	131	161	161
12-bit ADC Number of channels	3					
	14	20	24			
12-bit DAC Number of channels	Yes 2					
Maximum CPU frequency	180 MHz					
Operating voltage	1.7 to 3.6V ⁽²⁾					
Operating temperatures	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C Junction temperature: -40 to 105 °C / -40 to 125 °C					
Package	LQFP100	LQFP144	UFBGA169 WLCSP168	LQFP176 UFBGA176	LQFP208	TFBGA216

1. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. VDD/VDDA minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.19.2](#)).

1.1 Compatibility throughout the family

STM32F479xx devices are not compatible with other STM32F4xx devices.

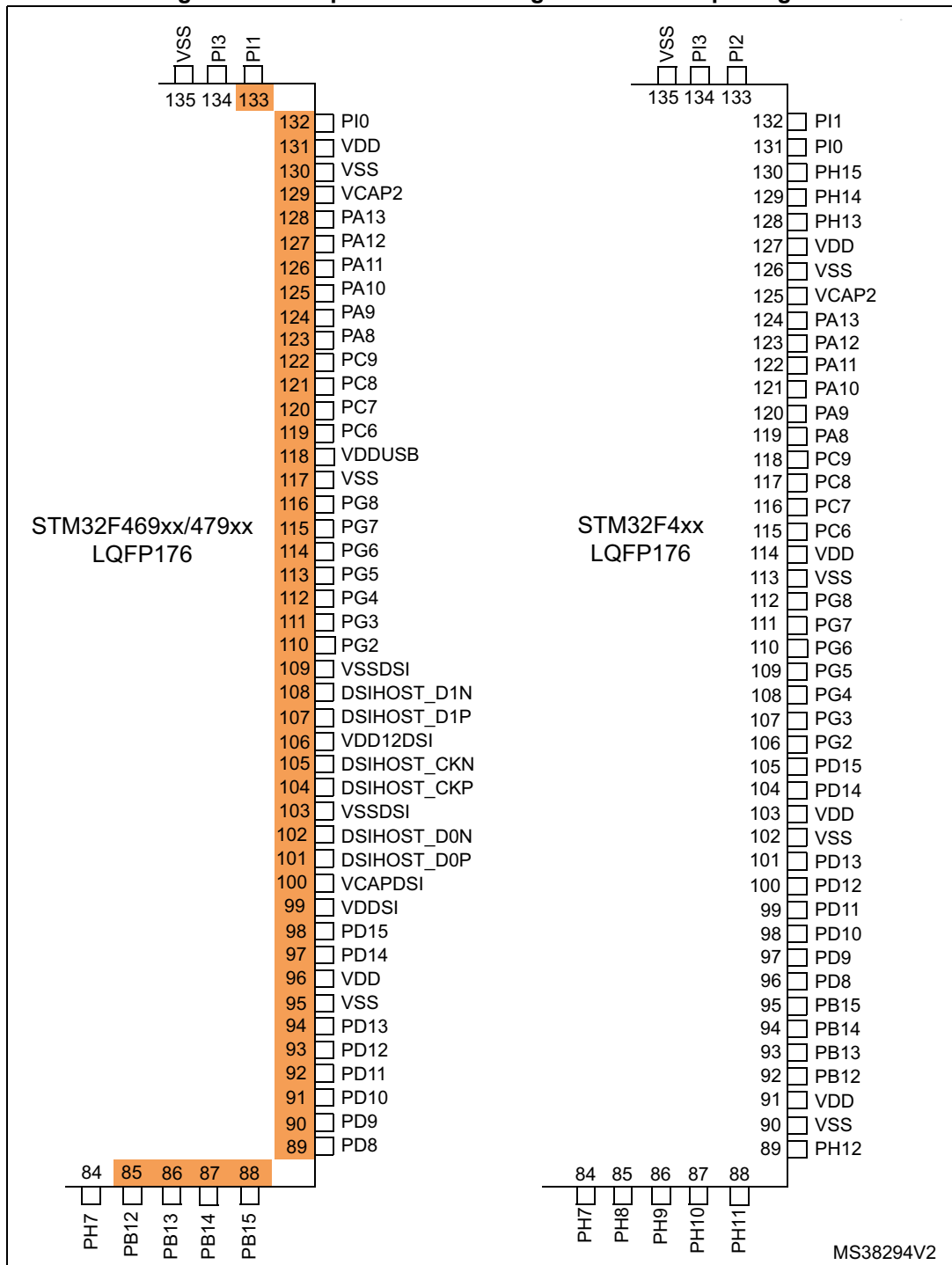
[Figure 1](#) and [Figure 2](#) show incompatible board designs, respectively, for LQFP176 and LQFP208 packages (highlighted pins).

The UFBGA176 and TFBGA216 ballouts are compatible with other STM32F4xx devices, only few IO port pins are substituted, as shown in [Figure 3](#) and [Figure 4](#).

The LQFP100, LQFP144 and UFBGA169 packages are incompatible with other STM32F4xx devices.

1.1.1 LQFP176 package

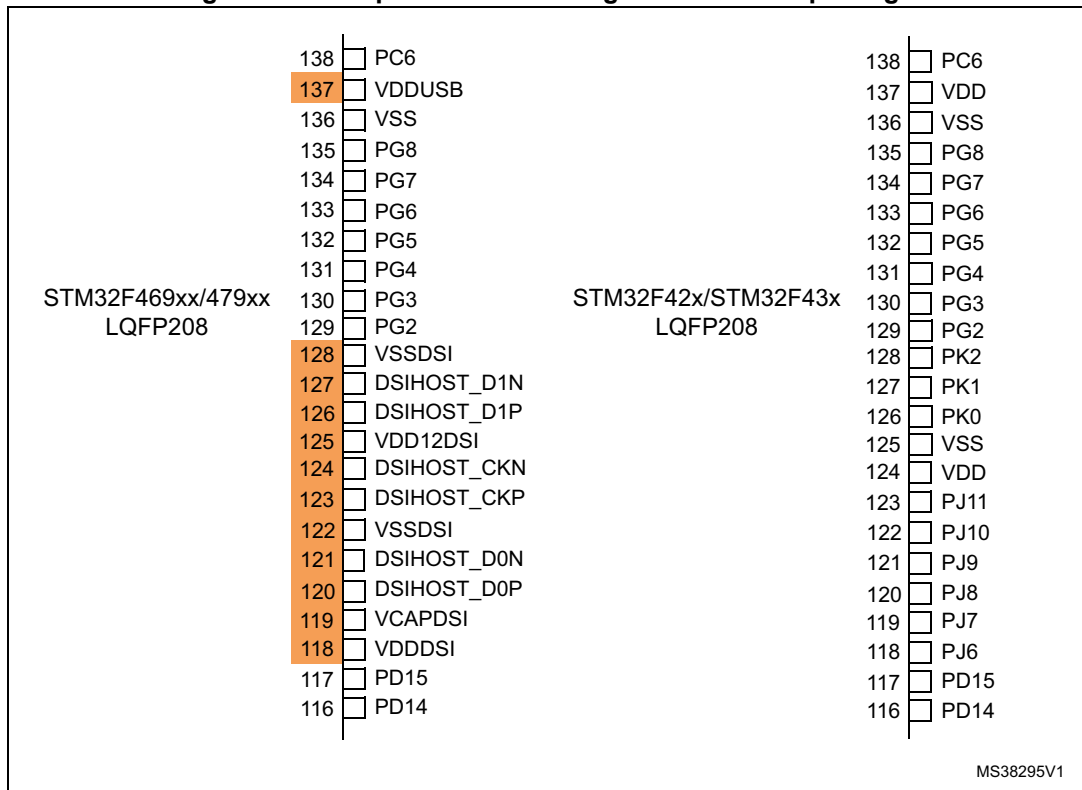
Figure 1. Incompatible board design for LQFP176 package



1. Pins from 85 to 133 are not compatible.

1.1.2 LQFP208 package

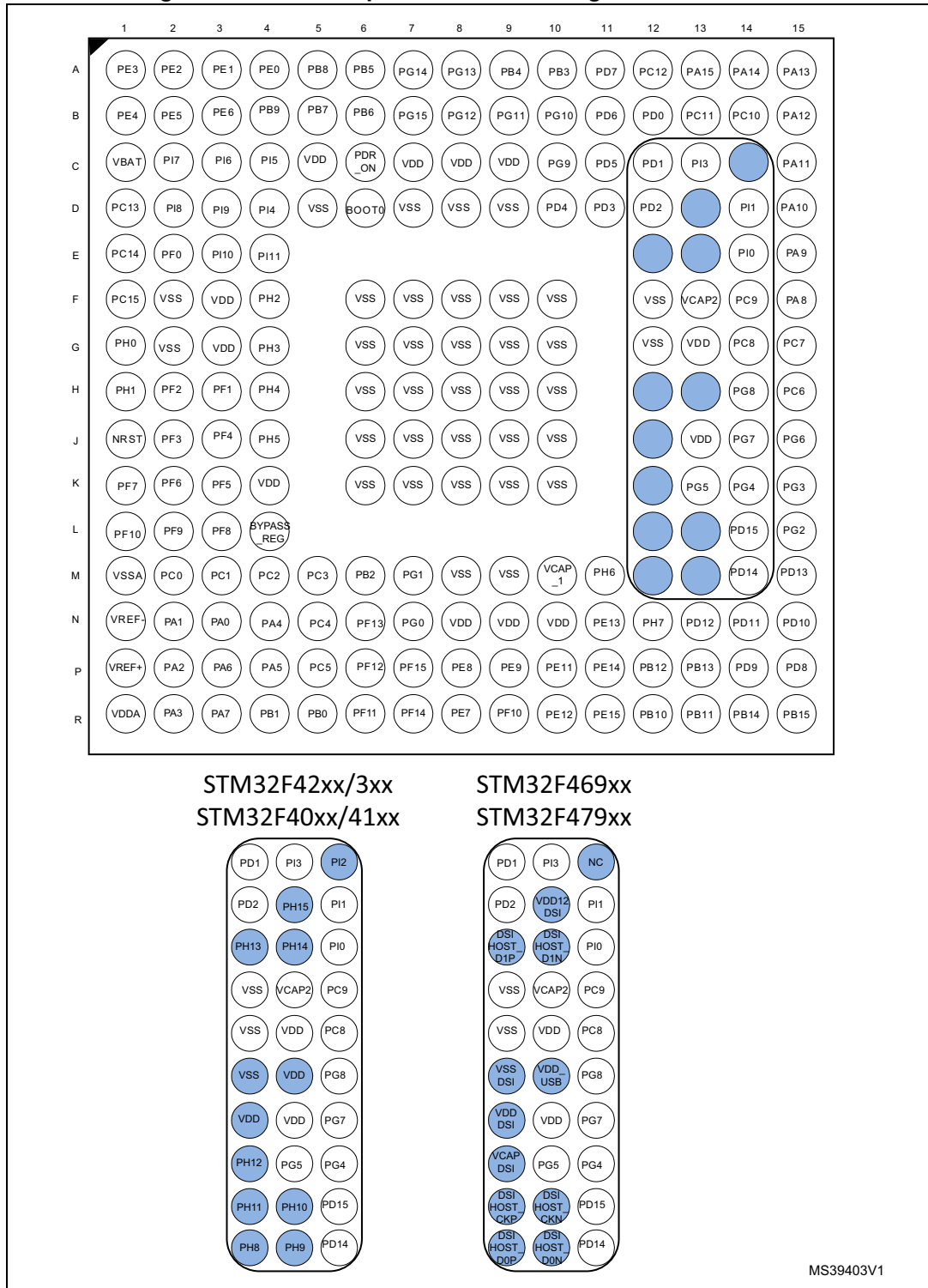
Figure 2. Incompatible board design for LQFP208 package



1. Pins from 118 to 128 and pin 137 are not compatible

1.1.3 UFBGA176 package

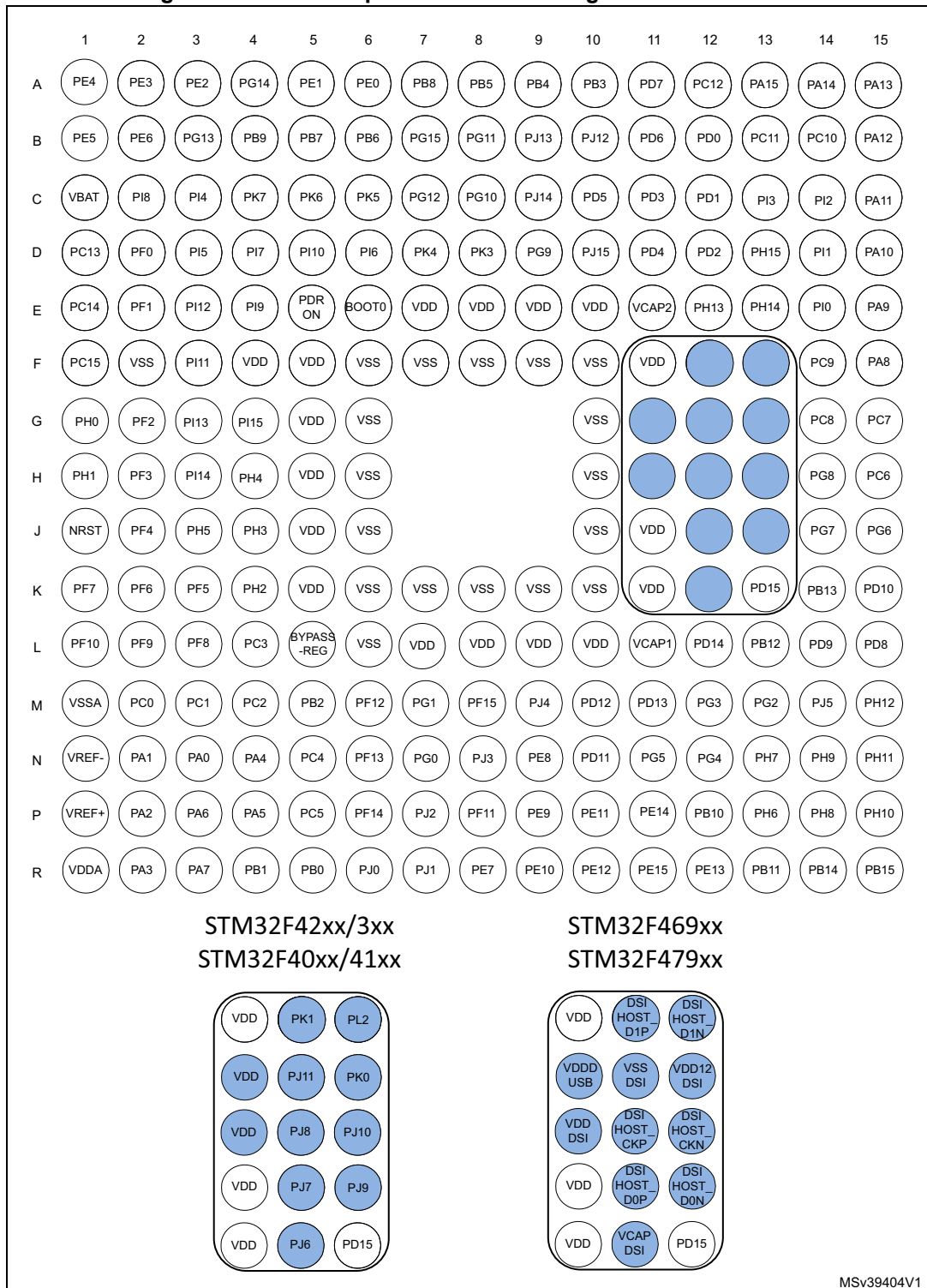
Figure 3. UFBGA176 port-to-terminal assignment differences



1. The highlighted pins are substituted with dedicated DSI IO pins on STM32F469xx/479xx devices.

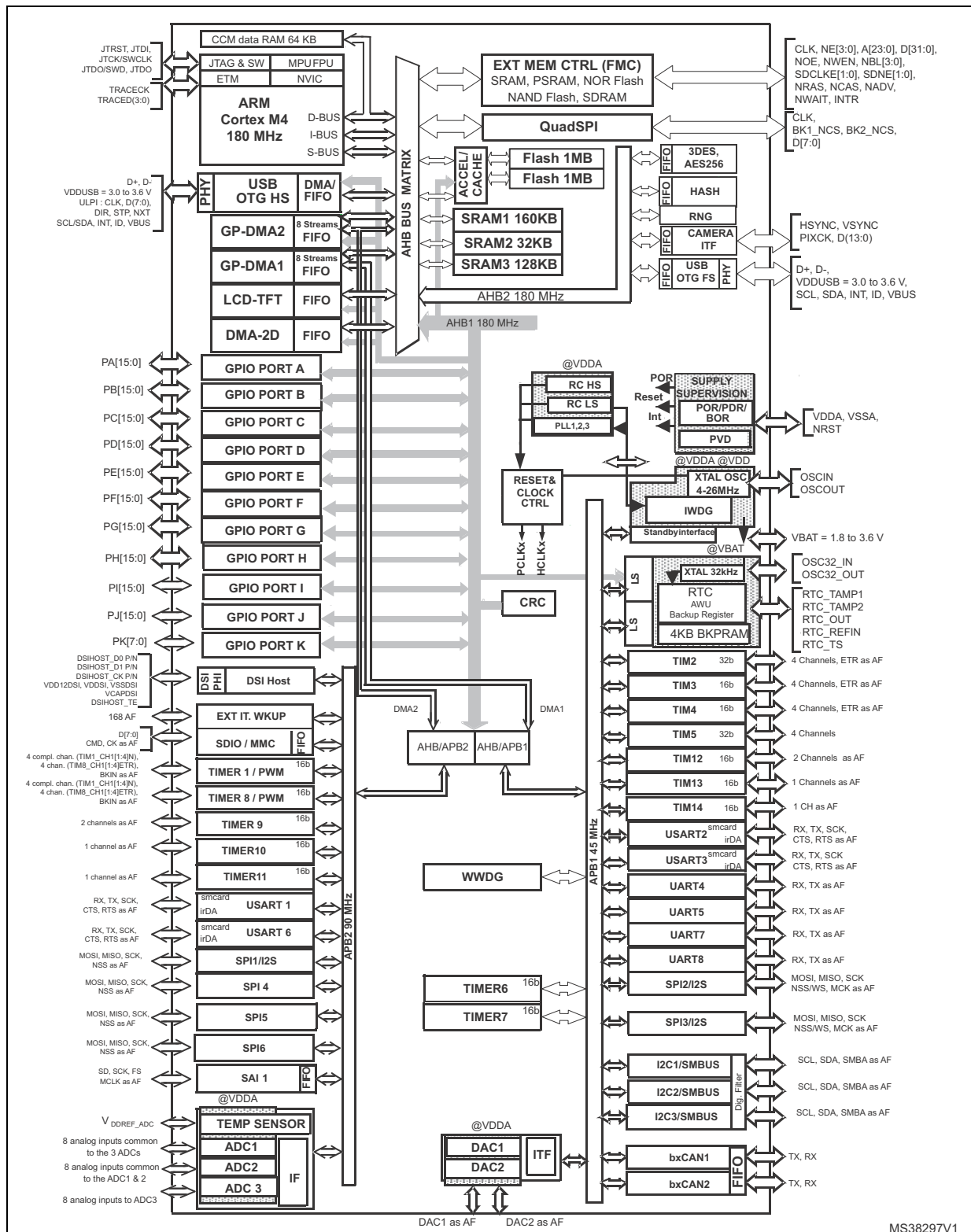
1.1.4 TFBGA216 package

Figure 4. TFBGA216 port-to-terminal assignment differences



1. The highlighted pins are substituted with dedicated DSI IO pins on STM32F469xx/479xx devices.

Figure 5. STM32F479xx block diagram



- The timers connected to APB2 are clocked from TIMxCLK up to 180 MHz, while the timers connected to APB1 are clocked from TIMxCLK either up to 90 MHz or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2 Functional overview

2.1 Arm[®] Cortex[®]-M4 with FPU and embedded Flash and SRAM

The Arm[®] Cortex[®]-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm[®] Cortex[®]-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F47x line is compatible with all Arm tools and software.

Figure 5 shows the general block diagram of the STM32F47x line.

Note: Cortex[®]-M4 with FPU core is binary compatible with the Cortex[®]-M3 core.

2.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator optimized for STM32 industry-standard Arm[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the Arm[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally require the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark[®] benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

2.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

2.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.6 Embedded SRAM

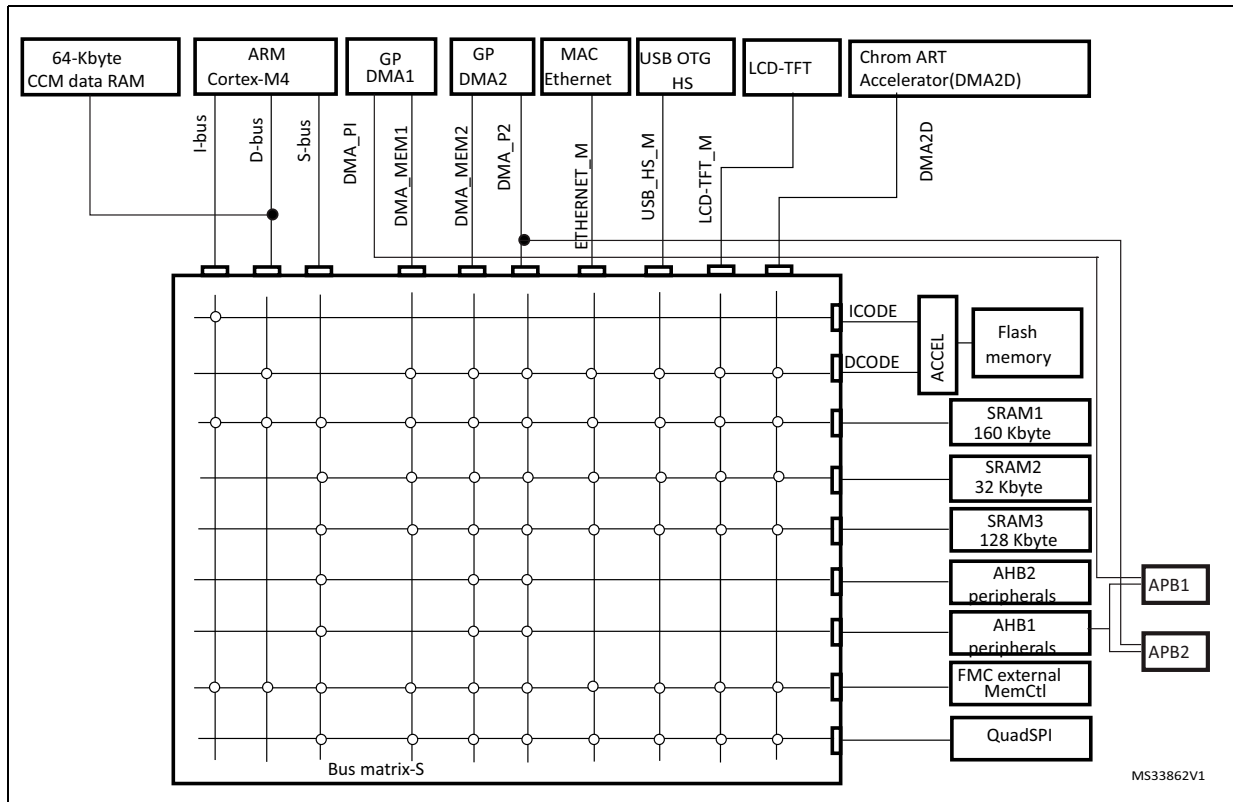
All devices embed:

- Up to 384Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

2.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 6. STM32F479xx Multi-AHB matrix



2.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1
- QUADSPI.

2.9 Flexible Memory Controller (FMC)

The Flexible memory controller (FMC) includes three memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller
- The Synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) controller

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
 - Static random access memory (SRAM)
 - NOR Flash memory/OneNAND Flash memory
 - PSRAM
 - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPDDR SDRAM) memories
- 8-, 16-, 32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

2.10 Quad-SPI memory interface (QUADSPI)

All STM32F479xx devices embeds a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual, Quad or Dual-flash SPI memories. It can work in direct mode through registers, external flash status register polling mode and memory mapped mode. Up to 256 Mbytes external Flash memory are mapped, supporting 8, 16 and 32-bit access. Code execution is supported.

The opcode and the frame format are fully programmable. Communication can be either in Single Data Rate or Dual Data Rate.

2.11 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

2.12 DSI Host (DSIHOST)

The DSI Host is a dedicated peripheral for interfacing with MIPI[®] DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC and a generic APB interface that can be used to transmit information to the display.

These interfaces are as follows:

- LTDC interface:
 - Used to transmit information in Video Mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).
 - Through a customized for mode, this interface can be used to transmit information in full bandwidth in the Adapted Command Mode (DBI).
- APB slave interface:
 - Allows the transmission of generic information in Command mode, and follows a proprietary register interface.
 - Can operate concurrently with either LTDC interface in either Video Mode or Adapted Command Mode.
- Video mode pattern generator:
 - Allows the transmission of horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

The DSI Host main features:

- Compliant with MIPI[®] Alliance standards
- Interface with MIPI[®] D-PHY
- Supports all commands defined in the MIPI[®] Alliance specification for DCS:
 - Transmission of all Command mode packets through the APB interface
 - Transmission of commands in low-power and high-speed during Video Mode
- Supports up to two D-PHY data lanes
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes
- 3D transmission support
- Configurable selection of system interfaces:
 - AMBA APB for control and optional support for Generic and DCS commands
 - Video Mode interface through LTDC
 - Adapted Command Mode interface through LTDC
- Independently programmable Virtual Channel ID in
 - Video Mode
 - Adapted Command Mode
 - APB Slave

Video Mode interfaces features

- LTDC interface color coding mappings into 24-bit interface:
 - 16-bit RGB, configurations 1, 2, and 3
 - 18-bit RGB, configurations 1 and 2
 - 24-bit RGB
- Programmable polarity of all LTDC interface signals
- Maximum resolution is limited by available DSI physical link bandwidth:
 - Number of lanes: 2
 - Maximum speed per lane: 500Mbps

Adapted interface features

- Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
- LTDC interface color coding mappings into 24-bit interface:
 - 16-bit RGB, configurations 1, 2, and 3
 - 18-bit RGB, configurations 1 and 2
 - 24-bit RGB

Video mode pattern generator

- Vertical and horizontal color bar generation without LTDC stimuli
- BER pattern without LTDC stimuli

2.13 Chrom-Art Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

2.14 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 93 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.15 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 159 GPIOs can be connected to the 16 external interrupt lines.

2.16 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 180 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 180 MHz while the maximum frequency of the high-speed APB domains is 90 MHz. The maximum allowed frequency of the low-speed APB domain is 45 MHz.

The devices embed a dedicated PLL (PLL12S) and PLLSAI which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

2.17 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory through a serial interface. Refer to application note AN2606 for details.

2.18 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.

Note: V_{DD}/V_{DDA} minimum value of 1.7 V is obtained when the internal reset is OFF (refer to [Section 2.19.2](#)). Refer to [Table 3](#) to identify the packages supporting this option.

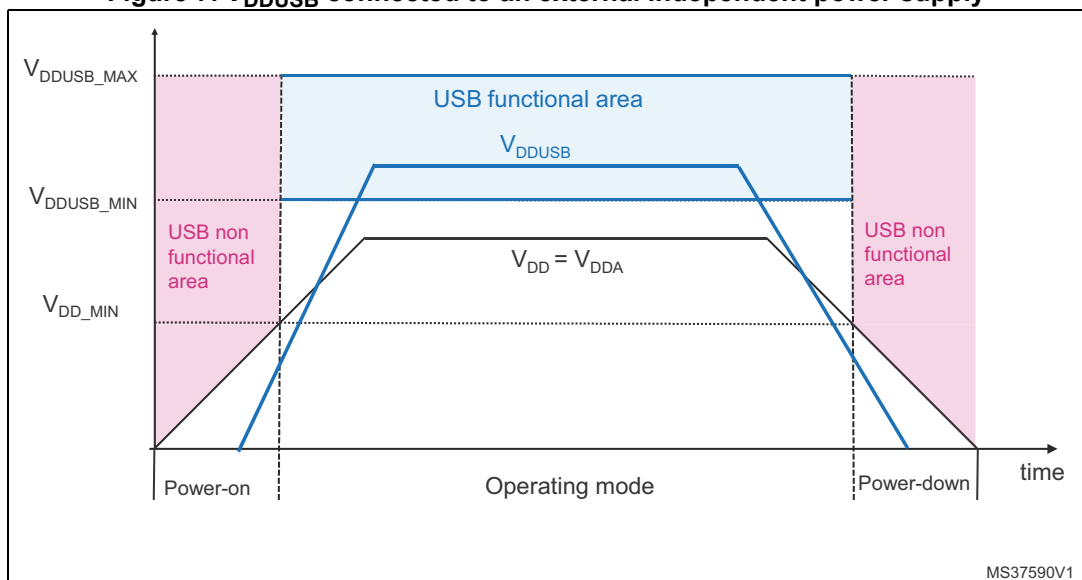
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDUSB} can be connected either to V_{DD} or an external independent power supply (3.0 to 3.6 V) for USB transceivers.

For example, when device is powered at 1.8V, an independent power supply 3.3 V can be connected to V_{DDUSB} . When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA} but it must be the last supply to be provided and the first to disappear.

The following conditions must be respected:

- During power-on phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- During power-down phase ($V_{DD} < V_{DD_MIN}$), V_{DDUSB} should be always lower than V_{DD}
- V_{DDUSB} rising and falling time rate specifications must be respected.
- In operating mode phase, V_{DDUSB} could be lower or higher than V_{DD} :
 - If USB (USB OTG_HS/OTG_FS) is used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DDUSB_MIN} and V_{DDUSB_MAX} . The V_{DDUSB} supplies both USB transceivers (USB OTG_HS and USB OTG_FS).
 - If only one USB transceiver is used in the application, the GPIOs associated to the other USB transceiver are still supplied by V_{DDUSB} .
 - If USB (USB OTG_HS/OTG_FS) is not used, the associated GPIOs powered by V_{DDUSB} are operating between V_{DD_MIN} and V_{DD_MAX} .
 - If USB (USB OTG_HS/OTG_FS) is not used and the associated GPIOs powered by V_{DDUSB} are not used, then V_{DDUSB} should be tied to V_{SS} or V_{DD} (V_{DDUSB} must not be floating).

Figure 7. V_{DDUSB} connected to an external independent power supply



The DSI (Display Serial Interface) sub-system uses several power supply pins that are independent from the other supply pins:

- VDDDSI is an independent DSI power supply dedicated for DSI Regulator and MIPI D-PHY. This supply must be connected to global VDD.
- VCAPDSI pin is the output of DSI Regulator (1.2 V), which must be connected externally to VDD12DSI.
- VDD12DSI pin is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 μF must be connected on VDD12DSI pin.
- VSSDSI pin is an isolated supply ground used for DSI sub-system.
- If DSI functionality is not used at all, then:
 - VDDDSI pin must be connected to global VDD.

- VCAPDSI pin must be connected externally to VDD12DSI but the external capacitor is no more needed.
- VSSDSI pin must be grounded.

2.19 Power supply supervisor

2.19.1 Internal reset ON

On packages embedding the PDR_ON pin, the power supply supervisor is enabled by holding PDR_ON high. On other packages the power supply supervisor is always enabled.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR/PDR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default BOR thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR} , without the need for an external reset circuit.

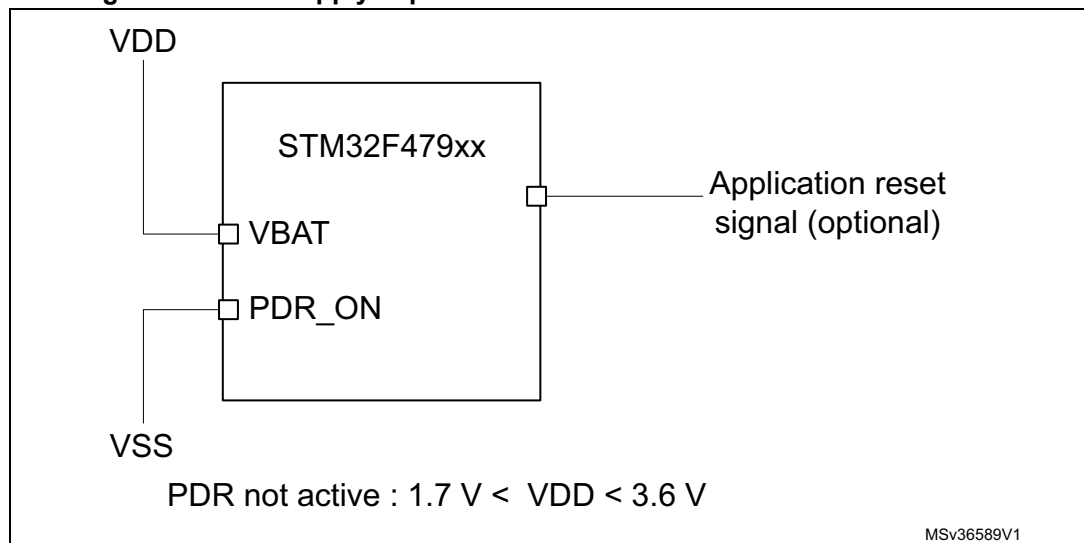
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.19.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and NRST and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON must be connected to VSS, as shown in [Figure 8](#).

Figure 8. Power supply supervisor interconnection with internal reset OFF



The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see [Figure 9](#)).

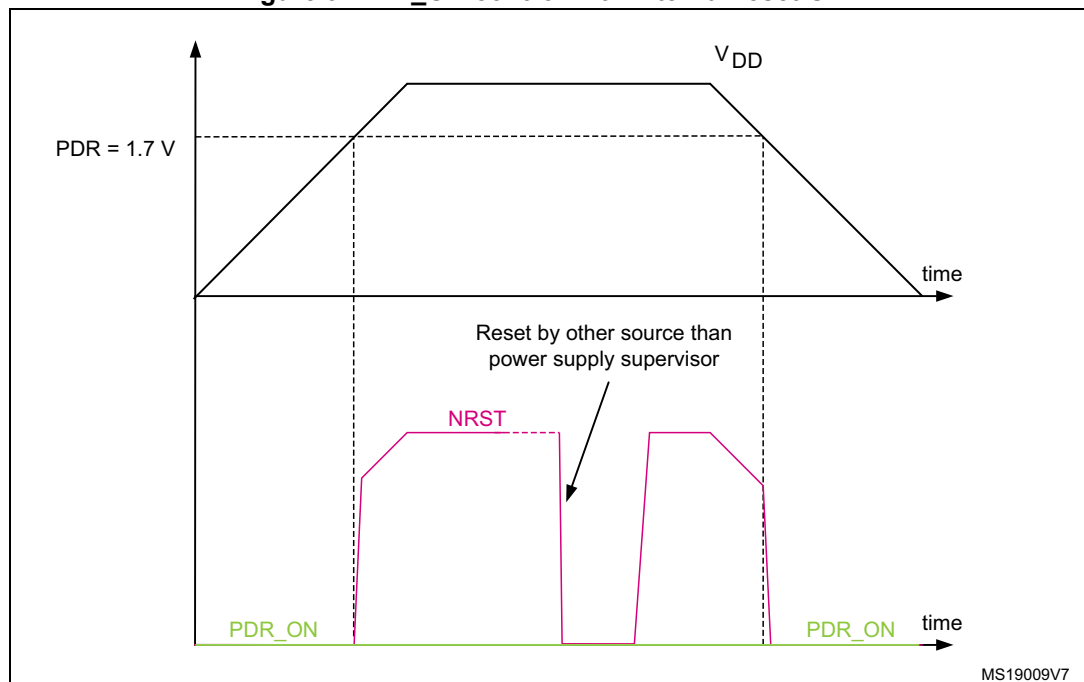
A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .

All packages allow to disable the internal reset through the PDR_ON signal when connected to V_{SS} .

Figure 9. PDR_ON control with internal reset OFF



1. PDR_ON signal to be kept always low.

2.20 Voltage regulator

The regulator has four operating modes:

- Regulator ON
 - Main regulator mode (MR)
 - Low power regulator (LPR)
 - Power-down
- Regulator OFF

2.20.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR mode used in Run/sleep modes or in Stop modes
 - In Run/Sleep mode

The MR mode is used either in the normal mode (default mode) or the over-drive mode (enabled by software). Different voltages scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption. The over-drive mode allows operating at a higher frequency than the normal mode for a given voltage scaling.
 - In Stop modes

The MR can be configured in two ways during stop mode:
MR operates in normal mode (default mode of MR in stop mode)
MR operates in under-drive mode (reduced leakage mode).
- LPR is used in the Stop modes:

The LP regulator mode is configured by software when entering Stop mode. Like the MR mode, the LPR can be configured in two ways during stop mode:

 - LPR operates in normal mode (default mode when LPR is ON)
 - LPR operates in under-drive mode (reduced leakage mode).
- Power-down is used in Standby mode.

The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Refer to [Table 3](#) for a summary of voltage regulator modes versus device operating modes.

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin. Refer to [Section 2.18](#) and [Table 124](#).

All packages have the regulator ON feature.

Table 3. Voltage regulator configuration mode versus device operating mode⁽¹⁾

Voltage regulator configuration	Run mode	Sleep mode	Stop mode	Standby mode
Normal mode	MR	MR	MR or LPR	-
Over-drive mode ⁽²⁾	MR	MR	-	-
Under-drive mode	-	-	MR or LPR	-
Power-down mode	-	-	-	Yes

1. '-' means that the corresponding configuration is not available.
2. The over-drive mode is not available when V_{DD} = 1.7 to 2.1 V.

2.20.2 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V_{12} voltage source through V_{CAP_1} and V_{CAP_2} pins.

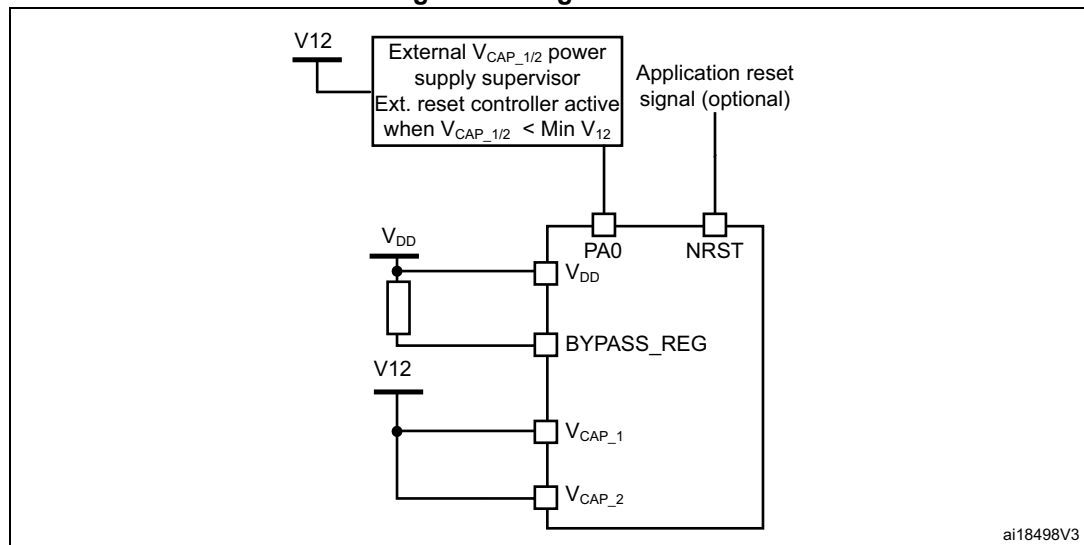
Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to [Operating conditions](#). The two 2.2 μF ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to [Section 2.18](#).

When the regulator is OFF, there is no more internal monitoring on V_{12} . An external power supply supervisor should be used to monitor the V_{12} of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V_{12} power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V_{12} logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

Figure 10. Regulator OFF

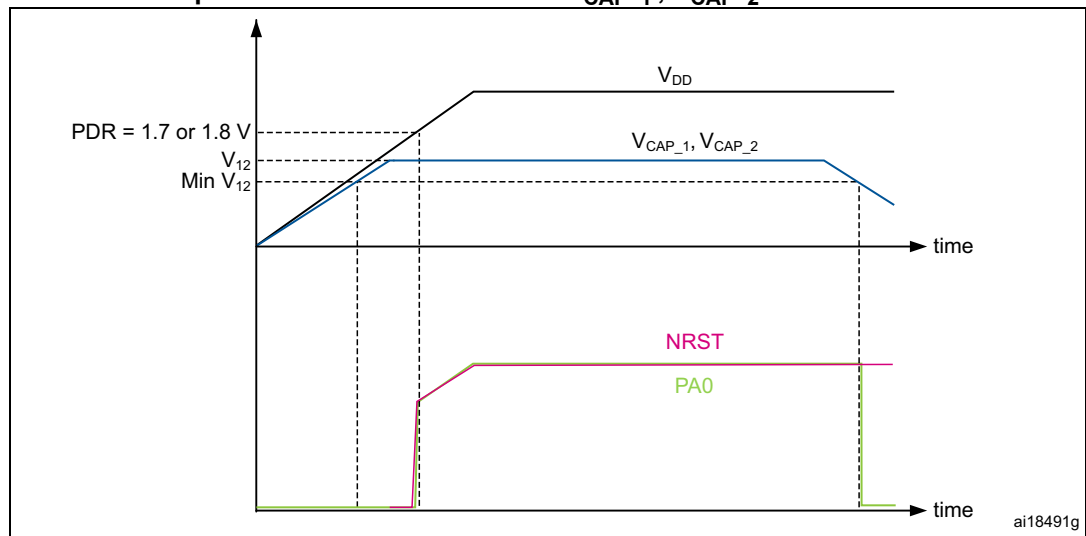


The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see [Figure 11](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 12](#)).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

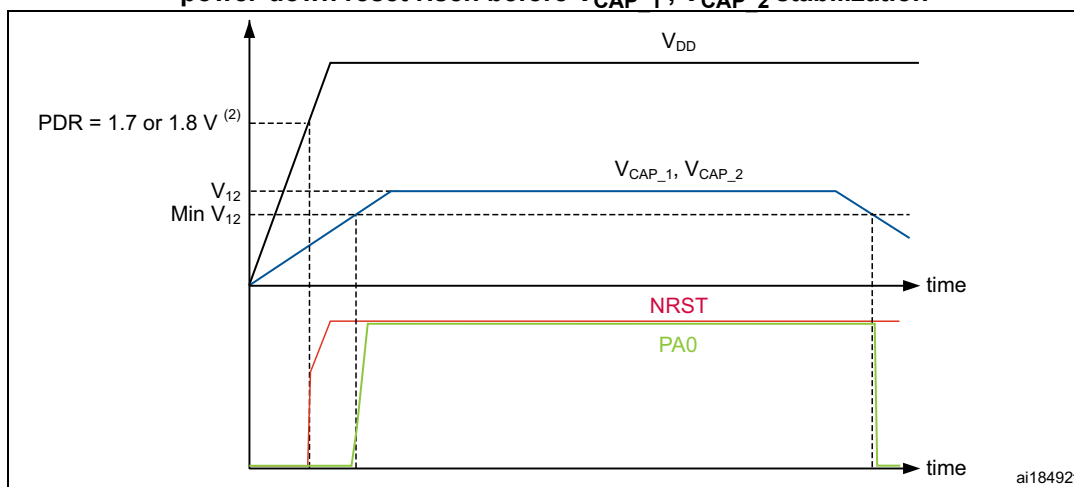
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application (see [Operating conditions](#)).

Figure 11. Startup in regulator OFF: slow V_{DD} slope - power-down reset risen after V_{CAP_1} , V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

Figure 12. Startup in regulator OFF mode: fast V_{DD} slope - power-down reset risen before V_{CAP_1} , V_{CAP_2} stabilization



1. This figure is valid whatever the internal reset mode (ON or OFF).

2.20.3 Regulator ON/OFF and internal reset ON/OFF availability

Table 4. Regulator ON/OFF and internal reset ON/OFF availability

Package	Regulator ON	Regulator OFF	Internal reset ON	Internal reset OFF
WLCSP168 UFBGA169 LQFP208	Yes	No	Yes PDR_ON set to V_{DD}	Yes PDR_ON set to V_{SS}
LQFP176 UFBGA176 TFBGA216	Yes BYPASS_REG set to V_{SS}	Yes BYPASS_REG set to V_{DD}		

2.21 Real-time clock (RTC), backup SRAM and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 4 Kbytes of backup SRAM
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The 4-Kbyte backup SRAM is an EEPROM-like memory area. It can be used to store data which need to be retained in VBAT and standby mode. This memory area is disabled by default to minimize power consumption (see [Section 2.22](#)). It can be enabled by software.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see [Section 2.22](#)).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

Like backup SRAM, the RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

2.22 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

The voltage regulator can be put either in main regulator mode (MR) or in low-power mode (LPR). Both modes can be configured as follows (see [Table 5](#)):

- Normal mode (default mode when MR or LPR is enabled)
- Under-drive mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm / wakeup / tamper / time stamp events, the USB OTG FS/HS wakeup or the Ethernet wakeup).

Table 5. Voltage regulator modes in stop mode

Voltage regulator configuration	Main regulator (MR)	Low-power regulator (LPR)
Normal mode	MR ON	LPR ON
Under-drive mode	MR in under-drive mode	LPR in under-drive mode

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The

PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain and the backup SRAM when selected.

The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm / wakeup / tamper /time stamp event occurs.

The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

2.23 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT} , external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD} .

2.24 Timers and watchdogs

The devices include two advanced-control timers, eight general-purpose timers, two basic timers and two watchdog timers.

All timer counters can be frozen in debug mode.

[Table 6](#) compares the features of the advanced-control, general-purpose and basic timers.

Table 6. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz) ⁽¹⁾
Advanced control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	90	180
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	45	90/180
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	90	180
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	90	180
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	45	90/180
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	45	90/180
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	45	90/180

1. The maximum timer clock is either 90 or 180 MHz depending on TIMPRE bit configuration in the RCC_DCKCFGR register.

2.24.1 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.24.2 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32F47x devices (see [Table 6](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

The STM32F47x include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10, TIM11, TIM12, TIM13, and TIM14**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, and TIM14 feature one independent channel, whereas TIM9 and TIM12 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

2.24.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

2.24.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

2.24.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.24.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

2.25 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 KHz), and fast (up to 400 KHz) modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see [Table 7](#)).

Table 7. Comparison of I2C analog and digital filters

Filter	Analog	Digital
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

2.26 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed four universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These six interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 11.25 Mbit/s. The other available interfaces communicate at up to 5.62 bit/s.

USART1, USART2, USART3 and USART6 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 8. USART feature comparison⁽¹⁾

Name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s		APB mapping
							Oversampling by 16	Oversampling by 8	
USART1	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
USART2	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
USART3	X	X	X	X	X	X	2.81	5.62	APB1 (max. 45 MHz)
UART4	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART5	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
USART6	X	X	X	X	X	X	5.62	11.25	APB2 (max. 90 MHz)
UART7	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)
UART8	X	-	X	-	X	-	2.81	5.62	APB1 (max. 45 MHz)

1. X = feature supported.

2.27 Serial peripheral interface (SPI)

The devices feature up to six SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1, SPI4, SPI5, and SPI6 can communicate at up to 45 Mbits/s, SPI2 and SPI3 can communicate at up to 22.5 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

2.28 Inter-integrated sound (I²S)

Two standard I²S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel.

Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I²S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I2Sx can be served by the DMA controller.

Note: For I2S2 full-duplex mode, I2S2_CK and I2S2_WS signals can be used only on GPIO Port B and GPIO Port D.

2.29 Serial Audio interface (SAI1)

The serial audio interface (SAI1) is based on two independent audio sub-blocks which can operate as transmitter or receiver with their FIFO. Many audio protocols are supported by each block: I2S standards, LSB or MSB-justified, PCM/DSP, TDM, AC'97 and SPDIF output, supporting audio sampling frequencies from 8 kHz up to 192 kHz. Both sub-blocks can be configured in master or in slave mode.

In master mode, the master clock can be output to the external DAC/CODEC at 256 times of the sampling frequency.

The two sub-blocks can be configured in synchronous mode when full-duplex mode is required.

SAI1 can be served by the DMA controller.

2.30 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I²S and SAI applications. It allows to achieve error-free I²S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

The PLLI2S configuration can be modified to manage an I²S/SAI sample rate change without disabling the main PLL (PLL) used for CPU, USB and Ethernet interfaces.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I²S/SAI flow with an external PLL (or Codec output).

2.31 Audio and LCD PLL(PLLSAI)

An additional PLL dedicated to audio and LCD-TFT is used for SAI1 peripheral in case the PLLI2S is programmed to achieve another audio sampling frequency (49.152 MHz or 11.2896 MHz) and the audio application requires both sampling frequencies simultaneously.

The PLLSAI is also used to generate the LCD-TFT clock.

2.32 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.33 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F4xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.34 Controller area network (bxCAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

2.35 Universal serial bus on-the-go full-speed (OTG_FS)

The device embeds an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 1.28 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- HNP/SNP/IP inside (no need for any external resistor)

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.36 Universal serial bus on-the-go high-speed (OTG_HS)

The device embeds a USB OTG high-speed (up to 480 Mb/s) device/host/OTG peripheral. The USB OTG HS supports both full-speed and high-speed operations. It integrates the transceivers for full-speed operation (12 MB/s) and features a UTMI low-pin interface (ULPI) for high-speed operation (480 MB/s). When using the USB OTG HS in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripheral is compliant with the USB 2.0 specification and with the OTG 2.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The major features are:

- Combined Rx and Tx FIFO size of 4 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode. The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.37 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can sustain a data transfer rate up to 54 Mbyte/s at 54 MHz. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image black & white.

2.38 Cryptographic accelerator

The devices embed a cryptographic accelerator. This cryptographic accelerator provides a set of hardware acceleration for the advanced cryptographic algorithms usually needed to provide confidentiality, authentication, data integrity and non repudiation when exchanging messages with a peer.

- These algorithms consists of:

Encryption/Decryption

- DES/TDES (data encryption standard/triple data encryption standard): ECB (electronic codebook) and CBC (cipher block chaining) chaining algorithms, 64-, 128- or 192-bit key
- AES (advanced encryption standard): ECB, CBC, GCM, CCM, and CTR (counter mode) chaining algorithms, 128, 192 or 256-bit key

Universal hash

- SHA-1 and SHA-2 (secure hash algorithms)
- MD5
- HMAC

The cryptographic accelerator supports DMA request generation.

2.39 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.40 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 90 MHz.

2.41 Analog-to-digital converters (ADCs)

Three 12-bit analog-to-digital converters are embedded and each ADC shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM5, or TIM8 timer.

2.42 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the same input channel as V_{BAT} , ADC1_IN18, which is used to convert the sensor output voltage into a digital value. When the temperature sensor and V_{BAT} conversion are enabled at the same time, only V_{BAT} conversion is performed.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

2.43 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 10-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the device. The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.44 Serial wire JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

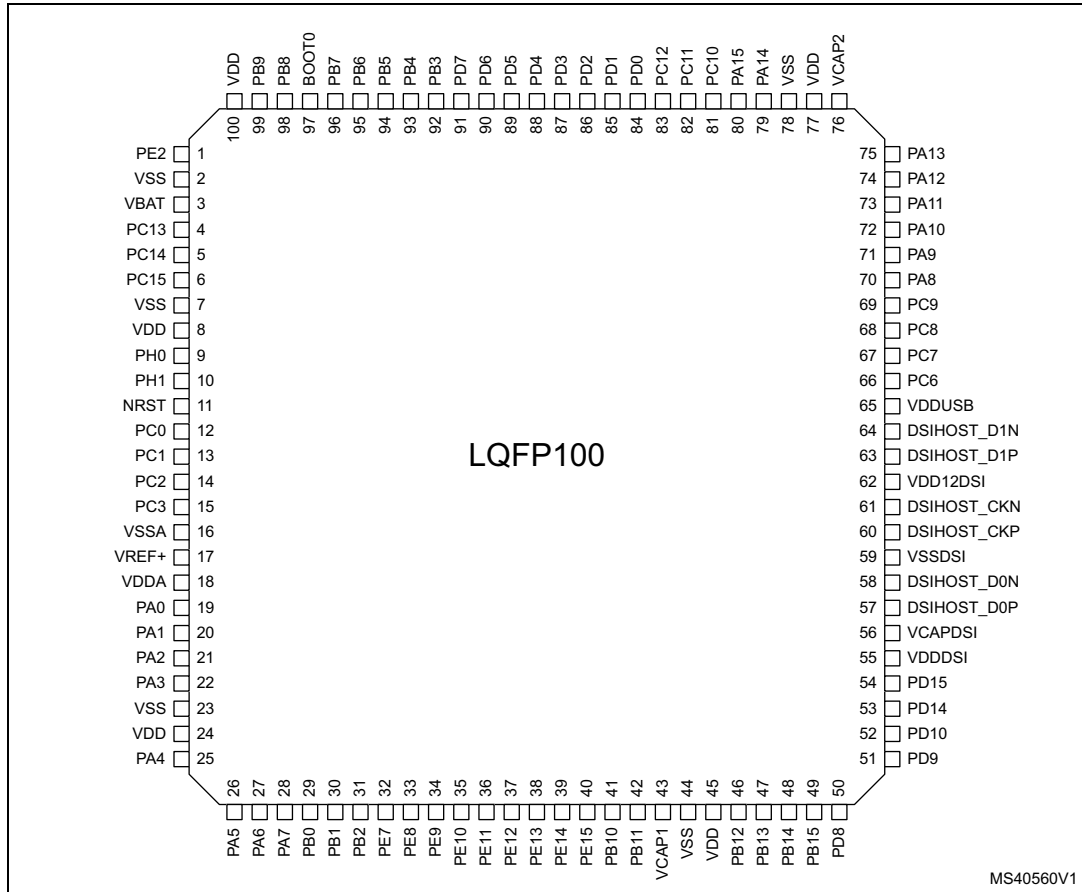
2.45 Embedded Trace Macrocell™

The Arm Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F47x through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

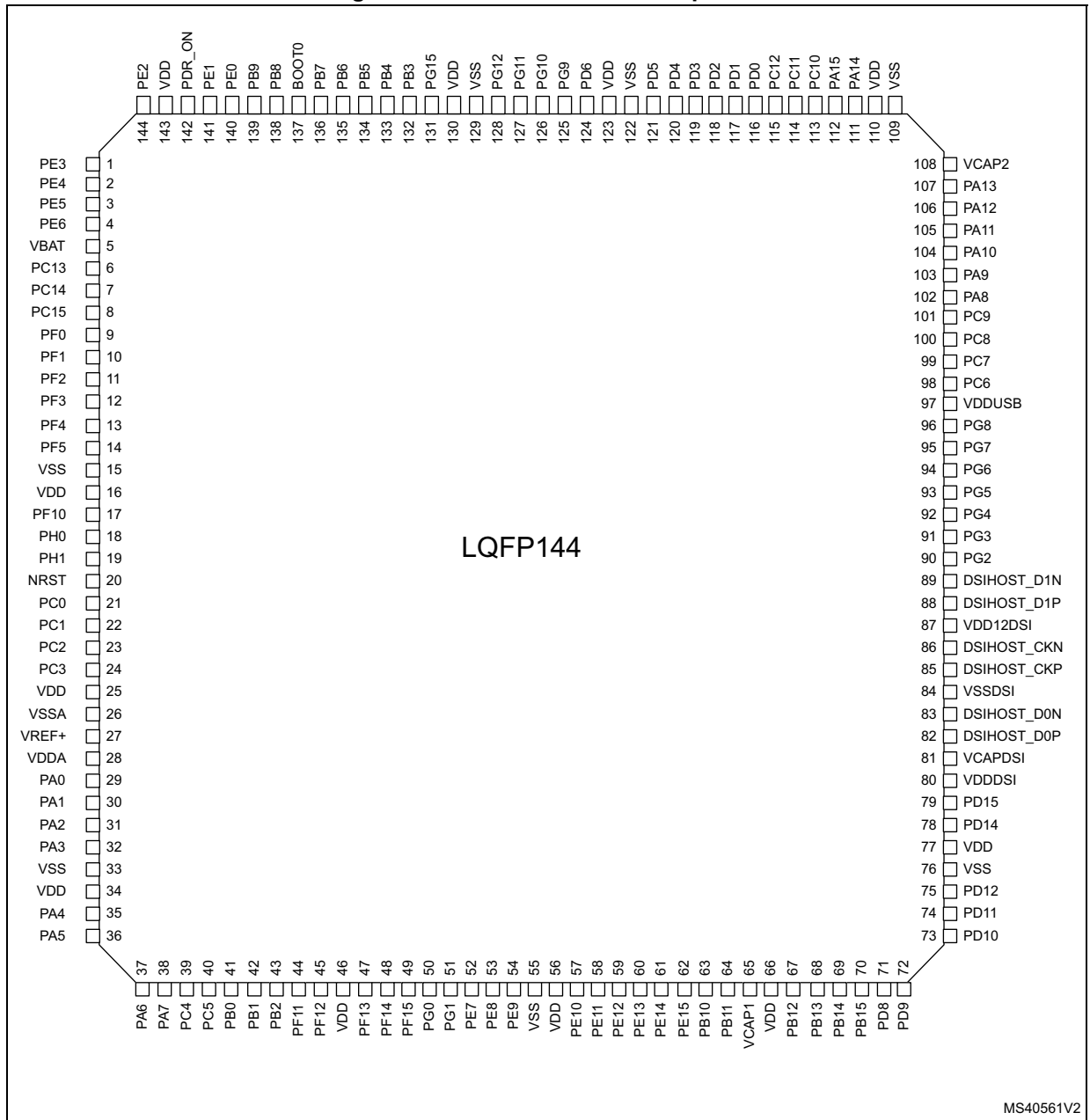
3 Pinouts and pin description

Figure 13. STM32F47x LQFP100 pinout



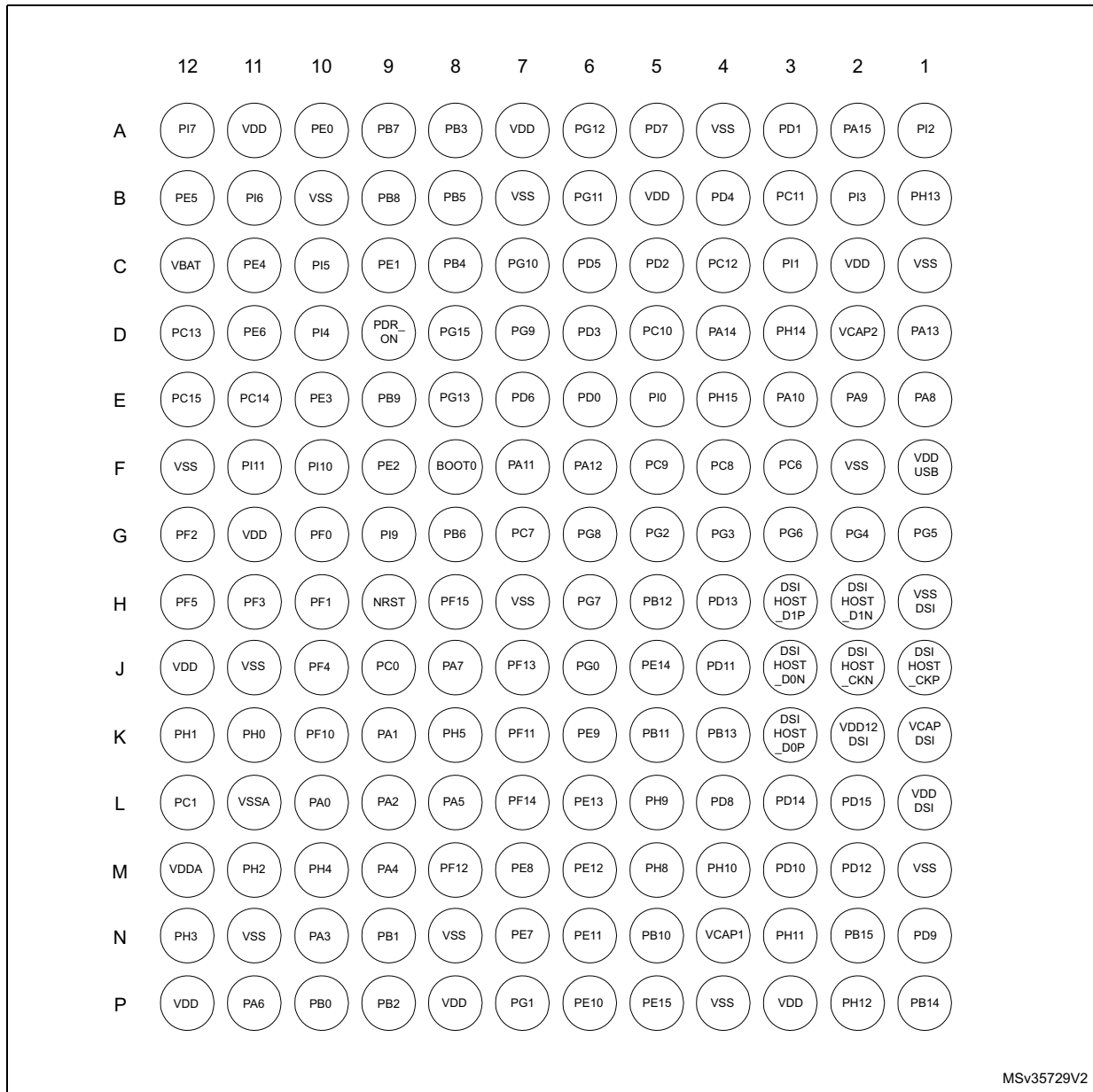
1. The above figure shows the package top view.

Figure 14. STM32F47x LQFP144 pinout



1. The above figure shows the package top view.

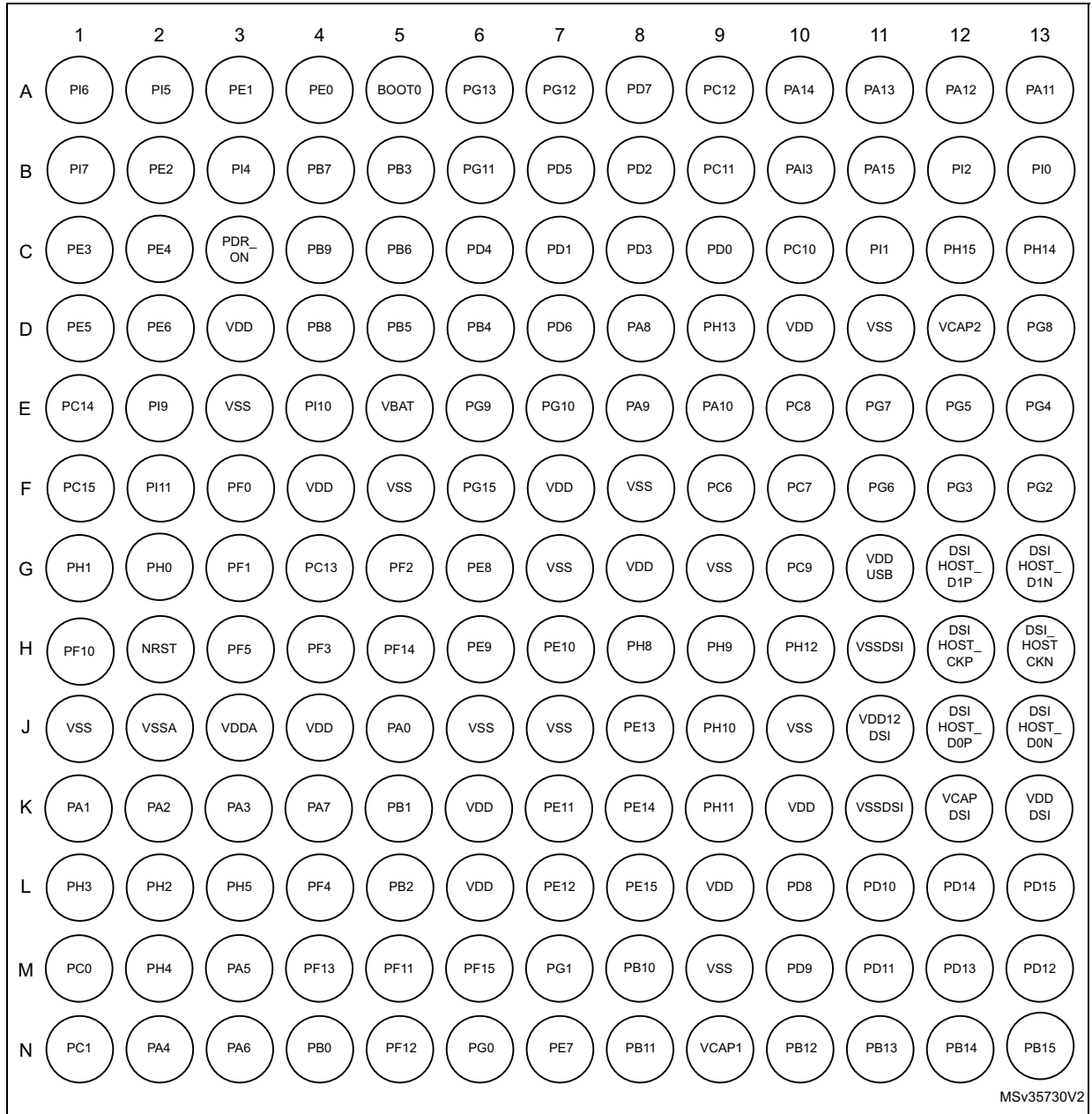
Figure 15. STM32F47x WLCSP168 pinout



MSv35729V2

1. The above figure shows the package bottom view.

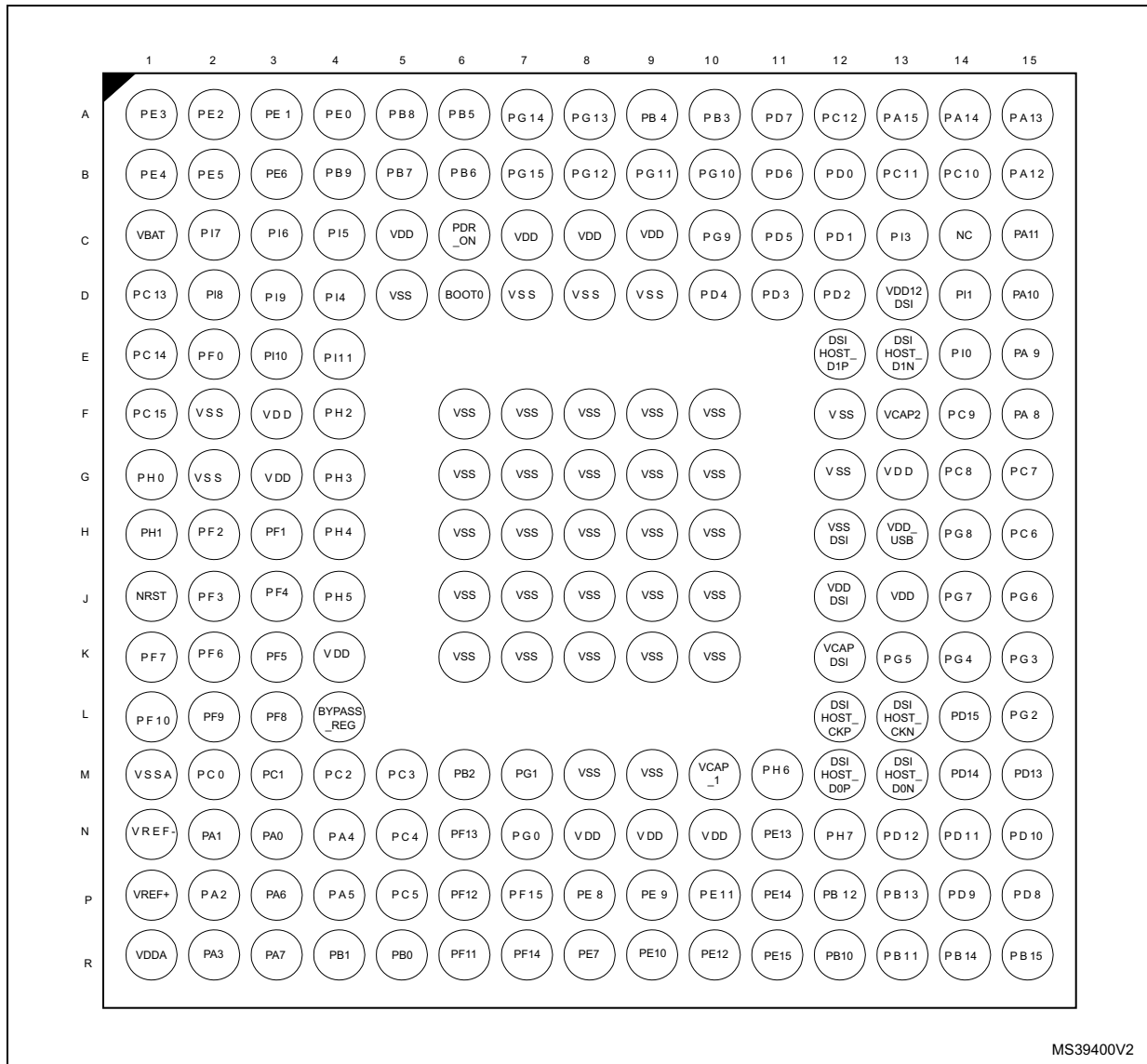
Figure 16. STM32F47x UFBGA169 ballout



MSv35730V2

1. The above figure shows the package top view.

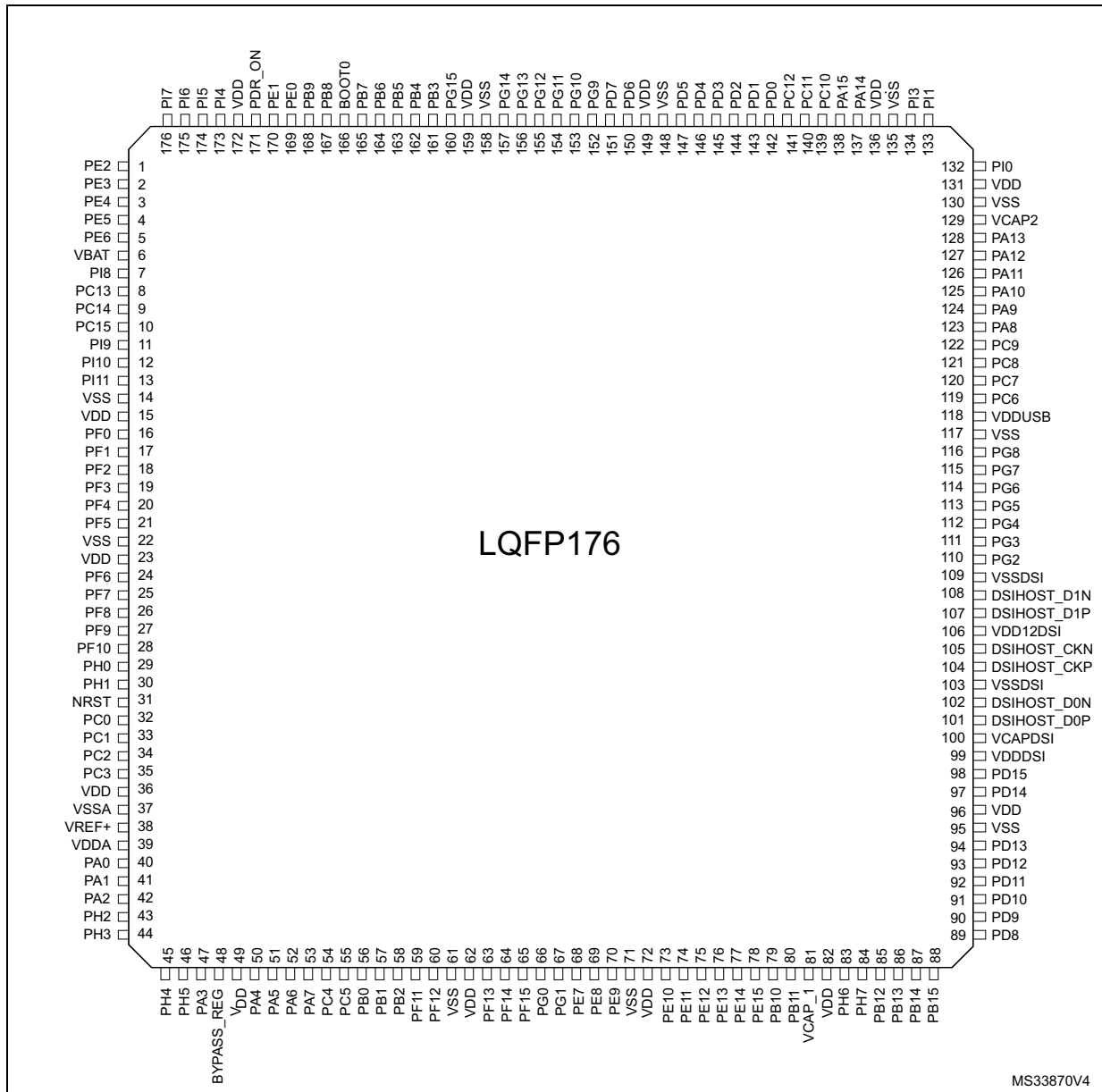
Figure 17. STM32F47x UFBGA176 ballout



MS39400V2

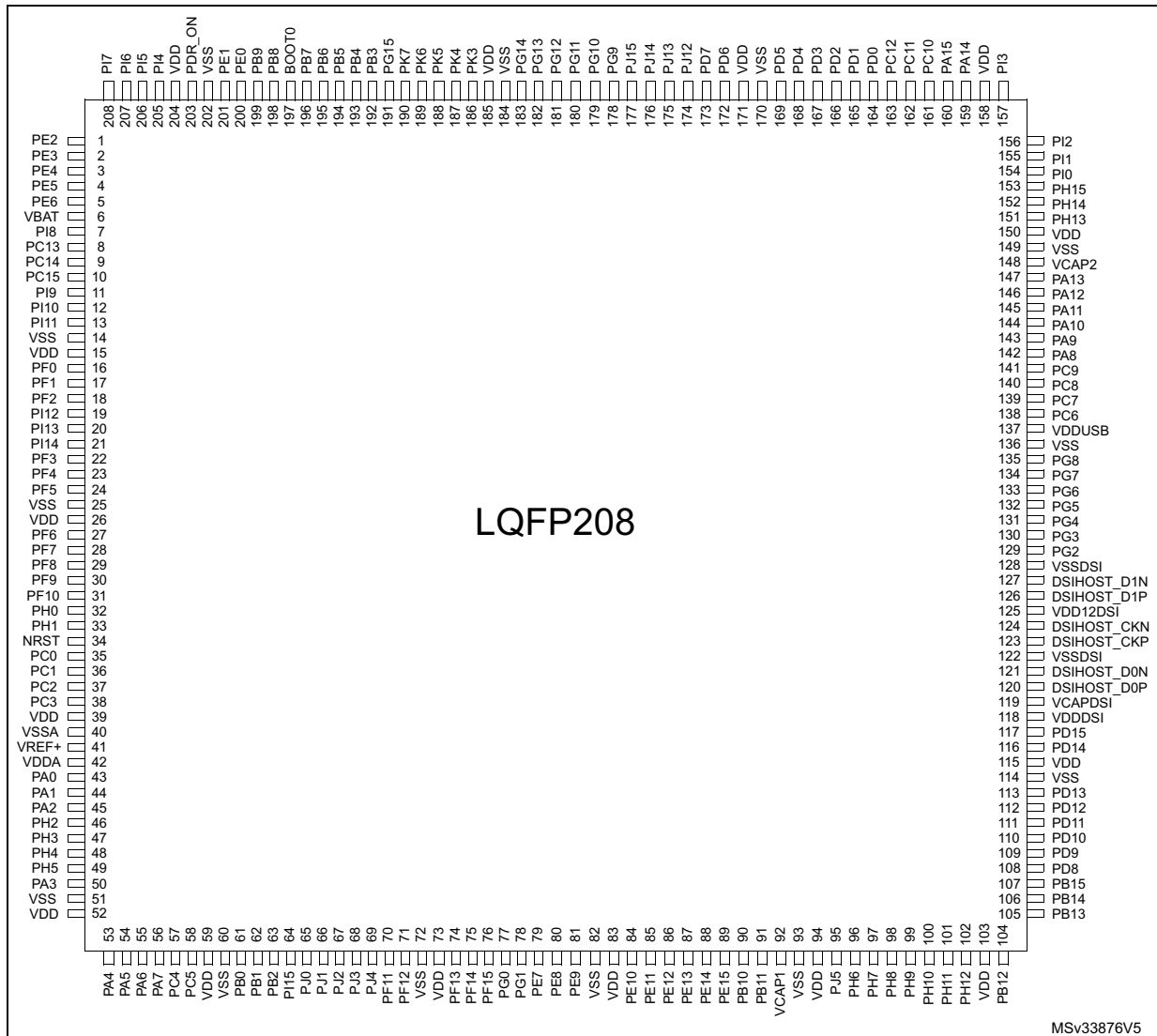
1. The above figure shows the package top view.

Figure 18. STM32F47x LQFP176 pinout



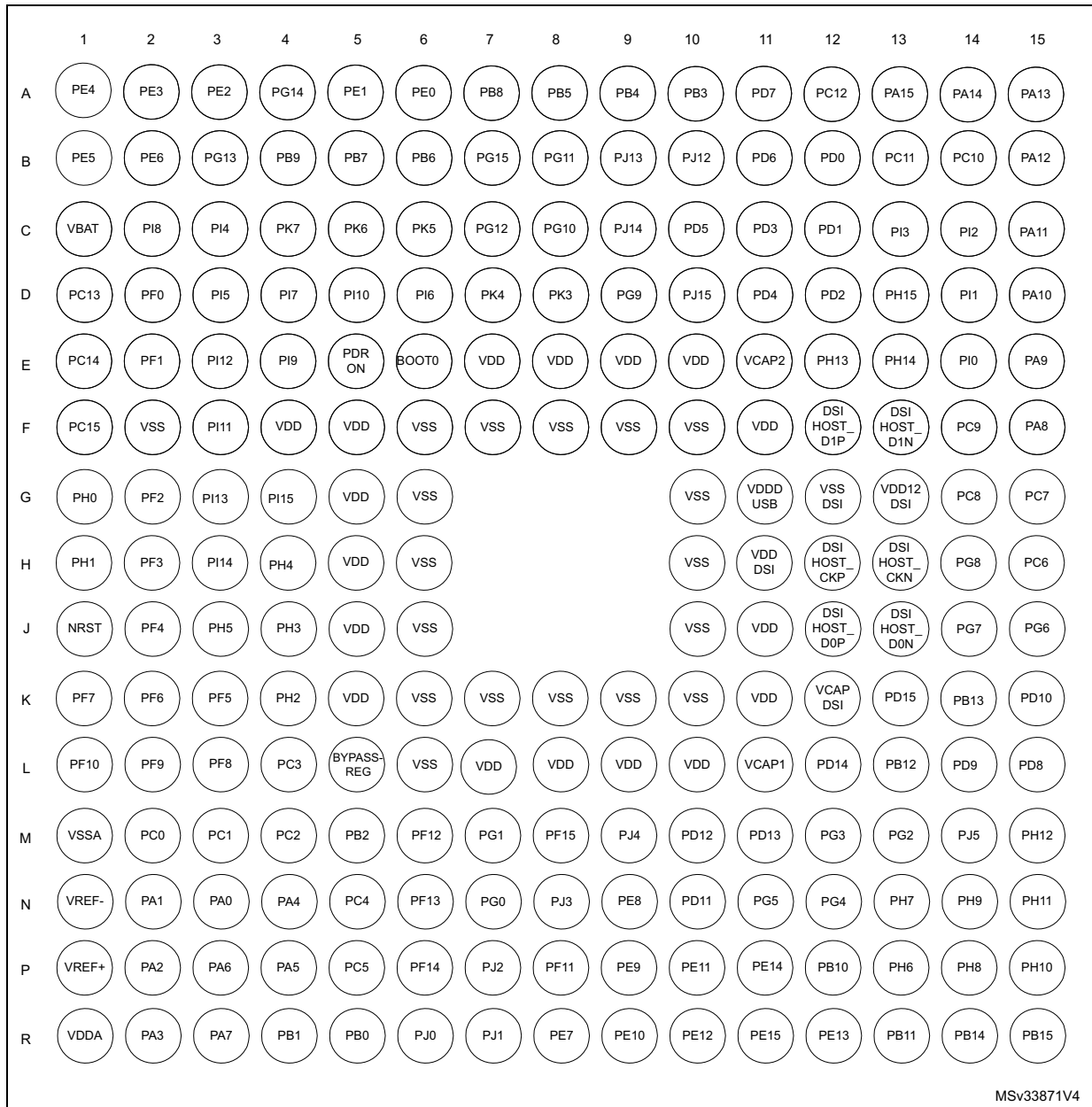
1. The above figure shows the package top view.

Figure 19. STM32F47x LQFP208 pinout



1. The above figure shows the package top view.

Figure 20. STM32F47x TFBGA216 ballout



MSv33871V4

1. The above figure shows the package top view.

Table 9. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TTa	3.3 V tolerant I/O directly connected to analog parts
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. STM32F479xx pin and ball definitions

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFPGA169	WLCSP168	UFPGA176	LQFP176	LQFP208	TFBGA216						
1	144	B2	F9	A2	1	1	A3	PE2	I/O	FT	-	TRACECLK, SPI4_SCK, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
NC (2)	1	C1	E10	A1	2	2	A2	PE3	I/O	FT	-	TRACED0, SAI1_SD_B, FMC_A19, EVENTOUT	-
NC (2)	2	C2	C11	B1	3	3	A1	PE4	I/O	FT	-	TRACED1, SPI4_NSS, SAI1_FS_A, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-
NC (2)	3	D1	B12	B2	4	4	B1	PE5	I/O	FT	-	TRACED2, TIM9_CH1, SPI4_MISO, SAI1_SCK_A, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
NC (2)	4	D2	D11	B3	5	5	B2	PE6	I/O	FT	-	TRACED3, TIM9_CH2, SPI4_MOSI, SAI1_SD_A, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
2	-	-	-	-	-	-	G6	VSS	S	-	-	-	-
-	-	-	-	-	-	-	F5	VDD	S	-	-	-	-
3	5	E5	C12	C1	6	6	C1	VBAT	S	-	-	-	-
-	-	-	-	D2	7	7	C2	PI8	I/O	FT	(3) (4)	EVENTOUT	RTC_TAMP1/ RTC_TAMP2/ RTC_TS
4	6	G4	D12	D1	8	8	D1	PC13	I/O	FT	(3) (4)	EVENTOUT	RTC_TAMP1/ RTC_TS/ RTC_OUT
5	7	E1	E11	E1	9	9	E1	PC14-OSC32_IN (PC14)	I/O	FT	(3) (4)	EVENTOUT	OSC32_IN
6	8	F1	E12	F1	10	10	F1	PC15- OSC32_OUT (PC15)	I/O	FT	(3) (4)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	G5	VDD	S	-	-	-	-
-	-	E2	G9	D3	11	11	E4	PI9	I/O	FT	-	CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-
-	-	E4	F10	E3	12	12	D5	PI10	I/O	FT	-	ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	F2	F11	E4	13	13	F3	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	-
-	-	F5	F12	F2	14	14	F2	VSS	S	-	-	-	-
-	-	F4	G11	F3	15	15	F4	VDD	S	-	-	-	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	9	F3	G10	E2	16	16	D2	PF0	I/O	FT		I2C2_SDA, FMC_A0, EVENTOUT	-
-	10	G3	H10	H3	17	17	E2	PF1	I/O	FT		I2C2_SCL, FMC_A1, EVENTOUT	-
-	11	G5	G12	H2	18	18	G2	PF2	I/O	FT		I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	-	-	19	E3	PI12	I/O	FT		LCD_HSYNC, EVENTOUT	-
-	-	-	-	-	-	20	G3	PI13	I/O	FT		LCD_VSYNC, EVENTOUT	-
-	-	-	-	-	-	21	H3	PI14	I/O	FT		LCD_CLK, EVENTOUT	-
-	12	H4	H11	J2	19	22	H2	PF3	I/O	FT	⁽⁵⁾	FMC_A3, EVENTOUT	ADC3_IN9
-	13	L4	J10	J3	20	23	J2	PF4	I/O	FT	⁽⁵⁾	FMC_A4, EVENTOUT	ADC3_IN14
-	14	H3	H12	K3	21	24	K3	PF5	I/O	FT	⁽⁵⁾	FMC_A5, EVENTOUT	ADC3_IN15
7	15	G7	J11	G2	22	25	H6	VSS	S	-	-	-	-
8	16	G8	J12	G3	23	26	H5	VDD	S	-	-	-	-
-	-	-	-	K2	24	27	K2	PF6	I/O	FT	⁽⁵⁾	TIM10_CH1, SPI5_NSS, SAI1_SD_B, UART7_Rx, QUADSPI_BK1_IO3, EVENTOUT	ADC3_IN4
-	-	-	-	K1	25	28	K1	PF7	I/O	FT	⁽⁵⁾	TIM11_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_Tx, QUADSPI_BK1_IO2, EVENTOUT	ADC3_IN5
-	-	-	-	L3	26	29	L3	PF8	I/O	FT	⁽⁵⁾	SPI5_MISO, SAI1_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_IN6
-	-	-	-	L2	27	30	L2	PF9	I/O	FT	⁽⁵⁾	SPI5_MOSI, SAI1_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_IN7
-	17	H1	K10	L1	28	31	L1	PF10	I/O	FT	⁽⁵⁾	QUADSPI_CLK, DCMI_D11, LCD_DE, EVENTOUT	ADC3_IN8
9	18	G2	K11	G1	29	32	G1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
10	19	G1	K12	H1	30	33	H1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
11	20	H2	H9	J1	31	34	J1	NRST	I/O	RST	-		
12	21	M1	J9	M2	32	35	M2	PC0	I/O	FT	⁽⁵⁾	OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_ IN10

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
13	22	N1	L12	M3	33	36	M3	PC1	I/O	FT	(5)	TRACED0, SPI2_MOSI/I2S2_SD, SAI1_SD_A, ETH_MDC, EVENTOUT	ADC123_ IN11
14	23	-	-	M4	34	37	M4	PC2	I/O	FT	(5)	SPI2_MISO, I2S2ext_SD, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_ IN12
15	24	-	-	M5	35	38	L4	PC3	I/O	FT	(5)	SPI2_MOSI/I2S2_SD, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC123_ IN13
-	25	-	-	-	36	39	J5	VDD	S	-	-	-	-
-	-	-	-	-	-	-	J6	VSS	S	-	-	-	-
16	26	J2	L11	M1	37	40	M1	VSSA	S	-	-	-	-
-	-	-	-	N1	-	-	N1	VREF-	S	-	-	-	-
17	27	-	-	P1	38	41	P1	VREF+	S	-	-	-	-
18	28	J3	M12	R1	39	42	R1	VDDA	S	-	-	-	-
19	29	J5	L10	N3	40	43	N3	PA0-WKUP(PA0)	I/O	FT	(6)	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII_CRS, EVENTOUT	ADC123_IN0, WKUP
20	30	K1	K9	N2	41	44	N2	PA1	I/O	FT	(5)	TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, ETH_MII_RX_CLK/ETH_R MII_REF_CLK, LCD_R2, EVENTOUT	ADC123_IN1
21	31	K2	L9	P2	42	45	P2	PA2	I/O	FT	(5)	TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, ETH_MDIO, LCD_R1, EVENTOUT	ADC123_IN2
-	-	L2	M11	F4	43	46	K4	PH2	I/O	FT	-	QUADSPI_BK2_IO0, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	-
-	-	L1	N12	G4	44	47	J4	PH3	I/O	FT	-	QUADSPI_BK2_IO1, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	-
-	-	M2	M10	H4	45	48	H4	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	L3	K8	J4	46	49	J3	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	-
22	32	K3	N10	R2	47	50	R2	PA3	I/O	FT	(5)	TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC123_IN3
23	33	J1	N11	-	-	51	K6	VSS	S	-	-	-	-
-	-	-	-	L4	48	-	L5	BYPASS_REG	I	FT	-	-	-
24	34	J4	P12	K4	49	52	K5	VDD	S	-	-	-	-
25	35	N2	M9	N4	50	53	N4	PA4	I/O	TTa	-	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_IN4, DAC_OUT1
26	36	M3	L8	P4	51	54	P4	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_IN5, DAC_OUT2
27	37	N3	P11	P3	52	55	P3	PA6	I/O	FT	(5)	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM13_CH1, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_IN6
28	38	K4	J8	R3	53	56	R3	PA7	I/O	FT	(5)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM14_CH1, QUADSPI_CLK, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_IN7
NC ⁽²⁾	39	-	-	N5	54	57	N5	PC4	I/O	FT	(5)	ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_IN14
NC ⁽²⁾	40	-	-	P5	55	58	P5	PC5	I/O	FT	(5)	ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT	ADC12_IN15
-	-	-	-	-	-	59	L7	VDD	S	-	-	-	-
-	-	-	-	-	-	60	L6	VSS	S	-	-	-	-
29	41	N4	P10	R5	56	61	R5	PB0	I/O	FT	(5)	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_IN8

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
30	42	K5	N9	R4	57	62	R4	PB1	I/O	FT	(5)	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_IN9
31	43	L5	P9	M6	58	63	M5	PB2- BOOT1(PB2)	I/O	FT	-	EVENTOUT	-
-	-	-	-	-	-	64	G4	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	-	-	65	R6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	-	-	66	R7	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	-	-	67	P7	PJ2	I/O	FT	-	DSIHOST_TE, LCD_R3, EVENTOUT	-
-	-	-	-	-	-	68	N8	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	-	-	69	M9	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	44	M5	K7	R6	59	70	P8	PF11	I/O	FT	-	SPI5_MOSI, FMC_SDNRAS, DCMI_D12, EVENTOUT	-
-	45	N5	M8	P6	60	71	M6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	J6	N8	M8	61	72	K7	VSS	S	-	-	-	-
-	46	K6	P8	N8	62	73	L8	VDD	S	-	-	-	-
-	47	M4	J7	N6	63	74	N6	PF13	I/O	FT	-	FMC_A7, EVENTOUT	-
-	48	H5	L7	R7	64	75	P6	PF14	I/O	FT	-	FMC_A8, EVENTOUT	-
-	49	M6	H8	P7	65	76	M8	PF15	I/O	FT	-	FMC_A9, EVENTOUT	-
-	50	N6	J6	N7	66	77	N7	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	51	M7	P7	M7	67	78	M7	PG1	I/O	FT	-	FMC_A11, EVENTOUT	-
32	52	N7	N7	R8	68	79	R8	PE7	I/O	FT	-	TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT	-
33	53	G6	M7	P8	69	80	N9	PE8	I/O	FT	-	TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT	-
34	54	H6	K6	P9	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, QUADSPI_BK2_IO2, FMC_D6, EVENTOUT	-
-	55	J7	-	M9	71	82	K8	VSS	S	-	-	-	-
-	56	L6	-	N9	72	83	L9	VDD	S	-	-	-	-
35	57	H7	P6	R9	73	84	R9	PE10	I/O	FT	-	TIM1_CH2N, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
36	58	K7	N6	P10	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, SPI4_NSS, FMC_D8, LCD_G3, EVENTOUT	-
37	59	L7	M6	R10	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, SPI4_SCK, FMC_D9, LCD_B4, EVENTOUT	-
38	60	J8	L6	N11	76	87	R12	PE13	I/O	FT	-	TIM1_CH3, SPI4_MISO, FMC_D10, LCD_DE, EVENTOUT	-
39	61	K8	J5	P11	77	88	P11	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, FMC_D11, LCD_CLK, EVENTOUT	-
40	62	L8	P5	R11	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12, LCD_R7, EVENTOUT	-
41	63	M8	N5	R12	79	90	P12	PB10	I/O	FT	-	TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
42	64	N8	K5	R13	80	91	R13	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSIHOST_TE, LCD_G5, EVENTOUT	-
43	65	N9	N4	M10	81	92	L11	VCAP1	S	-	-	-	-
44	-	M9	P4	-	-	93	K9	VSS	S	-	-	-	-
45	66	L9	P3	N10	82	94	L10	VDD	S	-	-	-	-
-	-	-	-	-	-	95	M14	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	P13	PH6	I/O	FT	-	I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	-	-	N12	84	97	N13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-
-	-	H8	M5	-	-	98	P14	PH8	I/O	FT	-	I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	H9	L5	-	-	99	N14	PH9	I/O	FT	-	I2C3_SMBA, TIM12_CH2, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	-	J9	M4	-	-	100	P15	PH10	I/O	FT	-	TIM5_CH1, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	K9	N3	-	-	101	N15	PH11	I/O	FT	-	TIM5_CH2, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	H10	P2	-	-	102	M15	PH12	I/O	FT	-	TIM5_CH3, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	H7	-	-	-	K10	VSS	S	-	-	-	-
-	66	-	-	-	-	103	K11	VDD	S	-	-	-	-
46	67	N10	H5	P12	85	104	L13	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII _TXD0, OTG_HS_ID, EVENTOUT	-
47	68	N11	K4	P13	86	105	K14	PB13	I/O	FT	-	TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII _TXD1, EVENTOUT	OTG_HS_ VBUS
48	69	N12	P1	R14	87	106	R14	PB14	I/O	FT	-	TIM1_CH2N, TIM8_CH2N, SPI2_MISO, I2S2ext_SD, USART3_RTS, TIM12_CH1, OTG_HS_DM, EVENTOUT	-
49	70	N13	N2	R15	88	107	R15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI/I2S2_SD, TIM12_CH2, OTG_HS_DP, EVENTOUT	-
50	71	L10	L4	P15	89	108	L15	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
51	72	M10	N1	P14	90	109	L14	PD9	I/O	FT	-	USART3_RX, FMC_D14, EVENTOUT	-
52	73	L11	M3	N15	91	110	K15	PD10	I/O	FT	-	USART3_CK, FMC_D15, LCD_B3, EVENTOUT	-
-	74	M11	J4	N14	92	111	N10	PD11	I/O	FT	-	USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	75	M13	M2	N13	93	112	M10	PD12	I/O	FT	-	TIM4_CH1, USART3_RTS, QUADSPI_BK1_IO1, FMC_A17/FMC_ALE, EVENTOUT	-
-	-	M12	H4	M15	94	113	M11	PD13	I/O	FT	-	TIM4_CH2, QUADSPI_BK1_IO3, FMC_A18, EVENTOUT	-
-	76	J10	M1	-	95	114	J10	VSS	S	-	-	-	-
-	77	K10	-	J13	96	115	J11	VDD	S	-	-	-	-
53	78	L12	L3	M14	97	116	L12	PD14	I/O	FT	-	TIM4_CH3, FMC_D0, EVENTOUT	-
54	79	L13	L2	L14	98	117	K13	PD15	I/O	FT	-	TIM4_CH4, FMC_D1, EVENTOUT	-
55	80	K13	L1	J12	99	118	H11	VDDDSI	S	-	-	-	-
-	-	-	-	-	-	-	H10	VSS	S	-	-	-	-
56	81	K12	K1	K12	100	119	K12	VCAPDSI	S	-	-	-	-
-	-	-	K2	D13	-	-	G13	VDD12DSI	S	-	-	-	-
57	82	J12	K3	M12	101	120	J12	DSIHOST_D0P	I/O	-	-	-	-
58	83	J13	J3	M13	102	121	J13	DSIHOST_D0N	I/O	-	-	-	-
59	84	K11	H1	H12	103	122	G12	VSSDSI	S	-	-	-	-
60	85	H12	J1	L12	104	123	H12	DSIHOST_CKP	I/O	-	-	-	-
61	86	H13	J2	L13	105	124	H13	DSIHOST_CKN	I/O	-	-	-	-
62	87	J11	-	D13	106	125	-	VDD12DSI	S	-	-	-	-
63	88	G12	H3	E12	107	126	F12	DSIHOST_D1P	I/O	-	-	-	-
64	89	G13	H2	E13	108	127	F13	DSIHOST_D1N	I/O	-	-	-	-
-	-	H11	-	H12	109	128	-	VSSDSI	S	-	-	-	-
-	90	F13	G5	L15	110	129	M13	PG2	I/O	FT	-	FMC_A12, EVENTOUT	-
-	91	F12	G4	K15	111	130	M12	PG3	I/O	FT	-	FMC_A13, EVENTOUT	-
-	92	E13	G2	K14	112	131	N12	PG4	I/O	FT	-	FMC_A14/FMC_BA0, EVENTOUT	-
-	93	E12	G1	K13	113	132	N11	PG5	I/O	FT	-	FMC_A15/FMC_BA1, EVENTOUT	-
-	94	F11	G3	J15	114	133	J15	PG6	I/O	FT	-	DCMI_D12, LCD_R7, EVENTOUT	-
-	95	E11	H6	J14	115	134	J14	PG7	I/O	FT	-	SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	96	D13	G6	H14	116	135	H14	PG8	I/O	FT	-	SPI6_NSS, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	-	G9	F2	G12	117	136	G10	VSS	S	-	-	-	-
65	97	G11	F1	H13	118	137	G11	VDDUSB	S	-	-	-	-
66	98	F9	F3	H15	119	138	H15	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, USART6_TX, SDIO_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-
67	99	F10	G7	G15	120	139	G15	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, SDIO_D7, DCMI_D1, LCD_G6, EVENTOUT	-
68	100	E10	F4	G14	121	140	G14	PC8	I/O	FT	-	TRACED1, TIM3_CH3, TIM8_CH3, USART6_CK, SDIO_D0, DCMI_D2, EVENTOUT	-
69	101	G10	F5	F14	122	141	F14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, QUADSPI_BK1_IO0, SDIO_D1, DCMI_D3, EVENTOUT	-
70	102	D8	E1	F15	123	142	F15	PA8	I/O	FT	-	MCO1, TIM1_CH1, I2C3_SCL, USART1_CK, OTG_FS_SOF, LCD_R6, EVENTOUT	-
71	103	E8	E2	E15	124	143	E15	PA9	I/O	FT	-	TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, DCMI_D0, EVENTOUT	OTG_FS_VBUS
72	104	E9	E3	D15	125	144	D15	PA10	I/O	FT	-	TIM1_CH3, USART1_RX, OTG_FS_ID, DCMI_D1, EVENTOUT	-
73	105	A13	F7	C15	126	145	C15	PA11	I/O	FT	-	TIM1_CH4, USART1_CTS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-
74	106	A12	F6	B15	127	146	B15	PA12	I/O	FT	-	TIM1_ETR, USART1_RTS, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
75	107	A11	D1	A15	128	147	A15	PA13(JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
76	108	D12	D2	F13	129	148	E11	VCAP2	S	-	-	-	-
-	109	D11	C1	F12	130	149	F10	VSS	S	-	-	-	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
77	110	D10	C2	G13	131	150	F11	VDD	S	-	-	-	-
-	-	D9	B1	-	-	151	E12	PH13	I/O	FT	-	TIM8_CH1N, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	C13	D3	-	-	152	E13	PH14	I/O	FT	-	TIM8_CH2N, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	C12	E4	-	-	153	D13	PH15	I/O	FT	-	TIM8_CH3N, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	B13	E5	E14	132	154	E14	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS ⁽⁷⁾ , FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	C11	C3	D14	133	155	D14	PI1	I/O	FT	-	SPI2_SCK/I2S2_CK ⁽⁷⁾ , FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	B12	A1	-	NC (2)	156	C14	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO, I2S2ext_SD, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	B10	B2	C13	134	157	C13	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, DCMI_D10, EVENTOUT	-
78	-	-	-	D9	135	-	F9	VSS	S	-	-	-	-
-	-	-	B5	C9	136	158	E10	VDD	S	-	-	-	-
79	111	A10	D4	A14	137	159	A14	PA14(JTCK- SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
80	112	B11	A2	A13	138	160	A13	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS, SPI3_NSS/I2S3_WS, EVENTOUT	-
81	113	C10	D5	B14	139	161	B14	PC10	I/O	FT	-	SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDIO_D2, DCMI_D8, LCD_R2, EVENTOUT	-
82	114	B9	B3	B13	140	162	B13	PC11	I/O	FT	-	I2S3ext_SD, SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDIO_D3, DCMI_D4, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
83	115	A9	C4	A12	141	163	A12	PC12	I/O	FT	-	TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDIO_CK, DCM1_D9, EVENTOUT	-
84	116	C9	E6	B12	142	164	B12	PD0	I/O	FT	-	CAN1_RX, FMC_D2, EVENTOUT	-
85	117	C7	A3	C12	143	165	C12	PD1	I/O	FT	-	CAN1_TX, FMC_D3, EVENTOUT	-
86	118	B8	C5	D12	144	166	D12	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDIO_CMD, DCMI_D11, EVENTOUT	-
87	119	C8	D6	D11	145	167	C11	PD3	I/O	FT	-	SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-
88	120	C6	B4	D10	146	168	D11	PD4	I/O	FT	-	USART2_RTS, FMC_NOE, EVENTOUT	-
89	121	B7	C6	C11	147	169	C10	PD5	I/O	FT	-	USART2_TX, FMC_NWE, EVENTOUT	-
-	122	F8	A4	D8	148	170	F8	VSS	S	-	-	-	-
-	123	F7	-	C8	149	171	E9	VDD	S	-	-	-	-
90	124	D7	E7	B11	150	172	B11	PD6	I/O	FT	-	SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, DCM1_D10, LCD_B2, EVENTOUT	-
91	-	A8	A5	A11	151	173	A11	PD7	I/O	FT	-	USART2_CK, FMC_NE1, EVENTOUT	-
-	-	-	-	-	-	174	B10	PJ12	I/O	FT	-	LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	-	-	175	B9	PJ13	I/O	FT	-	LCD_G4, LCD_B1, EVENTOUT	-
-	-	-	-	-	-	176	C9	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	-	-	177	D10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	125	E6	D7	C10	152	178	D9	PG9	I/O	FT	-	USART6_RX, QUADSPI_BK2_IO2, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	126	E7	C7	B10	153	179	C8	PG10	I/O	FT	-	LCD_G3, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	127	B6	B6	B9	154	180	B8	PG11	I/O	FT	-	ETH_MII_TX_EN/ETH_RMII_TX_EN, DCM1_D3, LCD_B3, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
-	128	A7	A6	B8	155	181	C7	PG12	I/O	FT	-	SPI6_MISO, USART6_RTS, LCD_B4, FMC_NE4, LCD_B1, EVENTOUT	-
-	-	A6	E8	A8	156	182	B3	PG13	I/O	FT	-	TRACED0, SPI6_SCK, USART6_CTS, ETH_MII_TXD0/ETH_RMII _TXD0, FMC_A24, LCD_R0, EVENTOUT	-
-	-	-	-	A7	157	183	A4	PG14	I/O	FT	-	TRACED1, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII _TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	129	-	B7	D7	158	184	F7	VSS	S	-	-	-	-
-	130	-	A7	C7	159	185	E8	VDD	S	-	-	-	-
-	-	-	-	-	-	186	D8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	-	-	187	D7	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	-	-	188	C6	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	-	-	189	C5	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	-	-	190	C4	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	131	F6	D8	B7	160	191	B7	PG15	I/O	FT	-	USART6_CTS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
92	132	B5	A8	A10	161	192	A10	PB3(JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK/I2S3_CK, EVENTOUT	-
93	133	D6	C8	A9	162	193	A9	PB4(NJTRST)	I/O	FT	-	NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, I2S3ext_SD, EVENTOUT	-
94	134	D5	B8	A6	163	194	A8	PB5	I/O	FT	-	TIM3_CH2, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/I2S3_SD, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, LCD_G7, EVENTOUT	-
95	135	C5	G8	B6	164	195	B6	PB6	I/O	FT	-	TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, FMC_SDNE1, DCMI_D5, EVENTOUT	-

Table 10. STM32F479xx pin and ball definitions (continued)

Pin number								Pin name (function after reset) ⁽¹⁾	Pin types	I/O structures	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA169	WLCSP168	UFBGA176	LQFP176	LQFP208	TFBGA216						
96	136	B4	A9	B5	165	196	B5	PB7	I/O	FT	-	TIM4_CH2, I2C1_SDA, USART1_RX, FMC_NL, DCMI_VSYNC, EVENTOUT	-
97	137	A5	F8	D6	166	197	E6	BOOT0	I	B	-	-	VPP
98	138	D4	B9	A5	167	198	A7	PB8	I/O	FT	-	TIM4_CH3, TIM10_CH1, I2C1_SCL, CAN1_RX, ETH_MII_TXD3, SDIO_D4, DCMI_D6, LCD_B6, EVENTOUT	-
99	139	C4	E9	B4	168	199	B4	PB9	I/O	FT	-	TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, CAN1_TX, SDIO_D5, DCMI_D7, LCD_B7, EVENTOUT	-
NC (2)	140	A4	A10	A4	169	200	A6	PE0	I/O	FT	-	TIM4_ETR, UART8_Rx, FMC_NBL0, DCMI_D2, EVENTOUT	-
NC (2)	141	A3	C9	A3	170	201	A5	PE1	I/O	FT	-	UART8_Tx, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	E3	B10	D5	-	202	F6	VSS	S	-	-	-	-
-	142	C3	D9	C6	171	203	E5	PDR_ON	S	-	-	-	-
100	143	D3	A11	C5	172	204	E7	VDD	S	-	-	-	-
-	-	B3	D10	D4	173	205	C3	PI4	I/O	FT	-	TIM8_BKIN, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	A2	C10	C4	174	206	D3	PI5	I/O	FT	-	TIM8_CH1, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	A1	B11	C3	175	207	D6	PI6	I/O	FT	-	TIM8_CH2, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	B1	A12	C2	176	208	D4	PI7	I/O	FT	-	TIM8_CH3, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

1. Function availability depends on the chosen device.
2. NC (not-connected) pins are not bonded. They must be configured by software to output push-pull and forced to "0" in the output data register to avoid extra current consumption in low power modes.
3. PC13, PC14, PC15 and PI8 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 and PI8 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF.
 - These I/Os must not be used as a current source (e.g. to drive an LED).
4. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F4xx reference manual, available from the STMicroelectronics website: www.st.com.
5. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).

6. If the device is delivered in an WLCSP168, UFBGA169, UFBGA176, LQFP176 or TFBGA216 package, and the BYPASS_REG pin is set to VDD (Regulator OFF/internal reset ON mode), then PA0 is used as an internal Reset (active low).
7. PI0 and PI1 cannot be used for I2S2 full-duplex mode.

Table 11. FMC pin definition

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF0	A0	-	-	A0
PF1	A1	-	-	A1
PF2	A2	-	-	A2
PF3	A3	-	-	A3
PF4	A4	-	-	A4
PF5	A5	-	-	A5
PF12	A6	-	-	A6
PF13	A7	-	-	A7
PF14	A8	-	-	A8
PF15	A9	-	-	A9
PG0	A10	-	-	A10
PG1	A11	-	-	A11
PG2	A12	-	-	A12
PG3	A13	-	-	
PG4	A14	-	-	BA0
PG5	A15	-	-	BA1
PD11	A16	A16	CLE	-
PD12	A17	A17	ALE	-
PD13	A18	A18	-	-
PE3	A19	A19	-	-
PE4	A20	A20	-	-
PE5	A21	A21	-	-
PE6	A22	A22	-	-
PE2	A23	A23	-	-
PG13	A24	A24	-	-
PG14	A25	A25	-	-
PD14	D0	DA0	D0	D0
PD15	D1	DA1	D1	D1
PD0	D2	DA2	D2	D2
PD1	D3	DA3	D3	D3
PE7	D4	DA4	D4	D4
PE8	D5	DA5	D5	D5
PE9	D6	DA6	D6	D6
PE10	D7	DA7	D7	D7
PE11	D8	DA8	D8	D8

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PE12	D9	DA9	D9	D9
PE13	D10	DA10	D10	D10
PE14	D11	DA11	D11	D11
PE15	D12	DA12	D12	D12
PD8	D13	DA13	D13	D13
PD9	D14	DA14	D14	D14
PD10	D15	DA15	D15	D15
PH8	D16	-	-	D16
PH9	D17	-	-	D17
PH10	D18	-	-	D18
PH11	D19	-	-	D19
PH12	D20	-	-	D20
PH13	D21	-	-	D21
PH14	D22	-	-	D22
PH15	D23	-	-	D23
PI0	D24	-	-	D24
PI1	D25	-	-	D25
PI2	D26	-	-	D26
PI3	D27	-	-	D27
PI6	D28	-	-	D28
PI7	D29	-	-	D29
PI9	D30	-	-	D30
PI10	D31	-	-	D31
PD7	NE1	NE1	-	-
PG9	NE2	NE2	NCE	-
PG10	NE3	NE3	-	-
PG11	-	-	-	-
PG12	NE4	NE4	-	-
PD3	CLK	CLK	-	-
PD4	NOE	NOE	NOE	-
PD5	NWE	NWE	NWE	-
PD6	NWAIT	NWAIT	NWAIT	-
PB7	NADV	NADV	-	-
PF6	-	-	-	-
PF7	-	-	-	-

Table 11. FMC pin definition (continued)

Pin name	NOR/PSRAM/SRAM	NOR/PSRAM Mux	NAND16	SDRAM
PF8	-	-	-	-
PF9	-	-	-	-
PF10	-	-	-	-
PG6	-	-	-	-
PG7	-	-	INT	-
PE0	NBL0	NBL0	-	NBL0
PE1	NBL1	NBL1	-	NBL1
PI4	NBL2	-	-	NBL2
PI5	NBL3	-	-	NBL3
PG8	-	-	-	SDCLK
PC0	-	-	-	SDNWE
PF11	-	-	-	SDNRAS
PG15	-	-	-	SDNCAS
PH2	-	-	-	SDCKE0
PH3	-	-	-	SDNE0
PH6	-	-	-	SDNE1
PH7	-	-	-	SDCKE1
PH5	-	-	-	SDNWE
PC2	-	-	-	SDNE0
PC3	-	-	-	SDCKE0
PB5	-	-	-	SDCKE1
PB6	-	-	-	SDNE1



Table 12. Alternate function

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS	
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	ETH_MII_CRS	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-	-	-	ETH_MDIO	-	-	LCD_R1	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENT OUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK	-	-	-	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BK1N	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCLK	LCD_G2	EVENT OUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	QUADSPI_CLK	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENT OUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	-	-	-	LCD_R6	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	DCMI_D0	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_RX	-	-	OTG_FS_ID	-	-	DCMI_D1	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENT OUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PA15	JTDI	TIM2_CH1/TIM2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/I2S3_WS	-	-	-	-	-	-	-	-	EVENT OUT	



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15		
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS		
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENT OUT	
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENT OUT	
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT	
	PB3	JTDO / TRACES WO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK/I2S3_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	-	-	-	-	-	-	-	-	EVENT OUT
	PB5	-	-	TIM3_CH2	-	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	LCD_G7	EVENT OUT	
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	-	FMC_SDNE1	DCMI_D5	-	EVENT OUT	
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FMC_NL	DCMI_VSYNC	-	EVENT OUT	
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	DCMI_D6	LCD_B6	EVENT OUT	
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	LCD_B7	EVENT OUT	
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENT OUT	
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	DSIHOST_TE	LCD_G5	EVENT OUT	
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	-	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	-	-	EVENT OUT	
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I2S2_CK	-	USART3_CTS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	-	EVENT OUT	
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	-	SPI2_MISO	I2S2ext_SD	USART3_RTS	-	TIM12_CH1	-	-	OTG_HS_DM	-	-	EVENT OUT	
PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI/I2S2_SD	-	-	-	TIM12_CH2	-	-	OTG_HS_DP	-	-	EVENT OUT		



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS	
Port C	PC0	-	-	-	-	-	-	-	-	-	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	LCD_R5	EVENT OUT
	PC1	TRACE_D0	-	-	-	-	SPI2_MOSI/I2S2_SD	SAI1_SD_A	-	-	-	-	ETH_MDC	-	-	-	EVENT OUT
	PC2	-	-	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDN_E0	-	-	EVENT OUT
	PC3	-	-	-	-	-	SPI2_MOSI/I2S2_SD	-	-	-	-	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENT OUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDN_E0	-	-	EVENT OUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	-	-	EVENT OUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S2_MCK	-	-	USART6_TX	-	-	-	SDIO_D6	DCMI_D0	LCD_HSYNC	EVENT OUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S3_MCK	-	USART6_RX	-	-	-	SDIO_D7	DCMI_D1	LCD_G6	EVENT OUT
	PC8	TRACE_D1	-	TIM3_CH3	TIM8_CH3	-	-	-	-	USART6_CK	-	-	-	SDIO_D0	DCMI_D2	-	EVENT OUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	-	QUADSPI_BK1_IO0	-	-	SDIO_D1	DCMI_D3	-	EVENT OUT
	PC10	-	-	-	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDIO_D2	DCMI_D8	LCD_R2	EVENT OUT
	PC11	-	-	-	-	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDIO_D3	DCMI_D4	-	EVENT OUT
	PC12	TRACE_D3	-	-	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENT OUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT	

DS1118 Rev 5

76/219



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS	
Port D	PD0	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FMC_D2	-	-	EVENT OUT	
	PD1	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FMC_D3	-	-	EVENT OUT	
	PD2	TRACE D2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	SDIO_CMD	DCMI_D11	-	EVENT OUT	
	PD3	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CTS	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENT OUT	
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	FMC_NOE	-	-	EVENT OUT	
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	FMC_NWE	-	-	EVENT OUT	
	PD6	-	-	-	-	-	SPI3_MOSI/I2S3_SD	SAI1_SD_A	USART2_RX	-	-	-	FMC_NWAIT	DCMI_D10	LCD_B2	EVENT OUT	
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	FMC_NE1	-	-	EVENT OUT	
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	FMC_D13	-	-	EVENT OUT	
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	FMC_D14	-	-	EVENT OUT	
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	FMC_D15	-	LCD_B3	EVENT OUT	
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	QUADSPI_BK1_IO0	-	-	FMC_A16/FMC_CLE	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	QUADSPI_BK1_IO1	-	-	FMC_A17/FMC_ALE	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	QUADSPI_BK1_IO3	-	-	FMC_A18	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	FMC_D0	-	-	EVENT OUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	FMC_D1	-	-	EVENT OUT	



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS	
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	UART8_Rx	-	-	-	FMC_NBL0	DCMI_D2	-	EVENT OUT	
	PE1	-	-	-	-	-	-	-	UART8_Tx	-	-	-	FMC_NBL1	DCMI_D3	-	EVENT OUT	
	PE2	TRACE CLK	-	-	-	-	SPI4_SCK	SAI1_MCLK_A	-	-	QUADSPI_BK1_IO2	-	ETH_MII_TXD3	FMC_A23	-	-	EVENT OUT
	PE3	TRACE D0	-	-	-	-	-	SAI1_SD_B	-	-	-	-	-	FMC_A19	-	-	EVENT OUT
	PE4	TRACE D1	-	-	-	-	SPI4_NSS	SAI1_FS_A	-	-	-	-	-	FMC_A20	DCMI_D4	LCD_B0	EVENT OUT
	PE5	TRACE D2	-	-	TIM9_CH1	-	SPI4_MISO	SAI1_SCK_A	-	-	-	-	-	FMC_A21	DCMI_D6	LCD_G0	EVENT OUT
	PE6	TRACE D3	-	-	TIM9_CH2	-	SPI4_MOSI	SAI1_SD_A	-	-	-	-	-	FMC_A22	DCMI_D7	LCD_G1	EVENT OUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	UART7_Rx	-	QUADSPI_BK2_IO0	-	FMC_D4	-	-	EVENT OUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	UART7_Tx	-	QUADSPI_BK2_IO1	-	FMC_D5	-	-	EVENT OUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO2	-	FMC_D6	-	-	EVENT OUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO3	-	FMC_D7	-	-	EVENT OUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	-	-	-	-	-	-	FMC_D8	-	LCD_G3	EVENT OUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	LCD_B4	EVENT OUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	LCD_DE	EVENT OUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	-	-	FMC_D11	-	LCD_CLK	EVENT OUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12	-	LCD_R7	EVENT OUT



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	FMC_A0	-	-	EVENT OUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	FMC_A1	-	-	EVENT OUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	FMC_A2	-	-	EVENT OUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	EVENT OUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	EVENT OUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	EVENT OUT
	PF6	-	-	-	TIM10_CH1	-	SPI5_NSS	SAI1_SD_B	-	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	-	EVENT OUT
	PF7	-	-	-	TIM11_CH1	-	SPI5_SCK	SAI1_MCLK_B	-	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	-	EVENT OUT
	PF8	-	-	-	-	-	SPI5_MISO	SAI1_SCK_B	-	-	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	EVENT OUT
	PF9	-	-	-	-	-	SPI5_MOSI	SAI1_FS_B	-	-	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	EVENT OUT
	PF10	-	-	-	-	-	-	-	-	-	QUADSPI_CLK	-	-	DCMI_D11	LCD_DE	EVENT OUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	-	FMC_SDN_RAS	DCMI_D12	-	EVENT OUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENT OUT
	PF13	-	-	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	EVENT OUT
	PF14	-	-	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	EVENT OUT
PF15	-	-	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	EVENT OUT	

Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS	
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT OUT	
	PG1	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT OUT	
	PG2	-	-	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	EVENT OUT	
	PG3	-	-	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	EVENT OUT	
	PG4	-	-	-	-	-	-	-	-	-	-	-	FMC_A14/FMC_BA0	-	-	EVENT OUT	
	PG5	-	-	-	-	-	-	-	-	-	-	-	FMC_A15/FMC_BA1	-	-	EVENT OUT	
	PG6	-	-	-	-	-	-	-	-	-	-	-		DCMI_D12	LCD_R7	EVENT OUT	
	PG7	-	-	-	-	-	-	SAI1_MCLK_A		USART6_CK	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENT OUT
	PG8	-	-	-	-	-	SPI6_NSS	-	-	USART6_RTS	-	-	ETH_PPS_OUT	FMC_SDCLK		LCD_G7	EVENT OUT
	PG9	-	-	-	-	-	-	-	-	USART6_RX	QUADSPI_BK2_IO2	-	-	FMC_NE2/FMC_NCE	DCMI_VSYN		EVENT OUT
	PG10	-	-	-	-	-	-	-	-		LCD_G3	-	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT OUT
	PG11	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_EN / ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENT OUT
	PG12	-	-	-	-	-	SPI6_MISO	-	-	USART6_RTS	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENT OUT
	PG13	TRACE_D0	-	-	-	-	SPI6_SCK	-	-	USART6_CTS	-	-	-	ETH_MII_TXD0 / ETH_RMII_TXD0	FMC_A24	LCD_R0	EVENT OUT
	PG14	TRACE_D1	-	-	-	-	SPI6_MOSI	-	-	USART6_TX	QUADSPI_BK2_IO3	-	-	ETH_MII_TXD1 / ETH_RMII_TXD1	FMC_A25	LCD_B0	EVENT OUT
PG15	-	-	-	-	-	-	-	-	USART6_CTS	-	-	-	FMC_SDNCS	DCMI_D13	-	EVENT OUT	



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15			
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS			
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT		
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT	
	PH2	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO0	-	ETH_MII_CRD	FMC_SDCKE0	-	LCD_R0	-	EVENT OUT	
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	-	ETH_MII_COL	FMC_SDN E0	-	LCD_R1	-	EVENT OUT	
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	-	-	LCD_G4	-	EVENT OUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	-	-	EVENT OUT
	PH6	-	-	-	-	I2C2_SMBA	SPI5_SCK	-	-	-	TIM12_CH1	-	ETH_MII_RXD2	FMC_SDN E1	-	-	-	-	EVENT OUT
	PH7	-	-	-	-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	-	-	EVENT OUT
	PH8	-	-	-	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	-	-	EVENT OUT
	PH9	-	-	-	-	I2C3_SMBA	-	-	-	-	TIM12_CH2	-	-	FMC_D17	DCMI_D0	LCD_R3	-	-	EVENT OUT
	PH10	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	-	-	EVENT OUT
	PH11	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	FMC_D19	DCMI_D2	LCD_R5	-	-	EVENT OUT
	PH12	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	-	-	EVENT OUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	-	-	CAN1_TX	-	FMC_D21	-	LCD_G2	-	-	EVENT OUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	-	-	-	-	FMC_D22	DCMI_D4	LCD_G3	-	-	EVENT OUT
PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	-	-	-	FMC_D23	DCMI_D11	LCD_G4	-	-	EVENT OUT	



Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/2/3	SPI1/2/3/4/5/6	SPI2/3/SAI1	SPI2/3/USART1/2/3	USART6/UART4/5/7/8	CAN1/2/TIM12/13/14/QUADSPI/LCD	QUADSPI/OTG2_HS/OTG1_FS	ETH	FMC/SDIO/OTG2_FS	DCMI/DSI/HOST	LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT OUT
	PI1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	FMC_D25	DCMI_D8	LCD_G6	EVENT OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	FMC_D27	DCMI_D10		EVENT OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	FMC_NBL2	DCMI_D5	LCD_B4	EVENT OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENT OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	FMC_D28	DCMI_D6	LCD_B6	EVENT OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	-	FMC_D29	DCMI_D7	LCD_B7	EVENT OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-		EVENT OUT
	PI9	-	-	-	-	-	-	-	-	-	CAN1_RX	-	FMC_D30	-	LCD_VSYNC	EVENT OUT
	PI10	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RX_ER	FMC_D31	LCD_HSYNC	EVENT OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	EVENT OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENT OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENT OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	LCD_R0	EVENT OUT



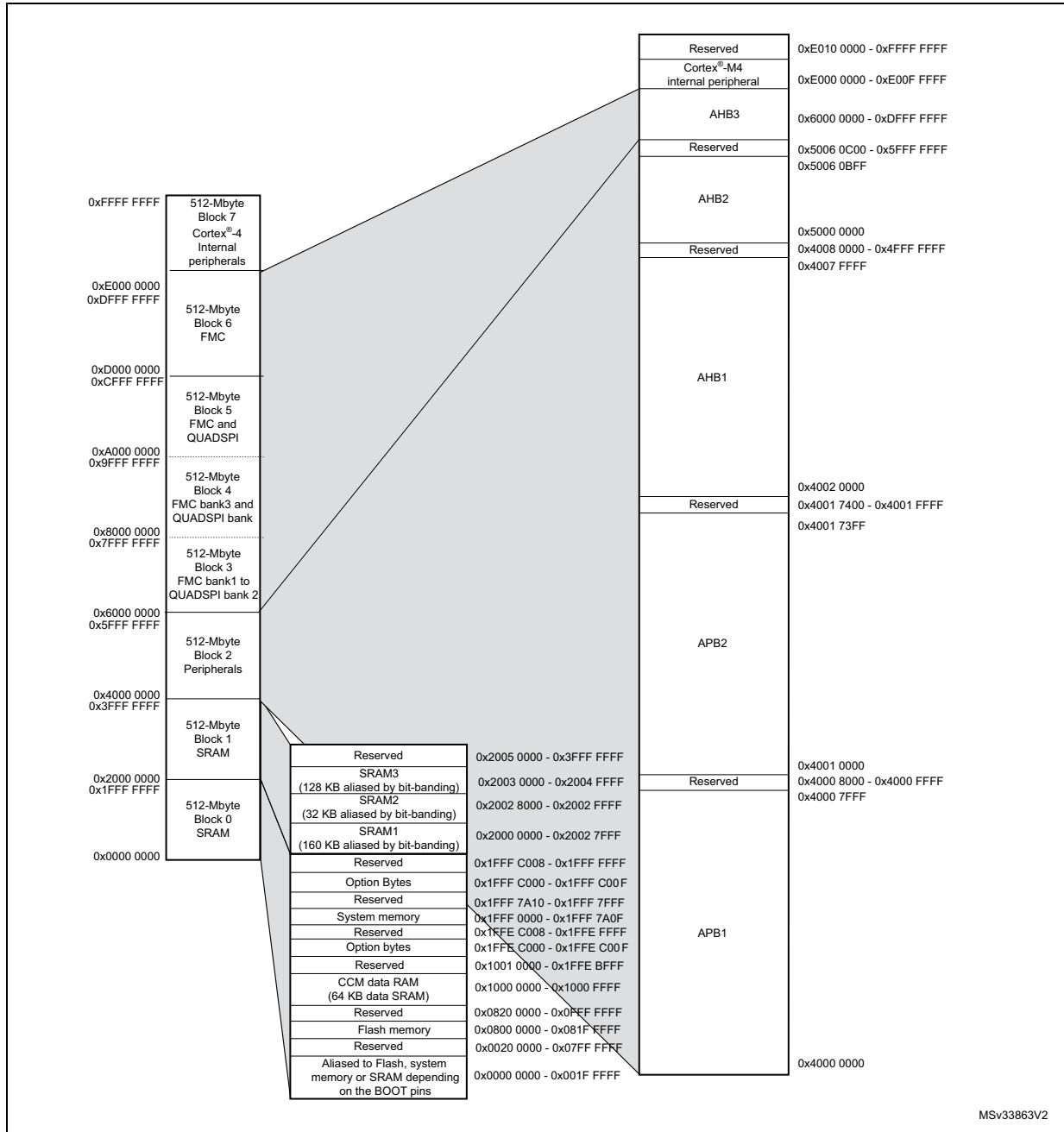
Table 12. Alternate function (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS	TIM1/2	TIM3/4/ 5	TIM8/9/ 10/11	I2C1/2/3	SPI1/2/3 I4/5/6	SPI2/3/ SAI1	SPI2/3/ USART 1/2/3	USAR T6/ UART 4/5/7/ 8	CAN1/2/ TIM12/ 13/14/ QUAD SPI/LCD	QUAD SPI/OT G2_HS /OTG1 _FS	ETH	FMC/ SDIO/ OTG2_ FS	DCMI/ DSI HOST	LCD	SYS
Port J	PJ0	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENT OUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENT OUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	DSIHOST _TE	LCD_R3	EVENT OUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENT OUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENT OUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENT OUT
	PJ12	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENT OUT
	PJ13	-	-	-	-	-	-	-	-	LCD_G4	-	-	-	-	LCD_B1	EVENT OUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENT OUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENT OUT
Port K	PK3	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENT OUT
	PK4	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENT OUT
	PK5	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENT OUT
	PK6	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENT OUT
	PK7	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENT OUT

4 Memory mapping

The memory map is shown in [Figure 21](#).

Figure 21. Memory map



MSV33863V2

Table 13. STM32F479xx register boundary addresses⁽¹⁾

Bus	Boundary address	Peripheral
-	0xE00F FFFF - 0xFFFF FFFF	Reserved
Cortex [®] -M4	0xE000 0000 - 0xE00F FFFF	Cortex [®] -M4 internal peripherals
AHB3	0xD000 0000 - 0xDFFF FFFF	FMC bank 6
	0xC000 0000 - 0xCFFF FFFF	FMC bank 5
	0xA000 1000 - 0xA0001FFF	Quad-SPI control register
	0xA000 2000 - 0xBFFF FFFF	Reserved
	0xA000 0000- 0xA000 0FFF	FMC control register
	0x9000 0000 - 0x9FFF FFFF	Quad-SPI bank
	0x8000 0000 - 0x8FFF FFFF	FMC bank 3
	0x7000 0000 - 0x7FFF FFFF	FMC bank 2 (reserved)
	0x6000 0000 - 0x6FFF FFFF	FMC bank 1
-	0x5006 0C00- 0x5FFF FFFF	Reserved
AHB2	0x5006 0800 - 0x5006 0BFF	RNG
	0x5006 0400 - 0x5006 07FF	HASH
	0x5006 0000 - 0x5006 03FF	CRYP
	0x5005 0400 - 0x5005 FFFF	Reserved
	0x5005 0000 - 0x5005 03FF	DCMI
	0x5004 0000- 0x5004 FFFF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS

Table 13. STM32F479xx register boundary addresses⁽¹⁾ (continued)

Bus	Boundary address	Peripheral
-	0x4008 0000- 0x4FFF FFFF	Reserved
AHB1	0x4004 0000 - 0x4007 FFFF	USB OTG HS
	0x4002 BC00- 0x4003 FFFF	Reserved
	0x4002 B000 - 0x4002 BBFF	Chrom (DMA2D)
	0x4002 9400 - 0x4002 AFFF	Reserved
	0x4002 9000 - 0x4002 93FF	ETHERNET MAC
	0x4002 8C00 - 0x4002 8FFF	
	0x4002 8800 - 0x4002 8BFF	
	0x4002 8400 - 0x4002 87FF	
	0x4002 8000 - 0x4002 83FF	
	0x4002 6800 - 0x4002 7FFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 5FFF	Reserved
	0x4002 4000 - 0x4002 4FFF	BKPSRAM
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2C00 - 0x4002 2FFF	Reserved
	0x4002 2800 - 0x4002 2BFF	GPIOK
	0x4002 2400 - 0x4002 27FF	GPIOJ
	0x4002 2000 - 0x4002 23FF	GPIOI
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GPIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 13. STM32F479xx register boundary addresses⁽¹⁾ (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 7400 - 0x4001 FFFF	Reserved
	0x4001 6C00 - 0x4001 73FF	DSI Host
	0x4001 6800 - 0x4001 6BFF	LCD-TFT
	0x4001 5C00 - 0x4001 67FF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	SPI6
	0x4001 5000 - 0x4001 53FF	SPI5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1 - ADC2 - ADC3
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
0x4001 0000 - 0x4001 03FF	TIM1	

Table 13. STM32F479xx register boundary addresses⁽¹⁾ (continued)

Bus	Boundary address	Peripheral
-	0x4000 8000- 0x4000 FFFF	Reserved
APB1	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	Reserved
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	Reserved
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
0x4000 0400 - 0x4000 07FF	TIM3	
0x4000 0000 - 0x4000 03FF	TIM2	

1. The reserved boundary address are shown in grayed cells

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ °C}$ and $T_A = T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 3.3\text{ V}$ (for the $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\sigma$).

5.1.3 Typical curves

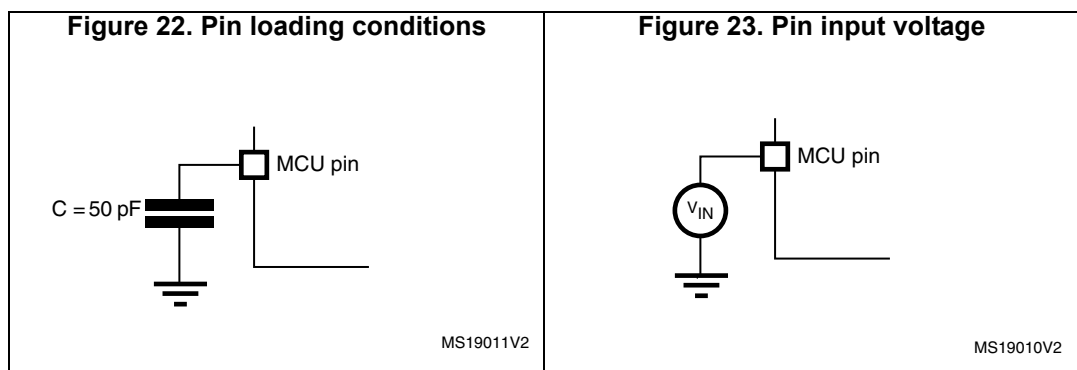
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 22](#).

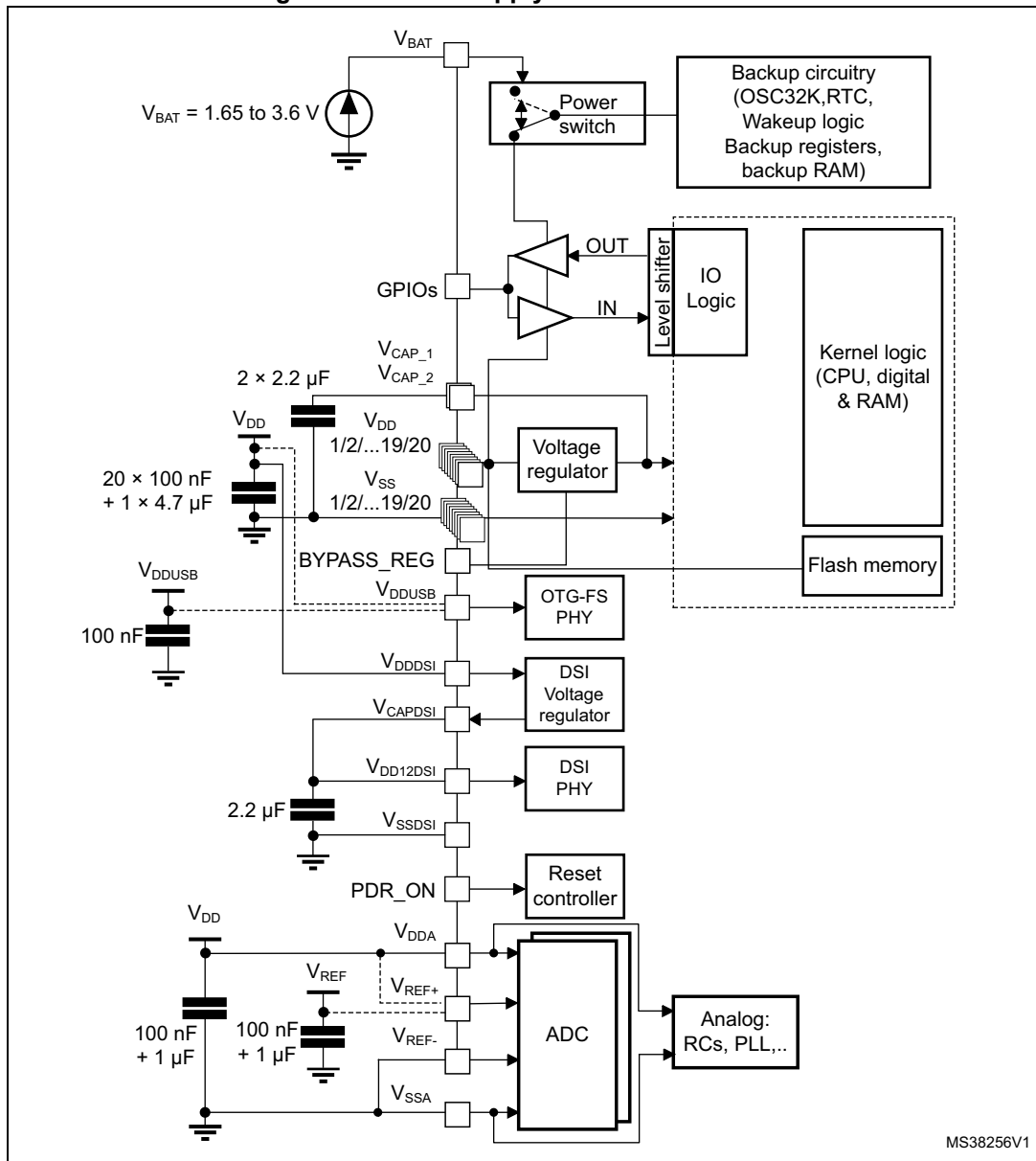
5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 23](#).



5.1.6 Power supply scheme

Figure 24. Power supply scheme

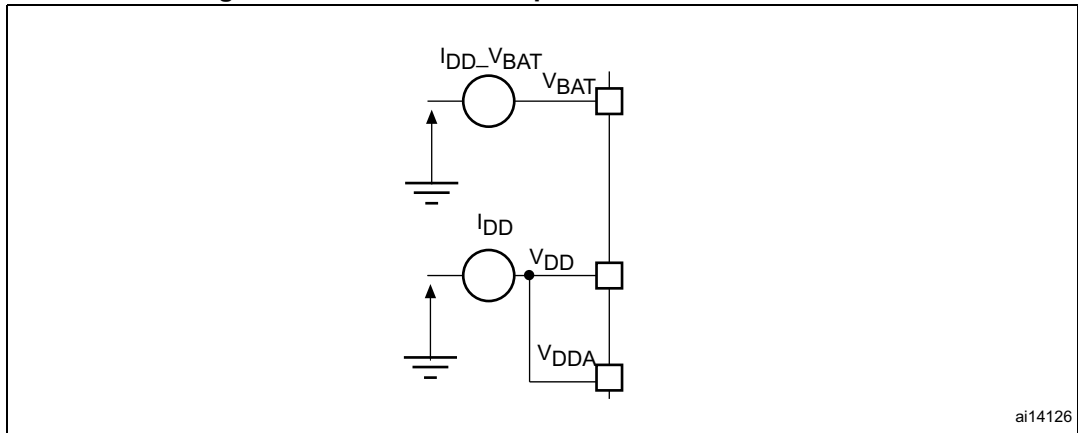


1. To connect BYPASS_REG and PDR_ON pins, refer to [Section 2.19](#) and [Section 2.20](#).
2. The two 2.2 μF ceramic capacitors on V_{CAP_1} and V_{CAP_2} should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 μF ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{D_{DA}} and V_{S_{SA}} must be connected to V_{DD} and V_{SS}, respectively.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{D_{DA}}/V_{S_{SA}} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

5.1.7 Current consumption measurement

Figure 25. Current consumption measurement scheme



ai14126

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 14](#), [Table 15](#), and [Table 16](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD-VSS}	External main supply voltage (including V_{DDA} , V_{DD} , V_{DDUSB} , V_{DDDSI} and V_{BAT}) ⁽¹⁾	- 0.3	4.0	V
V_{IN}	Input voltage on FT pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT pin	V_{SS}	9.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins ⁽³⁾	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 5.3.18		

1. All main power (V_{DD} , V_{DDA} , V_{DDUSB} , V_{DDDSI}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to [Table 15](#) for the values of the maximum allowed injected current.
3. Including V_{REF} pin

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source) ⁽¹⁾	290	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink) ⁽¹⁾	- 290	
ΣI_{VDDUSB}	Total current into V_{DDUSB} power line (source)	25	
I_{VDD}	Maximum current into each V_{DD_x} power line (source) ⁽¹⁾	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink) ⁽¹⁾	- 100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins ⁽²⁾	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	- 120	
$I_{INJ(PIN)}$ ⁽³⁾	Injected current on FT pins ⁽⁴⁾	- 5/+0	
	Injected current on NRST and BOOT0 pins ⁽⁴⁾		
	Injected current on TTa pins ⁽⁵⁾	±5	
$\Sigma I_{INJ(PIN)}$ ⁽⁵⁾	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	±25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in [Section 5.3.24](#).
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 14](#) for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	- 65 to +150	°C
T_J	Maximum junction temperature	125	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit	
f _{HCLK}	Internal AHB clock frequency	Power Scale 3 (VOS[1:0] bits in PWR_CR register = 0x01), Regulator ON, over-drive OFF	0	-	120	MHz	
		Power Scale 2 (VOS[1:0] bits in PWR_CR register = 0x10), Regulator ON	Over-drive OFF	0	-		144
			Over-drive ON		-		168
		Power Scale 1 (VOS[1:0] bits in PWR_CR register= 0x11), Regulator ON	Over-drive OFF	0	-		168
Over-drive ON	-		180				
f _{PCLK1}	Internal APB1 clock frequency	Over-drive OFF	0	-	42		
		Over-drive ON	0	-	45		
f _{PCLK2}	Internal APB2 clock frequency	Over-drive OFF	0	-	84		
		Over-drive ON	0	-	90		
V _{DD}	Standard operating voltage	-	1.7 ⁽²⁾	-	3.6	V	
V _{DDA} ⁽³⁾⁽⁴⁾	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V _{DD} ⁽⁵⁾	1.7 ⁽²⁾	-	2.4		
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6		
V _{DDUSB}	USB supply voltage (supply voltage for PA11, PA12, PB14 and PB15 pins)	USB not used	0	3.3	3.6		
		USB used	3.0	-	3.6		
V _{DDDSI}	DSI system operating voltage	-	1.7 ⁽²⁾	-	3.6		
V _{BAT}	Backup operating voltage	-	1.65	-	3.6		

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
V ₁₂	Regulator ON: 1.2 V internal voltage on V _{CAP_1} /V _{CAP_2} pins	Power Scale 3 ((VOS[1:0] bits in PWR_CR register = 0x01), 120 MHz HCLK max frequency)	1.08	1.14	1.20	V
		Power Scale 2 ((VOS[1:0] bits in PWR_CR register = 0x10), 144 MHz HCLK max frequency with over-drive OFF or 168 MHz with over-drive ON)	1.20	1.26	1.32	
		Power Scale 1 ((VOS[1:0] bits in PWR_CR register = 0x11), 168 MHz HCLK max frequency with over-drive OFF or 180 MHz with over-drive ON)	1.26	1.32	1.40	
	Regulator OFF: 1.2 V external voltage must be supplied from external regulator on V _{CAP_1} /V _{CAP_2} pins ⁽⁶⁾	Max frequency 120 MHz	1.10	1.14	1.20	V
		Max frequency 144 MHz	1.20	1.26	1.32	
		Max frequency 168 MHz	1.26	1.32	1.38	
V _{IN}	Input voltage on RST and FT pins ⁽⁷⁾	2 V ≤ V _{DD} ≤ 3.6 V	- 0.3	-	5.5	V
		V _{DD} ≤ 2 V	- 0.3	-	5.2	
	Input voltage on TTa pins	-	- 0.3	-	V _{DDA} + 0.3	
	Input voltage on BOOT0 pin	-	0	-	9	
P _D	Power dissipation at T _A = 85 °C for suffix 6 or T _A = 105 °C for suffix 7 ⁽⁸⁾	LQFP100	-	-	465	mW
		LQFP144	-	-	500	
		WLCSP168	-	-	645	
		UFBGA169	-	-	385	
		LQFP176	-	-	526	
		UFBGA176	-	-	513	
		LQFP208	-	-	1053	
		TFBGA216	-	-	690	
T _A	Ambient temperature for 6 suffix version	Maximum power dissipation	- 40	-	85	°C
		Low power dissipation ⁽⁹⁾	- 40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	- 40	-	105	
		Low power dissipation ⁽⁹⁾	- 40	-	125	
T _J	Junction temperature range	6 suffix version	- 40	-	105	
		7 suffix version	- 40	-	125	

1. The over-drive mode is not supported at the voltage ranges from 1.7 to 2.1 V.
2. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 2.19.2](#)).
3. When the ADC is used, refer to [Table 76](#).
4. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
5. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
6. The over-drive mode is not supported when the internal regulator is OFF.

7. To sustain a voltage higher than $V_{DD}+0.3$, the internal Pull-up and Pull-Down resistors must be disabled
8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} .
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} .

Table 18. Limitations depending on the operating power supply range

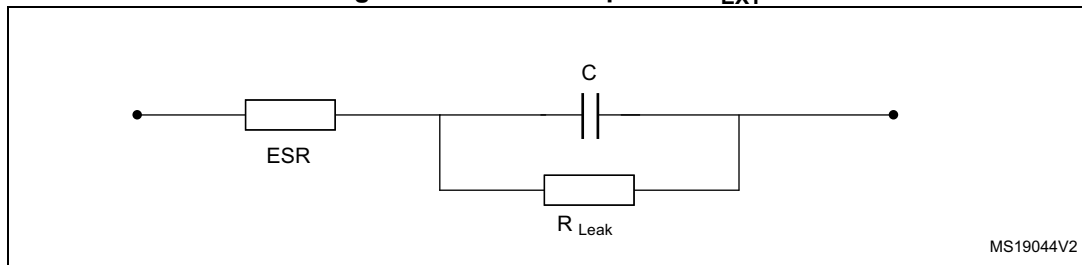
Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum HCLK frequency vs. Flash memory wait states ⁽¹⁾⁽²⁾	I/O operation	Possible Flash memory operations
$V_{DD} = 1.7$ to 2.1 V ⁽³⁾	Conversion time up to 1.2 Msps	20 MHz ⁽⁴⁾	168 MHz with 8 wait states and over-drive OFF	No I/O compensation	8-bit erase and program operations only
$V_{DD} = 2.1$ to 2.4 V		22 MHz	180 MHz with 8 wait states and over-drive ON		16-bit erase and program operations
$V_{DD} = 2.4$ to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	180 MHz with 7 wait states and over-drive ON	I/O compensation works	16-bit erase and program operations
$V_{DD} = 2.7$ to 3.6 V ⁽⁵⁾		30 MHz	180 MHz with 5 wait states and over-drive ON		32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 2.19.2](#)).
4. Prefetch is not available.
5. When V_{DDUSB} is connected to V_{DD} , the voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor C_{EXT} to the VCAP1/VCAP2 pins. C_{EXT} is specified in [Table 19](#).

Figure 26. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 19. VCAP1/VCAP2 operating conditions⁽¹⁾

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	2.2 μ F
ESR	ESR of external capacitor	< 2 Ω

1. When bypassing the voltage regulator, the two 2.2 μ F V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

5.3.3 Operating conditions at power-up / power-down (regulator ON)

Subject to general operating conditions for T_A .

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	μ s/V
	V_{DD} fall time rate	20	∞	

5.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A .

Table 21. Operating conditions at power-up / power-down (regulator OFF)⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	μ s/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

5.3.5 Reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 22. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	2.92	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
V _{PVDhyst} ⁽¹⁾	PVD hysteresis	-	-	100	-	mV
V _{POR/PDR}	Power-on/power-down reset threshold	Falling edge	1.60	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	
V _{PDRhyst} ⁽¹⁾	PDR hysteresis	-	-	40	-	mV
V _{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V _{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	V
		Rising edge	2.53	2.59	2.63	
V _{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	V
		Rising edge	2.85	2.92	2.97	
V _{BORhyst} ⁽¹⁾	BOR hysteresis	-	-	100	-	mV
T _{RSTTEMPO} ⁽¹⁾⁽²⁾	POR reset temporization	-	0.5	1.5	3.0	ms
I _{RUSH} ⁽¹⁾	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
E _{RUSH} ⁽¹⁾	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V _{DD} = 1.7 V, T _A = 105 °C, I _{RUSH} = 171 mA for 31 μs	-	-	5.4	μC

1. Guaranteed by design.

2. The reset temporization is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is read by the user application code.

5.3.6 Over-drive switching characteristics

When the over-drive mode switches from enabled to disabled or disabled to enabled, the system clock is stalled during the internal voltage set-up.

The over-drive switching characteristics are given in [Table 23](#). They are subject to general operating conditions for T_A .

Table 23. Over-drive switching characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{od_swen}	Over_drive switch enable time	HSI	-	45	-	μs
		HSE max for 4 MHz and min for 26 MHz	45	-	100	
		External HSE 50 MHz	-	40	-	
T_{od_swdis}	Over_drive switch disable time	HSI	-	20	-	
		HSE max for 4 MHz and min for 26 MHz.	20	-	80	
		External HSE 50 MHz	-	15	-	

1. Guaranteed by design.

5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 25](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark[®] code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to f_{HCLK} frequency and V_{DD} range (see [Table 18: Limitations depending on the operating power supply range](#)).
- When the regulator is OFF, the V_{12} is provided externally, as described in [Table 17: General operating conditions](#).
- The voltage scaling and over-drive mode are adjusted to f_{HCLK} frequency as follows:
 - Scale 3 for $f_{HCLK} \leq 120$ MHz
 - Scale 2 for $120 \text{ MHz} < f_{HCLK} \leq 144$ MHz
 - Scale 1 for $144 \text{ MHz} < f_{HCLK} \leq 180$ MHz. The over-drive is only ON at 180 MHz.
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when f_{HCLK} is higher than 25 MHz.
- The typical current consumption values are obtained for $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ voltage range and for ambient temperature $T_A = 25 \text{ }^\circ\text{C}$ unless otherwise specified.
- The maximum values are obtained for $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$ voltage range and a maximum ambient temperature (T_A), unless otherwise specified.
- For the voltage range $1.7 \text{ V} \leq V_{DD} \leq 2.1 \text{ V}$ the maximum frequency is 168 MHz.

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch) or RAM, regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in RUN mode	All Peripherals enabled ⁽²⁾⁽³⁾	180	103	109 ⁽⁴⁾	142	175 ⁽⁴⁾	mA
			168	94	99	124	149	
			150	84	89	114	140	
			144	77	81	104	127	
			120	57	60	79	98	
			90	43	46	64	84	
			60	30	33	51	70	
			30	16	19	37	57	
			25	14	16	34	54	
			16	7	10	28	48	
			8	4	7	26	46	
			4	3	6	24	44	
		2	3	5	23	43		
		All Peripherals disabled ⁽²⁾	180	50	56 ⁽⁴⁾	89	124 ⁽⁴⁾	
			168	45	51	75	102	
			150	41	46	70	97	
			144	37	42	63	88	
			120	28	31	49	69	
			90	21	24	42	63	
			60	15	17	36	56	
			30	9	11	29	49	
			25	7	10	28	48	
			16	4	7	25	45	
			8	3	6	22	44	
4	3		5	23	43			
2	2	5	23	43				

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. Guaranteed by test in production.

Table 25. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator disabled), regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾			Unit
					T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in RUN mode	All Peripherals enabled ⁽²⁾⁽³⁾	168	97	102	128	154	mA
			150	87	92	118	143	
			144	80	84	108	131	
			120	65	68	88	108	
			90	51	54	73	93	
			60	37	41	59	79	
			30	21	23	42	62	
		25	18	20	39	59		
		All Peripherals disabled	168	49	55	79	105	
			150	44	49	44	100	
			144	40	45	68	92	
			120	36	39	58	78	
			90	29	32	51	71	
			60	22	25	44	64	
30	13		15	34	54			
25	11	13	32	52				

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Table 26. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled except prefetch), regulator OFF

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ		Max ⁽¹⁾						Unit
				I _{DD12}	I _{DD}	T _A = 25 °C		T _A = 85 °C		T _A = 105 °C		
						I _{DD12}	I _{DD}	I _{DD12}	I _{DD}	I _{DD12}	I _{DD}	
I _{DD12} / I _{DD}	Supply current in RUN mode from V ₁₂ and V _{DD} supply	All Peripherals enabled ^{(2) (3)}	168	93	1	98	1	123	1	148	1	mA
			150	83	1	88	1	113	1	138	1	
			144	76	1	80	1	103	1	126	1	
			120	56	1	59	1	78	1	97	1	
			90	43	1	45	1	64	1	83	1	
			60	29	1	32	1	50	1	70	1	
			30	15	1	18	1	36	1	56	1	
		25	13	1	15	1	34	1	53	1		
		All Peripherals disabled	168	44	1	50	1	72	1	94	1	
			150	40	1	45	1	68	1	90	1	
			144	36	1	40	1	62	1	82	1	
			120	27	1	30	1	48	1	66	1	
			90	20	1	23	1	41	1	60	1	
			60	14	1	16	1	35	1	53	1	
30	8		1	10	1	28	1	47	1			
25	7	1	9	1	27	1	46	1				

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, DSI regulator, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

Table 27. Typical and maximum current consumption in Sleep mode, regulator ON

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾⁽²⁾⁽³⁾			Unit
					T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD}	Supply current in Sleep mode	All Peripherals enabled	180	78	88 ⁽⁴⁾	118	151 ⁽⁴⁾	mA
			168	71	76	101	127	
			150	64	71	94	119	
			144	58	62	85	109	
			120	43	46	65	85	
			90	33	37	54	74	
			60	23	25	44	63	
			30	13	15	34	53	
			25	11	13	32	52	
			16	5	8	27	47	
			8	4	7	25	45	
			4	3	5	24	44	
		2	2	5	23	43		
		All Peripherals disabled	180	23	29 ⁽⁴⁾	63	96 ⁽⁴⁾	
			168	21	25	50	76	
			150	19	23	48	74	
			144	17	31	43	67	
			120	13	16	34	54	
			90	10	13	31	51	
			60	7	10	28	48	
			30	5	7	25	45	
			25	4	7	25	45	
			16	2	5	23	43	
			8	2	5	23	43	
4	2		5	23	43			
2	2	4	23	42				

1. Guaranteed based on test during characterization.
2. When analog peripheral blocks such as ADCs, DACs, HSE, LSE, HSI, or LSI are ON, an additional power consumption should be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.
4. Guaranteed by test in production.

Table 28. Typical and maximum current consumption in Sleep mode, regulator OFF

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ		Max ⁽¹⁾						Unit
				I _{DD12}	I _{DD}	T _A = 25 °C		T _A = 85 °C		T _A = 105 °C		
						I _{DD12}	I _{DD}	I _{DD12}	I _{DD}	I _{DD12}	I _{DD}	
I _{DD12} / I _{DD}	Supply current in RUN mode from V ₁₂ and V _{DD} supply	All Peripherals enabled	168	70	1	75	1	100	1	126	1	mA
			150	63	1	70	1	93	1	118	1	
			144	57	1	61	1	84	1	108	1	
			120	42	1	45	1	64	1	84	1	
			90	32	1	36	1	53	1	73	1	
			60	22	1	24	1	43	1	63	1	
			30	12	1	14	1	33	1	53	1	
		25	10	1	12	1	31	1	51	1		
		All Peripherals disabled	168	20	1	24	1	49	1	75	1	
			150	18	1	22	1	47	1	73	1	
			144	16	1	19	1	42	1	66	1	
			120	12	1	14	1	33	1	53	1	
			90	10	1	12	1	30	1	50	1	
			60	7	1	9	1	27	1	47	1	
30	4		1	6	1	24	1	44	1			
25	4	1	6	1	24	1	44	1				

1. Guaranteed based on test during characterization.

Table 29. Typical and maximum current consumption in Stop mode

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾			Unit
				T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD_STOP_NM} (normal mode)	Supply current in Stop mode with voltage regulator in main regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.63	3	17	33	mA
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.58	3	17	33	
	Supply current in Stop mode with voltage regulator in Low Power regulator mode	Flash memory in Stop mode, all oscillators OFF, no independent watchdog	0.50	2	15	28	
		Flash memory in Deep power down mode, all oscillators OFF, no independent watchdog	0.44	2	15	28	
I _{DD_STOP_UDM} (under-drive mode)	Supply current in Stop mode with voltage regulator in main regulator and under-drive mode	Flash memory in Deep power down mode, main regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.21	1	6	12	
	Supply current in Stop mode with voltage regulator in Low Power regulator and under-drive mode	Flash memory in Deep power down mode, Low Power regulator in under-drive mode, all oscillators OFF, no independent watchdog	0.14	1	6	13	

1. Data based on characterization, tested in production.

Table 30. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions	Typ ⁽¹⁾			Max ⁽²⁾			Unit
			T _A = 25 °C			T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
			V _{DD} = 1.7 V	V _{DD} = 2.4 V	V _{DD} = 3.3 V	V _{DD} = 3.3 V			
I _{DD_STBY}	Supply current in Standby mode	Backup SRAM ON, RTC and LSE oscillator OFF	1.7	2.5	2.9	6 ⁽³⁾	18	35 ⁽³⁾	µA
		Backup SRAM OFF, RTC and LSE oscillator OFF	1.0	1.8	2.20	5 ⁽³⁾	15	30 ⁽³⁾	
		Backup SRAM OFF, RTC ON and LSE oscillator in Power Drive mode	1.7	2.7	3.2	7	20	39	
		Backup SRAM ON, RTC ON and LSE oscillator in Power Drive mode	2.4	3.4	4.0	8	25	48	
		Backup SRAM ON, RTC ON and LSE oscillator in High Drive mode	3.2	4.2	4.8	10	29	57	
		Backup SRAM OFF, RTC ON and LSE oscillator in High Drive mode	2.5	3.5	4.1	8	25	48	

1. PDR is off for V_{DD}=1.7 V. When the PDR is OFF (internal reset OFF), the typical current consumption is reduced by additional 1.2 µA
2. Based on characterization, not tested in production unless otherwise specified.
3. Based on characterization, tested in production.

Table 31. Typical and maximum current consumption in V_{BAT} mode

Symbol	Parameter	Conditions ⁽¹⁾	Typ			Max ⁽²⁾			Unit
			T _A = 25 °C			T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
			V _{BAT} = 1.7 V	V _{BAT} = 2.4 V	V _{BAT} = 3.3 V	V _{BAT} = 3.3 V			
I _{DD_VBAT}	Backup domain supply current	Backup SRAM ON, RTC ON and LSE oscillator in Low Power mode	1.431	1.577	1.825	1.9	12.0	24.0	µA
		Backup SRAM OFF, RTC ON and LSE oscillator in Low Power mode	0.720	0.849	1.060	1.1	7.0	13.9	
		Backup SRAM ON, RTC ON and LSE oscillator in High Drive mode	2.212	2.368	2.630	2.80	17.3	34.6	
		Backup SRAM OFF, RTC ON and LSE oscillator in High Drive mode	1.499	1.637	1.862	2.0	12.3	24.5	
		Backup SRAM ON, RTC and LSE OFF	0.710	0.720	0.760	0.8 ⁽³⁾	5.0	10.0 ⁽³⁾	
		Backup SRAM OFF, RTC and LSE OFF	0.018	0.020	0.024	0.2 ⁽³⁾	2.0	4.0 ⁽³⁾	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Based on characterization, tested in production.
3. Based on test during characterization.

Figure 27. Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in Low drive mode)

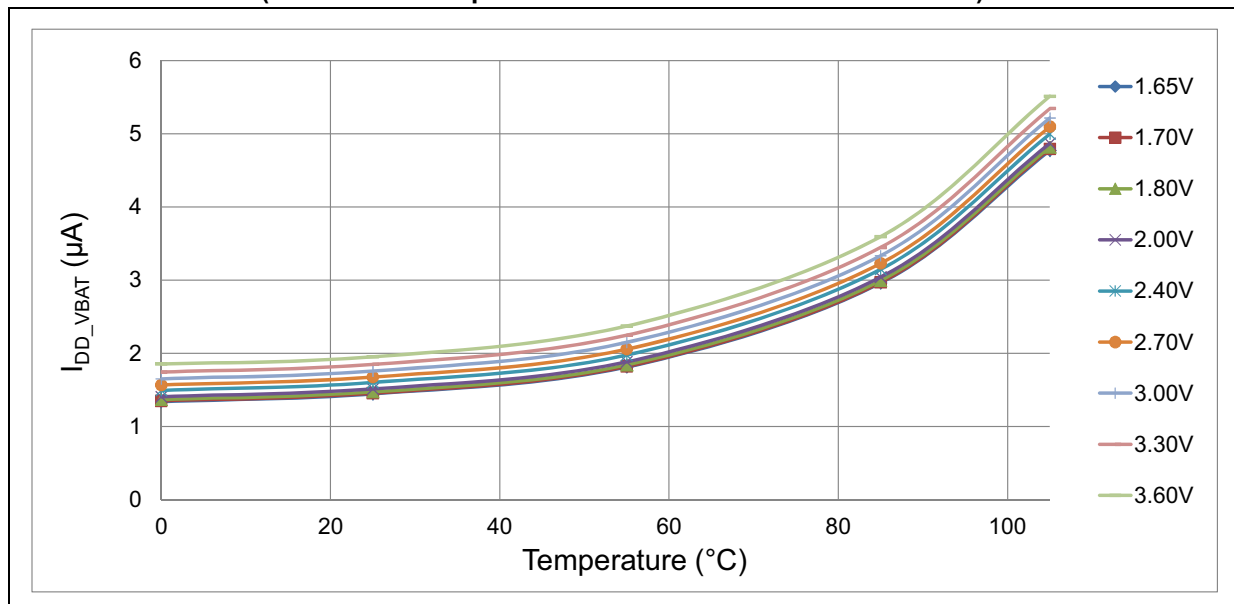
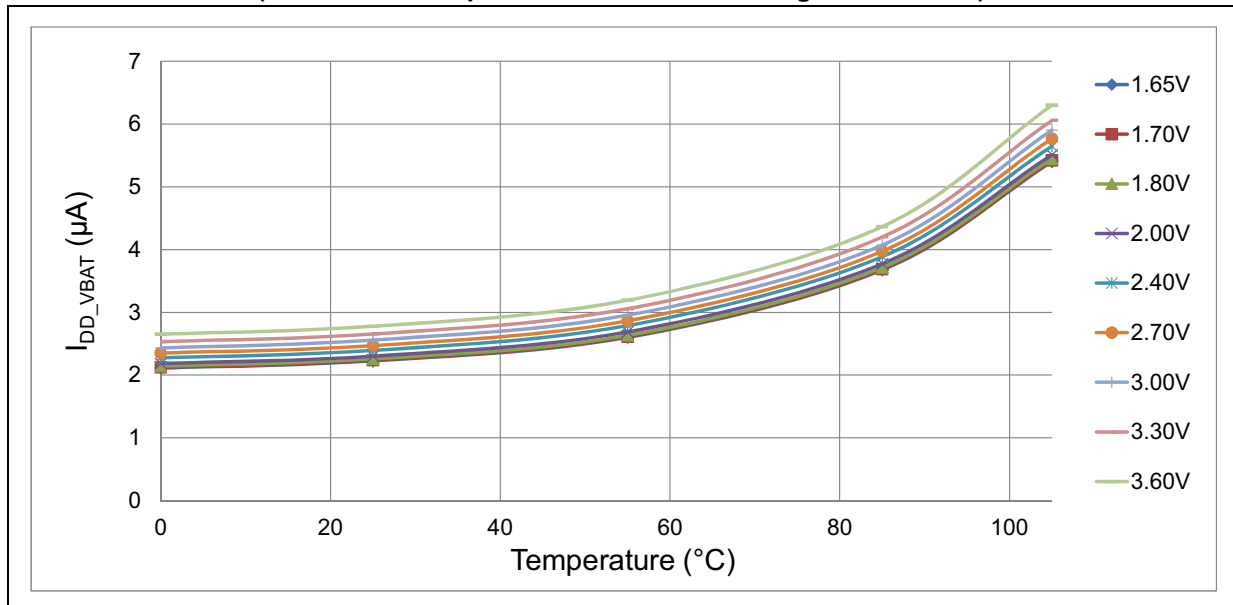


Figure 28. Typical V_{BAT} current consumption (RTC ON / backup SRAM ON and LSE in High drive mode)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 58: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 33](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses

the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 32. Switching output I/O current consumption⁽¹⁾

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit
I _{DDIO}	I/O switching Current	V _{DD} = 3.3 V C = C _{INT} ⁽²⁾	2 MHz	0.0	mA
			8 MHz	0.2	
			25 MHz	0.6	
			50 MHz	1.1	
			60 MHz	1.3	
			84 MHz	1.8	
			90 MHz	1.9	
		V _{DD} = 3.3 V C _{EXT} = 0 pF C = C _{INT} + C _{EXT} + C _S	2 MHz	0.1	
			8 MHz	0.4	
			25 MHz	1.23	
			50 MHz	2.43	
			60 MHz	2.93	
			84 MHz	3.86	
			90 MHz	4.07	

Table 32. Switching output I/O current consumption⁽¹⁾ (continued)

Symbol	Parameter	Conditions	I/O toggling frequency (fsw)	Typ	Unit			
I _{DDIO}	I/O switching Current	$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 10\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.18	mA			
			8 MHz	0.67				
			25 MHz	2.09				
			50 MHz	3.6				
			60 MHz	4.5				
			84 MHz	7.8				
		90 MHz	9.8					
		$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 22\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.26				
			8 MHz	1.01				
			25 MHz	3.14				
			50 MHz	6.39				
		$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 33\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	60 MHz	10.68				
			2 MHz	0.33				
			8 MHz	1.29				
			25 MHz	4.23				
						50 MHz	11.02	

1. C_S is the PCB board capacitance including the pad pin. C_S = 7 pF (estimated value).
2. This test is performed by cutting the LQFP176 package pin (pad removal).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- I/O compensation cell enabled.
- The ART accelerator is ON.
- Scale 1 mode selected, internal digital voltage V12 = 1.32 V.
- HCLK is the system clock. f_{PCLK1} = f_{HCLK}/4, and f_{PCLK2} = f_{HCLK}/2.
 The given value is calculated by measuring the difference of current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
 - f_{HCLK} = 180 MHz (Scale1 + over-drive ON), f_{HCLK} = 144 MHz (Scale 2), f_{HCLK} = 120 MHz (Scale 3)
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 33. Peripheral current consumption

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
AHB1 (up to 180 MHz)	GPIOA	3.16	3.00	2.58	μA/MHz
	GPIOB	2.67	2.62	2.25	
	GPIOC	2.42	2.31	2.10	
	GPIOD	2.22	2.10	1.79	
	GPIOE	2.60	2.48	2.23	
	GPIOF	2.39	2.27	2.08	
	GPIOG	2.27	2.13	1.98	
	GPIOH	2.34	2.20	2.02	
	GPIOI	2.52	2.37	2.17	
	GPIOJ	2.16	2.03	1.86	
	GPIOK	2.20	2.06	1.89	
	OTG_HS+ULPI	36.49	33.89	29.90	
	CRC	0.62	0.55	0.50	
	BKPSRAM	0.83	0.74	0.63	
	DMA1 ⁽²⁾	3.3 x N + 6.8	3 x N + 6.3	2.7 x N + 5.5	
	DMA2 ⁽²⁾	3.4 x N + 5.7	3.1 x N + 5.3	2.8 x N + 4.6	
DMA2D	33.33	30.66	26.98		
ETH_MAC ETH_MAC_TX ETH_MAC_RX ETH_MAC_PTP	22.30	20.69	18.19		
AHB2 (up to 180 MHz)	USB_OTG_FS	34.33	31.96	28.35	μA/MHz
	DVCM1	3.61	3.35	2.98	
	RNG	1.94	1.82	1.61	
	CRYP	2.42	2.24	2.00	
	HASH	4.14	3.80	3.35	
AHB3 (up to 180 MHz)	QUADSPI	16.83	15.57	13.83	μA/MHz
	FMC	17.22	15.92	14.00	
Bus matrix ⁽³⁾		12.17	11.19	9.97	μA/MHz

Table 33. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
APB1 (up to 45 MHz)	TIM2	19.11	17.56	15.33	μA/MHz
	TIM3	15.62	14.22	12.17	
	TIM4	16.22	14.64	12.83	
	TIM5	18.44	16.72	14.00	
	TIM6	3.18	2.69	2.17	
	TIM7	3.11	2.56	2.00	
	TIM12	8.67	7.56	6.50	
	TIM13	6.11	5.33	4.43	
	TIM14	6.44	5.61	4.67	
	PWR	17.44	15.61	13.53	
	USART2	5.44	4.64	3.93	
	USART3	5.51	4.72	4.00	
	UART4	5.22	4.64	3.83	
	UART5	5.33	4.64	3.83	
	UART7	5.56	4.78	4.10	
	UART8	5.24	4.64	3.93	
	I2C1	4.78	4.08	3.43	
	I2C2	5.11	4.50	3.73	
	I2C3	4.78	4.08	3.43	
	SPI2/I2S2 ⁽⁴⁾	4.11	3.53	3.00	
	SPI3/I2S3 ⁽⁴⁾	4.33	3.67	3.17	
	CAN1	8.89	7.83	6.87	
	CAN2	7.22	6.44	5.50	
DAC ⁽⁵⁾	2.89	2.69	2.40		
WWDG	1.73	1.44	1.00		

Table 33. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ) ⁽¹⁾			Unit
		Scale 1	Scale 2	Scale 3	
APB2 (up to 90 MHz)	SDIO	7.94	7.18	6.37	μA/MHz
	TIM1	19.44	17.81	15.80	
	TIM8	19.44	17.81	15.80	
	TIM9	8.44	7.60	6.77	
	TIM10	5.67	5.03	4.50	
	TIM11	5.72	5.10	4.55	
	ADC1 ⁽⁶⁾	5.06	4.54	4.05	
	ADC2 ⁽⁶⁾	5.00	4.47	3.97	
	ADC3 ⁽⁶⁾	5.26	4.75	4.17	
	USART1	4.83	4.33	3.83	
	USART6	4.83	4.33	3.83	
	SPI1	2.11	1.76	1.60	
	SPI4	2.11	1.69	1.60	
	SPI5	2.11	1.76	1.60	
	SPI6	2.11	1.76	1.60	
	SYSCFG	1.72	1.35	1.22	
	LTDC	37.61	34.53	30.60	
	SAI1	3.44	3.01	2.72	
DSI	32.98	30.32	26.87		

1. When the I/O compensation cell is ON, I_{DD} typical value increases by 0.22 mA.
2. DMA1/DMA2 current consumption is calculated by the equation. N: is the number of streams enabled, N= [1..8]
3. The BusMatrix is automatically active when at least one master is ON.
4. To enable an I2S peripheral, first set the I2SMOD bit and then the I2SE bit in the SPI_I2SCFGR register.
5. When the DAC is ON and EN1/2 bits are set in DAC_CR register, add an additional power consumption of 0.8 mA per DAC channel for the analog part.
6. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA per ADC for the analog part.

5.3.8 Wakeup time from low-power modes

The wakeup times given in [Table 34](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}=3.3$ V.

Table 34. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}^{(2)}$	Wakeup from Sleep	-	5	6	CPU clock cycles
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in normal mode	Main regulator is ON	12.9	15.0	μ s
		Main regulator is ON and Flash memory in Deep power down mode	105	120	
		Low power regulator is ON	22	28	
		Low power regulator is ON and Flash memory in Deep power down mode	114	130	
$t_{WUSTOP}^{(2)}$	Wakeup from Stop mode with MR/LP regulator in Under-drive mode	Main regulator in under-drive mode (Flash memory in Deep power-down mode)	107	114	
		Low power regulator in under-drive mode (Flash memory in Deep power-down mode)	115	121	
$t_{WUSTDBY}^{(2)(3)}$	Wakeup from Standby mode	-	318	371	

1. Based on test during characterization.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first
3. $t_{WUSTDBY}$ maximum value is given at -40 °C.

5.3.9 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 58](#). However, the recommended clock input waveform is shown in [Figure 29](#).

The characteristics given in [Table 35](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

Table 35. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{HSE_ext}}$	External user clock source frequency ⁽¹⁾		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{\text{DD}}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{\text{DD}}$	
$t_{\text{w(HSE)}}$ $t_{\text{w(HSE)}}$	OSC_IN high or low time ⁽¹⁾		5	-	-	ns
$t_{\text{r(HSE)}}$ $t_{\text{f(HSE)}}$	OSC_IN rise or fall time ⁽¹⁾		-	-	10	
$C_{\text{in(HSE)}}$	OSC_IN input capacitance ⁽¹⁾	-	-	5	-	pF
DuCy(HSE)	Duty cycle	-	45	-	55	%
I_{L}	OSC_IN Input leakage current	$V_{\text{SS}} \leq V_{\text{IN}} \leq V_{\text{DD}}$	-	-	± 1	μA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 58: I/O static characteristics](#). However, the recommended clock input waveform is shown in [Figure 30](#).

The characteristics given in [Table 36](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

Table 36. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{LSE_ext}}$	User External clock source frequency ⁽¹⁾		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{\text{DD}}$	-	V_{DD}	
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{\text{DD}}$	
$t_{\text{w(LSE)}}$ $t_{\text{f(LSE)}}$	OSC32_IN high or low time ⁽¹⁾		450	-	-	ns
$t_{\text{r(LSE)}}$ $t_{\text{f(LSE)}}$	OSC32_IN rise or fall time ⁽¹⁾		-	-	50	

Table 36. Low-speed external user clock characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{in(LSE)}$	OSC32_IN input capacitance ⁽¹⁾	-	-	5	-	pF
DuCy _(LSE)	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 29. High-speed external clock source AC timing diagram

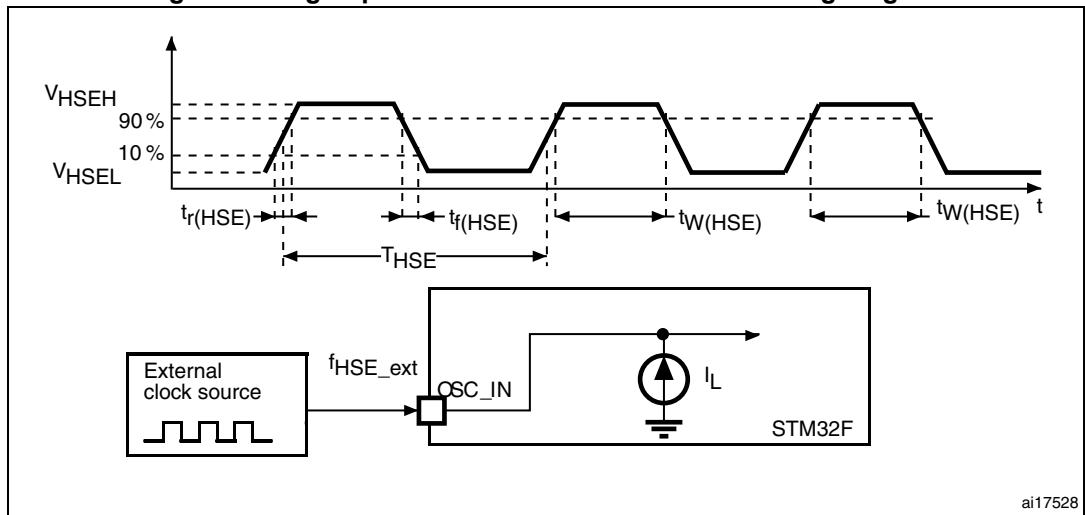
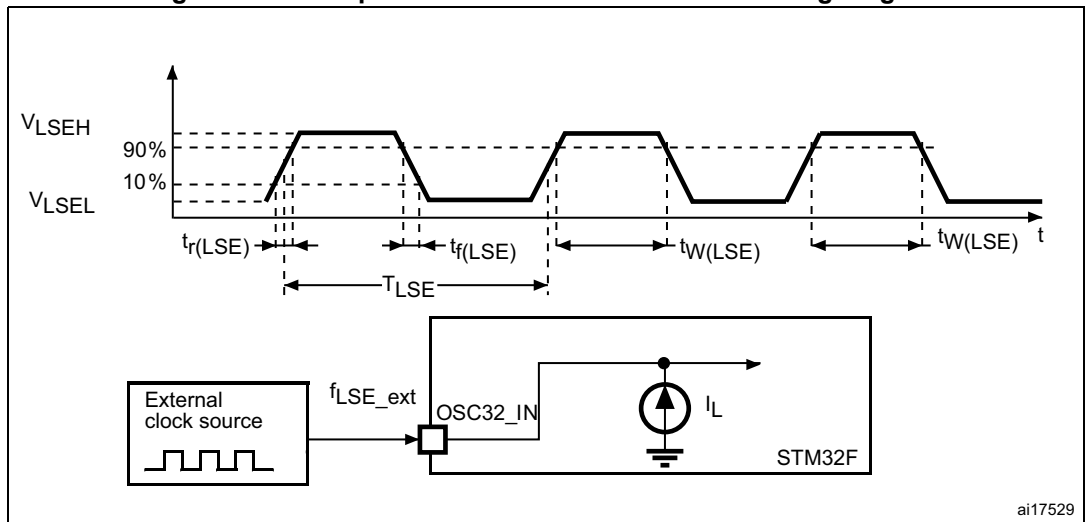


Figure 30. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 37](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. HSE 4-26 MHz oscillator characteristics (1)

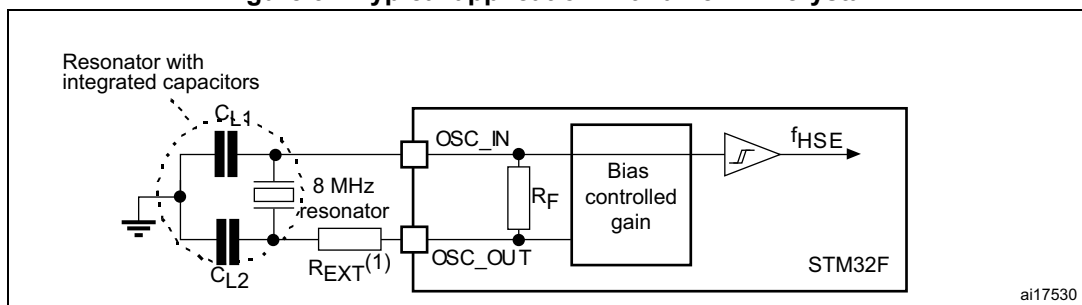
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	26	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
I_{DD}	HSE current consumption	$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=5\text{ pF}@25\text{ MHz}$	-	450	-	μA
		$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=10\text{ pF}@25\text{ MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy	-	- 500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 31](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from www.st.com.

Figure 31. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the informations given in this paragraph are based on characterization results obtained with typical external components specified in [Table 38](#).

In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

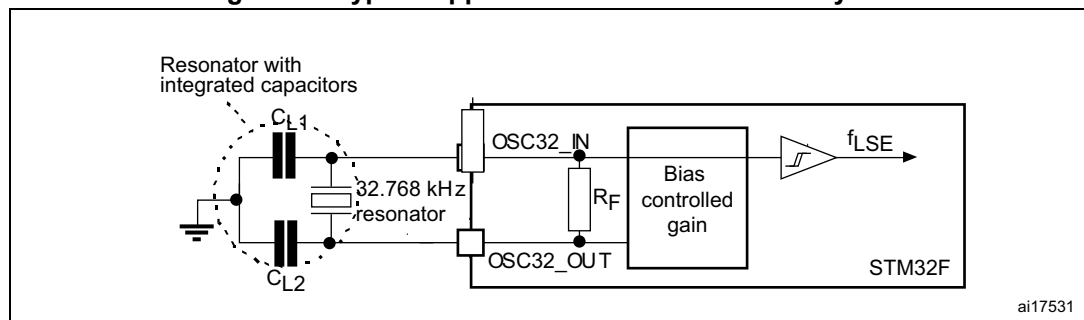
Table 38. LSE oscillator characteristics ($f_{LSE} = 32.768 \text{ kHz}$)⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	M Ω
I_{DD}	LSE current consumption	Low power mode ⁽²⁾	-	-	1	μA
		High drive mode ⁽²⁾	-	-	3	
ACC_{LSE} ⁽³⁾	LSE accuracy	-	- 500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Low power mode ⁽²⁾	-	-	0.56	$\mu\text{A/V}$
		High drive mode ⁽²⁾	-	-	1.5	
$t_{SU(LSE)}$ ⁽⁴⁾	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. LSE mode cannot be changed "on the fly" otherwise, a glitch can be generated on OSCIN pin.
3. This parameter depends on the crystal used in the application. Refer to application note AN2867.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is based on characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from www.st.com.

Figure 32. Typical application with a 32.768 kHz crystal



5.3.10 Internal clock source characteristics

The parameters given in [Table 39](#) and [Table 40](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

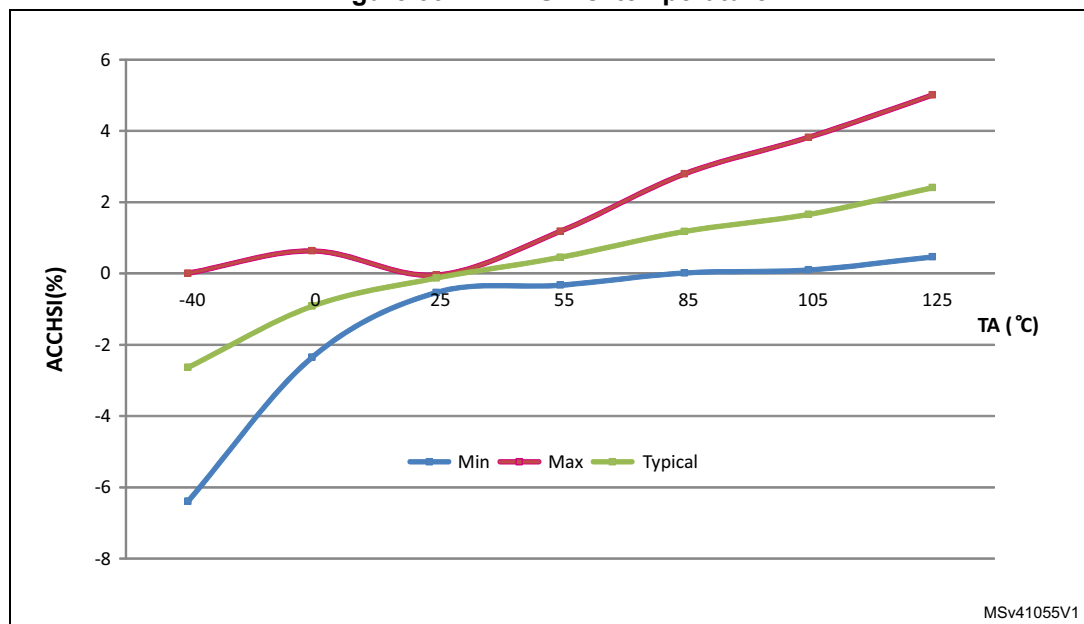
High-speed internal (HSI) RC oscillator

Table 39. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step ⁽²⁾	-	-	-	1	%
	HSI oscillator accuracy	$T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}^{(3)}$	- 8	-	4.5	%
		$T_A = -10 \text{ to } 85 \text{ }^\circ\text{C}^{(3)}$	- 4	-	4	%
	HSI oscillator accuracy	$T_A = 25 \text{ }^\circ\text{C}^{(4)}$	- 1	-	1	%
$t_{su(HSI)}^{(2)}$	HSI oscillator startup time	-	-	2.2	4	μs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	60	80	μA

- $V_{DD} = 3.3 \text{ V}$, $T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$ unless otherwise specified.
- Guaranteed by design
- Based on test during characterization.
- Factory calibrated, parts not soldered.

Figure 33. ACCHSI vs. temperature



- Based on test during characterization.