# 2X36 W digital dimmable ballast with L6574 and ST7FDALI

## Introduction

This document describes a high-efficiency, high power factor, low THD and digital dimming electronic ballast designed to drive 2X36 W T8 tube lamps.

The system consists of three main blocks:

The high-frequency ballast includes an active power factor correction circuit based on the L6562 for universal input voltage as well as a ballast control circuit based on the L6574. The digital dimming is performed by interfacing the ST7FDALI microcontroller with the analog half-bridge driver.

The DALI control unit is dedicated to address the slaves, to display the lamp status and to send the dimming commands. This unit is provided with a keyboard which allows setting different dimming scenes over a wide range (5-100%) as well as putting in standby and restarting the ballast. The DALI communication protocol includes single and group mode, as well as broadcast mode to address the slaves.

The AC-DC adapter is based on the VIPer12A-E. This is an offline double-output isolated power supply in DCM flyback configuration. The outputs are set for 20 V to supply the communication bus and for 5 V to supply the MASTER microcontroller.

The three blocks are described in detail and their performances are shown. In addition some of DALI basics are explained.

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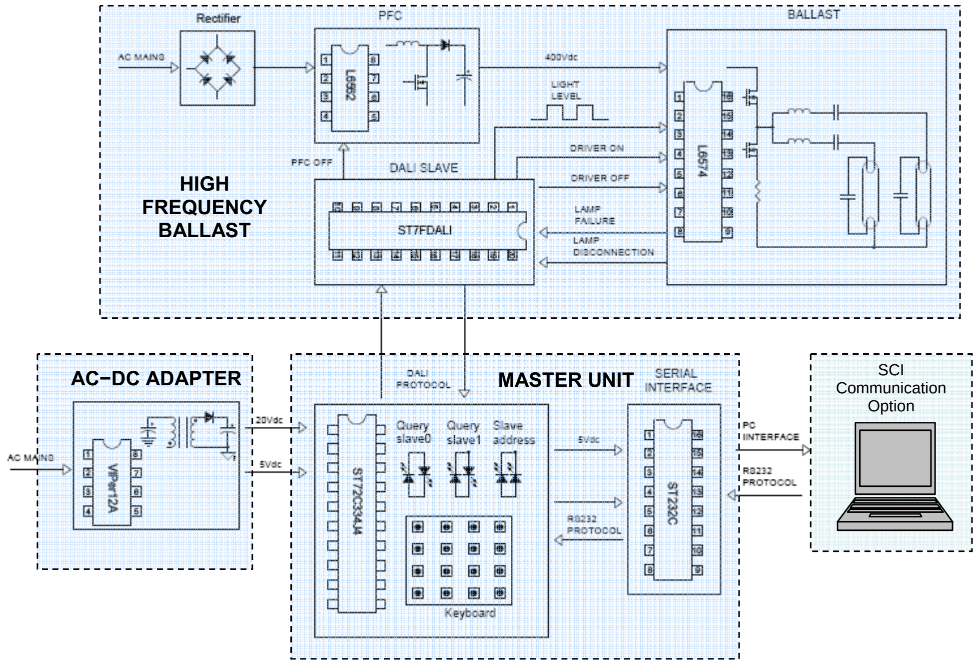
# 1 Block diagram and system operating conditions

*Figure 1* shows the block diagram of the system.

**Figure 1. System block diagram**




SCI communication is considered as an option.

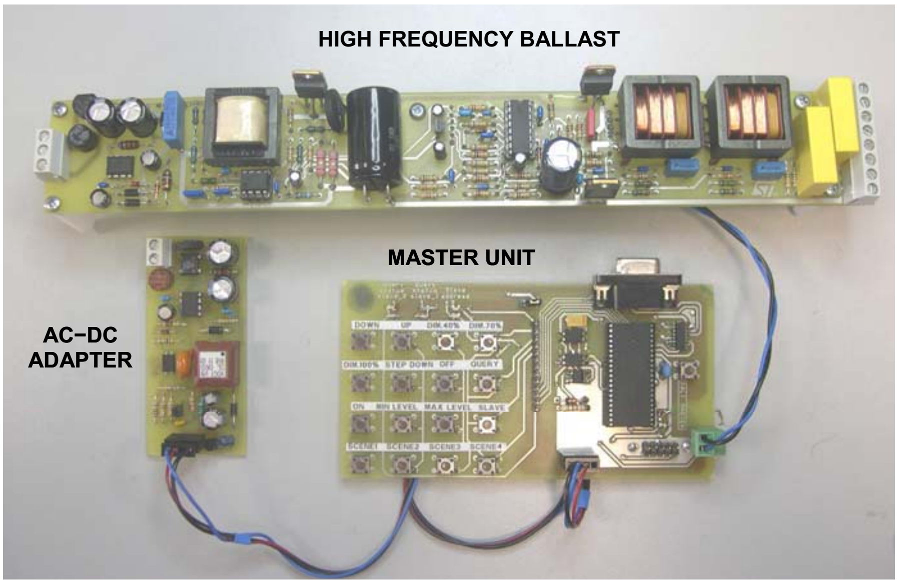
The present system has been designed according to the following specifications:

**Table 1. System operating conditions**

| Parameter | Value |
|---|---|
| Input voltage range | 176-265 Vac/50 Hz; 90-140 Vac/60 Hz |
| Lamp type | 2X36 W T8 tube lamps |
| Circuit power (max) | 80 W |
| Lamp power (max) | 72 W |
| Dimming range | 5% to 100% |
| Power factor | > 0.99 |
| Current THD | < 10% |
| Warm start | < 1.5 sec |
| Standby mode power | < 0. 6 W |

In addition to the previous specs, the DALI communications are optically isolated, the digital dimming is performed with high precision, and the lamp filament preheating time is programmable as well as the ignition time.

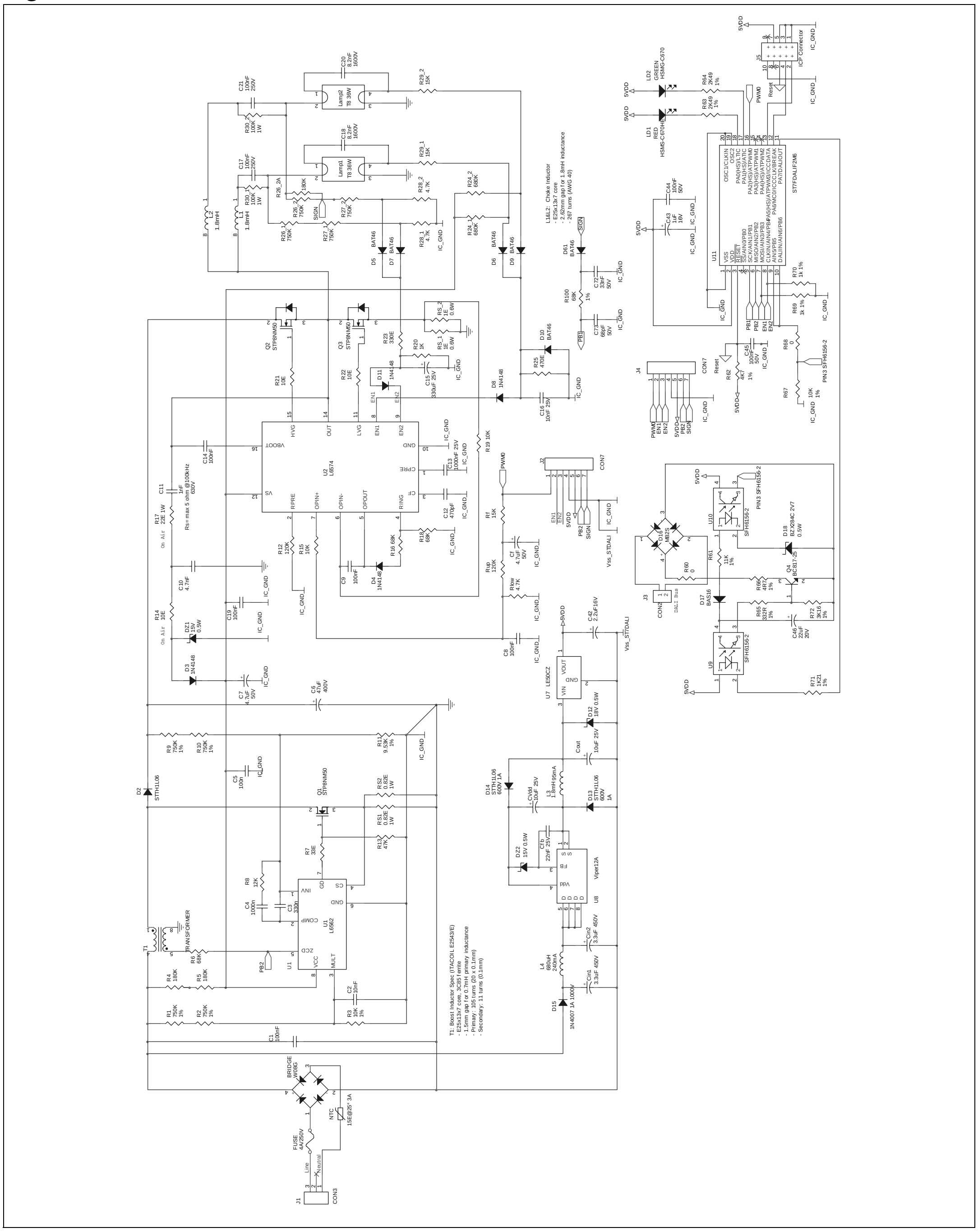
**Figure 2. 2X36 W digital dimmable ballast with L6574 and ST7FDALI**



# 2 High-frequency ballast

This section describes the high-frequency ballast board which includes the power factor correction stage, the half-bridge inverter driving circuitry, the output stage and the DALI slave unit. The schematic of the board is shown in *Figure 3*.

**Figure 3. Ballast schematic**



This block is essentially a "double board" as the DALI slave board and its external circuitry are mounted on a small separated board which is connected to the bottom side by means of a 7-pin connector. *Table 2* shows the ballast-slave communication.

**Table 2. Ballast-slave communication**

| Pin ref. | Description | Analog stage ←→ Microcontroller |
|---|---|---|
| 1 | PWM0 (ref op-amp) | ← |
| 2 | Disable L6574 EN1 & disconnected lamp | ←→ |
| 3 | Enable L6574 EN2 & not ignited lamp | ←→ |
| 4 | GND | ←→ |
| 5 | 5 VDD | → |
| 6 | PB2 disable PFC | ← |
| 7 | SIGN (lamp failure) | → |

**Table 3. Ballast bill of material**

| Reference | Value | Description |
|---|---|---|
| Bridge | W08G 1.5 A 800 V | Bridge rectifier |
| Cout, CVdd | 10 µF 25 V | Electrolytic cap |
| C7,Cf | 4.7 µF 50 V | Electrolytic cap |
| Cfb | 22 nF 25 V | Ceramic cap |
| Cin1,Cin2 | 3.3 µF 450 V | Electrolytic cap |
| C1 | 100 nF 400 V | Polyester cap |
| C2 | 10 nF 50 V | Ceramic cap |
| C3 | 330 nF 50 V | Ceramic cap |
| C4 | 1000 nF 50 V | Ceramic cap |
| C5,C8,C9,C19 | 100 nF 50 V | Ceramic cap |
| C6 | 47 µF 450 V | Electrolytic cap |
| C14 | 100 nF 100 V | Ceramic cap |
| C10 | 4.7 nF 100 V | Ceramic cap |
| C11 | 1 nF 630 V | Evox Rifa polypropylene cap $Rs_{max}$ = 5 Ω at 100 kHz |
| C12 | 470 pF 50 V | Ceramic cap |
| C13 | 1 µF 50 V | Ceramic cap |
| C15 | 330 µF 25 V | Electrolytic cap |
| C16 | 10 nF 25 V | Ceramic cap |
| C17, C21 | 100 nF 250 V | Polyester cap |
| C18,C20 | 8.2 nF 1600 V | Polyester cap |
| C42 | 2.2 µF16 V | Electrolytic cap |

**Table 3. Ballast bill of material (continued)**

| Reference | Value | Description |
|---|---|---|
| C43 | 1 µF 20 V | SMD tantalum cap |
| C44,C45 | 100 nF 50 V | 0805 SMD cap |
| C46 | 22 µF 20 V | SMD tantalum cap |
| C72 | 33 nF 50 V | 0805 SMD cap |
| C73 | 68 pF 50 V | 0805 SMD cap |
| DZ1,DZ2 | 15 V 0.5 W | Zener diode |
| D2,D13,D14 | STTH1L06 | STMicroelectronics ultrafast high voltage rectifier 1 A 600 V |
| D3,D4,D8,D11 | 1N4148 | Small signal rectifier 200 mA 100 V |
| D5,D6,D7,D9, D10,D61 | BAT46 DO 35 | STMicroelectronics small signal Schottky diode |
| D12 | 18 V 0.5 W | Zener diode |
| D15 | 1N4007 1 A 1000 V | General purpose rectifier |
| D16 | MB2S 0.5 A 200 V | SMD bridge rectifier |
| D17 | BAS16 | Small signal diode |
| D18 | BZX284C 2V7 | 0.5 W Zener diode |
| FUSE | 4 A 250 V | Radial fuse |
| J1 | Input 250 V connector | 3-way PCB screw terminal, 5.08 mm |
| J2 | Ballast-slave connector | 7-way strip line socket |
| J3 | Dali Bus | 2-way vertical PCB header, 3.81 mm pitch |
| J4 | Ballast-slave connector | 7-way strip line connector |
| J5 | ICP connector | 10-way 2-row vertical through-hole boxed header |
| J13 | | 4-way strip line socket |
| J14 | | 4-way strip line connector |
| Lamp 1 | Lamp connector | 4-way PCB screw terminal, 5.08 mm |
| Lamp 2 | Lamp connector | 4-way PCB screw terminal, 5.08 mm |
| LD1 | LS M67K-H2L1-1 | 2 mA red LED SMD 0805 |
| LD2 | LG M67K-G1J2-24 | 2 mA green LED SMD 0805 |
| L1,L2 | 1.8 mH | Choke inductor 2.62 mm gap, 267 turns (AWG40); E25x13x7 |
| L3 | 1.8 mH 95 mA | Epcos BC series Axial inductor |
| L4 | 680 µH 240 mA | Epcos LBC series Axial inductor |
| NTC | 15 Ω at 25 °C 3 A | Inrush current suppressor |
| Q1,Q2,Q3 | STP8NM50 TO220 | STMicroelectronics N-CHANNEL 550 V 0.7 Ω - 8 A MDmesh MOSFET |

Table 3. Ballast bill of material (continued)

| Reference | Value | Description |
|---|---|---|
| Q4 | BC817-25 | NPN small signal bipolar |
| RS_1,RS_2 | 1 Ω | 0.6 W 1% metal film resistor |
| RS1,RS2 | 0.82 Ω | 1 W resistor |
| R29_1, R29_2,Rf | 15 kΩ | Resistor |
| R28_1, R28_2,Rlow | 4.7 kΩ | Resistor |
| R12,Rup | 120 kΩ | Resistor |
| R1,R2,R9, R10, R26_1, R26_2, R27_1, R27_2 | 750 kΩ | 0.6 W 1% resistor |
| R15,R19 | 10 kΩ | Resistor |
| R3 | 10 kΩ | 0.6 W 1% resistor |
| R4,R5, R26_2A | 180 kΩ | Resistor |
| R6,R16,R18 | 68 kΩ | Resistor |
| R7 | 33 Ω | Resistor |
| R8 | 12 kΩ | Resistor |
| R11 | 9.53 kΩ | 1% Resistor |
| R13 | 47 kΩ | Resistor |
| R14,R21,R22 | 10 Ω | Resistor |
| R17 | 22 Ω | 1 W resistor |
| R20 | 1 kΩ | Resistor |
| R23 | 330 Ω | Resistor |
| R25 | 470 Ω | Resistor |
| R60,R68 | 0 Ω | SMD resistor 0805 |
| R61 | 11 kΩ | 1% SMD resistor 0805 |
| R62 | 4.7 kΩ | 1% SMD resistor 0805 |
| R63,R64 | 1 kΩ | 1% SMD resistor 0805 |
| R65 | 330 Ω | 1% SMD resistor 0805 |
| R66 | 4.7 Ω | 1% SMD resistor 0805 |
| R67 | 10 kΩ | 1% SMD resistor 0805 |
| R69,R70 | 1 kΩ | 1% SMD resistor 0805 |
| R71 | 1.2 kΩ | 1% SMD resistor 0805 |
| R72 | 3 kΩ | 1% SMD resistor 0805 |

Table 3. Ballast bill of material (continued)

| Reference | Value | Description |
|---|---|---|
| R100 | 68 kΩ | 1% SMD resistor 0805 |
| R24_1,R24_2 | 680 kΩ | Resistor |
| R30_1,R30_2 | 100 kΩ | 2 W resistor |
| T1 | Transformer | Choke boost inductor (ITACOIL E2543/E) |
| U1 | L6562N | STMicroelectronics transition-mode PFC controller |
| U2 | L6574 | STMicroelectronics ballast driver |
| U7 | LE50CZ TO-92 | STMicroelectronics very low drop voltage regulators |
| U8 | VIPer12A-E DIP8 | STMicroelectronics offline SMPS primary IC 730 V 0.4 A 27R |
| U9,U10 | SFH6156-2 | Optocoupler |
| U11 | ST7FDALIF2M6 SO20 | STMicroelectronics<br>8-bit MCU with single voltage Flash memory, data EEPROM, ADC, timers, SPI, DALI |

*Note: Resistors are 0.25 W unless specified. Q1, Q2 &Q3 are mounted with 8 °C/W heatsink.*

## 2.1 PFC converter

This block allows drawing a quasi-sinusoidal current from the mains, in phase with the line voltage in order to get a PF very close to 1 (more than 0.99).

To achieve such high PF the boost topology is implemented because of the advantages it offers:

- Minimum number of external components, thus making it a low-cost solution
- Low input di/dt thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter
- The switch is source-grounded, therefore is easy to drive

However, boost topology requires the DC output voltage (400 Vdc) to be higher than the maximum expected line peak voltage.

ST's L6562 has been used as the driver. It implements a transition mode control (fixed ON time, variable frequency), that, for such output power, is preferred to the fixed frequency average current mode being simpler and cheaper. The circuit operates on the boundary between continuous and discontinuous current mode.

Besides providing good results in terms of power factor, this IC considerably reduces the Total Harmonic Distortion (THD) as it reduces the conduction dead-angle that occurs to the AC input current near the zero-crossings of the line voltage.

The basic design specifications are listed in *Table 4*.

**Table 4. PFC operating conditions**

| Parameter | Value |
|---|---|
| Mains voltage range: Virms(min) - Virms(max) | 90 – 265 Vac |
| Regulated DC output voltage: Vo | 400 Vdc |
| Rated output power: Po | 75 W |
| Minimum switching frequency: $f_{sw}$ | 35 kHz |
| Maximum output voltage ripple: ΔVo | < ± 10 V |
| Maximum overvoltage admitted: $\Delta V_{OVP}$ | 60 V |
| Expected efficiency: $\eta_{PFC}$ | > 90 V |

For reference, it is useful to define also the following quantities:

- Input power: Pi (= Po / η) ≈ 80 W
- Maximum mains RMS current: Iirms (= Pi/Virms(min)) ≈ 1 A
- Rated output current: Io (= Po/Vo) ≈ 0.2 A

The design guidelines are deeply explained in AN966 ("L6561, enhanced transition mode power factor corrector"), AN1757 ("Switching from the L6561 to the L6562) and AN1089 ("control loop model of L6561-based TM PFC"). The main design formulas are summarized as follows in *Table 5*.

**Table 5. Power stage design equations**

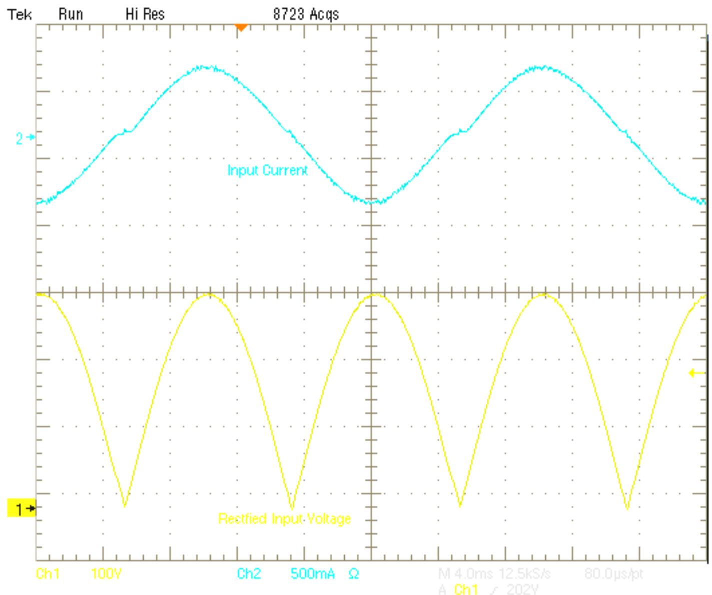
| Input capacitor (C1) | Boost inductor | Power MOSFET (Q1) | Boost diode (D1) |
|---|---|---|---|
| $C1 = \frac{Irms}{2\pi \cdot fsw \cdot r \cdot Vinrmsmin}$ | $Volume \geq 4K \cdot L \cdot I^2 irms$ | $BV_{DSS} = Vo + \Delta V_{OVP} + Vmargin$ | |
| where $r = 0.01 \div 0.1$ | $L = \frac{V^2 irms \cdot (Vo - \sqrt{2} \cdot Virms)}{2 \cdot f_{sw} \cdot Pi \cdot Vo}$ | $Pon = I^2 Qrms \cdot R_{DS(on)}$ | $V_{RRM} = 1.2 \cdot Vo$ |
| Output capacitor (C6) | where $K \cong 14 \cdot 10^{-3} \cdot \frac{le}{lgap}$ | where $I_{Qrms} = 2\sqrt{2} \cdot Iirms \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{Virms}{Vo}}$ | $I_F = 3 \cdot Io$ |
| $C6 \geq \frac{Po}{4\pi \cdot f \cdot Vo \cdot \Delta Vo}$ | $Pcu = \frac{4}{3} \cdot I^2 irms \cdot Rcu$ | $Pcross = Vo \cdot Iirms \cdot t_{fall} \cdot f_{sw}$ | $P_{losses} = V_T \cdot I_{DC} + Rd \cdot I^2 rms$ |
| | | $Pcap = \left(3.3Coss \cdot V^{1.5} drain + \frac{1}{2} Cd \cdot V^2 drain\right) \cdot f_{sw}$ | |

**Table 6. L6562 biasing circuitry design equations**

| Pin 1 (INV) | Pin 2 (COMP) | Pin 3 MULT | Pin 4 (CS) |
|---|---|---|---|
| $\Delta OVP = R_{high} \cdot 40 \cdot 10^{-6}$<br>$V_{out} = 2.5 \cdot \frac{(R_{high} + R_{low})}{R_{low}}$ | A RC-C network is placed between this pin and pin 1, leading to a low crossover frequency (some tens of hertz) as well as to an adequate phase margin. | $Rlow = \frac{V_{MULTpkx}}{250 \cdot 10^{-6}} = \frac{2.5}{250 \cdot 10^{-6}}$<br>$\frac{R_{low}}{R_{low} + R_{high}} = \frac{2.5}{\sqrt{2} \cdot V_{inrmsmax}}$<br>A small capacitor of 10 nF filters the signal on MULT pin. | $R_{sense} \le \frac{1.65 \cdot \left(2.5 \cdot \frac{V_{inrmsmin}}{V_{inrmsmax}}\right)}{2 \cdot \sqrt{2} \cdot I_{inrms}}$<br>$Pd = Rs \cdot I^{2}_{Qrms}$ |
| **Pin 5 (ZCD)** | **Pin 6 (GND)** | **Pin 7 (GD)** | **Pin 8 Vcc** |
| $m = \frac{(Vout - \sqrt{2} \cdot V_{inrmsmax})}{2.1 \cdot 1.15}$<br>$R6 \ge \frac{(Vout - \sqrt{2} \cdot V_{inrmsmin})}{m \cdot 3 \cdot 10^{-3}}$ | IC ground. As a layout hint, this pin has to be kept separated from power ground. All the IC signals have to be referred to this pin. | Gate driver.<br>A "bleeder" resistor between the gate and the source is used to avoid undesired switch-on, without affecting the power consumption. | The supply voltage is provided by a capacitive power supply connected to the half-bridge inverter.<br>$R_{start} = \frac{V_{inrmsmin} \cdot \sqrt{2}}{I_{startup}}$ |

The PFC preregulator performances are shown in the following graphs:

**Figure 4. PFC performances at 230 Vac-50 Hz**



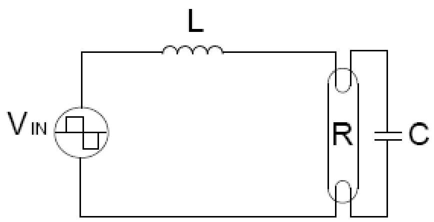

CH1 (yellow): rectified input voltage
CH2 (blue): input current

## 2.2 Half-bridge inverter and ballast

A voltage fed series resonant half-bridge inverter has been implemented to drive the tubes. This topology allows to easily operates in zero-voltage switching (ZVS) resonant mode, heavily reducing the transistor switching losses and the electromagnetic interference. In addition it guarantees design simplicity and low cost.

A parallel configuration has been chosen for the output stage. The half-bridge inverter operating conditions and the ballast design have been obtained by assuming, for each lamp, the following basic model:

**Figure 5. Lamp ballast model**




To increase the life time of the lamps a current mode preheat was preferred. The preheating current brings the cathodes to the correct temperature, then a high voltage ignites the lamp and finally the correct current guarantees the running power. These phases are ensured by changing the frequency of the input voltage and properly selecting $V_{IN}$, L and C. During preheating and ignition, the lamp is not conducting and the circuit is reduced to a series L-C. During running, the lamp is conducting and the circuit is an L in series with a parallel R-C. To determine the optimum values for L and C and to calculate the ballast operating frequencies the transfer functions for each mode of operation have to be inspected.

The table below shows the parameters and the values for a T8 36 W tube lamp which need to be known in order to calculate the ballast operating conditions.

**Table 7. Lamp parameters**

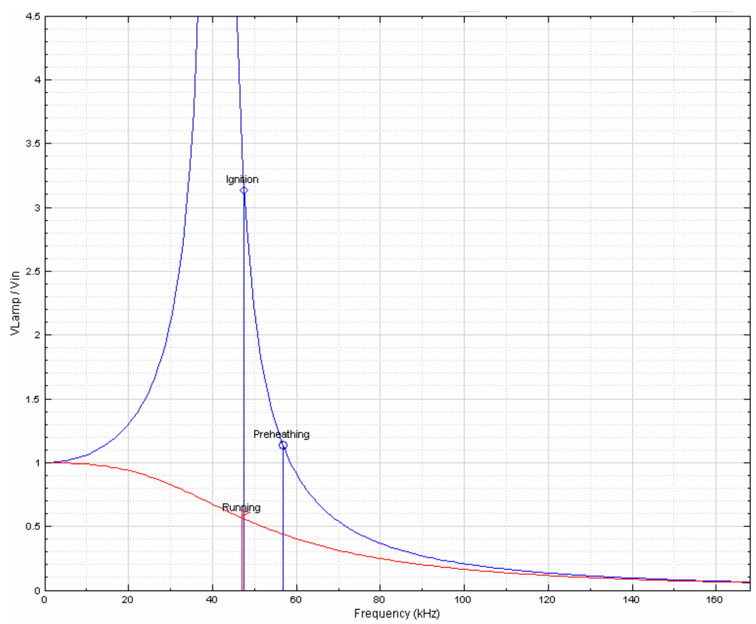
| Parameter | Value |
|---|---|
| Input DC bus voltage: Vdc | 400 V |
| Preheat current: Iph | 0.6 A |
| Preheat time: Tph | 1 sec |
| Max preheat voltage: Vphmax | 300 Vpk |
| Ignition voltage: Vign | 800 Vpk |
| Running lamp power: Prun | 34 W |
| Running lamp voltage: Vrun | 144 Vpk |
| Expected efficiency: η | 95% |

Once the lamp and its parameters have been chosen, the ballast design will be optimized by selecting the resonant components L and C as follows:

- Set Tpre
- Select frunmin (> 20 kHz)
- Choose Δf = fmax-frunmin
- Select L & C such that fph > frun
- Select half-bridge switches
- Select L6574 biasing circuitry

The magnitude of the transfer function (lamp voltage divided by input voltage) for the two circuit configurations (preheating-ignition and running) illustrates the operating frequencies and where they lie with respect to one another.

**Figure 6. Ballast transfer functions (magnitude)**




The currents and voltages corresponding to the resulting operating frequencies determine the maximum current and voltage ratings for the inductor, capacitor, and the switches, which, in turn, directly determine the size and cost of the ballast.

Moreover the zero-voltage switching is ensured as shown by the curves above in *Figure 6*. STP8NM50 (8 A, 550 V) has been selected as power switch according to the current stress and the input DC voltage.

The half-bridge inverter driving circuitry is based on the high performance L6574 which is an OFF-LINE half-bridge driver designed in 600 V BCD technology, including all the features needed to drive and properly control the tubes. A dedicated timing section in the L6574 allows setting the necessary parameters for proper preheat and ignition of the lamps. Also, an op-amp is available to implement closed-loop control of the lamp current during normal lamp burning. To avoid cross conduction of the power MOSFETs the internal logic ensures a minimum deadtime. Moreover the L6574 is provided with two lamp status control functions to protect the application against lamp failure as well as lamp disconnection. Finally it is possible to modulate the output power in order to allow dimming by varying the switching frequency.

The ballast operating frequencies determine the L6574 biasing circuitry as explained in AN993 "Electronic Ballast With PFC Using L6574 and L6561" and as summarized below.

**Table 8. L6574 biasing circuitry design equations for operating conditions**

| Pin 1 (CPRE) | Pin 2 (RPRE) | Pin 3 (CF) | Pin 4 (RIGN) | Pin 5 (OPOUT) |
|---|---|---|---|---|
| $T_{ph} = 1.5 \cdot C_{PRE}$ <br> $T_{sh} = \frac{K_{PRE}}{10} \cdot C_{PRE}$ | $fph - frun = \frac{1.41}{R_{PRE}Cf}$ | $frun = \frac{1.41}{RignCf}$ | $frun = \frac{1.41}{RignCf}$ | A capacitor is connected between this pin and OPIN- for the current feedback loop compensation. It set also the turn on delay in a dimming application. |

## 2.2.1 Lamp dimming

In this system the lamps are dimmed down to 5% by interfacing the ST7FDALI microcontroller with the analog driver L6574.

A PWM output of the ST7FDALI microcontroller is used to generate a 0-5 V PWM at 4 kHz. Its integrated value gives the op amp voltage reference. The dimming level is set by varying the PWM duty cycle from 70% (100% dimming) to 14% (5% dimming). This modification allows changing the L6574 op-amp positive reference voltage from 120 mV to 20 mV which increases the switching frequency and reduces the current in the load.

On the slave unit the duty cycle values have been calculated according the DALI protocol brightness values, listed in *Figure 7*.

**Figure 7. DALI protocol brightness values**

| n | X | n | X | n | X | n | X | n | X |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |
| 1 | 0.100 | 52 | 0.402 | 103 | 1.620 | 154 | 6.520 | 205 | 26.241 |
| 2 | 0.103 | 53 | 0.414 | 104 | 1.665 | 155 | 6.700 | 206 | 26.967 |
| 3 | 0.106 | 54 | 0.425 | 105 | 1.711 | 156 | 6.886 | 207 | 27.713 |
| 4 | 0.109 | 55 | 0.437 | 106 | 1.758 | 157 | 7.076 | 208 | 28.480 |
| 5 | 0.112 | 56 | 0.449 | 107 | 1.807 | 158 | 7.272 | 209 | 29.269 |
| 6 | 0.115 | 57 | 0.461 | 108 | 1.857 | 159 | 7.473 | 210 | 30.079 |
| 7 | 0.118 | 58 | 0.474 | 109 | 1.908 | 160 | 7.680 | 211 | 30.911 |
| 8 | 0.121 | 59 | 0.487 | 110 | 1.961 | 161 | 7.893 | 212 | 31.767 |
| 9 | 0.124 | 60 | 0.501 | 111 | 2.015 | 162 | 8.111 | 213 | 32.646 |
| 10 | 0.128 | 61 | 0.515 | 112 | 2.071 | 163 | 8.336 | 214 | 33.550 |
| 11 | 0.131 | 62 | 0.529 | 113 | 2.128 | 164 | 8.567 | 215 | 34.479 |
| 12 | 0.135 | 63 | 0.543 | 114 | 2.187 | 165 | 8.804 | 216 | 35.433 |
| 13 | 0.139 | 64 | 0.559 | 115 | 2.248 | 166 | 9.047 | 217 | 36.414 |
| 14 | 0.143 | 65 | 0.574 | 116 | 2.310 | 167 | 9.298 | 218 | 37.422 |
| 15 | 0.147 | 66 | 0.590 | 117 | 2.374 | 168 | 9.555 | 219 | 38.457 |
| 16 | 0.151 | 67 | 0.606 | 118 | 2.440 | 169 | 9.820 | 220 | 39.522 |
| 17 | 0.155 | 68 | 0.623 | 119 | 2.507 | 170 | 10.091 | 221 | 40.616 |
| 18 | 0.159 | 69 | 0.640 | 120 | 2.577 | 171 | 10.371 | 222 | 41.740 |
| 19 | 0.163 | 70 | 0.658 | 121 | 2.648 | 172 | 10.658 | 223 | 42.895 |
| 20 | 0.168 | 71 | 0.676 | 122 | 2.721 | 173 | 10.953 | 224 | 44.083 |
| 21 | 0.173 | 72 | 0.695 | 123 | 2.797 | 174 | 11.256 | 225 | 45.303 |
| 22 | 0.177 | 73 | 0.714 | 124 | 2.874 | 175 | 11.568 | 226 | 46.557 |
| 23 | 0.182 | 74 | 0.734 | 125 | 2.954 | 176 | 11.888 | 227 | 47.846 |
| 24 | 0.187 | 75 | 0.754 | 126 | 3.035 | 177 | 12.217 | 228 | 49.170 |
| 25 | 0.193 | 76 | 0.775 | 127 | 3.119 | 178 | 12.555 | 229 | 50.531 |
| 26 | 0.198 | 77 | 0.796 | 128 | 3.206 | 179 | 12.902 | 230 | 51.930 |
| 27 | 0.203 | 78 | 0.819 | 129 | 3.294 | 180 | 13.260 | 231 | 53.367 |
| 28 | 0.209 | 79 | 0.841 | 130 | 3.386 | 181 | 13.627 | 232 | 54.844 |
| 29 | 0.215 | 80 | 0.864 | 131 | 3.479 | 182 | 14.004 | 233 | 56.362 |
| 30 | 0.221 | 81 | 0.888 | 132 | 3.576 | 183 | 14.391 | 234 | 57.922 |
| 31 | 0.227 | 82 | 0.913 | 133 | 3.675 | 184 | 14.790 | 235 | 59.526 |
| 32 | 0.233 | 83 | 0.938 | 134 | 3.776 | 185 | 15.199 | 236 | 61.173 |
| 33 | 0.240 | 84 | 0.964 | 135 | 3.881 | 186 | 15.620 | 237 | 62.866 |
| 34 | 0.246 | 85 | 0.991 | 136 | 3.988 | 187 | 16.052 | 238 | 64.607 |
| 35 | 0.253 | 86 | 1.018 | 137 | 4.099 | 188 | 16.496 | 239 | 66.395 |
| 36 | 0.260 | 87 | 1.047 | 138 | 4.212 | 189 | 16.953 | 240 | 68.233 |
| 37 | 0.267 | 88 | 1.076 | 139 | 4.329 | 190 | 17.422 | 241 | 70.121 |
| 38 | 0.275 | 89 | 1.105 | 140 | 4.449 | 191 | 17.905 | 242 | 72.062 |
| 39 | 0.282 | 90 | 1.136 | 141 | 4.572 | 192 | 18.400 | 243 | 74.057 |
| 40 | 0.290 | 91 | 1.167 | 142 | 4.698 | 193 | 18.909 | 244 | 76.107 |
| 41 | 0.298 | 92 | 1.200 | 143 | 4.828 | 194 | 19.433 | 245 | 78.213 |
| 42 | 0.306 | 93 | 1.233 | 144 | 4.962 | 195 | 19.971 | 246 | 80.378 |
| 43 | 0.315 | 94 | 1.267 | 145 | 5.099 | 196 | 20.524 | 247 | 82.603 |
| 44 | 0.324 | 95 | 1.302 | 146 | 5.240 | 197 | 21.092 | 248 | 84.889 |
| 45 | 0.332 | 96 | 1.338 | 147 | 5.385 | 198 | 21.675 | 249 | 87.239 |
| 46 | 0.342 | 97 | 1.375 | 148 | 5.535 | 199 | 22.275 | 250 | 89.654 |
| 47 | 0.351 | 98 | 1.413 | 149 | 5.688 | 200 | 22.892 | 251 | 92.135 |
| 48 | 0.361 | 99 | 1.452 | 150 | 5.845 | 201 | 23.526 | 252 | 94.686 |
| 49 | 0.371 | 100 | 1.492 | 151 | 6.007 | 202 | 24.177 | 253 | 97.307 |
| 50 | 0.381 | 101 | 1.534 | 152 | 6.173 | 203 | 24.846 | 254 | 100.000 |
| 51 | 0.392 | 102 | 1.576 | 153 | 6.344 | 204 | 25.534 | | |

To avoid the presence of stationary waves along the tubes at minimum dimming level, a resistor of 100 kΩ / 2 W has been placed in parallel to the battery capacitor of each lamp. The resistance value ensures an additional current of 2 mA on the cathodes without affecting the ballast efficiency.

Finally, during the startup sequence the frequency always goes from fmax to fmin, independently of the set dimming level. Only after lamp turn-on does the frequency move towards higher values.

### 2.2.2 Supply section

To supply the DALI slave microcontroller an AC-DC buck converter based on the VIPer12A-E and L78L05 has been implemented on the ballast board. It converts the rectified and filtered mains to a 5 V regulated output voltage dedicated to the microcontroller. The converter works in discontinuous current mode adjusting the duty cycle of the VIPer12A-E power switch in order to deliver the energy from the input to the output by means of an inductor. PWM driver, power switch, thermal and overcurrent protection are integrated in the same silicon chip ensuring minimum size and good performances at very low cost.

Thanks to this implementation strategy the microcontroller is always supplied, allowing the lamps to turn on, even when L6562 and L6574 are in a latched shutdown state.

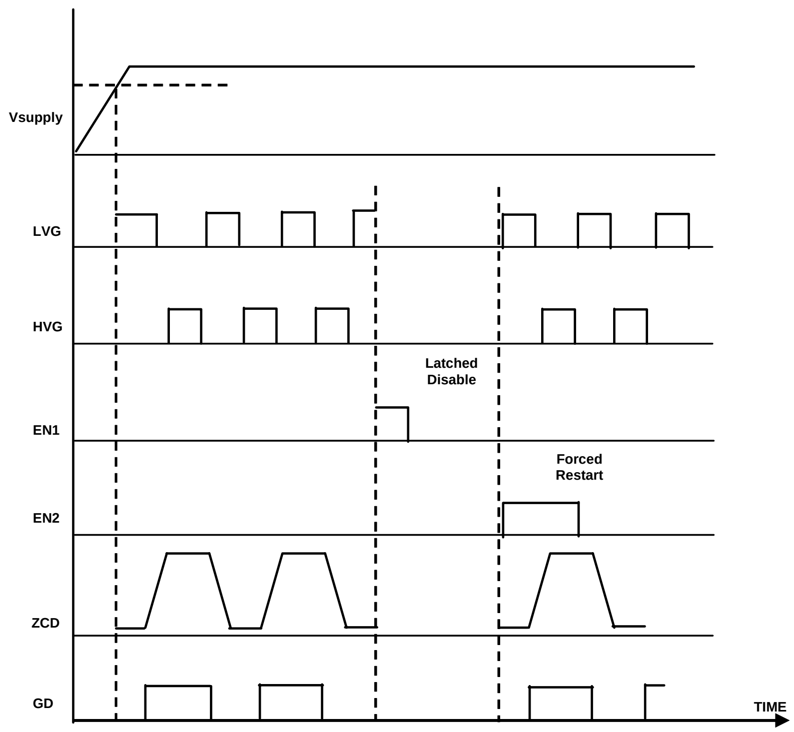
The startup procedure is very important in an application that contains two different sections. The ballast section starts before the PFC, avoiding any extra voltage at the PFC section output, and consequently the L6562 OVP activation. This behavior is guaranteed under all conditions because the VS turn-on threshold of L6574 is lower than that of the L6562. The turn-on threshold is reached by a resistor chosen in order to ensure the startup current of both the L6562 and the L6574. When the ballast section is running, the charge pump (C11, R14, D3 and DZ1) supplies both the devices and the filter R17-C10 allows to reduce the noise at Vcc.

### 2.2.3 Lamp turn-on and lamp turn-off

To get low-power consumption (less than 0.6 W) during the lamps' turnoff state, both the half-bridge and the PFC have to be disabled, even in the presence of the mains at the ballast input. To manage this standby condition the L6574 control section and the L6562 ZCD pin are interfaced with the DALI slave microcontroller.

Short pulses (> 200 nsec) at the EN1 and EN2 inputs are recognized by the L6574. In particular, EN1 high (> 0.6 V) stops all the half-bridge functions and puts the L6574 in a latched shutdown state. At the same time, by forcing externally the ZCD pin to a voltage below 150 mV, the L6562 is stopped. To cancel this status, in order to turn on the lamps, a pulse (>0.6 V) is sent by the microcontroller to the L6574 second control pin EN2 and the ZCD pin external pull down is removed. The half-bridge driver restarts the preheating and ignition procedure, and the L6562 performs again its operation. The controls timing diagram is shown in *Figure 8*.

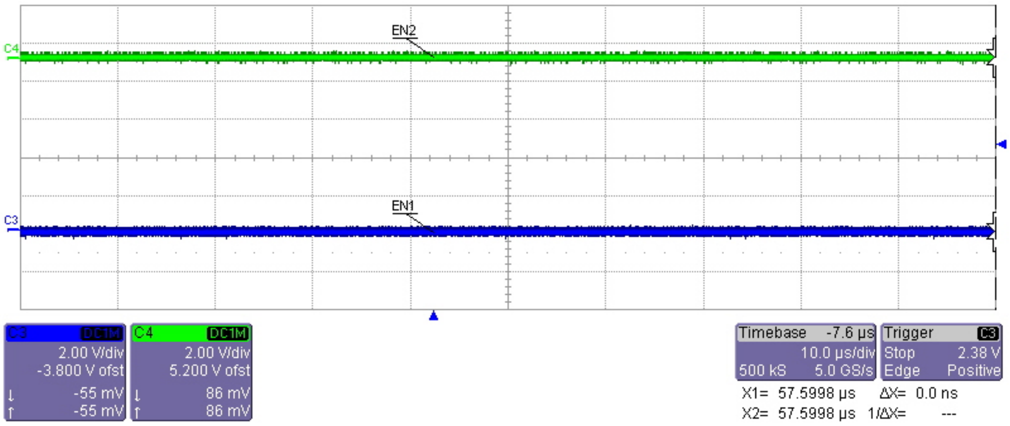
**Figure 8. Ballast controls timing chart**




On the slave unit the turning ON/OFF process is implemented by setting the pins PB3 (EN1) and PB4 (EN2) as output pull-up, while PB2 (ZCD) as output open drain. The three corresponding bits in the port data register are clear by software. To "switch on" the ballast, a pulse must be sent to PB4 (EN2 signal) and the third bit must be set in the port B (ZCD) data register. To "switch off" the ballast, a pulse must be sent to PB3 (EN1 signal) and the third bit must be cleared in the port B (ZCD signal) data register.

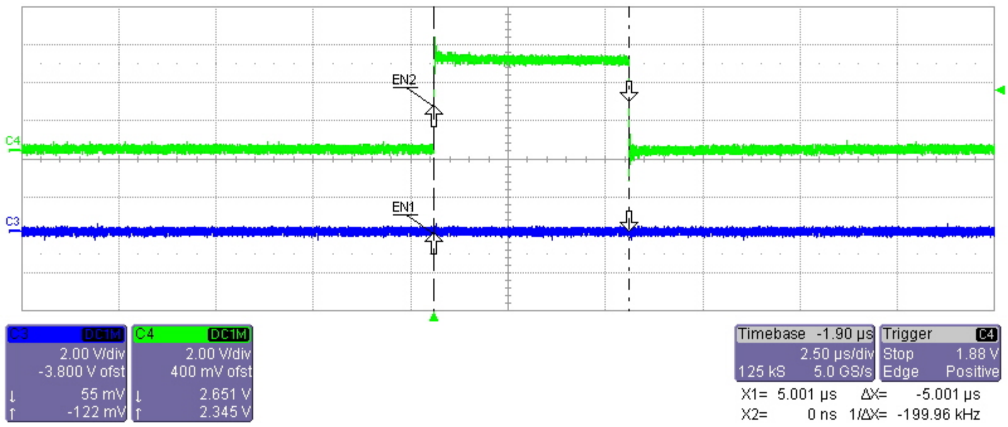
*Figure 9*, *10*, and *11* show the idle state and the turn-on/off commands.

**Figure 9. Idle state**



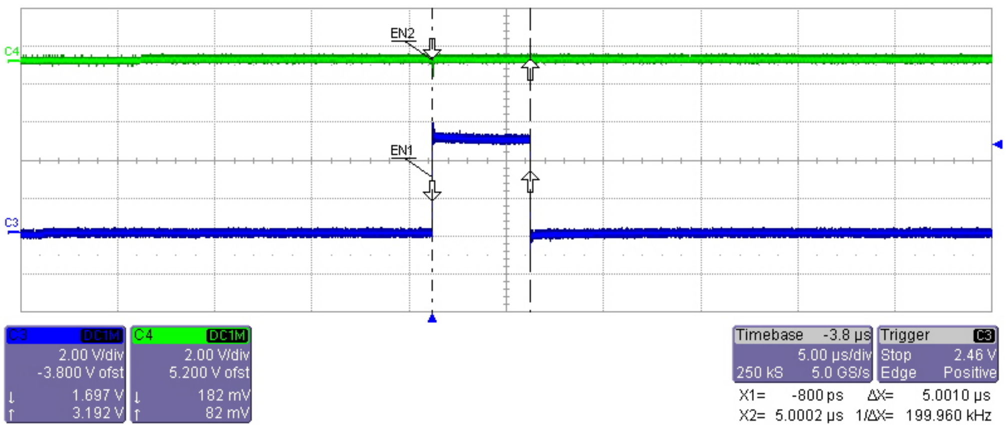

CH3 (blue): EN1 low level
CH4 (green): EN2 low level

**Figure 10. Turn-on procedure**




CH3 (blue): EN1 low level
CH4 (green): EN2 pulse

**Figure 11. Turn-off procedure**




CH3 (blue): EN1 pulse
CH4 (green): EN2 low level

### 2.2.4 Verification of lamp status

This function detects a lamp disconnection or a lamp failure on the slave board. The microcontroller performs a double check: one on the PB1 pin for the lamp hardware status and one on the flag "LAMP_ARC_POWER_ON" for the lamp software status. If the PB1 logical level is low and the flag is true, lamp disconnection happened. The condition is recorded on ST7FDALI, so when the microcontroller receives a "query frame" from the master, it changes the PB3 (EN1) and PB4 (EN2) configuration from input to output, and sends a byte answer as 'STATUS INFORMATION' described below:

- bit 0 status of ballast; '1'= NOK
- bit 1 Lamp failure; '1'= NOK
- bit 2 Lamp arc power on; '0' = OFF
- bit 3 Query: Limit Error; '0' = Last requested arc power level is between MIN..MAX LEVEL or OFF
- bit 4 Fade ready; '0' = fade is ready; '1' = fade is running
- bit 5 Query: 'RESET STATE'? '0' = 'No'
- bit 6 Query: Missing short address? '0' = 'No'
- bit 7 Query: 'POWER FAILURE'? '0' = 'No'; 'RESET' or an arc power control command has been received after last power-on

When the master receives this frame, it displays the lamp status by means of two LEDs (green stands for ok, red for status not ok). Once the failure condition has been detected and solved, an "ON" command has to be sent to the slave, allowing the master's microcontroller to toggle again the LED status from red to green. From the analog side, to detect a disconnection or a failure event for each lamp, two signal Schottky diodes have been used to bias the EN1 or EN2 pin of L6574. The failure condition is detected both at startup and when running.

The forward and backward frame timing is shown in *Figure 12* and *13*:

**Figure 12. Forward frame timing**

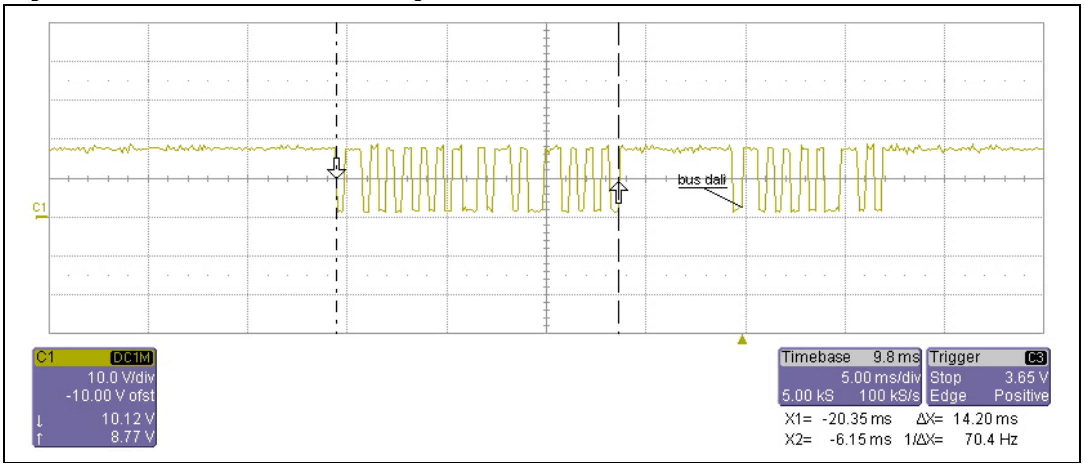
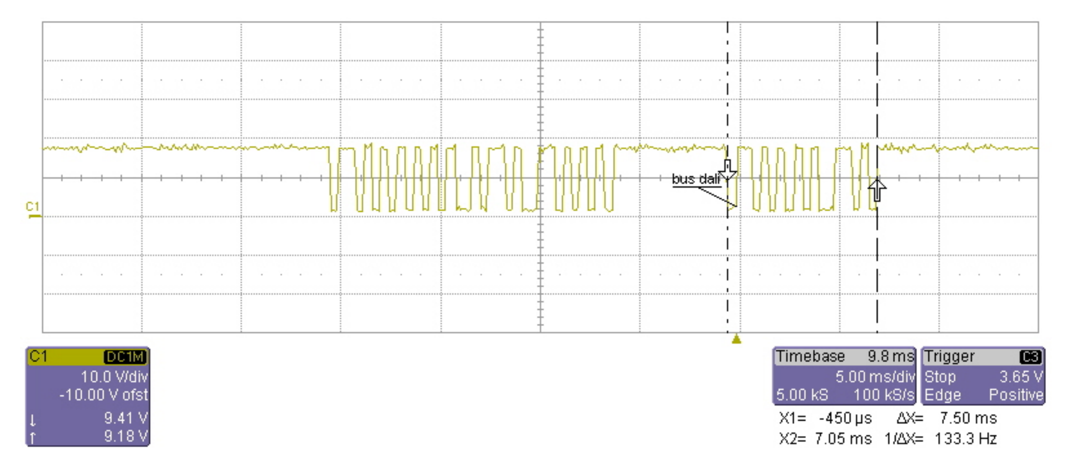


**Figure 13. Backward frame timing**

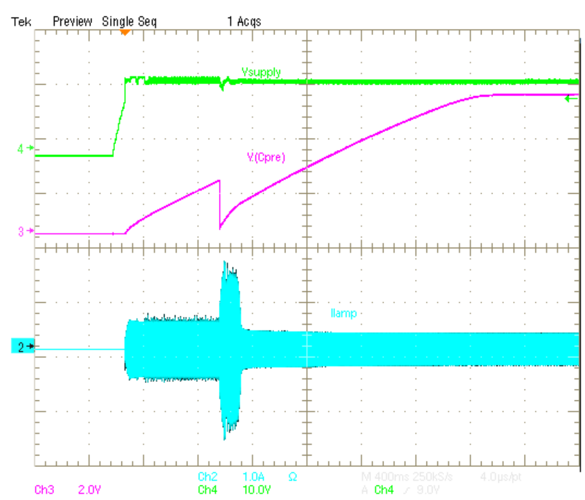



The forward as well as the backward frame duration is the same for all kinds of commands.

### 2.2.5 Ballast performances

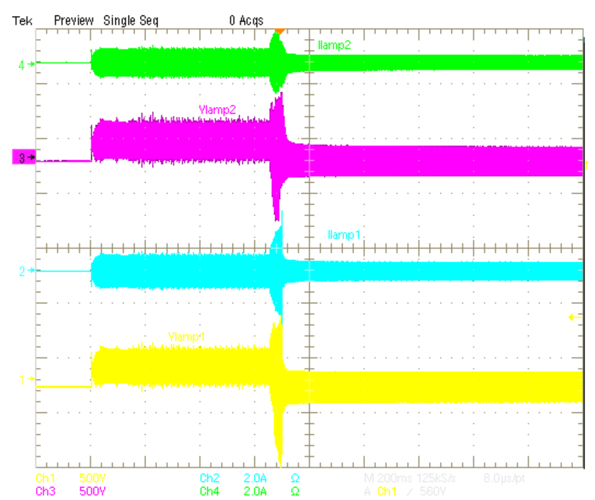
In this section the main ballast waveforms are shown.

**Figure 14. Ballast startup at 230 Vac-full power**



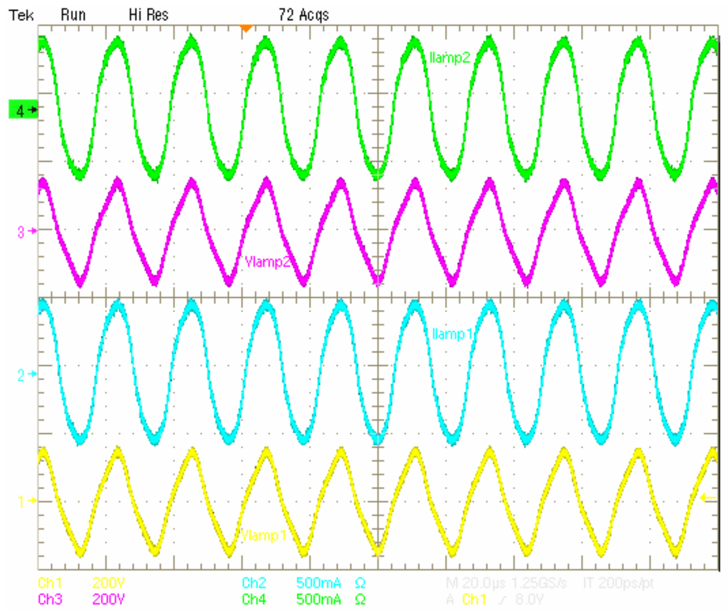

CH2 (blue): lamp current
CH3 (magenta): $V_{CPRE}$
CH4 (green): supply voltage

**Figure 15. Lamps turn-on at 230 Vac-full power**




CH1 (yellow): lamp1 voltage
CH2 (blue): lamp1 current
CH3 (magenta): lamp2 voltage
CH4 (green): lamp2 current

**Figure 16. Lamps running at 230 Vac - full power**




CH1 (yellow): lamp1 voltage
CH2 (blue): lamp1 current
Ch3 (magenta): lamp2 voltage
CH4 (green): lamp2 current

**Table 9. Ballast performances**

| Vin (Vac) | Pin (W) | PF | THD (%) | Po (W) | η(%) |
|---|---|---|---|---|---|
| 90 | 76.5 | 0.999 | 3.9 | 66 | 86.2 |
| 110 | 75.5 | 0.999 | 3.6 | 66 | 87.4 |
| 140 | 74.2 | 0.998 | 5.5 | 66 | 89 |
| 176 | 73.7 | 0.997 | 7.2 | 66 | 90 |
| 230 | 73 | 0.997 | 7.3 | 66 | 90 |
| 265 | 72.8 | 0.996 | 8.3 | 66 | 91 |

The efficiency of the system is a little bit lower than a standard HF ballast due to the supply section of the slave and the resistors in series to the lamp's cathode used to ensure a minimum current at low dimming level.

# 3 DALI master unit

The ST2C334J4 microcontroller is used as master, implementing the DALI Peripheral via software.

The communication master-slave uses a 20 V bus. To adapt the TTL level of the microcontroller to the communication bus level, two opto-couplers and a NPN transistor BC-817 have been used.

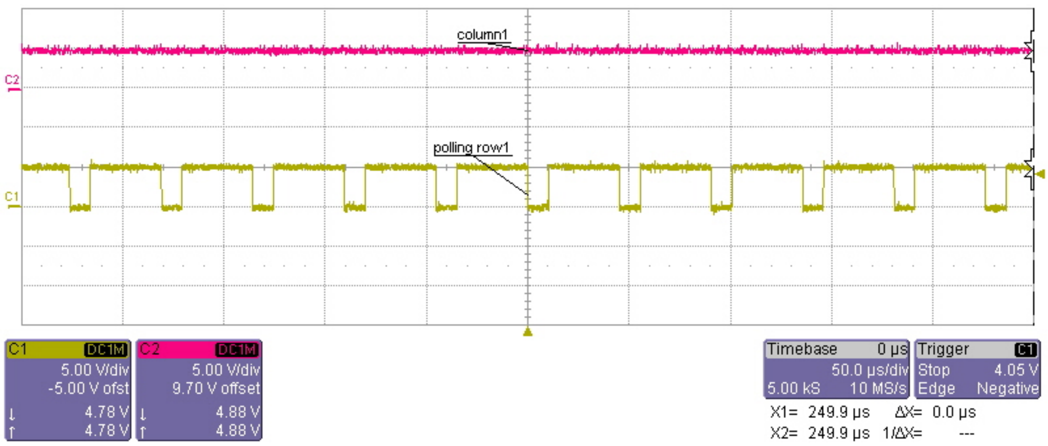
The RS232 interface with ST232C is available on the board to implement the SCI communication as an option. This option expects the use of a PC to address the ballast either with broadcast or group or single mode thanks to a GUI called (DALI Power Control).

The DALI master unit has been thought of as a standalone solution. In fact it is provided with a keyboard to manage the DALI commands, to address the slaves and to display the lamps' status.

The keyboard is made up of 16 push buttons controlled by means of a matrix representation. In particular the first four pins of PORTD are associated to the rows and the first four pins of PORTB to the columns.

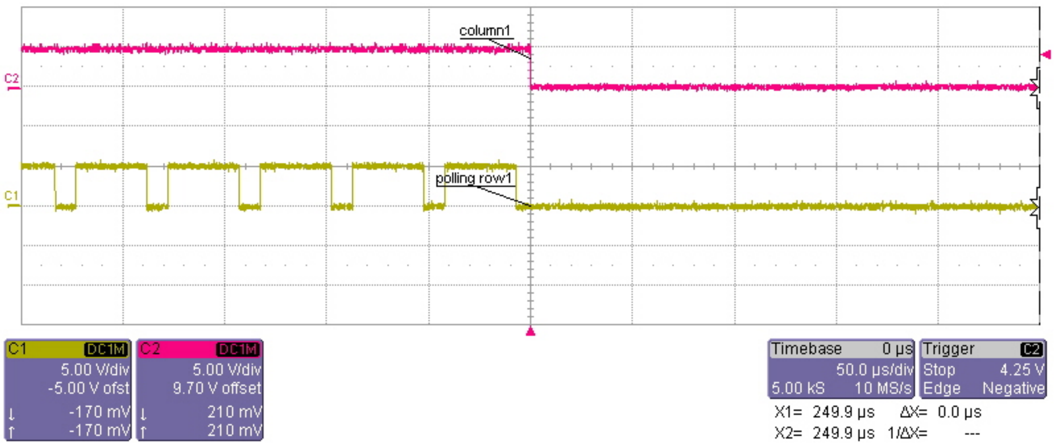
The check of the keyboard is implemented as a loop mode by clearing the PDDR register port and setting the PBDR register port sequentially. When a button is pressed, the pin of the port B corresponding to the interested column goes down and this condition is taken over by an interrupt condition. Inside the interrupt routine, a read procedure of the port registers PDDR and PBDR is expected and by this information the pressed button is acknowledged. The "press button" procedure is described by *Figure 17* and *18*.

**Figure 17. Polling keyboard**




CH1 (yellow): row polling
CH2 (purple): column level

**Figure 18. Pressed button event**




CH1 (yellow): row polling
CH2 (purple): column level

## 3.1 Master unit schematic and bill of material

The schematic of the master unit is shown in *Figure 19*.

**Figure 19. Master unit schematic**

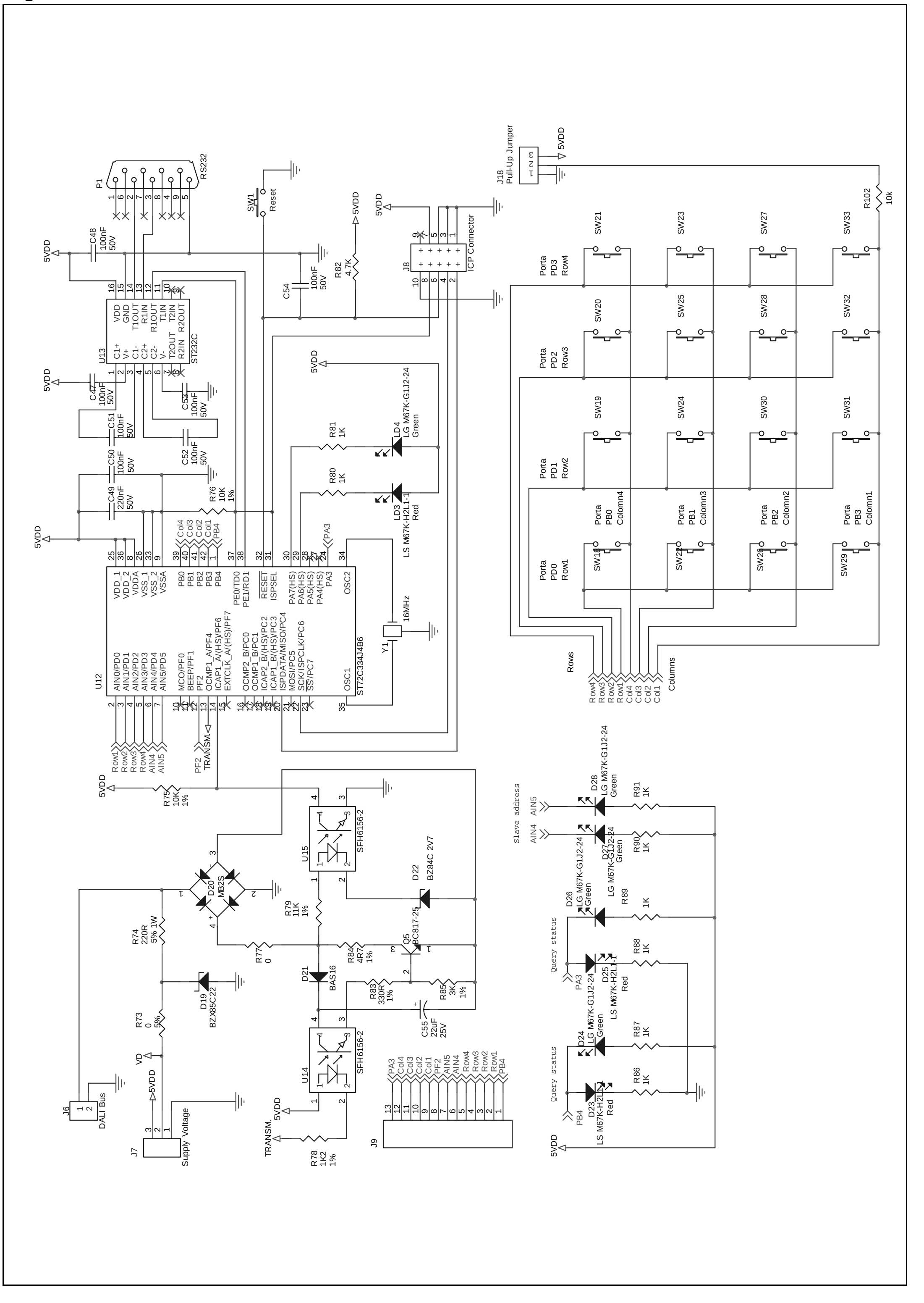


**Table 10. Master unit bill of material**

| Reference | Value | Description |
|---|---|---|
| C47,C48,C50,C51,C52, C53,C54 | 100 nF 50 V | Ceramic capacitor SMD 0805 |
| C49 | 220 nF 50 V | Ceramic capacitor SMD 0805 |
| C55 | 22 µF 25 V | Tantalum capacitor SMD |
| D19 | BZX85C22 | 22 V 0.5 W Zener diode |
| D20 | MB2S | SMD bridge rectifier |
| D21 | BAS16 | SMD diode |
| D22 | BZ84C 2V7 | 2.7 V 0.5 W Zener SMD diode |
| D23,D25 | LS M67K-H2L1-1 | Red SMD LED 2 mA, 0805 |
| D24,D26,D27,D28 | LG M67K-G1J2-24 | Green SMD LED 2 mA, 0805 |
| J6 | DALI BUS | 2-way single row, header shrouded |
| J7 | Supply voltage | 3-way single row header shrouded |
| J8 | ICP connector | 10-way 2-row vertical through-hole boxed header, 2.54 mm pitch/grid |
| J9 | | 13-way strip line connector (not mounted) |
| J12 | Pull-up jumper | 3-way strip line connector |
| LD3 | LS M67K-H2L1-1 | Red SMD LED 2 mA, 0805 |
| LD4 | LG M67K-G1J2-24 | Green SMD LED 2 mA, 0805 |
| P1 | Serial connector | 9-way 90° PCB mount D plug |
| Q5 | BC817-25 | SMD NPN transistor |
| R73 | 0 | Resistor SMD 1206 |
| R77 | 0 | Resistor SMD 0805 |
| R74 | 220 Ω | 1 W 5% resistor |
| R75,R76 | 10 kΩ | 1% resistor SMD 0805 |
| R78 | 1.2 kΩ | 1% resistor SMD 0805 |
| R79 | 11 kΩ | 1% resistor SMD 0805 |
| R80,R81 | 1 kΩ | Resistor SMD 0805 |
| R82 | 4.7 kΩ | Resistor SMD 0805 |
| R83 | 330 Ω | 1% Resistor SMD 0805 |
| R84 | 4.7 Ω | 1% Resistor SMD 0805 |
| R85 | 3 kΩ | 1% Resistor SMD 0805 |
| R86,R87,R88,R89,R90, R91 | 1 kΩ | Resistor SMD 0805 |
| R101 | 10 kΩ | Resistor SMD 0805 |
| SW1 | Reset | THT button |

**Table 10. Master unit bill of material (continued)**

| Reference | Value | Description |
|---|---|---|
| SW2, SW3, SW4, SW5, SW6, SW7, SW8, SW9, SW10, SW11, SW12, SW13, SW14, SW15, SW16, SW17 | Keyboard | THT button |
| U12 | ST72C334J4B6 PSDIP42 | STMicroelectronics<br>8-bit MCU with single voltage flash memory, Adc, 16-bit timers, SPI, SCI interface |
| U13 | ST232C SOP | STMicroelectronics 5 V powered multi-channel<br>RS-232 drivers and receivers |
| U14,U15 | SFH6156-2 | SMD Opto-coupler |
| Y1 | 16 MHz | Oscillator |

*Note: Resistors are 0.25 W unless specified*

# 4 Basics of DALI

DALI stands for "Digital Addressable Lighting Interface". It is a standard interface for lighting control solutions, defined by the main lighting manufacturers and standardized as IEC 929.

The DALI protocol is implemented on a master-slave architecture.

It uses the bi-phase Manchester asynchronous serial data format. All the bits of the frame are bi-phase encoded except the two stop bits. Following are some of the standard features:

- Transmission rate at 1.2 kHz.
- Bi-phase bit period is 833.33 µS ±10%.

A forward frame consists of 19 bi-phase encoded bits:

- 1 start bit (0->1: logical '1')
- 1 address byte (8-bit address)
- 1 data byte (8-bit data)
- 2 high level stop bits (no change of phase)

A backward frame consists of 11 bi-phase encoded bits:

- 1 start bit (0->1: logical '1')
- 1 data byte (8-bit data)
- 2 high level stop bits (no change of phase)

Each frame has 2 stop bits which do not contain any change of phase.

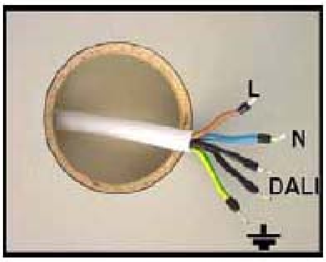
The setting time between two subsequent forward frames is 9.17 ms (minimum), while the delay between forward and backward frame goes from 2.92 ms to 9.17 ms. If a backward frame has not been started after 9.17 ms, this is interpreted as "no answer".

In the event of code violation, the frame is ignored and the system is ready again for data reception.

The main advantages of the DALI system can be summarized as follows:

- Simple wiring: all of the units in the system are interconnected using a simple five-core cable.

**Figure 20. Cable wiring**



- No mains switching required: lamps can be dimmed or switched on and off using control system commands without any need for mains switching.
- Easy system re-configuration: the configuration of the system can be changed quickly without any modification to the hardware.
- Easy system modification: if the lighting system needs to be enlarged, new components can be added anywhere on the DALI cable.
- It is possible to define light scenes. A scene means a particular light level intensity. 16 scenes can be defined at maximum.

**Figure 21. Master flowchart**

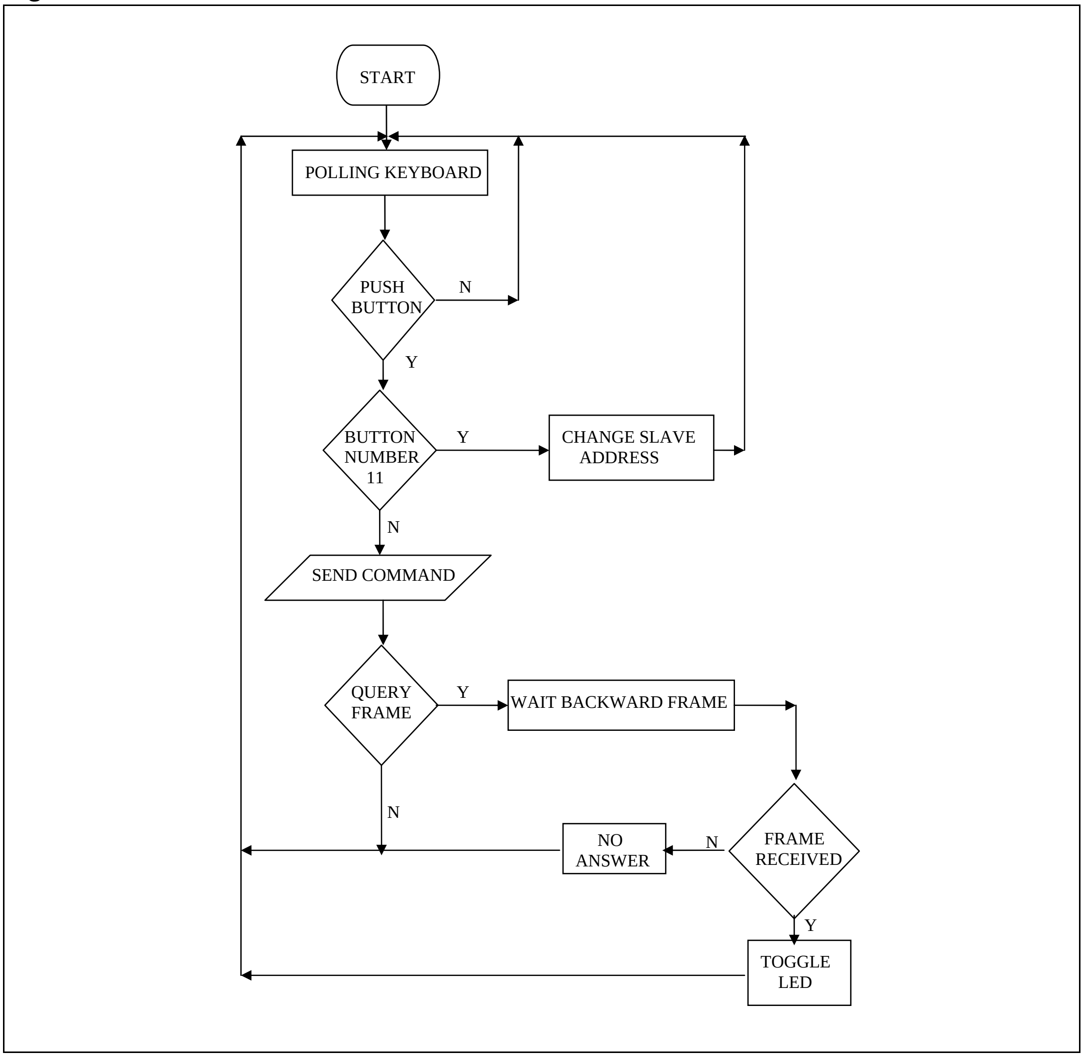
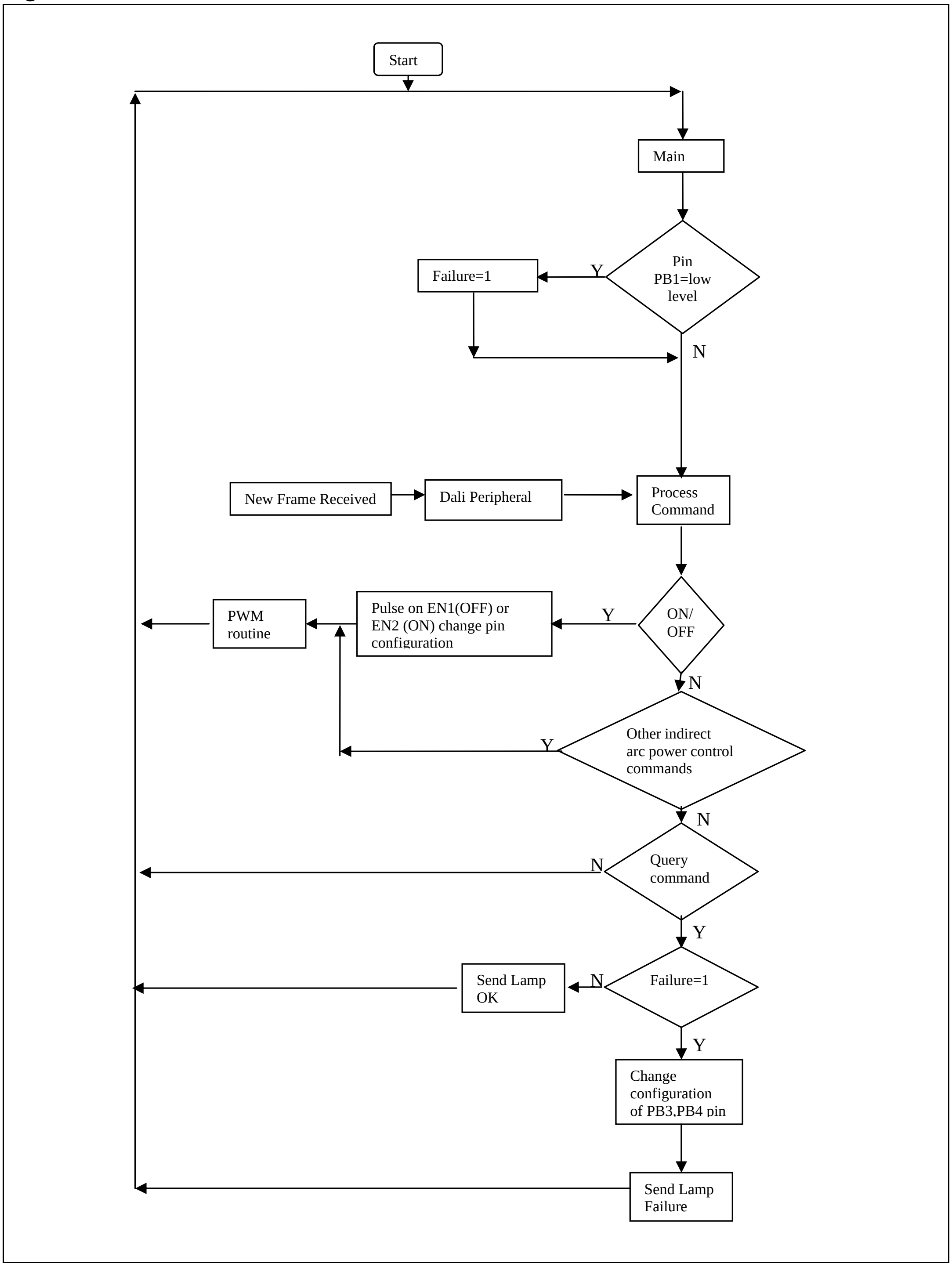


**Figure 22. Slave flowchart**



# 5 DALI master AC-DC adapter

This is an offline wide-range double-output SMPS based on the VIPer12A-E. The first output, 20 V at 100 mA, is dedicated to the bus communication allowing to address up to 64 slaves, while the second one delivers 5 V at 10 mA to the MASTER DALI microcontroller thanks to a linear post-regulator.

The VIPer12A-E combines on the same silicon chip a dedicated current mode PWM controller, a high voltage power MOSFET and the protection features (thermal, overcurrent, and overvoltage) which increases the converter reliability and saves size, parts count and cost.

The converter topology is an isolated flyback designed to work in discontinuous current mode according to the following specifications:

**Table 11. SMPS operating conditions**

| Parameter | Value |
|---|---|
| Input voltage range | 90 – 265 Vac |
| Input frequency range | 50/60 Hz |
| Output voltage 1 | V1=20 V |
| Output voltage 2 | V2=5 V |
| Output current 1 | I1=100 mA |
| Output current 2 | I2=10 mA |
| Output power (peak) | 2.2 W |
| Line regulation | +/- 1% |
| Load regulation | +/- 1% |
| EMI | EN55015 |

## 5.1 Adapter description

The schematic of the board is shown in *Figure 23*.

The AC input is rectified by the diodes bridge and then filtered by the bulk capacitor C1, and C2 to generate the high voltage DC.

The input EMI filter is a simple CLC PI filter for both differential and common mode noise suppression.

An NTC limits the inrush current and ensures a reliable operation of the bridge at startup.

The switching frequency is fixed at 60 kHz by the IC internal oscillator allowing optimization of the transformer size and cost. An RCD snubber circuit (R92, C59, D30) reduces the leakage inductance voltage spike and the voltage ringing on the drain pin of VIPer12A-E.

As soon as the voltage is applied on the input of the converter the high voltage startup current source connected to the drain pin is activated and starts to charge the Vdd capacitor C8 by a constant current of 1mA. When the voltage across this capacitor reaches the Vddon threshold (about 14 V) the VIPer12AS-E starts to switch. During normal operation the smart power IC is powered by the auxiliary winding of the transformer via the diode D31. No spike killer for the auxiliary voltage fluctuations is needed thanks to the wide range of the Vdd pin (9-38 V). The primary current is measured using the integrated current sensing for current mode operation.

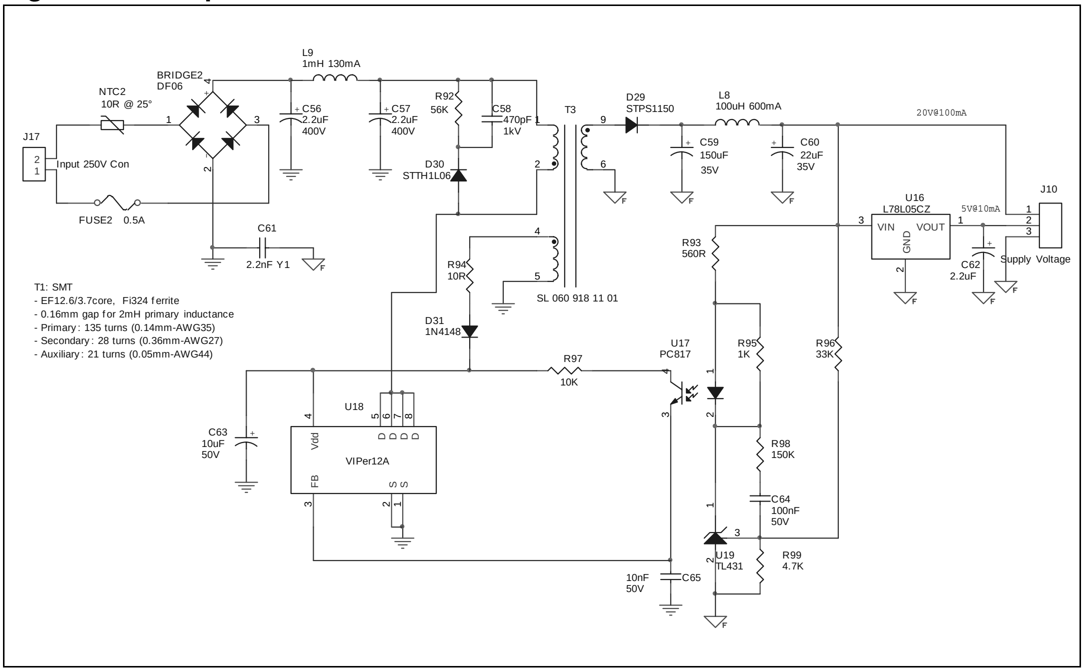
The output rectifier D29 has been chosen in accordance with the maximum reverse voltage and power dissipation. In particular a 1 A - 150 V power Schottky, type STPS1150, has been selected.

The output voltage regulation is performed by secondary feedback on the 20 V output while the 5 V output, is linearly post-regulated from the 20 V output. This operation is performed by a low drop voltage regulator, L78L05CZ, in the TO92 package. The feedback network consists of a programmable voltage reference, TL431, driving an optocoupler which ensures the required insulation between the primary and secondary sections. The optotransistor drives directly the VIPer12A-E feedback pin which controls the operation of the IC.

A small LC filter has been added on the 20 V output in order to reduce the high frequency ripple with reasonable output capacitor value.

The flyback transformer is a layer type based on the EF13 core and Fi 324 ferrite, manufactured by Vogt, and ensures safety insulation in accordance with the EN60950. *Figure 26* shows the main features of the transformer. The power supply has been implemented on a double-sided 35 µm PCB in FR-4, sizing 81 x 37 mm.

**Figure 23. Adapter schematic**



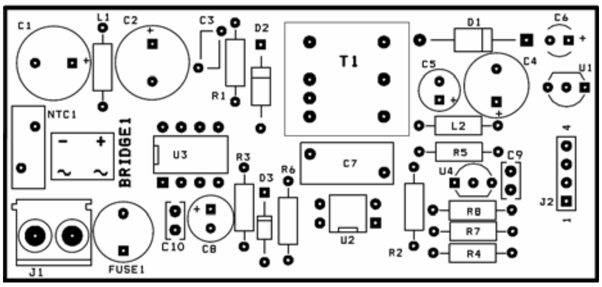



**Figure 24. Adapter PCB layout - top side - silkscreen (to scale)**

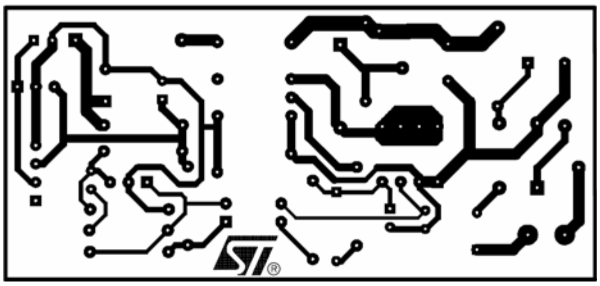
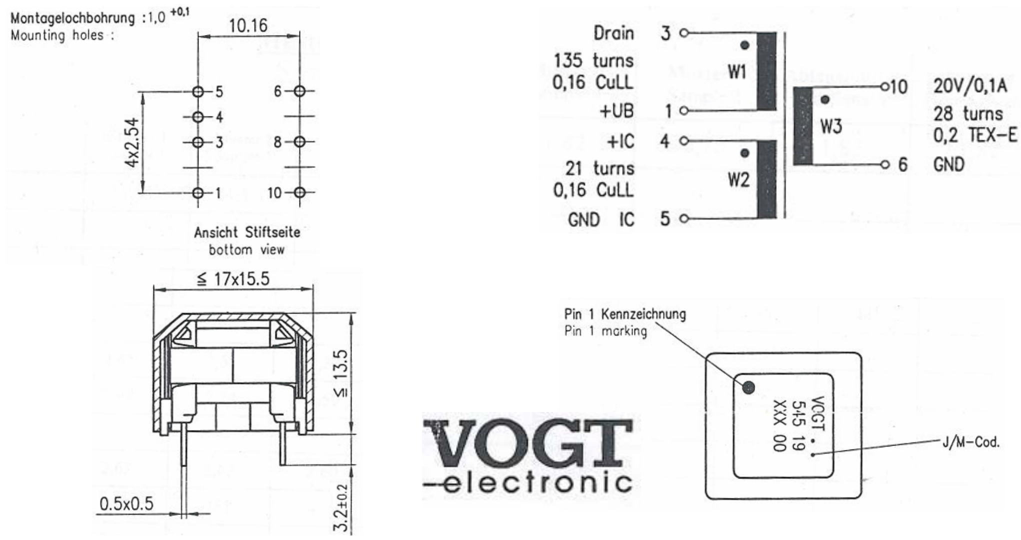


**Figure 25. Adapter PCB layout - bottom side - copper tracks (to scale)**

**Figure 26. Flyback transformer**




- Operating switching frequency: 60 kHz
- Core geometry: EF 12.6/3.7
- Core material: FI 324 or equivalent
- Primary inductance value: 2 mH
- Leakage inductance: 75 µH
- Air gap length: 0.16 mm
- Safety: EN60950

## 5.2 Adapter bill of material

Table 12. Adapter bill of material

| Reference | Value | Description |
|---|---|---|
| BRIDGE2 | DF06M 1 A 600 V | Bridge rectifier |
| C56,C57 | 2.2 µF 400 V | Electrolytic cap |
| C58 | 470 pF 1 kV | Ceramic cap |
| C59 | 150 µF 35 V | Low ESR electrolytic cap |
| C60 | 22 µF 35 V | Low ESR electrolytic cap |
| C61 | 2.2 nF Y1 | Y1 ceramic cap |
| C62 | 2.2 µF 25 V | Electrolytic cap |
| C63 | 10 µF 50 V | Electrolytic cap |
| C64 | 100 nF 50 V | Ceramic cap |
| C65 | 10 nF 50 V | Ceramic cap |
| D29 | STPS1150 | STMicroelectronics power Schottky rectifier 1 A 150 V |
| D30 | STTH1L06 | STMicroelectronics ultrafast high-voltage rectfifier 1 A 600 V |
| D31 | 1N4148 | Small signal rectifier 200 mA 100 V |
| FUSE2 | 0.5 A | Radial fuse |
| J10 | Supply voltage | 3-way single row shrouded header |
| J11 | Input 250 V connector | 2-way PCB screw terminal, 5.08 mm |
| L8 | 100 µH 600 mA | Axial inductor |
| L9 | 1 mH 130 mA | Axial inductor |
| NTC2 | 10 Ω @ 25° | Inrush current suppressor |
| R92 | 56 kΩ | Resistor, metal film 0.25 W |
| R93 | 560 Ω | Resistor, metal film 0.25W |
| R94 | 10 Ω | Resistor, metal film 0.25 W |
| R95 | 1 kΩ | Resistor, metal film 0.25 W |
| R96 | 33 kΩ | Resistor, metal film 0.25 W |
| R97 | 10 kΩ | Resistor, metal film 0.25 W |
| R98 | 150 kΩ | Resistor, metal film 0.25 W |
| R99 | 4.7 kΩ | Resistor, metal film 0.25 W |
| T3 | SL 060 918 11 01 | VOGT SMT |
| U16 | L78L05CZ TO92 | STMicroelectronics positive voltage regulator |
| U17 | PC817 | Sharp Optocoupler 5 kV |
| U18 | VIPer12A-E DIP8 | STMicroelectronics offline SMPS primary IC 730 V 0.4 A 27 Ω |
| U19 | TL431 TO92 | STMicroelectronics programmable voltage reference |

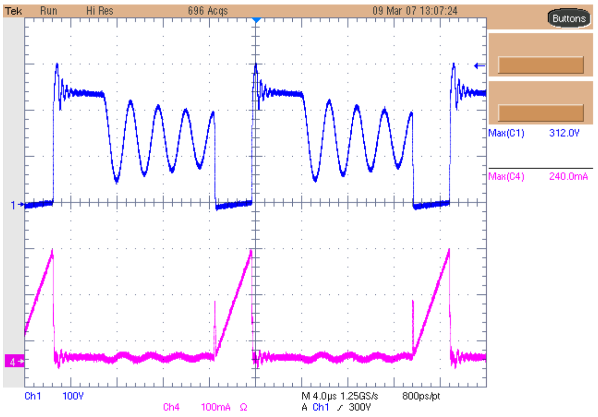
## 5.3 Adapter performances

Several tests have been performed on the board to evaluate the converter behavior in terms of efficiency, stability, safe operating area of the devices, line & load regulation and EMI performances.

### 5.3.1 Steady state tests

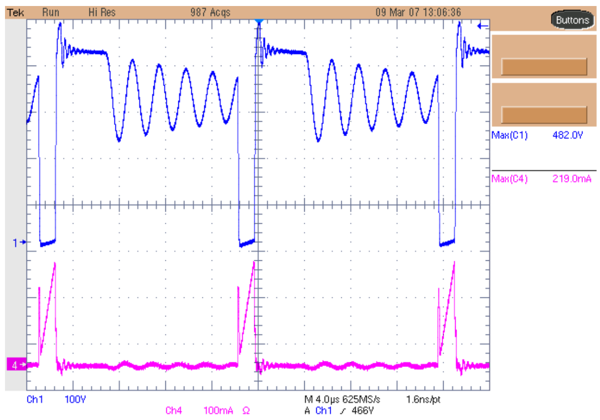
These tests have been performed at the input voltage of 110 Vac and 230 Vac at full and minimum load condition.

**Figure 27. VIPer12A-E steady state behavior at full load at 110 Vac - 60 Hz**




CH1 (blue): drain voltage
CH4 (purple): drain current

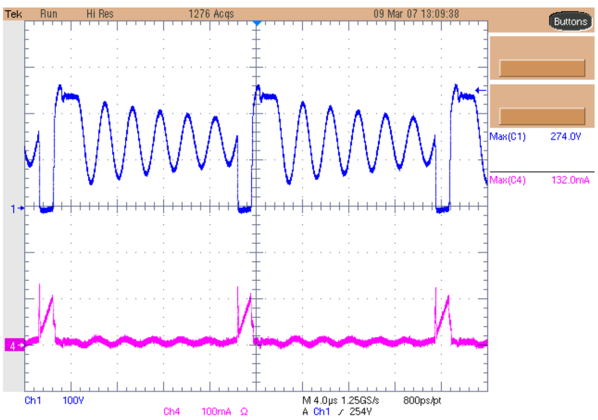
**Figure 28. VIPer12A-E steady state behavior at full load at 230 Vac - 50 Hz**




CH1 (blue): drain voltage
CH4 (purple): drain current

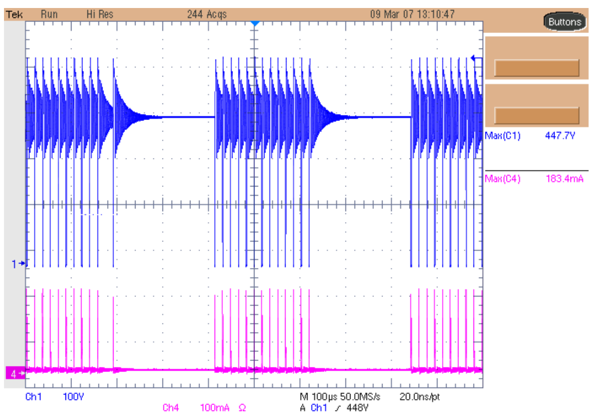
As shown by the waveforms the power supply operates in discontinuous current mode.

**Figure 29. VIPer12A-E steady state behavior at minimum load at 110 Vac - 60 Hz**




CH1 (blue): drain voltage
CH4 (purple): drain current

**Figure 30. VIPer12A-E steady state behavior at minimum load at 230 Vac - 50 Hz**



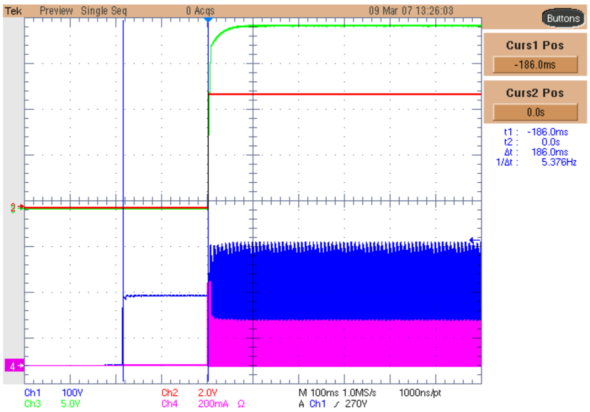

CH1 (blue): drain voltage
CH4 (purple): drain current

At minimum load the VIPer12A-E ensures the burst mode operation, saving the input power consumption.

### 5.3.2 Startup behavior

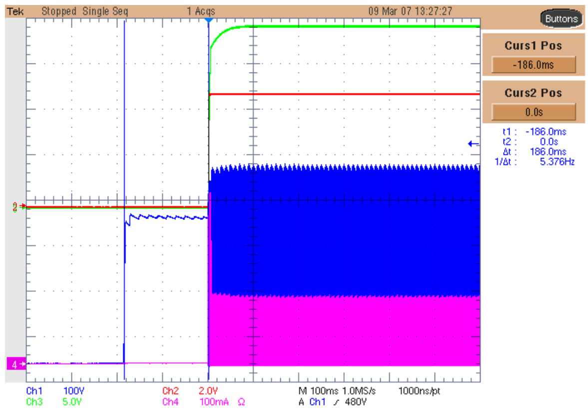
*Figure 31*, *32*, *33*, and *34* show the typical waveforms during the startup of the power supply. In particular, the full load condition is considered since it represents the heaviest case in terms of voltage and current stress, as well as the minimum load condition for loop stability and voltage stress.

**Figure 31. Startup waveforms at full load at 110 Vac - 60 Hz**



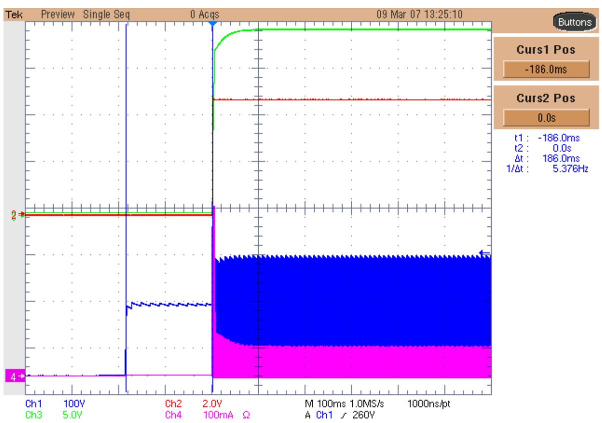

CH1 (blue): drain voltage
CH2 (red): 5 Vout
CH3 (green): 20 Vout
CH4 (purple): drain current

**Figure 32. Startup waveforms at full load at 230 Vac - 50 Hz**



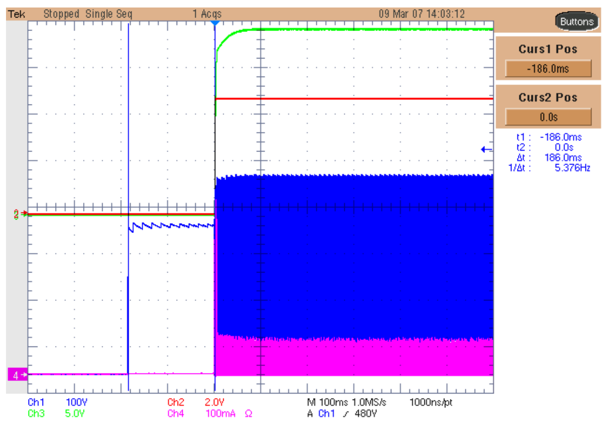

CH1 (blue): drain voltage
CH2 (red): 5 Vout
CH3 (green): 20 Vout
CH4 (purple): drain current

**Figure 33. Startup waveforms at minimum load at 110 Vac - 60 Hz**



CH1 (blue): drain voltage
CH2 (red): 5 Vout
CH3 (green): 20 Vout
CH4 (purple): drain current

**Figure 34. Startup waveforms at minimum load at 230 Vac - 50 Hz**



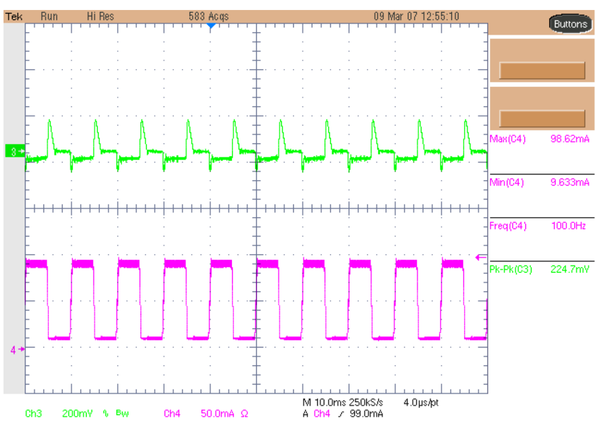
CH1 (blue): drain voltage
CH2 (red): 5 Vout
CH3 (green): 20 Vout
CH4 (purple): drain current

There is no overshoot on the output voltages and the measured wakeup time is 180 mS.

### 5.3.3 Dynamic load tests

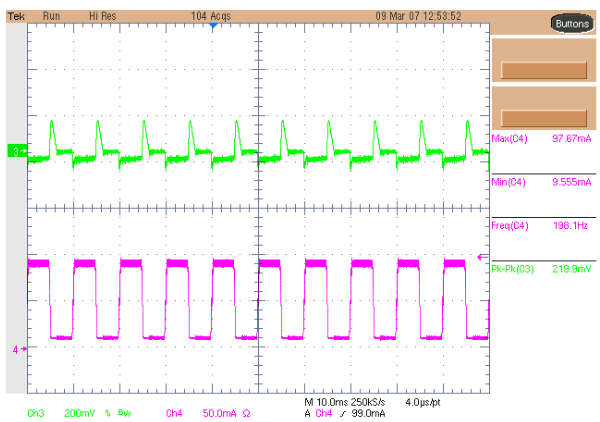
These tests show the transient load response at 110 Vac and 230 Vac mains when the 20 V output current is increased from 10% to 90% of the maximum value.

**Figure 35. Dynamic load waveforms at 110 Vac - 60 Hz**



CH3 (green): 20 Vout voltage ripple
CH4 (purple): 20 Vout current

**Figure 36. Dynamic load waveforms at 230 Vac - 50 Hz**



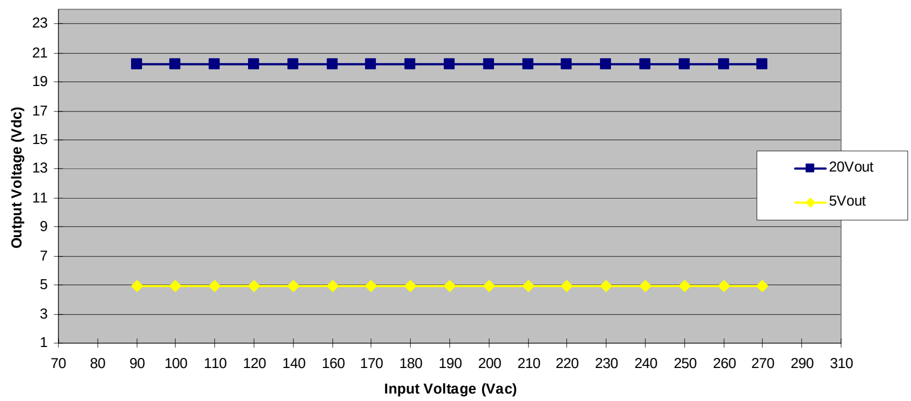
CH3 (green): 20 Vout voltage ripple
CH4 (purple): 20 Vout current

In the worst case the result is 224 mV or 1.12% of dynamic load regulation which indicates a very good dynamic behavior.

### 5.3.4 Line regulation

For this test the output power is kept at the peak value (2.2 W) while the line voltage is slowly increased from 85 Vac to 265 Vac. The board has a line regulation of +0.9%.

**Figure 37. Line regulation**

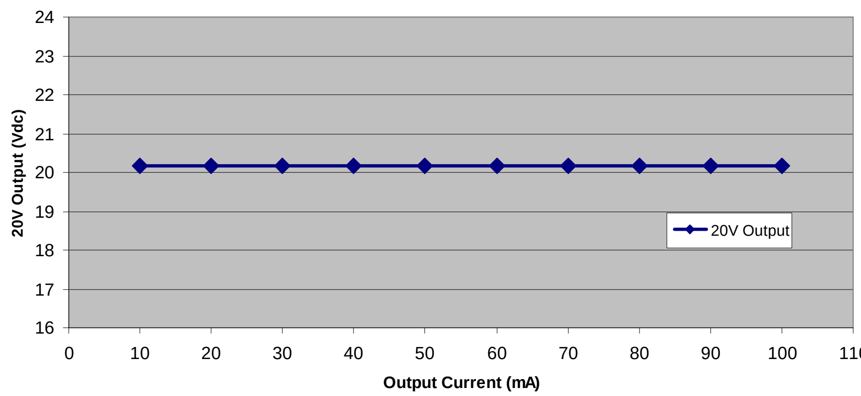



### 5.3.5 Load regulation

As the 5 V output is obtained by a linear regulator, the load regulation measurements have been performed only on 20 V output by changing its load from 10 mA to full load 100 mA. The input voltage is kept at the nominal value of 230 Vac.

The board has a load regulation of +0.9%.

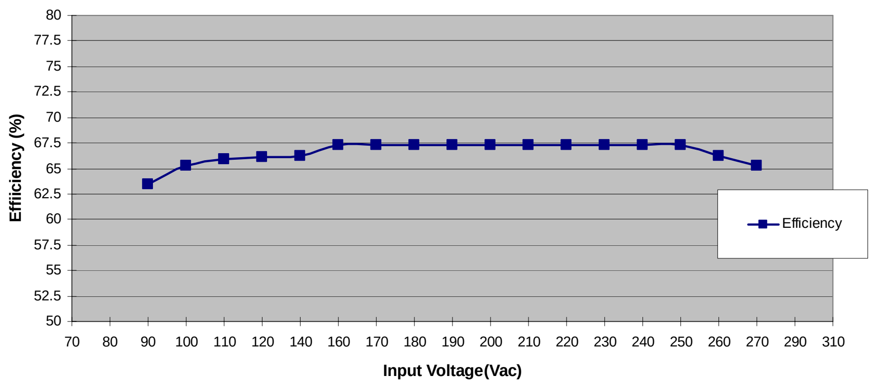
**Figure 38. Load regulation**



### 5.3.6 Efficiency variation

For this test the efficiency is measured when the line input is varied from 85 Vac to 264 Vac at full load. The average efficiency is 66.5%. A moderate value is typical of low power applications.

**Figure 39. Efficiency variations vs. input voltage at full load**




### 5.3.7 Conducted emissions test

Conducted emissions have been measured in neutral and line wires, using peak detector and considering the limits for lighting applications i.e. EN55015. The measurements have been performed at 110 Vac and 230 Vac line with fully loaded outputs. The results are shown in *Figure 40*, *41*, *42*, and *43*.

Since the emission level is below both the quasi-peak and average limits with acceptable margin, the power supply passes the pre-compliance test.

**Figure 40. Conducted emissions at 110 Vac 60 Hz - full load - line 1 peak detector**

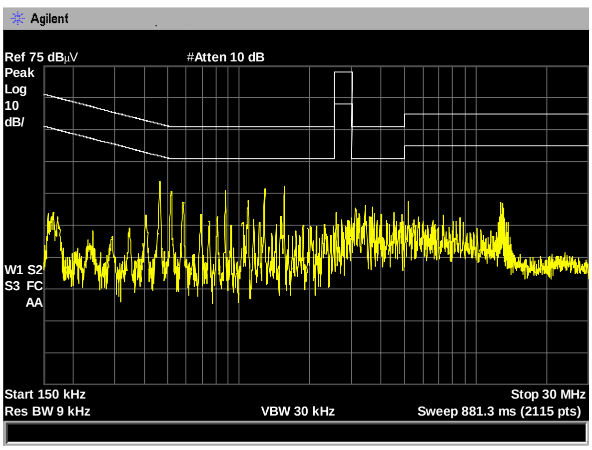



**Figure 41. Conducted emissions at 110 Vac 60 Hz - full load - line 2 peak detector**

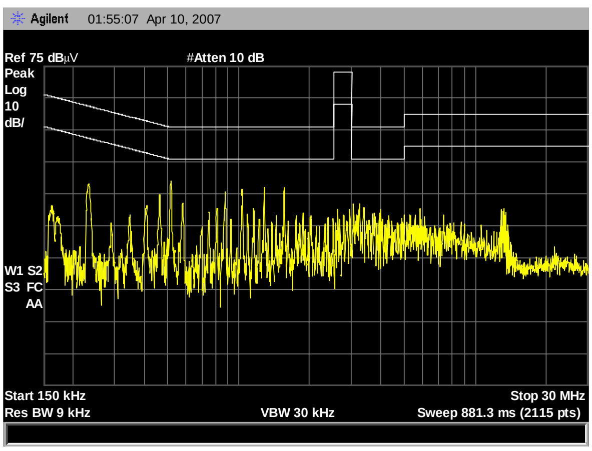


**Figure 42. Conducted emissions at 230 Vac 50 Hz - full load - line 1 peak detector**

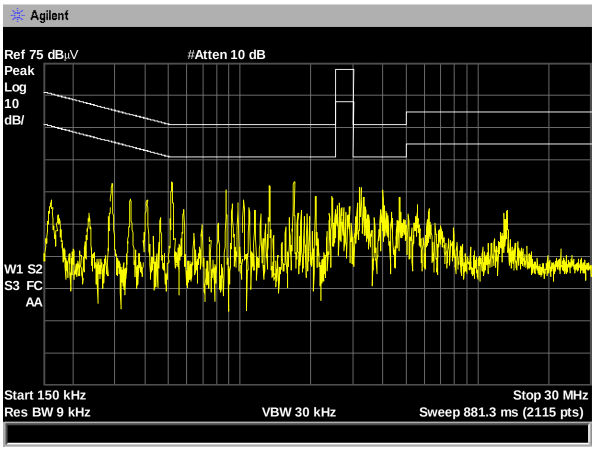
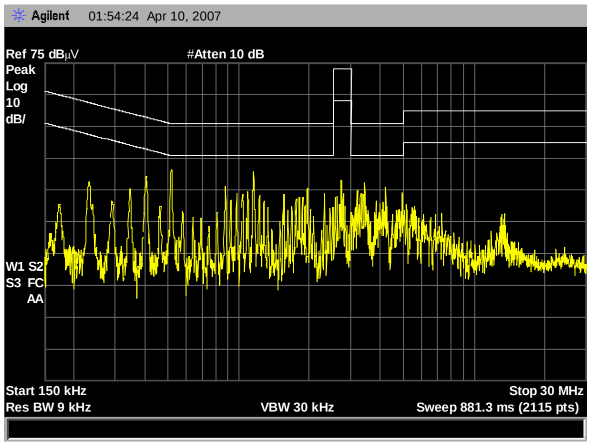



**Figure 43. Conducted emissions at 230 Vac 50 Hz - full load - line 2 peak detector**




# 6 References

1. "L6561, enhanced transition mode power factor corrector" (AN966)
2. "Switching from the L6561 to the L6562" (AN1757)
3. "Control loop modelling of L6561-based TM PFC" (AN1089)
4. "Electronic Ballast With Pfc Using L6574 And L6561" (AN993)
5. "Choosing A Dali Implementation Strategy With ST7DALI" (AN1756)
6. "Hardware Implementation for ST7DALI-EVAL" (AN1900)

# 7 Revision history

**Table 13. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-Mar-2008 | 1 | Initial release |

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