

True low-power platform (58.3 $\mu\text{A}/\text{MHz}$, and 0.64 μA for operation with only LVD) for the general-purpose applications, with 1.6-V to 5.5-V operation, 16-Kbyte code flash memory, and 33 DMIPS at 24 MHz

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- $V_{DD} = 1.6 \text{ V to } 5.5 \text{ V}$
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 μs : @ 24 MHz operation with high-speed on-chip oscillator) to ultra-low speed (66.6 μs : @ 15 kHz operation with low-speed on-chip oscillator clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 Mbytes
- General-purpose registers: (8-bit register $\times 8$) \times 4 banks
- On-chip RAM: 1.5 Kbytes

Code flash memory

- Code flash memory: 16 Kbytes
- Block size: 1 Kbytes
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 2 Kbytes
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD} = 1.8 \text{ to } 5.5 \text{ V}$

High-speed on-chip oscillator

- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: $\pm 1.0\%$ ($V_{DD} = 1.8 \text{ to } 5.5 \text{ V}$, $T_A = -20 \text{ to } +85^\circ\text{C}$)

Middle-speed on-chip oscillator

- Selectable from 4 MHz, 2 MHz, and 1 MHz.

Operating ambient temperature

- $T_A = -40 \text{ to } +85^\circ\text{C}$ (A: Consumer applications)
- $T_A = -40 \text{ to } +105^\circ\text{C}$ (G: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event link controller (ELC)

- Event signals of 18 types can be linked to the specified peripheral function.

Serial interfaces

- CSI: 4 channels
- UART: 2 channel
- I²C/simplified I²C: 4 channels
- Multimaster I²C: 2 channels

Timers

- 16-bit timer (TAU): 4 channels
- TKB: 1 channel
- 12-bit interval timer: 1 channel
- 8-bit interval timer: 2 channels
- Watchdog timer: 1 channel

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 10 to 11 channels
- Internal reference voltage (1.45 V) and temperature sensor

D/A converter

- 8/10-bit resolution D/A converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 2 channels (channel 1: output to the ANO1 pin, channel 0: output to the comparator)
- Output voltage: 0 V to V_{DD}
- Real-time output function

Comparator

- 2 channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode

PGA

- 1 channels

I/O ports

- I/O port: 17 to 21 (N-ch open drain I/O [V_{DD} withstand voltage^{Note 1}/EV_{DD} withstand voltage^{Note 2}]: 10 to 14)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3.0 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit
- On-chip data operation circuit

Note 1. 16, 20, 24-pin products

Note 2. 25-pin products

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G11 | | | | |
|-----------|------------|--------|----------|----------|----------|----------|----------|
| | | | 10 pins | 16 pins | 20 pins | 24 pins | 25 pins |
| 16 KB | 2 KB | 1.5 KB | R5F1051A | R5F1054A | R5F1056A | R5F1057A | R5F1058A |

Remark The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

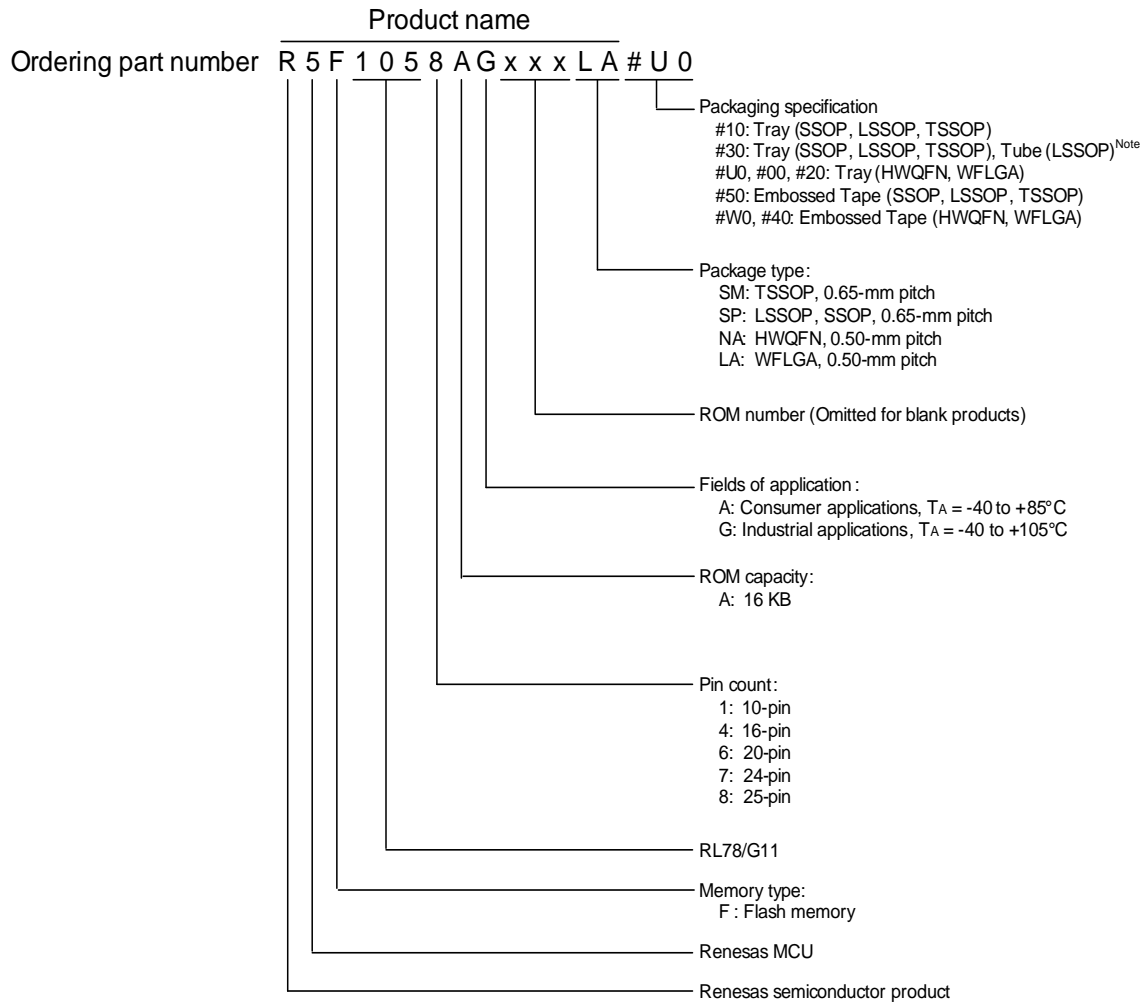
R5F105xA (x = 1, 4, 6, 7, 8): Start address FF900H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.2 Ordering Information

<R>

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11



Note The packaging specification is only "Tube" for products in the 20-pin LSSOP.

<R>

| Pin Count | Package | Ordering Part Number | | RENESAS Code |
|-----------|---|--------------------------|--------------------------|--------------|
| | | Product Name | Packaging Specifications | |
| 10 pins | 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65-mm pitch) | R5F1051AGSP, R5F1051AASP | #10, #30, #50 | PLSP0010JA-A |
| 16 pins | 16-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch) | R5F1054AGSP, R5F1054AASP | #10, #30, #50 | PRSP0016JC-B |
| | 16-pin plastic HWQFN (3 × 3 mm, 0.50-mm pitch) | R5F1054AGNA, R5F1054AANA | #00, #20, #40 | PWQN0016KD-A |
| 20 pins | 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch) | R5F1056AGSP, R5F1056AASP | #30, #50 | PLSP0020JB-A |
| | 20-pin plastic TSSOP (4.4 × 6.5 mm, 0.65-mm pitch) | R5F1056AGSM, R5F1056AASM | #10, #30, #50 | PTSP0020JI-A |
| 24 pins | 24-pin plastic HWQFN (4 × 4 mm, 0.50-mm pitch) | R5F1057AGNA, R5F1057AANA | #U0, #W0 | PWQN0024KE-A |
| | | R5F1057AGNA, R5F1057AANA | #00, #20, #40 | PWQN0024KF-A |
| 25 pins | 25-pin plastic WFLGA (3 × 3 mm, 0.50-mm pitch) | R5F1058AGLA, R5F1058AALA | #U0, #W0 | PWLG0025KA-A |

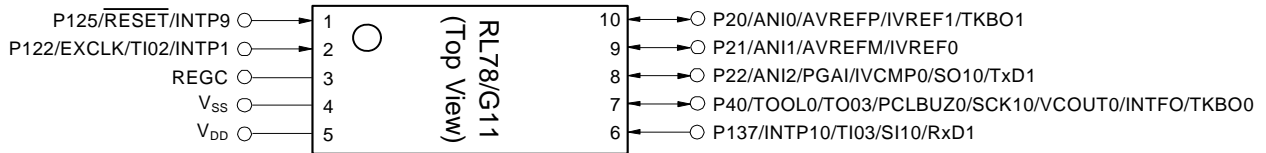
Caution 1. For the fields of application, refer to Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11.

Caution 2. The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

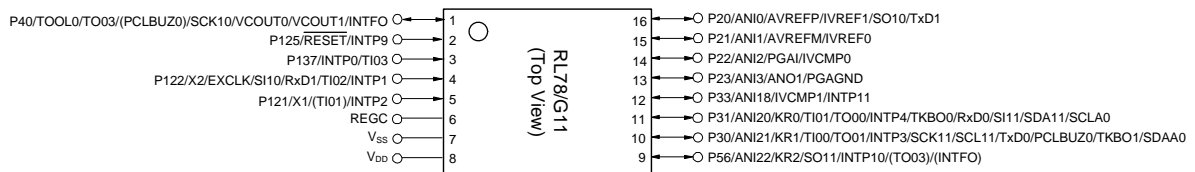
1.3.1 10-pin products

- 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65-mm pitch)



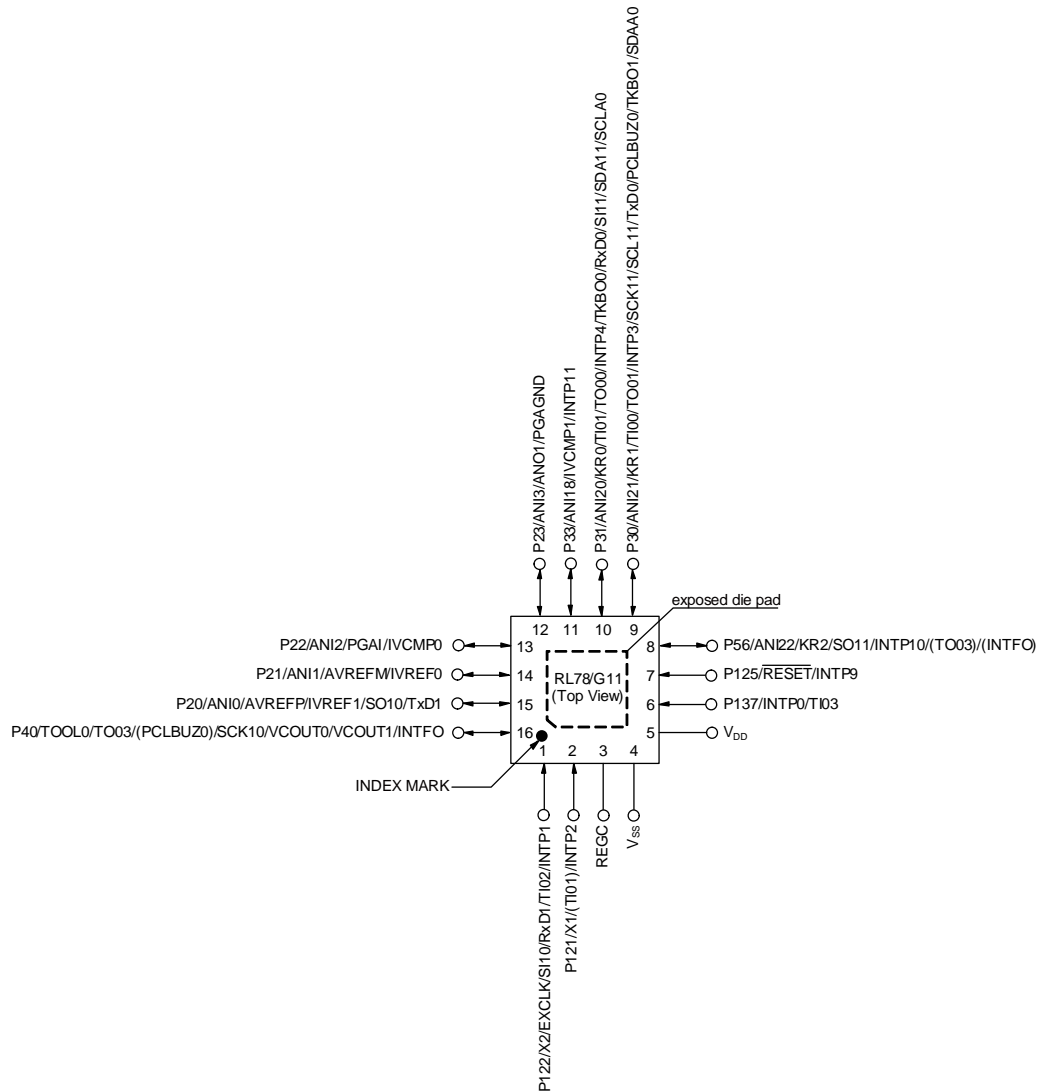
1.3.2 16-pin products

- 16-pin plastic SSOP (4.4 × 5.0 mm, 0.65-mm pitch)



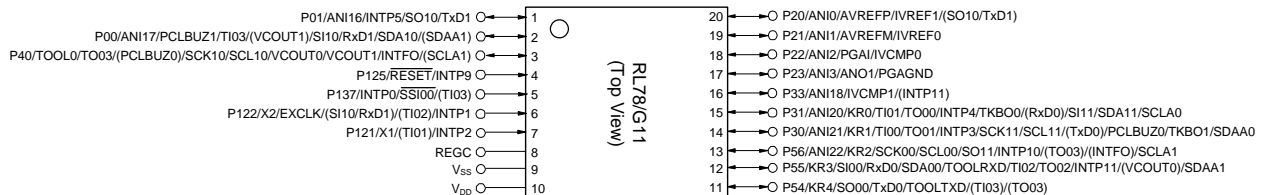
<R>

- 16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)



1.3.3 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)
- 20-pin plastic TSSOP (4.4 × 6.5 mm, 0.65-mm pitch)



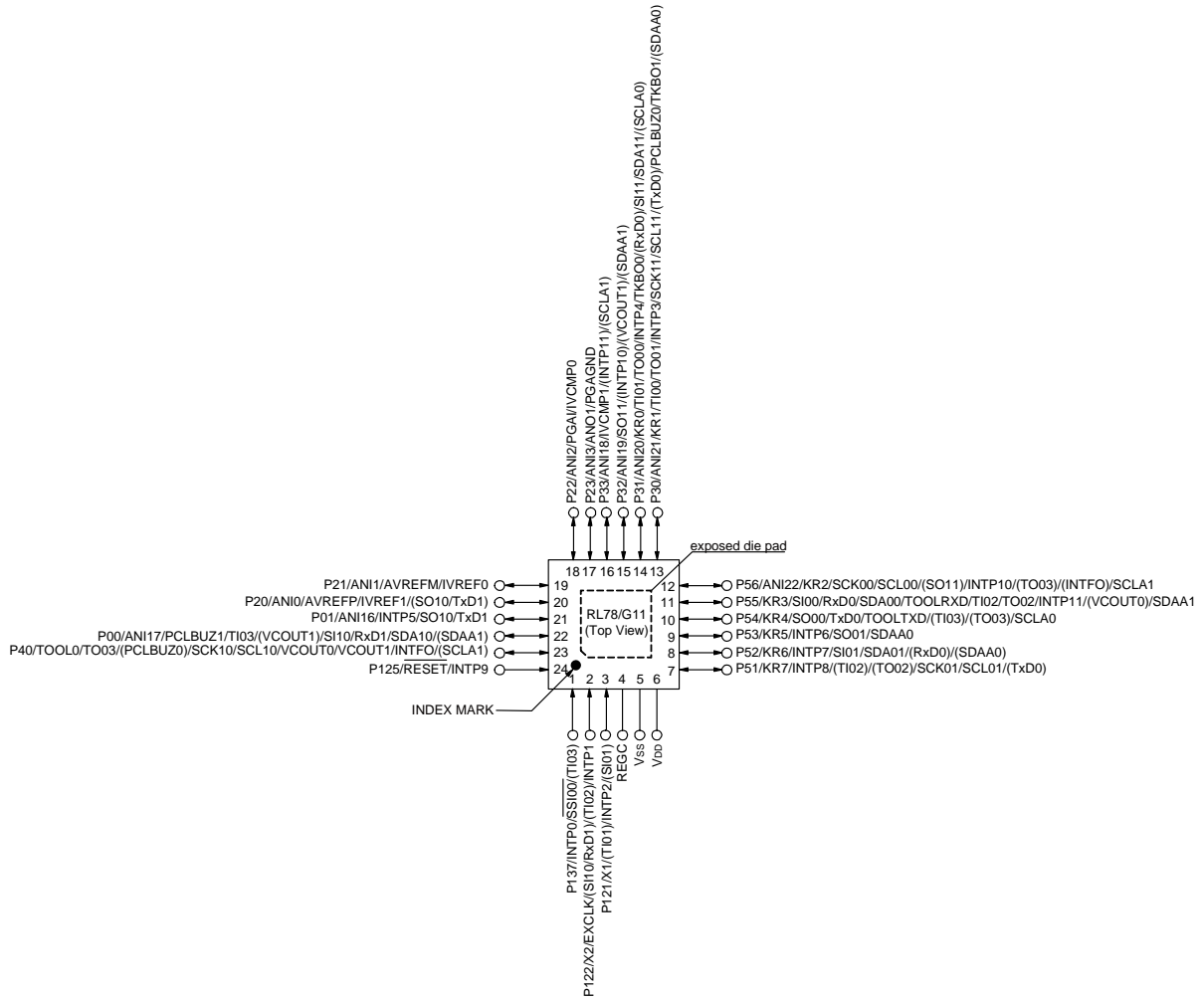
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

1.3.4 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5-mm pitch)



Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

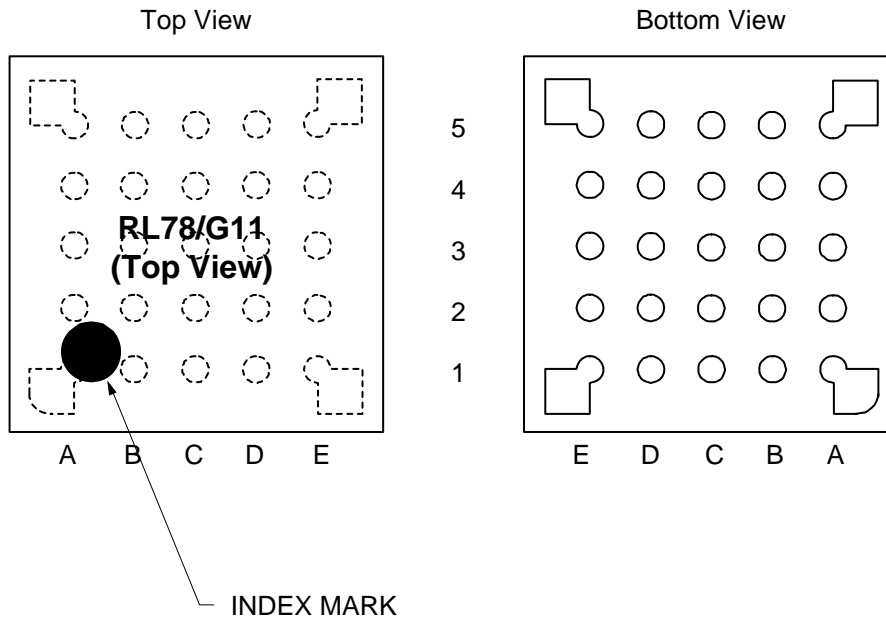
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. It is recommended to connect an exposed die pad to Vss.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

1.3.5 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.5-mm pitch)



| | A | B | C | D | E | |
|---|---|---|--|---|--|---|
| 5 | P40/TOOL0/TO03/(PC LBUZ0)/SCK10/SCL10/VCOU0/VCOU1/INTFO/(SCLA1) | P125/RESET/INTP9 | P01/ANI16/INTP5/SO10/TxD1 | P20/ANI0/AVREFP/IVREF1/(SO10/TxD1) | P21/ANI1/AVREFM/IVREF0 | 5 |
| 4 | P122/X2/EXCLK/(SI10/RxD1)/(TI02)/INTP1 | P137/INTP0/SSI00/(TI03) | P00/ANI17/PCLBUZ1/TI03/(VCOU1)/SI10/RxD1/SDA10/(SDAA1) | P22/ANI2/PGAI/IVCMP0 | P23/ANI3/ANO1/PGA GND | 4 |
| 3 | P121/X1/(TI01)/INTP2/(SI01) | V _{DD} | EV _{DD} | P33/ANI18/IVCMP1/(INTP11)/(SCLA1) | P32/ANI19/SO11/(INTP10)/(VCOU1)/(SDAA1) | 3 |
| 2 | REGC | V _{SS} | P30/ANI21/KR1/TI00/TO01/INTP3/SCK11/SCL11/(TxD0)/PCLBUZ0/TKBO1/(SDAA0) | P31/ANI20/KR0/TI01/TO00/INTP4/TKBO0/(RxD0)/SI11/SDA11/(SCLA0) | P56/ANI22/KR2/SCK00/SCL00/(SO11)/INTP10/(TO03)/(INTFO)/SCLA1 | 2 |
| 1 | P51/KR7/INTP8/(TI02)/(TO02)/SCK01/SCL01/(TxD0) | P52/KR6/INTP7/SI01/SDA01/(RxD0)/(SDAA0) | P53/KR5/INTP6/SO01/SDAA0 | P54/KR4/SO00/TxD0/TOOLTxD/(TI03)/(TO03)/SCLA0 | P55/KR3/SI00/RxD0/SDA00/TOOLRXD/TI02/TO02/INTP11/(VCOU0)/SDAA1 | 1 |
| | A | B | C | D | E | |

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

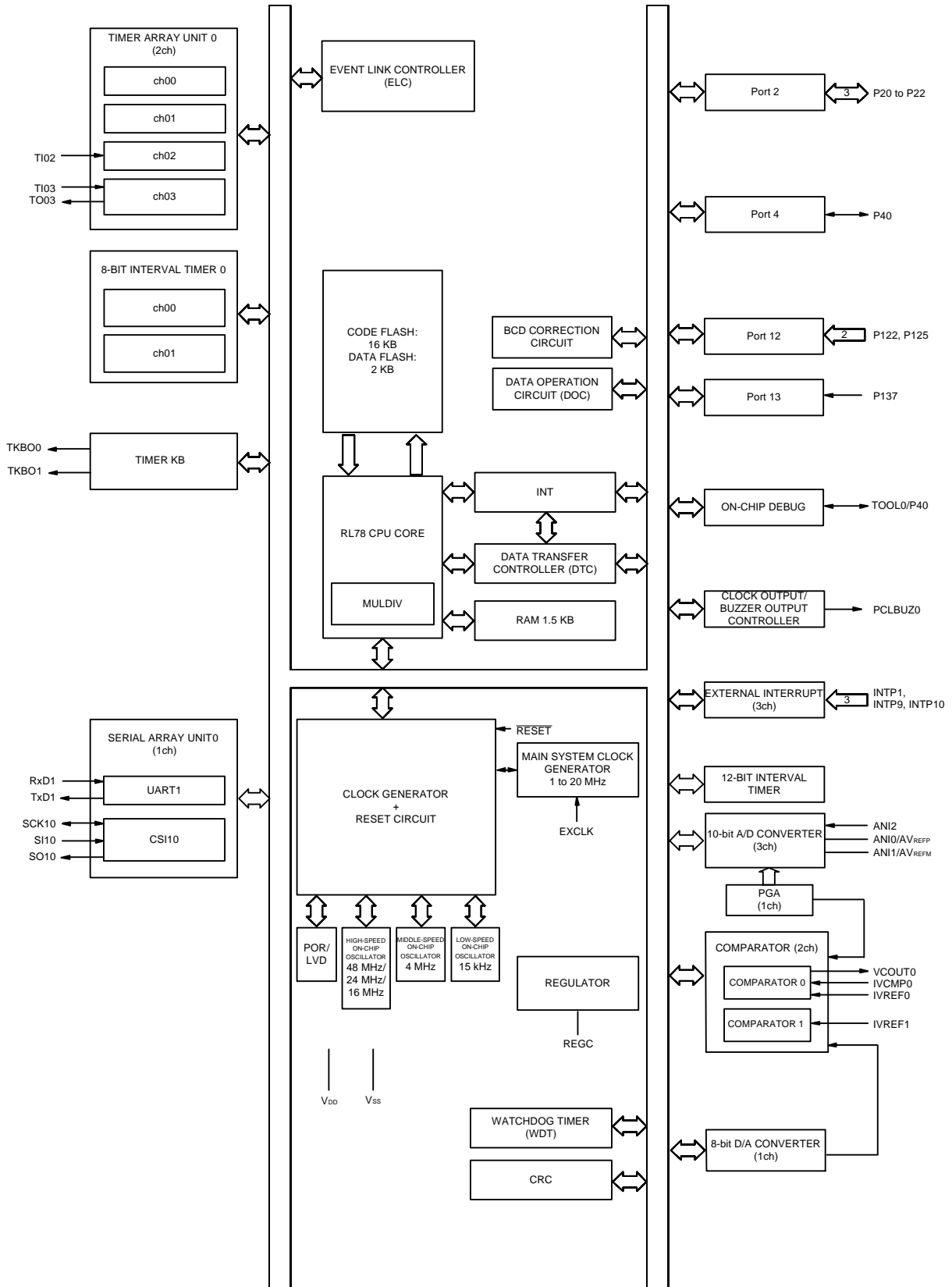
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

1.4 Pin Identification

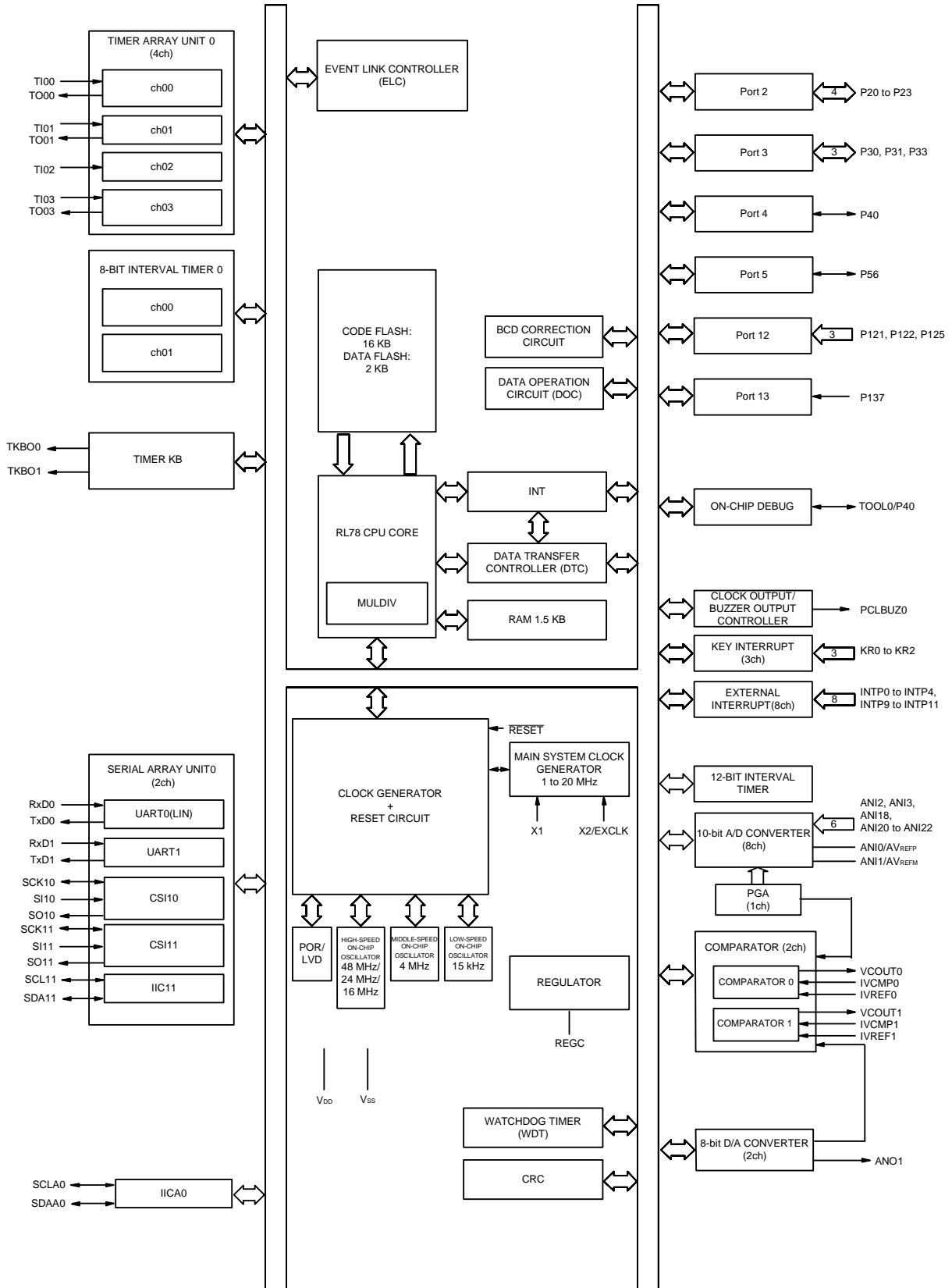
| | | | |
|------------------|--|-------------------------------|---|
| ANI0 to ANI3, | | PCLBUZ0, PCLBUZ1 | : Programmable clock output/buzzer output |
| ANI16 to ANI22 | : Analog input | REGC | : Regulator capacitance |
| ANO1 | : Analog output | $\overline{\text{RESET}}$ | : Reset |
| AVREFM | : A/D converter reference potential (- side) input | RxD0, RxD1 | : Receive data |
| AVREFP | : A/D converter reference potential (+ side) input | SCK00, SCK01, SCK10, SCK11 | : Serial clock input/output |
| EVDD | : Power supply | SCLA0, SCLA1 | : Serial clock input/output |
| EXCLK | : External clock input (main system clock) | SCL00, SCL01, SCL10, SCL11 | : Serial clock output |
| INTP0 to INTP11 | : External interrupt input | SDAA0, SDAA1 | : Serial data input/output |
| INTFO | : Interrupt Flag output | SDA00, SDA01, SDA10, SDA11 | : Serial data input/output |
| IVCMP0, IVCMP1 | : Comparator input | SI00, SI01, SI10, SI11 | : Serial data input |
| IVREF0, IVREF1 | : Comparator reference input | SO00, SO01, SO10, SO11 | : Serial data output |
| KR0 to KR7 | : Key return | $\overline{\text{SSI00}}$ | : Serial interface chip select input |
| PGAI, PGAGND | : PGA Input | TI00 to TI03 | : Timer input |
| P00 to P01 | : Port 0 | TKBO0, TKBO1 | : TMKB output |
| P20 to P23 | : Port 2 | TO00 to TO03 | : Timer output |
| P30 to P33 | : Port 3 | TOOL0 | : Data input/output for tool |
| P40 | : Port 4 | TOOLRXD, TOOLTXD | : Data input/output for external device |
| P51 to P56 | : Port 5 | TxD0, TxD1 | : Transmit data |
| P121, P122, P125 | : Port 12 | VCOUT0, VCOUT1 | : Comparator output |
| P137 | : Port 13 | VDD | : Power supply |
| | | VSS | : Ground |
| | | X1, X2 | : Crystal oscillator (main system clock) |

1.5 Block Diagram

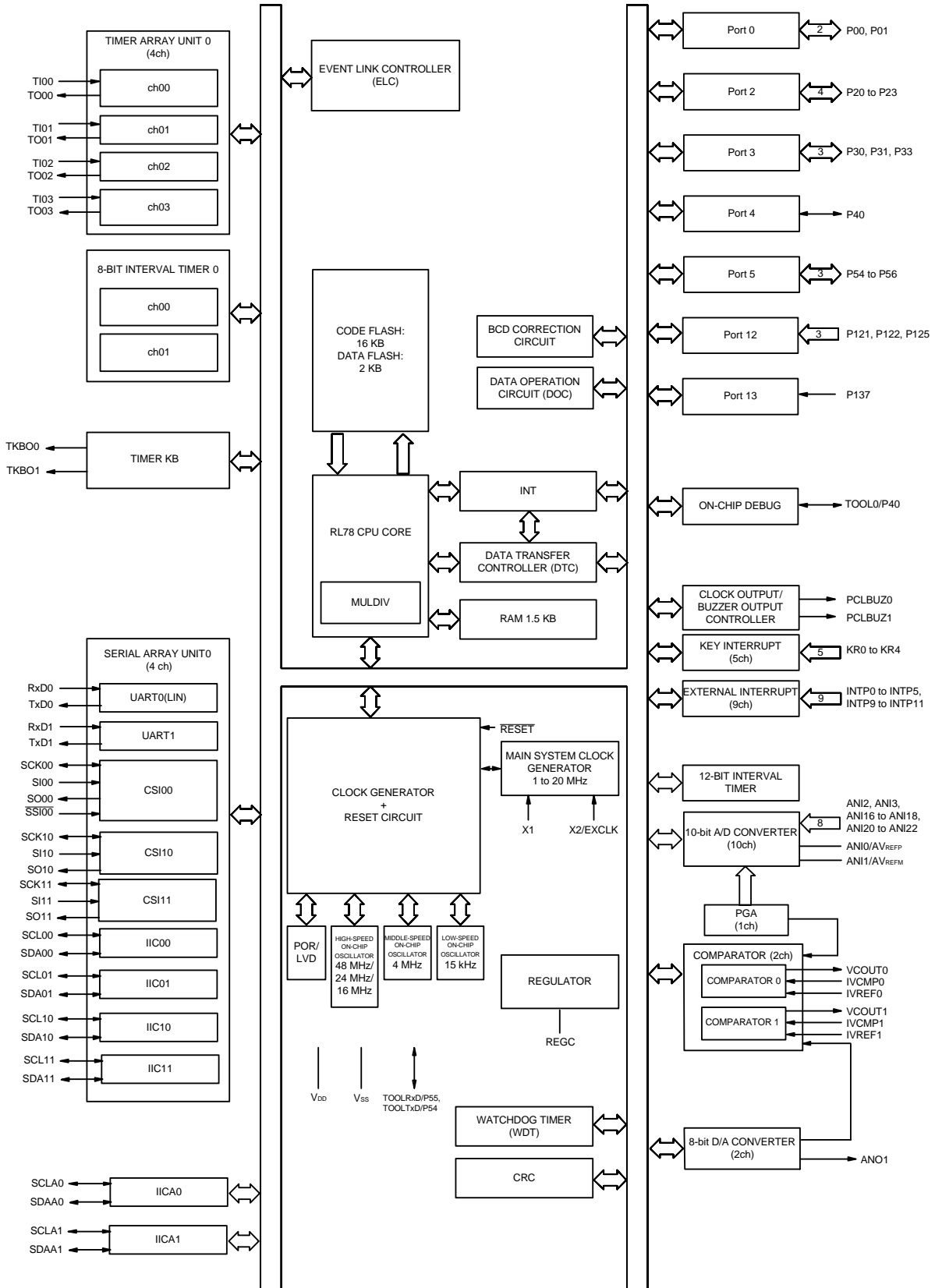
1.5.1 10-pin products



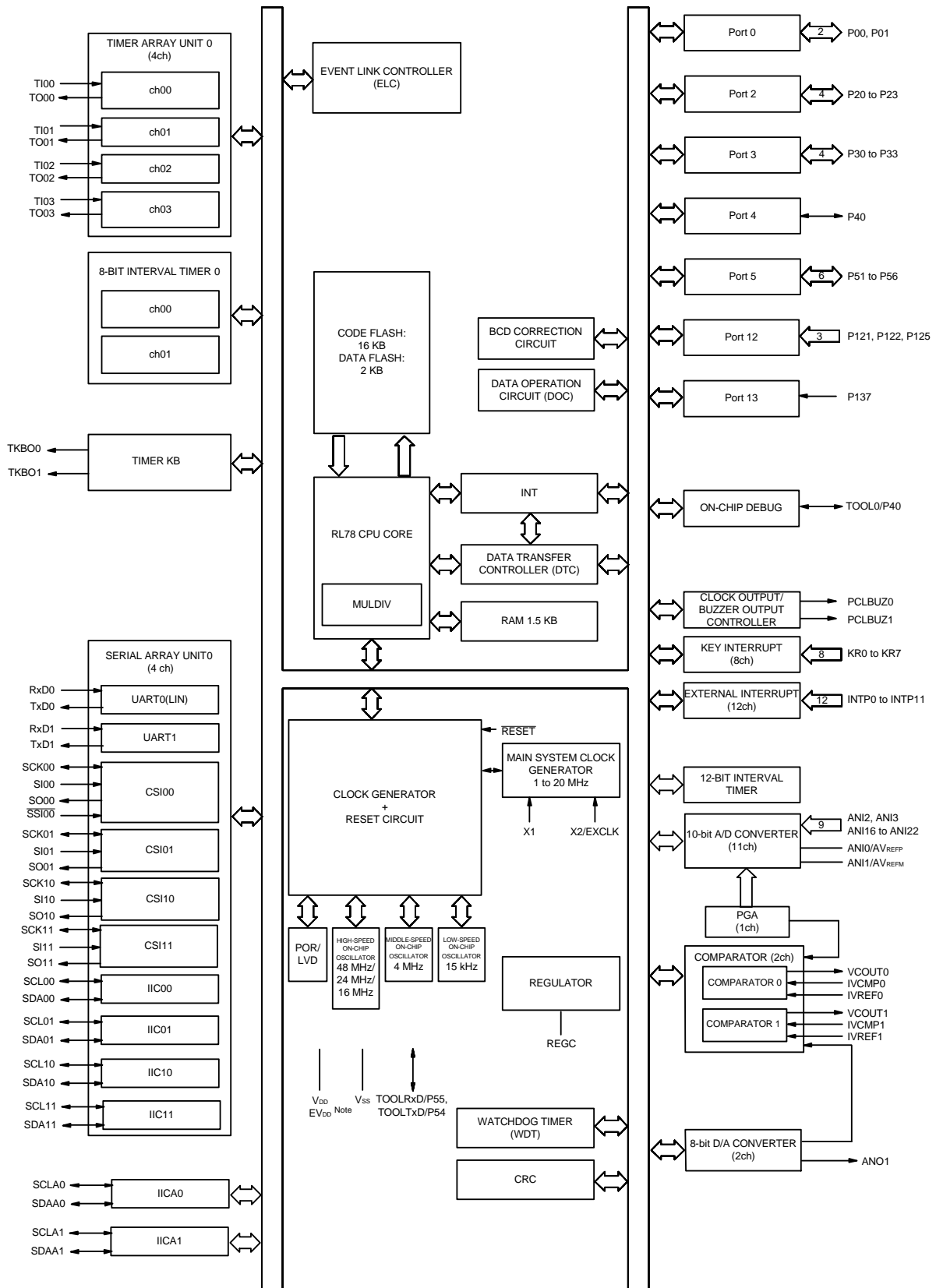
1.5.2 16-pin products



1.5.3 20-pin products



1.5.4 24-pin, 25-pin products



Note 25-pin products

1.6 Outline of Functions

This outline describes the functions at the time when Peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3) are set to 00H.

(1/2)

| Item | | 10-pin | 16-pin | 20-pin | 24-pin | 25-pin |
|------------------------------------|--|--|----------|----------|----------|----------|
| | | R5F1051A | R5F1054A | R5F1056A | R5F1057A | R5F1058A |
| Code flash memory (KB) | | 16 Kbytes | | | | |
| Data flash memory (KB) | | 2 Kbytes | | | | |
| RAM | | 1.5 Kbytes | | | | |
| Address space | | 1 Mbytes | | | | |
| Main system clock | High-speed system clock (f _{MX}) | X1 (crystal/ceramic) oscillation ^{Note} , external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V 1 to 16 MHz: V _{DD} = 2.4 to 5.5 V 1 to 8 MHz: V _{DD} = 1.8 to 5.5 V 1 to 4 MHz: V _{DD} = 1.6 to 5.5 V | | | | |
| | High-speed on-chip oscillator clock (f _{IH}) Max: 24 MHz | HS (High-speed main) mode: 1 to 24 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V), LP (Low-power main) mode: 1 MHz (V _{DD} = 1.8 to 5.5 V) | | | | |
| | Middle-speed on-chip oscillator clock (f _{IM}) Max: 4 MHz | LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V), LP (Low-power main) mode: 1 MHz (V _{DD} = 1.8 to 5.5 V) | | | | |
| Subsystem clock | Low-speed on-chip oscillator clock (f _{IL}) | 15 kHz (typ.): V _{DD} = 1.6 to 5.5 V | | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | | |
| Minimum instruction execution time | | 0.04167 μs (High-speed on-chip oscillator clock: f _{IH} = 24 MHz operation) | | | | |
| | | 0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation) | | | | |
| Instruction set | | <ul style="list-style-type: none"> Data transfer (8/16 bits) Adder and subtractor/logical operation (8/16 bits) Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) Multiplication and Accumulation (16 bits × 16 bits + 32 bits) Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | |
| I/O port | Total | 7 | 13 | 17 | 21 | |
| | CMOS I/O | 4 | 9 | 13 | 17 | |
| | CMOS input | 3 | 4 | | | |
| Timer | 16-bit timer | 4 channels | | | | |
| | Watchdog timer | 1 channel | | | | |
| | Timer KB | 1 channel | | | | |
| | 12-bit interval timer | 1 channel | | | | |
| | 8/16-bit interval timer | 2 channels (8 bit)/1 channel (16 bit) | | | | |
| | Timer output | 3 | 5 | 6 | | |

Note 16, 20, 24, 25-pin products

Caution The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F105xA (x = 1, 4, 6, 7, 8): Start address FF900H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

(2/2)

| Item | 10-pin | | 16-pin | | 20-pin | | 24-pin | | 25-pin | |
|---------------------------------|--|------------------------------|--|------------|--|-------------|--|-------------|----------|--|
| | R5F1051A | | R5F1054A | | R5F1056A | | R5F1057A | | R5F1058A | |
| Clock output/buzzer output | 1 | | | | 2 | | | | | |
| | <ul style="list-style-type: none"> 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) 117 Hz, 234 Hz, 469 Hz, 938 Hz, 1.875 kHz, 3.75 kHz, 7.5 kHz (subsystem clock: $f_{IL} = 15$ kHz operation) | | | | | | | | | |
| 10-bit resolution A/D converter | External | 3 channels | | 8 channels | | 10 channels | | 11 channels | | |
| | Internal | 1 channel | | | | | | | | |
| 8-bit D/A converter | 1 channel | | | 2 channels | | | | | | |
| Comparator (Window Comparator) | 1 channel | | | 2 channels | | | | | | |
| PGA | 1 channel | | | | | | | | | |
| Data Operation Circuit (DOC) | Comparison, addition, and subtraction of 16-bit data | | | | | | | | | |
| Serial interface | [10-pin products] <ul style="list-style-type: none"> CSI: 1 channel/UART: 1 channel [16-pin products] <ul style="list-style-type: none"> CSI: 2 channels/UART: 2 channels/simplified I²C: 1 channel [20-pin products] <ul style="list-style-type: none"> CSI: 3 channel/UART: 2 channel/simplified I²C: 3 channel [24-pin, 25-pin products] <ul style="list-style-type: none"> CSI: 4 channels/UART: 2 channel/simplified I²C: 4 channels | | | | | | | | | |
| | I ² C bus | None | | 1 channel | | 2 channels | | | | |
| Data transfer controller (DTC) | 13 sources | | 22 sources | | 23 sources | | 24 sources | | | |
| Event link controller (ELC) | Event input: 11 Event trigger output: 3 | | Event input: 16 Event trigger output: 4 | | Event input: 17 Event trigger output: 4 | | Event input: 18 Event trigger output: 4 | | | |
| Vectored interrupt sources | Internal | 20 | | 24 | | 25 | | | | |
| | External | 3 | | 9 | | 10 | | 13 | | |
| Key interrupt | None | | 3 | | 5 | | 8 | | | |
| Reset | <ul style="list-style-type: none"> Reset by \overline{RESET} pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution Internal reset by RAM parity error Internal reset by illegal-memory access | | | | | | | | | |
| Power-on-reset circuit | <ul style="list-style-type: none"> Power-on-reset: $1.51 \pm 0.04V$ ($T_A = -40$ to $+85^\circ C$) $1.51 \pm 0.06V$ ($T_A = +85$ to $+105^\circ C$) Power-down-reset: $1.50 \pm 0.04 V$ ($T_A = -40$ to $+85^\circ C$) $1.50 \pm 0.06V$ ($T_A = +85$ to $+105^\circ C$) | | | | | | | | | |
| Voltage detector | Power on | 1.67 V to 4.06 V (14 stages) | | | | | | | | |
| | Power down | 1.63 V to 3.98 V (14 stages) | | | | | | | | |
| On-chip debug function | Provided (Disable to tracing) | | | | | | | | | |
| Power supply voltage | $V_{DD} = 1.6$ to $5.5 V$ | | | | | | | | | |
| Operating ambient temperature | $T_A = -40$ to $+85^\circ C$ (Consumer applications) $T_A = -40$ to $+105^\circ C$ (Industrial applications) | | | | | | | | | |

2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications (TA = -40 to +85°C)

R5F105xxAxx

G: When the products "G: Industrial applications (TA = -40 to +105°C)" is used in the range of TA = -40 to +85°C

R5F105xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G11 User's Manual.

Caution 3. The EVDD pin is not present on products with 24 or less pins. Accordingly, replace EVDD with VDD and the voltage condition $1.6 \leq EVDD \leq 5.5 \text{ V}$ with $1.6 \leq VDD \leq 5.5 \text{ V}$.

2.1 Absolute Maximum Ratings

(1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|--------------------|--|--|------|
| Supply voltage | V _{DD} | | -0.5 to +6.5 | V |
| | EV _{DD} | | -0.5 to +6.5 | V |
| | AV _{REFP} | | 0.3 to V _{DD} + 0.3 Note 2 | V |
| | AV _{REFM} | | -0.3 to V _{DD} + 0.3 Note 2 and AV _{REFM} ≤ AV _{REFP} | V |
| REGC pin input voltage | V _{IREGC} | REGC | -0.3 to +2.8 and -0.3 to V _{DD} + 0.3 Note 1 | V |
| Input voltage | V _{I1} | P00, P01, P30 to P33, P40, and P51 to P56 | -0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 Note 2 | V |
| | V _{I2} | P20 to P23, P121, P122, P125, P137, EXCLK, RESET | -0.3 to V _{DD} + 0.3 Note 2 | V |
| Output voltage | V _{O1} | P00, P01, P30 to P33, P40, and P51 to P56 | -0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 Note 2 | V |
| | V _{O2} | P20 to P23 | -0.3 to V _{DD} + 0.3 Note 2 | V |
| Analog input voltage | V _{AI1} | ANI16 to ANI22 | -0.3 to EV _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 Notes 2, 3 | V |
| | V _{AI2} | ANI0 to ANI3 | -0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 Notes 2, 3 | V |

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(2/2)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|-------------------------------|------------------|----------------------------------|------------------------|-------------|------|
| Output current, high | IOH1 | Per pin | | -40 | mA |
| | | Total of all pins -170 mA | P00, P01, P40 | -70 | mA |
| | | | P30 to P33, P51 to P56 | -100 | mA |
| | IOH2 | Per pin | P20 to P23 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | IOL1 | Per pin | | 40 | mA |
| | | Total of all pins 170 mA | P00, P01, P40 | 70 | mA |
| | | | P30 to P33, P51 to P56 | 100 | mA |
| | IOL2 | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 4 | mA |
| Operating ambient temperature | T _A | In normal operation mode | | -40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | T _{stg} | | | -65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Resonator | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---------------------|------|------|------|------|
| X1 clock oscillation frequency (fx) ^{Note} | Ceramic resonator/ crystal resonator | 2.7 V ≤ VDD ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ VDD < 2.7 V | 1.0 | | 16.0 | |
| | | 1.8 V ≤ VDD < 2.4 V | 1.0 | | 8.0 | |
| | | 1.6 V ≤ VDD < 1.8 V | 1.0 | | 4.0 | |

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|------------------|---------------------|---------------------|-------|------|------|---|
| High-speed on-chip oscillator clock frequency ^{Notes 1, 2} | f _{IH} | 2.7 V ≤ VDD ≤ 5.5 V | 1 | | 24 | MHz | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | 1 | | 16 | | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | 1 | | 8 | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | 1 | | 4 | | |
| High-speed on-chip oscillator clock frequency accuracy | | TA = -20 to +85°C | 1.8 V ≤ VDD ≤ 5.5 V | -1 | | 1 | % |
| | | | 1.6 V ≤ VDD < 1.8 V | -5 | | 5 | |
| | | TA = -40 to -20°C | 1.8 V ≤ VDD ≤ 5.5 V | -1.5 | | 1.5 | % |
| | | | 1.6 V ≤ VDD < 1.8 V | -5.5 | | 5.5 | |
| Middle-speed on-chip oscillator oscillation frequency ^{Note 2} | f _{IM} | | 1 | | 4 | MHz | |
| Middle-speed on-chip oscillator oscillation frequency accuracy | | | -12 | | +12 | % | |
| Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy | D _{IMT} | | | 0.008 | | %/°C | |
| Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy | D _{IMV} | TA = 25°C | 2.1 V ≤ VDD ≤ 5.5 V | | 0.02 | %/V | |
| | | | 2.0 V ≤ VDD < 2.1 V | | -12 | | |
| | | | 1.6 V ≤ VDD < 2.0 V | | 10 | | |
| Low-speed on-chip oscillator clock frequency ^{Note 2} | f _{IL} | | | 15 | | kHz | |
| Low-speed on-chip oscillator clock frequency accuracy | | | -15 | | +15 | % | |

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------|---|---|----------------------|----------------|-----------------|--------|
| Output current, high Note 1 | IOH1 | Per pin for P00, P01, P30 to P33, P40, and P51 to P56 | | | -10.0 Note 2 | mA |
| | | Total of P00, P01, and P40 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | -42.0 | mA |
| | | | 2.7 V ≤ EVDD < 4.0 V | | -10.0 | mA |
| | | | 1.8 V ≤ EVDD < 2.7 V | | -5.0 | mA |
| | | | 1.6 V ≤ EVDD < 1.8 V | | -2.5 | mA |
| | | Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | -80.0 | mA |
| | | | 2.7 V ≤ EVDD < 4.0 V | | -19.0 | mA |
| | | | 1.8 V ≤ EVDD < 2.7 V | | -10.0 | mA |
| | | | 1.6 V ≤ EVDD < 1.8 V | | -5.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | -122.0 |
| IOH2 | Per pin for P20 to P23 | | | -0.1 Note 2 | mA | |
| | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ VDD ≤ 5.5 V | | | -0.4 | mA |

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)
<Example> Where n = 80% and IOH = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---|--------|---|---|----------------------|----------------|------|-------|
| Output current, low Note 1 | IOL1 | Per pin for P00, P01, P30 to P33, P40, and P51 to P56 | | | 20.0 Note 2 | mA | |
| | | | Total of P00, P01, and P40 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | 70.0 | mA |
| | | | | 2.7 V ≤ EVDD < 4.0 V | | 15.0 | mA |
| | | | | 1.8 V ≤ EVDD < 2.7 V | | 9.0 | mA |
| | | | | 1.6 V ≤ EVDD < 1.8 V | | 4.5 | mA |
| | | | Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | 80.0 | mA |
| | | | | 2.7 V ≤ EVDD < 4.0 V | | 35.0 | mA |
| | | | | 1.8 V ≤ EVDD < 2.7 V | | 20.0 | mA |
| | | | | 1.6 V ≤ EVDD < 1.8 V | | 10.0 | mA |
| | | | Total of all pins (When duty ≤ 70% Note 3) | | | | 150.0 |
| | IOL2 | Per pin for P20 to P23 | | | 0.4 Note 2 | mA | |
| Total of all pins (When duty ≤ 70% Note 3) | | | 1.6 V ≤ VDD ≤ 5.5 V | | 1.6 | mA | |

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(3/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------|------------------|--|--|----------------------|------|----------------------|---|
| Input voltage, high | V _{IH1} | P00, P01, P30 to P33, P40, and P51 to P56 | Normal mode | 0.8 EV _{DD} | | EV _{DD} | V |
| | V _{IH2} | P00, P30 to P32, P40, P51 to P56 | TTL mode 4.0 V ≤ EV _{DD} ≤ 5.5 V | 2.2 | | EV _{DD} | V |
| | | | TTL mode 3.3 V ≤ EV _{DD} < 4.0 V | 2.0 | | EV _{DD} | V |
| | | | TTL mode 1.6 V ≤ EV _{DD} < 3.3 V | 1.5 | | EV _{DD} | V |
| | V _{IH3} | P20 to P23 (digital input) | | 0.7 V _{DD} | | V _{DD} | V |
| | V _{IH4} | P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8 V _{DD} | | V _{DD} | V |
| Input voltage, low | V _{IL1} | P00, P01, P30 to P33, P40, and P51 to P56 | Normal mode | 0 | | 0.2 EV _{DD} | V |
| | V _{IL2} | P00, P30 to P32, P40, P51 to P56 | TTL mode 4.0 V ≤ EV _{DD} ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL mode 3.3 V ≤ EV _{DD} < 4.0 V | 0 | | 0.5 | V |
| | | | TTL mode 1.6 V ≤ EV _{DD} < 3.3 V | 0 | | 0.32 | V |
| | V _{IL3} | P20 to P23 (digital input) | | 0 | | 0.3 V _{DD} | V |
| | V _{IL4} | P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2 V _{DD} | V |

Caution The maximum value of V_{IH} of pins P00, P01, P20, P30 to P33, P40 and P51 to P56 is V_{DD} or EV_{DD}, even in the N-ch open-drain mode.

(P20: V_{DD})

(P00, P01, P30 to P33, P40, P51 to P56: EV_{DD})

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(4/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|----------------------|--------|---|---|------------|------|------|---|
| Output voltage, high | VOH1 | P00, P01, P30 to P33, P40, and P51 to P56 | 4.0 V ≤ EVDD ≤ 5.5 V, IOH = -10.0 mA | EVDD - 1.5 | | | V |
| | | | 4.0 V ≤ EVDD ≤ 5.5 V, IOH = -3.0 mA | EVDD - 0.7 | | | V |
| | | | 2.7 V ≤ EVDD ≤ 5.5 V, IOH = -2.0 mA | EVDD - 0.6 | | | V |
| | | | 1.8 V ≤ EVDD ≤ 5.5 V, IOH = -1.5 mA | EVDD - 0.5 | | | V |
| | | | 1.6 V ≤ EVDD ≤ 5.5 V, IOH = -1.0 mA | EVDD - 0.5 | | | V |
| | VOH2 | P20 to P23 | 1.6 V ≤ VDD ≤ 5.5 V, IOH = -100 μA | VDD - 0.5 | | | V |
| Output voltage, low | VOL1 | P00, P01, P30 to P33, P40, and P51 to P56 | 4.0 V ≤ EVDD ≤ 5.5 V, IOL = 20.0 mA | | | 1.3 | V |
| | | | 4.0 V ≤ EVDD ≤ 5.5 V, IOL = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ EVDD ≤ 5.5 V, IOL = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ EVDD ≤ 5.5 V, IOL = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ EVDD ≤ 5.5 V, IOL = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ EVDD ≤ 5.5 V, IOL = 0.3 mA | | | 0.4 | V |
| | VOL2 | P20 to P23 | 1.6 V ≤ VDD ≤ 5.5 V, IOL = 400 μA | | | 0.4 | V |

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(5/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|-----------------------------|--------|---|-------------------------|---------------------------------------|------|------|-----|----|
| Input leakage current, high | ILI1 | P00, P01, P30 to P33, P40, and P51 to P56 | VI = EVDD | | 1 | μA | | |
| | ILI2 | P20 to P23, P125, P137, $\overline{\text{RESET}}$ | VI = VDD | | 1 | μA | | |
| | ILI3 | P121, P122, X1, X2, EXCLK | VI = VDD | In input port or external clock input | 1 | μA | | |
| | | | | In resonator connection | 10 | μA | | |
| Input leakage current, low | ILIL1 | P00, P01, P30 to P33, P40, and P51 to P56 | VI = VSS | | -1 | μA | | |
| | ILIL2 | P20 to P23, P125, P137, $\overline{\text{RESET}}$ | VI = VSS | | -1 | μA | | |
| | ILIL3 | P121, P122, X1, X2, EXCLK | VI = VSS | In input port or external clock input | -1 | μA | | |
| | | | | In resonator connection | -10 | μA | | |
| On-chip pull-up resistance | RU | P00, P01, P30 to P33, P40, P51 to P56, P125 | VI = VSS, In input port | | 10 | 20 | 100 | kΩ |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/4)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | |
|--------------------------|---|-------------------------------|---|--------------------------------|--|----------------------|----------------------|------|------|-----|
| Supply current Note 1 | IDD1 | Operating mode | Basic operation | HS (high-speed main) mode | fHOCO = 48 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 1.7 | | mA |
| | | | | | | VDD = 3.0 V | | 1.7 | | |
| | | | | | fHOCO = 24 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 1.4 | | |
| | | | | | | VDD = 3.0 V | | 1.4 | | |
| | | | | | | VDD = 5.0 V | | 3.5 | 6.9 | |
| | | | | | | VDD = 3.0 V | | 3.5 | 6.9 | |
| | | | Normal operation | HS (high-speed main) mode | fHOCO = 48 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 3.2 | 6.3 | |
| | | | | | | VDD = 3.0 V | | 3.2 | 6.3 | |
| | | | | | fHOCO = 24 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 2.4 | 4.6 | |
| | | | | | | VDD = 3.0 V | | 2.4 | 4.6 | |
| | | | | | fHOCO = 16 MHz ^{Note 3} fIH = 16 MHz ^{Note 3} | VDD = 5.0 V | | 1.1 | 2.0 | |
| | | | | | | VDD = 3.0 V | | 1.1 | 2.0 | |
| | | Normal operation | LS (low-speed main) mode (MCSEL = 0) | fIH = 8 MHz ^{Note 3} | VDD = 3.0 V | | 0.72 | 1.3 | | |
| | | | | | VDD = 2.0 V | | 0.72 | 1.3 | | |
| | | | | fIM = 4 MHz ^{Note 6} | VDD = 3.0 V | | 0.58 | 1.1 | | |
| | | | | | VDD = 2.0 V | | 0.58 | 1.1 | | |
| | | Normal operation | LV (low-voltage main) mode | fIH = 4 MHz ^{Note 3} | VDD = 3.0 V | | 1.2 | 1.8 | | |
| | | | | | VDD = 2.0 V | | 1.2 | 1.8 | | |
| | | Normal operation | LP (low-power main) mode (MCSEL = 1) | fIH = 1 MHz ^{Note 3} | VDD = 3.0 V | | 290 | 480 | | |
| | | | | | VDD = 2.0 V | | 290 | 480 | | |
| | | | | fIM = 1 MHz ^{Note 6} | VDD = 3.0 V | | 124 | 230 | | |
| | | | | | VDD = 2.0 V | | 124 | 230 | | |
| | | Normal operation | HS (high-speed main) mode | fMX = 20 MHz ^{Note 2} | VDD = 5.0 V | Square wave input | | 2.7 | 5.3 | |
| | | | | | | Resonator connection | | 2.8 | 5.5 | |
| | | | | | VDD = 3.0 V | Square wave input | | 2.7 | 5.3 | |
| | | | | | | Resonator connection | | 2.8 | 5.5 | |
| | | | | | fMX = 10 MHz ^{Note 2} | VDD = 5.0 V | Square wave input | | 1.8 | 3.1 |
| | | | | | | | Resonator connection | | 1.9 | 3.2 |
| VDD = 3.0 V | Square wave input | | | | 1.8 | 3.1 | | | | |
| | Resonator connection | | | | 1.9 | 3.2 | | | | |
| Normal operation | LS (low-speed main) mode (MCSEL = 0) | | | fMX = 8 MHz ^{Note 2} | VDD = 3.0 V | Square wave input | | 0.9 | 1.9 | |
| | | | | | | Resonator connection | | 1.0 | 2.0 | |
| Normal operation | LS (low-speed main) mode (MCSEL = 1) | | | fMX = 8 MHz ^{Note 2} | VDD = 2.0 V | Square wave input | | 0.9 | 1.9 | |
| | | | | | | Resonator connection | | 1.0 | 2.0 | |
| Normal operation | LS (low-speed main) mode (MCSEL = 1) | fMX = 4 MHz ^{Note 2} | VDD = 3.0 V | Square wave input | | 0.6 | 1.1 | | | |
| | | | | Resonator connection | | 0.6 | 1.2 | | | |
| Normal operation | LP (low-power main) mode (MCSEL = 1) | fMX = 4 MHz ^{Note 2} | VDD = 2.0 V | Square wave input | | 0.6 | 1.1 | | | |
| | | | | Resonator connection | | 0.6 | 1.2 | | | |
| Normal operation | LP (low-power main) mode (MCSEL = 1) | fMX = 1 MHz ^{Note 2} | VDD = 3.0 V | Square wave input | | 100 | 190 | | | |
| | | | | Resonator connection | | 145 | 250 | | | |
| Normal operation | LP (low-power main) mode (MCSEL = 1) | fMX = 1 MHz ^{Note 2} | VDD = 2.0 V | Square wave input | | 100 | 190 | | | |
| | | | | Resonator connection | | 145 | 250 | | | |

(Notes and Remarks are listed on the next page.)

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/4)

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|--------------------------|------------------|----------------|------------------|---------------------------|---|------------------|------|------|------|------|
| Supply current Note 1 | I _{DD1} | Operating mode | Normal operation | Subsystem clock operation | f _{IL} = 15 kHz, T _A = -40°C Note 5 | Normal operation | | 1.8 | 5.9 | μA |
| | | | | | f _{IL} = 15 kHz, T _A = +25°C Note 5 | Normal operation | | 1.9 | 5.9 | |
| | | | | | f _{IL} = 15 kHz, T _A = +85°C Note 5 | Normal operation | | 2.3 | 8.7 | |

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock is stopped.

Note 5. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(3/4)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit | | | |
|--------------------------|----------------------------|--------------|---|--|-------------------------|--|------|------|------|----|
| Supply current Note 1 | I _{DD2} Note 2 | HALT mode | HS (high-speed main) mode | f _{HOCO} = 48 MHz ^{Note 4} | V _{DD} = 5.0 V | | 0.59 | 2.43 | mA | |
| | | | | f _{IH} = 24 MHz ^{Note 4} | V _{DD} = 3.0 V | | 0.59 | 2.43 | | |
| | | | | f _{HOCO} = 24 MHz ^{Note 4} | V _{DD} = 5.0 V | | 0.41 | 1.83 | | |
| | | | | f _{IH} = 24 MHz ^{Note 4} | V _{DD} = 3.0 V | | 0.41 | 1.83 | | |
| | | | | f _{HOCO} = 16 MHz ^{Note 4} | V _{DD} = 5.0 V | | 0.39 | 1.38 | | |
| | | | | f _{IH} = 16 MHz ^{Note 4} | V _{DD} = 3.0 V | | 0.39 | 1.38 | | |
| | | | LS (low-speed main) mode (MCSEL = 0) | f _{IH} = 8 MHz ^{Note 4} | V _{DD} = 3.0 V | | 250 | 710 | μA | |
| | | | | | V _{DD} = 2.0 V | | 250 | 710 | | |
| | | | LS (low-speed main) mode (MCSEL = 1) | f _{IH} = 4 MHz ^{Note 4} | V _{DD} = 3.0 V | | 204 | 400 | μA | |
| | | | | | V _{DD} = 2.0 V | | 204 | 400 | | |
| | | | | f _{IM} = 4 MHz ^{Note 6} | V _{DD} = 3.0 V | | 43 | 250 | | |
| | | | LV (low-voltage main) mode | f _{IH} = 4 MHz ^{Note 4} | V _{DD} = 3.0 V | | 450 | 700 | μA | |
| | | | | | V _{DD} = 2.0 V | | 450 | 700 | | |
| | | | LP (low-power main) mode (MCSEL = 1) | f _{IH} = 1 MHz ^{Note 4} | V _{DD} = 3.0 V | | 192 | 400 | μA | |
| | | | | | V _{DD} = 2.0 V | | 192 | 400 | | |
| | | | | f _{IM} = 1 MHz ^{Note 6} | V _{DD} = 3.0 V | | 28 | 100 | | |
| | | | HS (high-speed main) mode | f _{MX} = 20 MHz ^{Note 3} | V _{DD} = 5.0 V | Square wave input | | 0.20 | 1.55 | mA |
| | | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | | V _{DD} = 3.0 V | Square wave input | | 0.20 | 1.55 | |
| | | | | f _{MX} = 10 MHz ^{Note 3} | V _{DD} = 5.0 V | Square wave input | | 0.15 | 0.86 | |
| | | | | | | Resonator connection | | 0.30 | 0.93 | |
| | | | | | V _{DD} = 3.0 V | Square wave input | | 0.15 | 0.86 | |
| | | | LS (low-speed main) mode (MCSEL = 0) | f _{MX} = 8 MHz ^{Note 3} | V _{DD} = 3.0 V | Square wave input | | 68 | 550 | μA |
| | | | | | | Resonator connection | | 125 | 590 | |
| | | | LS (low-speed main) mode (MCSEL = 1) | f _{MX} = 4 MHz ^{Note 3} | V _{DD} = 3.0 V | Square wave input | | 23 | 128 | μA |
| | | | | | | Resonator connection | | 65 | 200 | |
| | | | LP (low-power main) mode (MCSEL = 1) | f _{MX} = 4 MHz ^{Note 3} | V _{DD} = 3.0 V | Square wave input | | 10 | 64 | μA |
| | | | | | | Resonator connection | | 59 | 150 | |
| | | | Subsystem clock operation | | | f _{IL} = 15 kHz, T _A = -40°C ^{Note 5} | | 0.48 | 1.22 | μA |
| | | | | | | f _{IL} = 15 kHz, T _A = +25°C ^{Note 5} | | 0.55 | 1.22 | |
| | | | | | | f _{IL} = 15 kHz, T _A = +85°C ^{Note 5} | | 0.80 | 3.30 | |

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
- Note 2.** When the HALT instruction is executed in the flash memory.
- Note 3.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.
- Note 4.** When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.
- Note 5.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.
- Note 6.** When the high-speed system clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(4/4)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--------------------------|----------------|---------------------|------------|------|------|------|------|
| Supply current Note 1 | IDD3 Note 2 | STOP mode Note 3 | TA = -40°C | | 0.19 | 0.51 | μA |
| | | | TA = +25°C | | 0.25 | 0.51 | |
| | | | TA = +50°C | | 0.28 | 1.10 | |
| | | | TA = +70°C | | 0.38 | 1.90 | |
| | | | TA = +85°C | | 0.60 | 3.30 | |

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. The values do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

Peripheral Functions (Common to all products)

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|--------------------------------|--|---|------|------|-------|------|
| Low-speed on-chip oscillator operating current | IFIL Note 1 | | | | 0.22 | | μA |
| 12-bit interval timer operating current | ITMKA Notes 1, 3, 4 | fIL = 15 kHz fMAIN stopped (per unit) | | | 0.02 | | μA |
| 8-bit interval timer operating current Notes 1, 9 | ITMT | fIL = 15 kHz fMAIN stopped (per unit) | 8-bit counter mode × 2-channel operation | | 0.04 | | μA |
| | | | 16-bit counter mode operation | | 0.03 | | μA |
| Watchdog timer operating current | IWD _T Notes 1, 3, 5 | fIL = 15 kHz fMAIN stopped (per unit) | | | 0.22 | | μA |
| A/D converter operating current | IADC Notes 1, 6 | During maximum-speed conversion | Normal mode, AVREFP = VDD = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, AVREFP = VDD = 3.0 V | | 0.5 | 0.7 | mA |
| Internal reference voltage (1.45 V) current Notes 1, 10 | IADREF | | | | 85.0 | | μA |
| Temperature sensor operating current | ITMPS Note 1 | | | | 85.0 | | μA |
| D/A converter operating current | IDAC Notes 1, 14 | Per channel | | | | 1.5 | mA |
| PGA operating current | IPGA Notes 1, 2 | | | | 480 | 700 | μA |
| Comparator operating current | ICMP Note 8 | VDD = 5.0 V, Regulator output voltage = 2.1 V | Comparator high-speed mode Window mode | | 12.5 | | μA |
| | | | Comparator low-speed mode Window mode | | 3.0 | | |
| | | | Comparator high-speed mode Standard mode | | 6.5 | | |
| | | | Comparator low-speed mode Standard mode | | 1.9 | | |
| | | VDD = 5.0 V, Regulator output voltage = 1.8 V | Comparator high-speed mode Window mode | | 8.0 | | |
| | | | Comparator low-speed mode Window mode | | 2.2 | | |
| | | | Comparator high-speed mode Standard mode | | 4.0 | | |
| | | | Comparator low-speed mode Standard mode | | 1.3 | | |
| LVD operating current | ILVD Notes 1, 7 | | | | 0.10 | | μA |
| Self-programming operating current | IFSP Notes 1, 12 | | | | 2.0 | 12.20 | mA |
| BGO current | IBGO Notes 1, 11 | | | | 2.0 | 12.20 | mA |
| SNOOZE operating current | ISNOZ Note 1 | ADC operation fIH = 24 MHz, AVREFP = VDD = 3.0 V | Mode transition Note 13 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed | | 1.20 | 1.44 | mA |
| | | CSI/UART operation fIH = 24 MHz | | 0.70 | 0.84 | mA | |
| | ISNOZM Note 1 | ADC operation fIM = 4 MHz, AVREFP = VDD = 3.0 V | Mode transition Note 13 | | 0.05 | 0.08 | mA |
| | | | The A/D conversion operations are performed | | 0.67 | 0.78 | mA |
| | | CSI operation, fIM = 4 MHz | | 0.06 | 0.08 | mA | |

(Notes and Remarks are listed on the next page.)

- Note 1.** Current flowing to V_{DD}.
- Note 2.** Operable range is 2.7 to 5.5 V.
- Note 3.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and high-speed system clock are stopped.
- Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
- Note 8.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{COMP} when the comparator circuit is in operation.
- Note 9.** Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 8-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
- Note 10.** Current consumed by generating the internal reference voltage (1.45 V).
- Note 11.** Current flowing during programming of the data flash.
- Note 12.** Current flowing during self-programming.
- Note 13.** For transition time to the SNOOZE mode, see **24.3.3 SNOOZE mode** in the RL78/G11 User's Manual.
- Note 14.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DAC} when the D/A converter operates in an operation mode or the HALT mode.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/2)

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-------------------------------|--|-------------------------------|--|---------|------|------|
| Instruction cycle (minimum instruction execution time) | TCY | Main system clock (fMAIN) operation | HS (high-speed main) mode | 2.7 V ≤ VDD ≤ 5.5 V | 0.04167 | 1 | μs |
| | | | | 2.4 V ≤ VDD < 2.7 V | 0.0625 | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ VDD ≤ 5.5 V PMMC. MCSEL = 0 | 0.125 | 1 | μs |
| | | | | 1.8 V ≤ VDD ≤ 5.5 V PMMC. MCSEL = 1 | 0.25 | 1 | μs |
| | | | LP (low-power main) mode | 1.8 V ≤ VDD ≤ 5.5 V | 1 | | μs |
| | | | LV (low-voltage main) mode | 1.6 V ≤ VDD ≤ 5.5 V | 0.25 | 1 | μs |
| | | Subsystem clock (fSUB) operation | fil | 1.8 V ≤ VDD ≤ 5.5 V | | 66.7 | μs |
| | | In the self- programming mode | HS (high-speed main) mode | 2.7 V ≤ VDD ≤ 5.5 V | 0.04167 | 1 | μs |
| | | | | 2.4 V ≤ VDD < 2.7 V | 0.0625 | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ VDD ≤ 5.5 V | 0.125 | 1 | μs |
| LV (low-voltage main) mode | 1.8 V ≤ VDD ≤ 5.5 V | | 0.25 | 1 | μs | | |
| External system clock frequency | fEX | 2.7 V ≤ VDD ≤ 5.5 V | | 1 | | 20 | MHz |
| | | 2.4 V ≤ VDD < 2.7 V | | 1 | | 16 | MHz |
| | | 1.8 V ≤ VDD < 2.4 V | | 1 | | 8 | MHz |
| | | 1.6 V ≤ VDD < 1.8 V | | 1 | | 4 | MHz |
| External system clock input high-/low- level width | tEXH, tEXL | 2.7 V ≤ VDD ≤ 5.5 V | | 24 | | | ns |
| | | 2.4 V ≤ VDD < 2.7 V | | 30 | | | ns |
| | | 1.8 V ≤ VDD < 2.4 V | | 60 | | | ns |
| | | 1.6 V ≤ VDD < 1.8 V | | 120 | | | ns |
| T100 to T103 input high-/low-level width | tTIH, tTIL ^{Note} | | | 1/fMCK + 10 | | | ns |

Note Following conditions must be satisfied on low level interface of EVDD < VDD.

1.8 V ≤ EVDD ≤ 2.7 V: MIN. 125 ns

1.6 V ≤ EVDD < 1.8 V: MIN. 250 ns

Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

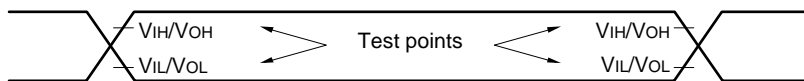
(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

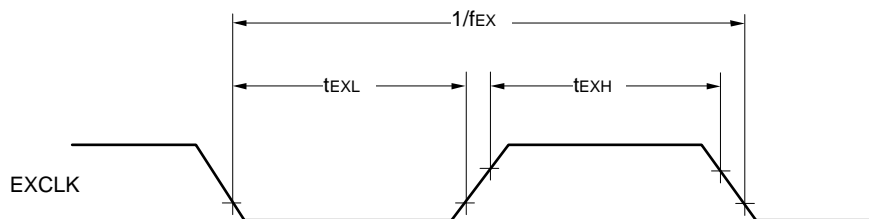
| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit | | | |
|---|--------------------------------|--|--|---------------------------------|----------------------|------|------|------|------|-----|-----|
| TO00 to TO03, TKBO0, and TKBO1 output frequency Note | fro | TO00 to TO03, TKBO0, and TKBO1 (in the case of output from port pins other than P20) | HS (high-speed main) mode | 4.0 V ≤ EVDD ≤ 5.5 V | | | 12 | MHz | | | |
| | | | | 2.7 V ≤ EVDD < 4.0 V | | | 8 | | | | |
| | | | | 1.8 V ≤ EVDD < 2.7 V | | | 4 | | | | |
| | | | | 1.6 V ≤ EVDD < 1.8 V | | | 2 | | | | |
| | | | LS (low-speed main) mode | 1.8 V ≤ EVDD ≤ 5.5 V | | | 4 | | | | |
| | | | | 1.6 V ≤ EVDD < 1.8 V | | | 2 | | | | |
| | | | LP (low-power main) mode | 1.8 V ≤ EVDD ≤ 5.5 V | | | | | | 0.5 | |
| | | | | 1.6 V ≤ EVDD ≤ 5.5 V | | | | | | 2 | |
| | | | TKBO1 (in the case of output from P20) | HS (high-speed main) mode | 4.0 V ≤ VDD ≤ 5.5 V | | | | | | 1.5 |
| | | | | | 2.7 V ≤ VDD < 4.0 V | | | | | | 1.2 |
| | | 2.4 V ≤ VDD < 2.7 V | | | | | 1 | | | | |
| | | LS (low-speed main) mode | | 4.0 V ≤ VDD ≤ 5.5 V | | | | | 1.5 | | |
| | | | | 2.7 V ≤ VDD < 4.0 V | | | | | 1.2 | | |
| | | | | 2.4 V ≤ VDD < 2.7 V | | | | | 1 | | |
| | | | | 1.8 V ≤ VDD < 2.4 V | | | | | 0.75 | | |
| | | LP (low-power main) mode | | 1.8 V ≤ VDD ≤ 5.5 V | | | | | 0.5 | | |
| | | | | LV (low-voltage main) mode | 4.0 V ≤ VDD ≤ 5.5 V | | | | | 1.5 | |
| | | 2.7 V ≤ VDD < 4.0 V | | | | | 1.2 | | | | |
| 2.4 V ≤ VDD < 2.7 V | | | | | | 1 | | | | | |
| 1.8 V ≤ VDD < 2.4 V | | | | | | 0.75 | | | | | |
| 1.6 V ≤ VDD < 1.8 V | | | | | | 0.5 | | | | | |
| PCLBUZ0, PCLBUZ1 output frequency | fpCL | HS (high-speed main) mode | 4.0 V ≤ EVDD ≤ 5.5 V | | | | | 16 | | | |
| | | | 2.7 V ≤ EVDD < 4.0 V | | | | | 8 | | | |
| | | | 1.8 V ≤ EVDD < 2.7 V | | | | | 4 | | | |
| | | | 1.6 V ≤ EVDD < 1.8 V | | | | | 2 | | | |
| | | LS (low-speed main) mode | 1.8 V ≤ EVDD ≤ 5.5 V | | | | | 4 | | | |
| | | | 1.6 V ≤ EVDD < 1.8 V | | | | | 2 | | | |
| | | LP (low-power main) mode | | | 1.6 V ≤ EVDD ≤ 5.5 V | | | | 1 | | |
| | | LV (low-voltage main) mode | 1.8 V ≤ EVDD ≤ 5.5 V | | | | | 4 | | | |
| | | | 1.6 V ≤ EVDD < 1.8 V | | | | | 2 | | | |
| | | Interrupt input high-/ low-level width | tINTH, | INTP0 to INTP2, INTP9 | | | 1 | | | μs | |
| tINTL | INTP3 to INTP8, INTP10, INTP11 | | | 1 | | | | | | | |
| Key interrupt input low-level width | tKR | KR0 to KR7 | | | 1.8 V ≤ EVDD ≤ 5.5 V | 250 | | ns | | | |
| | | | | | 1.6 V ≤ EVDD < 1.8 V | 1 | | μs | | | |
| RESET low-level width | tRSL | | | | 10 | | | μs | | | |

Note When duty is 50%.

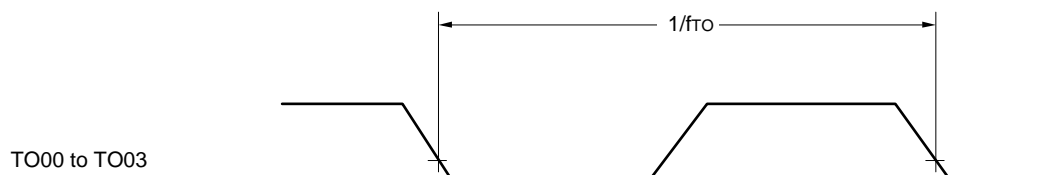
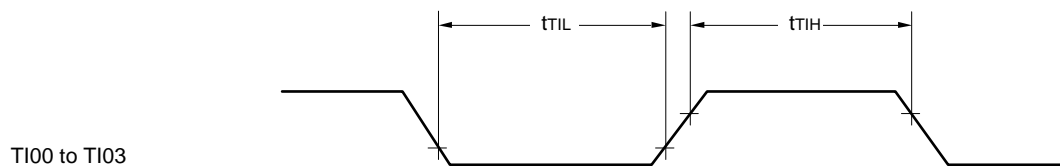
AC Timing Test Points



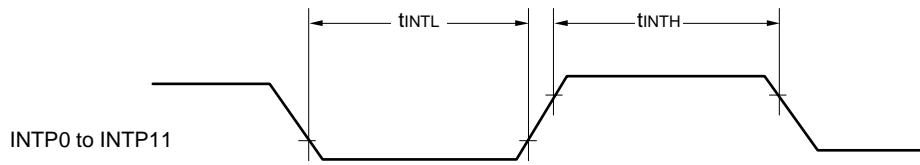
External System Clock Timing



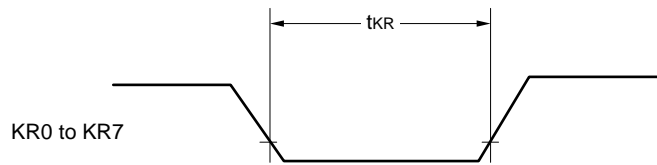
TI/TO Timing



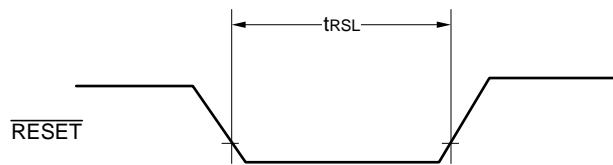
Interrupt Request Input Timing



Key Interrupt Input Timing

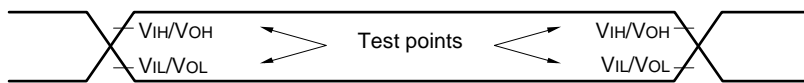


$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

When P01, P30, P31 and P54 are used as Tx/Dq pins

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|--|--------|--|---------------------------|---------------------|--------------------------|---------------------|--------------------------|---------------------|----------------------------|---------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1, 2 | | 2.7 V ≤ EVDD ≤ 5.5 V | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | bps |
| | | Theoretical value of the maximum transfer rate f _{mck} = f _{clk} Note 3 | | 4.0 | | 1.3 | | 0.1 | | 0.6 | Mbps |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | bps |
| | | Theoretical value of the maximum transfer rate f _{mck} = f _{clk} Note 3 | | 4.0 | | 1.3 | | 0.1 | | 0.6 | Mbps |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | bps |
| | | Theoretical value of the maximum transfer rate f _{mck} = f _{clk} Note 3 | | 4.0 | | 1.3 | | 0.1 | | 0.6 | Mbps |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | | — | | f _{mck} /6 | | f _{mck} /6 | | f _{mck} /6 | bps |
| Theoretical value of the maximum transfer rate f _{mck} = f _{clk} Note 3 | | — | | 1.3 | | 0.1 | | 0.6 | Mbps | | |

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. Following conditions must be satisfied on low level interface of EVDD < VDD.

2.4 V ≤ EVDD < 2.7 V: MAX.2.6 Mbps

1.8 V ≤ EVDD < 2.4 V: MAX.1.3 Mbps

1.6 V ≤ EVDD < 1.8 V: MAX.0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{clk}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ EVDD ≤ 5.5 V)

16 MHz (2.4 V ≤ EVDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ EVDD ≤ 5.5 V)

LP (low-power main) mode: 1 MHz (1.8 V ≤ EVDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ EVDD ≤ 5.5 V)

Caution Select the normal input buffer for the Rx/Dq pin and the normal output mode for the Tx/Dq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

When P20 is used as TxD1 pin

(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---------------|--------|--|---------------------------|--------------------------------------|--------------------------|-----------------------------------|--------------------------|-----------------------------------|----------------------------|-----------------------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | 4.0 V ≤ VDD ≤ 5.5 V | | f _{mck} /6 Notes 1, 2, 3 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Notes 1, 3 | | 1.5 | | 1.3 | | 0.1 | | 0.6 | Mbps |
| | | 2.7 V ≤ VDD ≤ 5.5 V | | f _{mck} /6 Notes 1, 2, 3 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Notes 1, 3 | | 1.2 | | 1.2 | | 0.1 | | 0.6 | Mbps |
| | | 2.4 V ≤ VDD ≤ 5.5 V | | f _{mck} /6 Notes 1, 2, 3 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Notes 1, 3 | | 1.0 | | 1.0 | | 0.1 | | 0.6 | Mbps |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | | f _{mck} /6 Notes 1, 2 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Notes 1, 3 | | | | 0.6 | | 0.1 | | 0.6 | Mbps |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | | | | | | | f _{mck} /6 Notes 1, 2 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Notes 1, 3 | | | Using prohibited | | Using prohibited | | Using prohibited | 0.5 | Mbps |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | | | | | | | f _{mck} /6 Notes 1, 2 | bps |
| | | Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Notes 1, 3 | | | | | | | | 0.5 | Mbps |

Note 1. f_{mck} is a frequency selected by setting the CKS bit in the SPS and SMR registers.

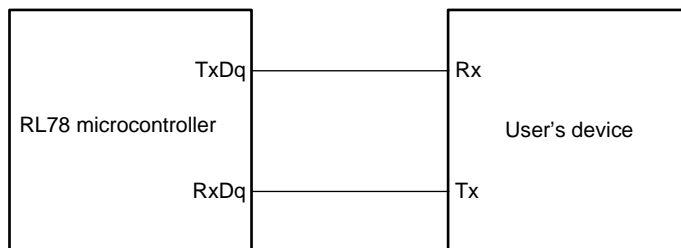
Note 2. The transfer rate of 4800 bps is only supported in the SNOOZE mode.
Note that the SNOOZE mode is not supported when f_{HOCO} is 48 MHz.

Note 3. f_{CLK} in each operating mode is as follows.:

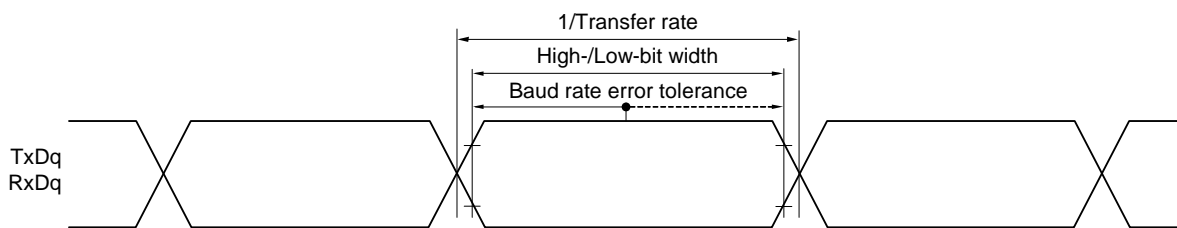
- HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
- LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
- LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
- LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3 and 5)

Remark 2. f_{MC}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|--------|----------------------|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 2/fCLK | 83.3 | | 250 | | 2000 | | 500 | | ns |
| SCKp high-/low-level width | tkL1 | 4.0 V ≤ EVDD ≤ 5.5 V | tkCY1/2 - 7 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | ns |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | tkCY1/2 - 10 | | | | | | | | ns |
| Slp setup time (to SCKp↑) Note 1 | tSIK1 | 4.0 V ≤ EVDD ≤ 5.5 V | 23 | | 110 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | 33 | | | | | | | | ns |
| Slp hold time (from SCKp↑) Note 2 | tKS11 | | 10 | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | tkSO1 | C = 20 pF Note 4 | | 10 | | 20 | | 20 | | 20 | ns |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**When P01, P32, P53, P54 and P56 are used as SOMn pins****(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|--|------------|----------------------|---------------------------|------------------|--------------------------|---------------|--------------------------|---------------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 4/fCLK | 2.7 V ≤ EVDD ≤ 5.5 V | 167 | | 500 | | 4000 | | 1000 | ns |
| | | | 2.4 V ≤ EVDD ≤ 5.5 V | 250 | | | | | | | |
| | | | 1.8 V ≤ EVDD ≤ 5.5 V | 500 | | | | | | | |
| | | | 1.7 V ≤ EVDD ≤ 5.5 V | 1000 | 1000 | | | | | | |
| | | | 1.6 V ≤ EVDD ≤ 5.5 V | Using prohibited | | | | | | | |
| SCKp high-/low-level width | tkH1, tkL1 | 4.0 V ≤ EVDD ≤ 5.5 V | tkCY1/2- 12 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | ns | |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | tkCY1/2- 18 | | | | | | | | |
| | | 2.4 V ≤ EVDD ≤ 5.5 V | tkCY1/2- 38 | | | | | | | | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | tkCY1/2- 50 | | | | | | | | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | tkCY1/2- 100 | tkCY1/2 - 100 | | tkCY1/2 - 100 | | tkCY1/2 - 100 | | | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | Using prohibited | | | | | | | | |
| Slp setup time (to SCKp↑) Note 1 | tsIK1 | 4.0 V ≤ EVDD ≤ 5.5 V | 44 | | 110 | | 110 | | 110 | ns | |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | | | | | | | | | |
| | | 2.4 V ≤ EVDD ≤ 5.5 V | 75 | | | | | | | | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 110 | | | | | | | | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 220 | 220 | | 220 | | 220 | | | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | Using prohibited | | | | | | | | |
| Slp hold time (from SCKp↑) Note 2 | tkSI1 | 1.7 V ≤ EVDD ≤ 5.5 V | 19 | | 19 | | 19 | | 19 | ns | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | Using prohibited | | | | | | | | |
| Delay time from SCKp↓ to SOp output Note 3 | tkSO1 | C = 30 pF Note 4 | 1.7 V ≤ EVDD ≤ 5.5 V | 33.4 | | 33.4 | | 33.4 | | 33.4 | ns |
| | | | 1.6 V ≤ EVDD ≤ 5.5 V | Using prohibited | | | | | | | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin**(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|---------------|---------------------|---------------------|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 4/fCLK | 4.0 V ≤ VDD ≤ 5.5 V | 600 | | 600 | | 4000 | | 1000 | | ns |
| | | | 2.7 V ≤ VDD ≤ 5.5 V | 850 | | 850 | | | | | | |
| | | | 2.4 V ≤ VDD ≤ 5.5 V | 1000 | | 1000 | | | | | | |
| | | | 1.8 V ≤ VDD ≤ 5.5 V | — | | 1500 | | | | 1500 | | |
| | | | 1.7 V ≤ VDD ≤ 5.5 V | — | | — | | — | | 2000 | | |
| | | | 1.6 V ≤ VDD ≤ 5.5 V | — | | — | | — | | — | | |
| SCKp high-/low-level width | tkH1, tkL1 | 4.0 V ≤ VDD ≤ 5.5 V | | tkCY1/2 - 12 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | ns |
| | | 2.7 V ≤ VDD ≤ 5.5 V | | tkCY1/2 - 18 | | | | | | | | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | | tkCY1/2 - 38 | | | | | | | | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | | | | | | | | |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | — | | — | | — | | tkCY1/2 - 100 | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | — | | — | | — | | — | | |
| Slp setup time (to SCKp↑) Note 1 | tSIK1 | 4.0 V ≤ VDD ≤ 5.5 V | | 44 | | 110 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ VDD ≤ 5.5 V | | | | | | | | | | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | | 75 | | | | | | | | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | | | | | | | | |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | — | | — | | — | | 220 | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | — | | — | | — | | — | | |
| Slp hold time (from SCKp↑) Note 2 | tkSI1 | 2.4 V ≤ VDD ≤ 5.5 V | | 19 | | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | | | | | | | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | — | | — | | — | | | | |
| Delay time from SCKp↓ to SOp output Note 3 | tkSO1 | C = 30 pF Note 4 | 2.4 V ≤ VDD ≤ 5.5 V | | 150 | | 250 | | 250 | | 300 | ns |
| | | | 1.8 V ≤ VDD ≤ 5.5 V | | — | | | | | | | |
| | | | 1.6 V ≤ VDD ≤ 5.5 V | | — | | — | | — | | | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 4 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

When P01, P32, P53, P54 and P56 are used as SOMn pins

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/2)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|--------------------------------------|------------|----------------------|-----------------|---------------------------|--------------|--------------------------|-------------|--------------------------|------|----------------------------|------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 3 | tkcy2 | 4.0 V ≤ EVDD ≤ 5.5 V | fMCK > 20 MHz | 8/fMCK | — | — | — | — | — | — | ns | |
| | | | fMCK ≤ 20 MHz | 6/fMCK | 6/fMCK | 6/fMCK | 6/fMCK | | | | | |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | fMCK > 16 MHz | 8/fMCK | — | — | — | | | | | |
| | | | fMCK ≤ 16 MHz | 6/fMCK | 6/fMCK | 6/fMCK | 6/fMCK | | | | | |
| | | 2.4 V ≤ EVDD ≤ 5.5 V | 6/fMCK and 500 | — | — | — | — | | | | | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 6/fMCK and 750 | — | — | — | — | | | | | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 6/fMCK and 1500 | 6/fMCK and 1500 | — | — | — | | | | | |
| 1.6 V ≤ EVDD ≤ 5.5 V | — | — | — | — | — | | | | | | | |
| SCKp high-/low-level width | tkH2, tkL2 | 4.0 V ≤ EVDD ≤ 5.5 V | tkcy2/2 - 7 | tkcy2/2 - 7 | tkcy2/2 - 7 | tkcy2/2 - 7 | tkcy2/2 - 7 | tkcy2/2 - 7 | ns | | | |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | tkcy2/2 - 8 | tkcy2/2 - 8 | tkcy2/2 - 8 | tkcy2/2 - 8 | tkcy2/2 - 8 | | | | | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | tkcy2/2 - 18 | tkcy2/2 - 18 | tkcy2/2 - 18 | tkcy2/2 - 18 | | | | | | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | tkcy2/2 - 66 | tkcy2/2 - 66 | tkcy2/2 - 66 | tkcy2/2 - 66 | | | | | | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | — | — | — | | | | | | |
| Slp setup time (to SCKp↑) Note 1 | tsik2 | 2.7 V ≤ EVDD ≤ 5.5 V | 1/fMCK + 20 | 1/fMCK + 30 | 1/fMCK + 30 | 1/fMCK + 30 | 1/fMCK + 30 | ns | | | | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 1/fMCK + 30 | 1/fMCK + 30 | 1/fMCK + 30 | 1/fMCK + 30 | | | | | | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 1/fMCK + 40 | 1/fMCK + 40 | 1/fMCK + 40 | 1/fMCK + 40 | | | | | | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | — | — | — | | | | | | |
| Slp hold time (from SCKp↑) Note 2 | tksl2 | 1.8 V ≤ EVDD ≤ 5.5 V | 1/fMCK + 31 | 1/fMCK + 31 | 1/fMCK + 31 | 1/fMCK + 31 | ns | | | | | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 1/fMCK + 250 | 1/fMCK + 250 | 1/fMCK + 250 | 1/fMCK + 250 | | | | | | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | — | — | — | | | | | | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit | | |
|---|--------|---------------------|---------------------------|-----------------|--------------------------|-----------------|--------------------------|-----------------|----------------------------|-----------------|-----------------|-----------------|----|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | | |
| Delay time from SCKp↓ to SOp output Note 1 | tkso2 | C = 30 pF Note 2 | 2.7 V ≤ EVDD ≤ 5.5 V | | 2/fmck + 44 | | 2/fmck + 110 | | 2/fmck + 110 | | 2/fmck + 110 | ns | |
| | | | 2.4 V ≤ EVDD ≤ 5.5 V | | 2/fmck + 75 | | | | | | | | |
| | | | 1.8 V ≤ EVDD ≤ 5.5 V | | 2/fmck + 110 | | | | | | | | |
| | | | 1.7 V ≤ EVDD ≤ 5.5 V | | 2/fmck + 220 | | 2/fmck + 220 | | 2/fmck + 220 | | 2/fmck + 220 | | |
| | | | 1.6 V ≤ EVDD ≤ 5.5 V | | — | | | | | | | | |
| SSI00 setup time | tssik | DAPmn = 0 | 2.7 V ≤ VDD ≤ 5.5 V | 120 | | 120 | | 120 | | 120 | | ns | |
| | | | 1.8 V ≤ VDD < 2.7 V | 200 | | 200 | | 200 | | 200 | | | |
| | | | 1.7 V ≤ VDD < 1.8 V | 400 | | 400 | | 400 | | 400 | | | |
| | | | 1.6 V ≤ VDD < 1.7 V | — | | | | | | | | | |
| | | DAPmn = 1 | 2.7 V ≤ VDD ≤ 5.5 V | 1/fmck + 120 | | 1/fmck + 120 | | 1/fmck + 120 | | 1/fmck + 120 | | 1/fmck + 120 | ns |
| | | | 1.8 V ≤ VDD < 2.7 V | 1/fmck + 200 | | 1/fmck + 200 | | 1/fmck + 200 | | 1/fmck + 200 | | 1/fmck + 200 | |
| | | | 1.7 V ≤ VDD < 1.8 V | 1/fmck + 400 | | 1/fmck + 400 | | 1/fmck + 400 | | 1/fmck + 400 | | 1/fmck + 400 | |
| | | | 1.6 V ≤ VDD < 1.7 V | — | | | | | | | | | |
| SSI00 hold time | tkssi | DAPmn = 0 | 2.7 V ≤ VDD ≤ 5.5 V | 1/fmck + 120 | | 1/fmck + 120 | | 1/fmck + 120 | | 1/fmck + 120 | | ns | |
| | | | 1.8 V ≤ VDD < 2.7 V | 1/fmck + 200 | | 1/fmck + 200 | | 1/fmck + 200 | | 1/fmck + 200 | | | |
| | | | 1.7 V ≤ VDD < 1.8 V | 1/fmck + 400 | | 1/fmck + 400 | | 1/fmck + 400 | | 1/fmck + 400 | | | |
| | | | 1.6 V ≤ VDD < 1.7 V | — | | | | | | | | | |
| | | DAPmn = 1 | 2.7 V ≤ VDD ≤ 5.5 V | 120 | | 120 | | 120 | | 120 | | 120 | ns |
| | | | 1.8 V ≤ VDD < 2.7 V | 200 | | 200 | | 200 | | 200 | | 200 | |
| | | | 1.7 V ≤ VDD < 1.8 V | 400 | | 400 | | 400 | | 400 | | 400 | |
| | | | 1.6 V ≤ VDD < 1.7 V | — | | | | | | | | | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fmck: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin**(TA = -40 to +85°C, 1.6 V ≤ EVDD = VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|------------|---------------------|-----------------------|---------------------------|------------------|--------------------------|--------------|--------------------------|--------------|----------------------------|--------------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | tkcy2 | 4.0 V ≤ VDD ≤ 5.5 V | fMCK > 20 MHz | 14/fMCK | — | — | — | — | — | — | ns | |
| | | | fMCK ≤ 20 MHz | 12/fMCK | — | — | — | — | — | | | |
| | | 2.7 V ≤ VDD ≤ 5.5 V | fMCK > 16 MHz and 850 | 14/fMCK and 850 | — | — | — | — | — | — | | |
| | | | fMCK ≤ 16 MHz | 12/fMCK and 850 | — | — | — | — | — | — | | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | | — | 12/fMCK and 1000 | — | — | — | — | — | | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | — | 12/fMCK | — | — | — | — | | |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | 12/fMCK | | |
| 1.6 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | — | | | | |
| SCKp high-/low-level width | tkH2, tkL2 | 4.0 V ≤ VDD ≤ 5.5 V | | tkcy2/2 - 7 | — | tkcy2/2 - 7 | — | tkcy2/2 - 7 | — | tkcy2/2 - 7 | ns | |
| | | 2.7 V ≤ VDD ≤ 5.5 V | | tkcy2/2 - 8 | — | tkcy2/2 - 8 | — | tkcy2/2 - 8 | — | tkcy2/2 - 8 | | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | — | tkcy2/2 - 18 | — | tkcy2/2 - 18 | — | tkcy2/2 - 18 | | |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | tkcy2/2 - 66 | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | — | | |
| Slp setup time (to SCKp↑) Note 1 | tsik2 | 2.7 V ≤ VDD ≤ 5.5 V | | 1/fMCK + 20 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | ns | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | | 1/fMCK + 30 | — | — | — | — | — | — | | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | — | | |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | 1/fMCK + 40 | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | — | | |
| Slp hold time (from SCKp↑) Note 2 | tkSI2 | 2.4 V ≤ VDD ≤ 5.5 V | | 1/fMCK + 31 | — | 1/fMCK + 31 | — | 1/fMCK + 31 | — | 1/fMCK + 31 | ns | |
| | | 1.8 V ≤ VDD ≤ 5.5 V | | — | — | 1/fMCK + 31 | — | 1/fMCK + 31 | — | 1/fMCK + 31 | | |
| | | 1.7 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | 1/fMCK + 250 | | |
| | | 1.6 V ≤ VDD ≤ 5.5 V | | — | — | — | — | — | — | — | | |
| Delay time from SCKp↓ to SOp output Note 3 | tkSO2 | C = 30 pF Note 4 | 2.7 V ≤ VDD ≤ 5.5 V | — | 2/fMCK + 160 | — | 2/fMCK + 260 | — | 2/fMCK + 260 | — | 2/fMCK + 260 | ns |
| | | | 2.4 V ≤ VDD ≤ 5.5 V | — | 2/fMCK + 190 | — | — | — | — | — | | |
| | | | 1.8 V ≤ VDD ≤ 5.5 V | — | — | — | — | — | — | — | | |
| | | | 1.7 V ≤ VDD ≤ 5.5 V | — | — | — | — | — | — | — | | |
| | | | 1.6 V ≤ VDD ≤ 5.5 V | — | — | — | — | — | — | — | 2/fMCK + 320 | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

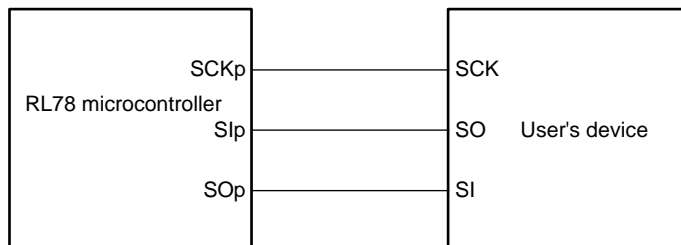
Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM

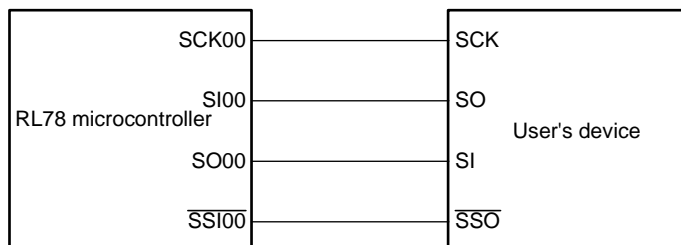
numbers (g = 0, 4 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
 n: Channel number (mn = 00 to 03))

CSI mode connection diagram (during communication at same potential)

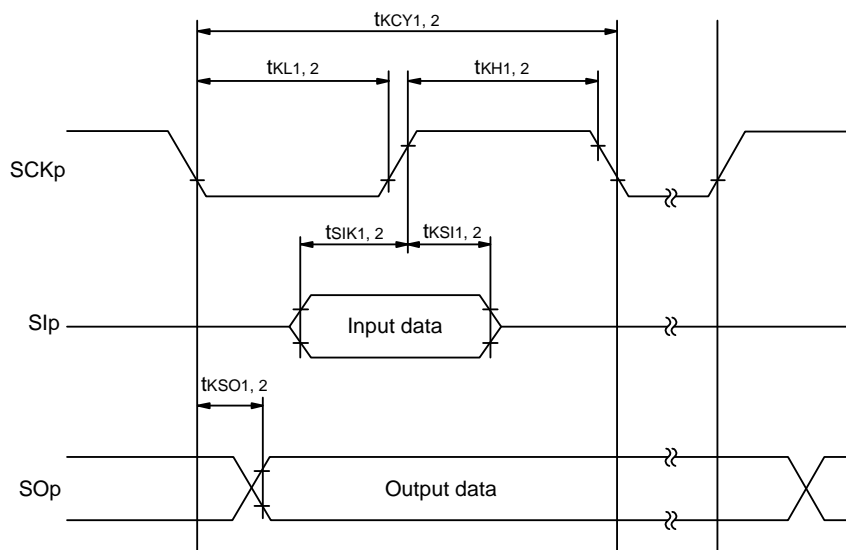


**CSI mode connection diagram (during communication at same potential)
 (Slave Transmission of slave select input function (CSI00))**

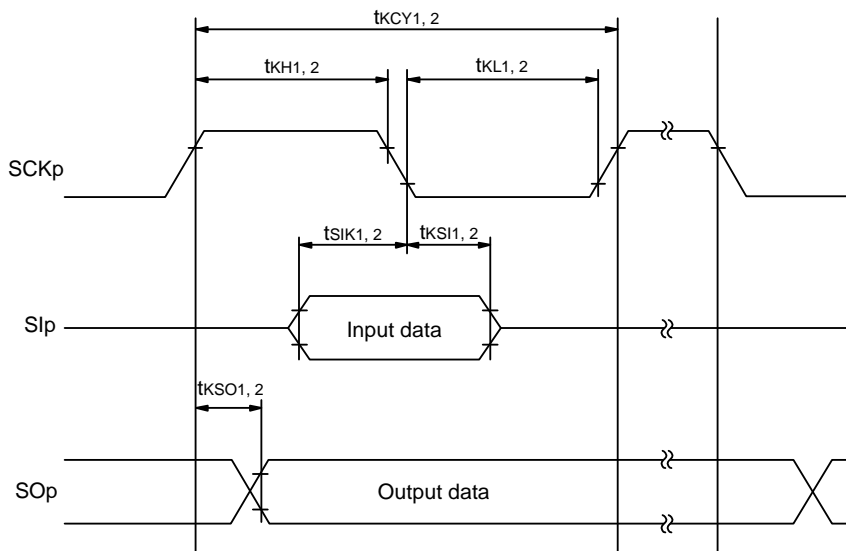


Remark p: CSI number (p = 00, 01, 10 and 11)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(5) During communication at same potential (simplified I²C mode)

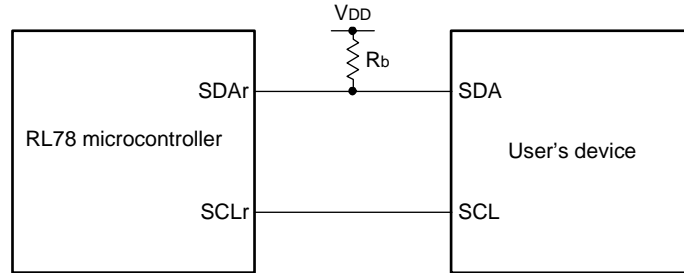
(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|-------------------------------|-------------------------|--|---------------------------------------|----------------|---------------------------------------|---------------|---------------------------------------|---------------|---------------------------------------|---------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | f _{SCL} | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | | 250 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | | 400 Note 1 | | | | | | | |
| | | 1.8 V ≤ EVDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ | | 300 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | |
| | | 1.7 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | |
| | | 1.6 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | | — | | | | | | | |
| Hold time when SCLr = "L" | t _{LOW} | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 475 | | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 1150 | | | | | | | | |
| | | 1.8 V ≤ EVDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ | 1550 | | 1550 | | 1550 | | 1550 | | |
| | | 1.7 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | 1850 | | 1850 | | 1850 | | 1850 | | |
| | | 1.6 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | — | | | | | | | | |
| Hold time when SCLr = "H" | t _{HIGH} | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 475 | | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 1150 | | | | | | | | |
| | | 1.8 V ≤ EVDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ | 1550 | | 1550 | | 1550 | | 1550 | | |
| | | 1.7 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | 1850 | | 1850 | | 1850 | | 1850 | | |
| | | 1.6 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | — | | | | | | | | |
| Data setup time (reception) | t _{SETUP: DAT} | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 1/f _{MCK} + 85 Note 2 | | 1/f _{MCK} + 145 Note 2 | | 1/f _{MCK} + 145 Note 2 | | 1/f _{MCK} + 145 Note 2 | | ns |
| | | 1.8 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 1/f _{MCK} + 145 Note 2 | | | | | | | | |
| | | 1.8 V ≤ EVDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ | 1/f _{MCK} + 230 Note 2 | | 1/f _{MCK} + 230 Note 2 | | 1/f _{MCK} + 230 Note 2 | | 1/f _{MCK} + 230 Note 2 | | |
| | | 1.7 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | 1/f _{MCK} + 290 Note 2 | | 1/f _{MCK} + 290 Note 2 | | 1/f _{MCK} + 290 Note 2 | | 1/f _{MCK} + 290 Note 2 | | |
| | | 1.6 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | — | | | | | | | | |
| Data hold time (transmission) | t _{HD: DAT} | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | | 355 | | 355 | | 355 | | 355 | |
| | | 1.8 V ≤ EVDD < 2.7 V, Cb = 100 pF, Rb = 5 kΩ | | 405 | | 405 | | 405 | | 405 | |
| | | 1.7 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | | | | | | | | | |
| | | 1.6 V ≤ EVDD < 1.8 V, Cb = 100 pF, Rb = 5 kΩ | — | — | | | | | | | |

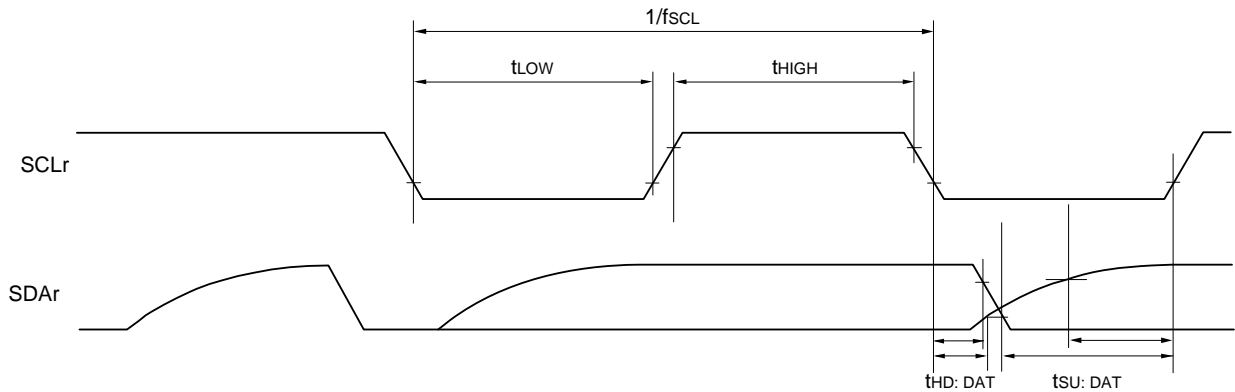
- Note 1.** The value must be equal to or less than $f_{MCK}/4$.
- Note 2.** Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.

Caution Select the normal input buffer and the N-ch open drain output (EVDD tolerance) mode for the $SDAr$ pin and the normal output mode for the $SCLr$ pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. $R_b[\Omega]$: Communication line ($SDAr$) pull-up resistance, $C_b[F]$: Communication line ($SDAr$, $SCLr$) load capacitance
 r: IIC number (r = 00, 01, 10 and 11), g: PIM number (g = 0, 3 and 5), h: POM number (h = 0, 3 and 5)

Remark 2. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the $CKSmn$ bit of serial mode register mn ($SMRmn$). m: Unit number (m = 0),
 n: Channel number (n = 0 to 3), $mn = 00$ to 03)

(6) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (UART mode) (dedicated baud rate generator output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit | |
|---------------|--------|------------|--|------|--------------------------|------|--------------------------|------|----------------------------|------|----------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Transfer rate | | reception | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | | fMCK/6 Note 1 | | fMCK/6 Note 1 | | fMCK/6 Note 1 | | fMCK/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 4.0 | | 1.3 | | 0.1 | | 0.6 | Mbps |
| | | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | | fMCK/6 Note 1 | | fMCK/6 Note 1 | | fMCK/6 Note 1 | | fMCK/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 4.0 | | 1.3 | | 0.1 | | 0.6 | Mbps |
| | | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V | | fMCK/6 Notes 1, 2, 4 | | fMCK/6 Notes 1, 2 | | fMCK/6 Notes 1, 2 | | fMCK/6 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 4.0 | | 1.3 | | 0.1 | | 0.6 | Mbps |

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.**Note 2.** Use it with EVDD ≥ Vb.**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LP (low-power main) mode: 1 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Note 4. The following conditions are required for low voltage interface when EVDD < VDD

2.4 V ≤ EVDD < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD < 2.4 V: MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EVDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.**Remark 1.** Vb[V]: Communication line voltage**Remark 2.** q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3, 5 and 12)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03))

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit | |
|---------------|--------|--------------|--|------|--------------------------|------|--------------------------|------|----------------------------|------|----------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Transfer rate | | Transmission | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | | Note 1 | | Note 1 | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V | | 2.8 Note 2 | | 2.8 Note 2 | | 2.8 Note 2 | | 2.8 Note 2 | Mbps |
| | | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | | Note 3 | | Note 3 | | Note 3 | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V | | 1.2 Note 4 | | 1.2 Note 4 | | 1.2 Note 4 | | 1.2 Note 4 | Mbps |
| | | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V | | Notes 5, 6 | | Notes 5, 6 | | Notes 5, 6 | | Notes 5, 6 | bps |
| | | | Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V | | 0.43 Note 7 | | 0.43 Note 7 | | 0.43 Note 7 | | 0.43 Note 7 | Mbps |

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ and $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $2.7\text{ V} \leq EV_{DD} \leq 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

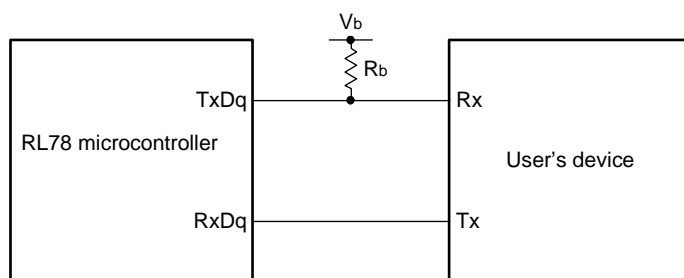
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

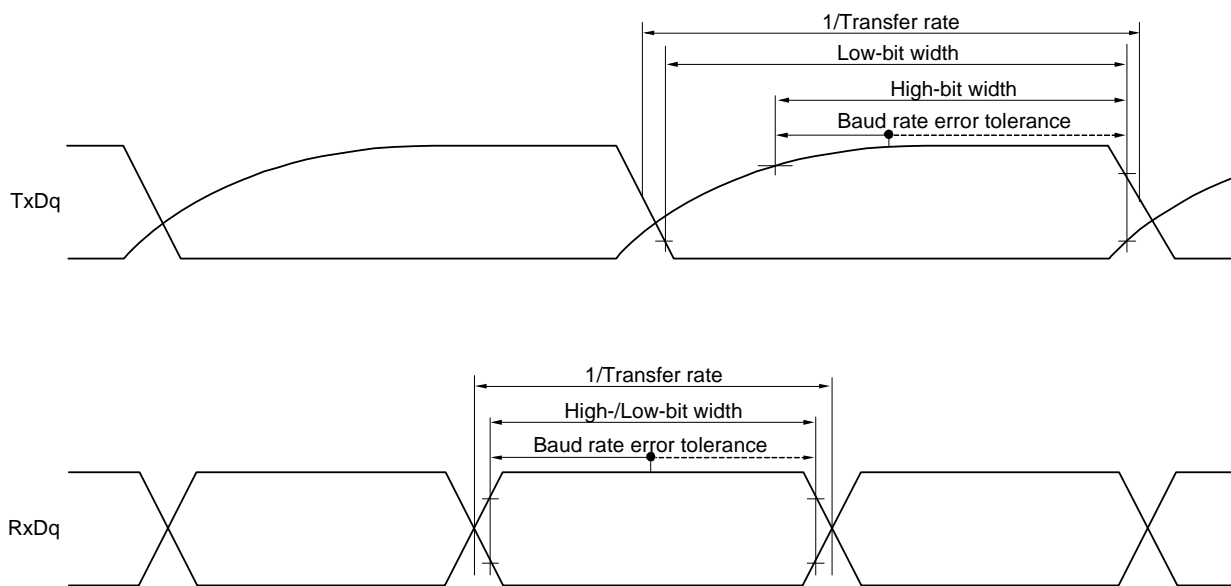
Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3, 5 and 12)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(TA = -40 to +85°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|--|--------|---|---|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 2/fCLK | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | 200 | | 1150 | | 1150 | | 1150 | | ns |
| | | tkCY1 ≥ 2/fCLK | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | 300 | | | | | | | | ns |
| SCKp high-level width | tkH1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | tkCY1/2 - 120 | | tkCY1/2 - 120 | | tkCY1/2 - 120 | | tkCY1/2 - 120 | | ns |
| SCKp low-level width | tkL1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | tkCY1/2 - 7 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | tkCY1/2 - 10 | | | | | | | | |
| Slp setup time (to SCKp↑) Note 1 | tSIK1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | 58 | | 479 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | 121 | | | | | | | | |
| Slp hold time (from SCKp↑) Note 1 | tKSI1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | 10 | | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | | | | | | | | | |
| Delay time from SCKp↓ to SOP output Note 1 | tkSO1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | | 60 | | 60 | | 60 | | 60 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | | 130 | | 130 | | 130 | | 130 | |
| Slp setup time (to SCKp↓) Note 2 | tSIK1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | 23 | | 110 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | 33 | | | | | | | | |
| Slp hold time (from SCKp↓) Note 2 | tKSI1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | 10 | | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | | | | | | | | | |

(TA = -40 to +85°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|--------|---|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Delay time from SCKp↑ to SOp output ^{Note 2} | tkso1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ | | 10 | | 10 | | 10 | | 10 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ | | | | | | | | | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EVDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 5)

Remark 3. fмск: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|-----------------------|--------|---|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 4/fCLK 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 300 | | 1150 | | 1150 | | 1150 | | ns |
| | | | 500 | | | | | | | | ns |
| | | | 1150 | | | | | | | | ns |
| SCKp high-level width | tkH1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | tkCY1/2 - 75 | | tkCY1/2 - 75 | | tkCY1/2 - 75 | | tkCY1/2 - 75 | | ns |
| | | | tkCY1/2 - 170 | | tkCY1/2 - 170 | | tkCY1/2 - 170 | | tkCY1/2 - 170 | | ns |
| | | | tkCY1/2 - 458 | | tkCY1/2 - 458 | | tkCY1/2 - 458 | | tkCY1/2 - 458 | | ns |
| SCKp low-level width | tkL1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | tkCY1/2 - 12 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | tkCY1/2 - 50 | | ns |
| | | | tkCY1/2 - 18 | | | | | | | | ns |
| | | | tkCY1/2 - 50 | | | | | | | | ns |

Note Use it with EVDD ≥ Vb.**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output (EVDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

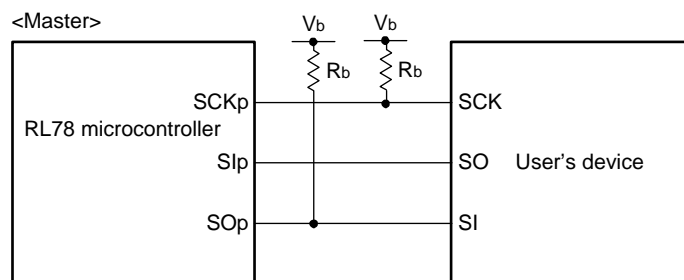
(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|--|--------|--|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Slp setup time (to SCKp↑) Note 1 | tsIK1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 81 | | 479 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | 177 | | | | | | | | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | 479 | | | | | | | | |
| Slp hold time (from SCKp↑) Note 1 | tkSI1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 19 | | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | | | | | | | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | | | | | | | | |
| Delay time from SCKp↓ to SOp output Note 1 | tkSO1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | | 100 | | 100 | | 100 | | 100 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | 195 | | 195 | | 195 | | 195 | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | 483 | | 483 | | 483 | | 483 | |
| Slp setup time (to SCKp↓) Note 2 | tsIK1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 44 | | 110 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | | | | | | | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | 110 | | | | | | | | |
| Slp hold time (from SCKp↓) Note 2 | tkSI1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 19 | | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | | | | | | | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | | | | | | | | |
| Delay time from SCKp↑ to SOp output Note 2 | tkSO1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | | 25 | | 25 | | 25 | | 25 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | | | | | | | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | | | | | | | | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 3.** Use it with EVDD ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EVDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

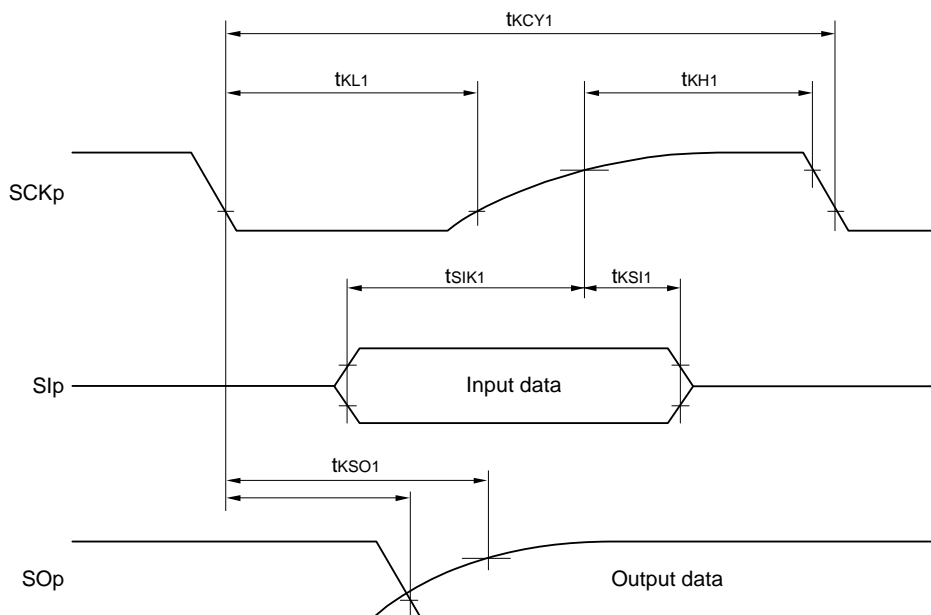
CSI mode connection diagram (during communication at different potential)

Remark 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

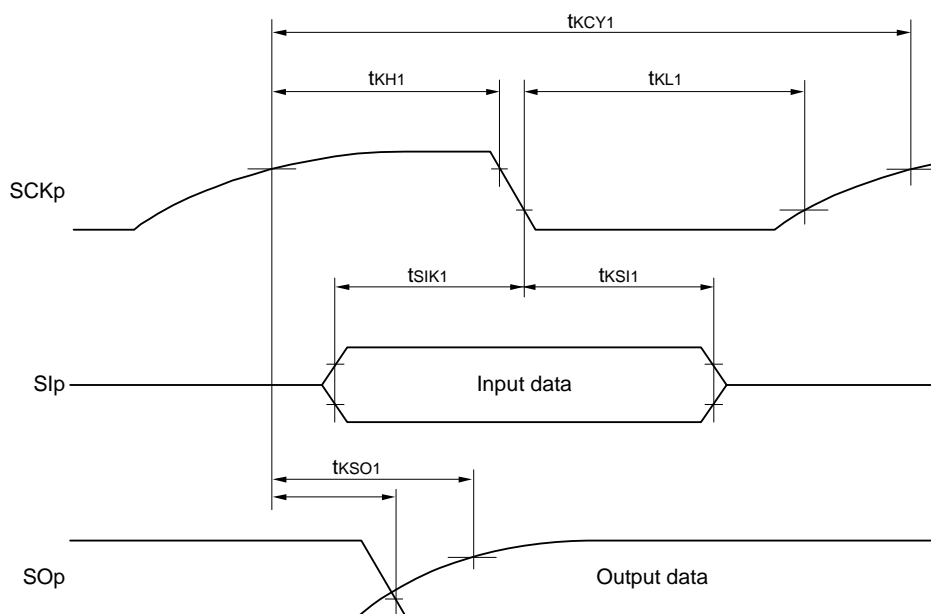
Remark 2. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{mck} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(9) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to 85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

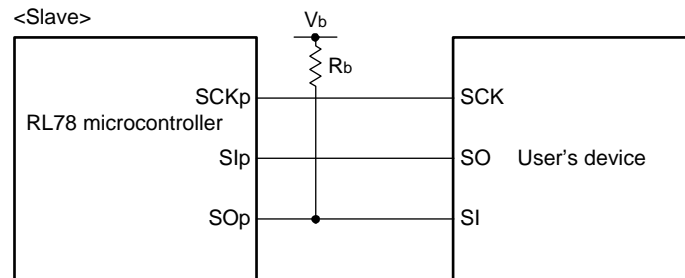
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|---|--|--|---------------------------|--------------|--------------------------|--------------|--------------------------|--------------|----------------------------|--------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time <small>Note 1</small> | tkcy2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | 20 MHz < fMCK ≤ 24 MHz | 12/fMCK | — | — | — | — | — | — | ns |
| | | | 8 MHz < fMCK ≤ 20 MHz | 10/fMCK | — | — | — | — | — | — | ns |
| | | | 4 MHz < fMCK ≤ 8 MHz | 8/fMCK | — | 16/fMCK | — | — | — | — | ns |
| | | | fMCK ≤ 4 MHz | 6/fMCK | — | 10/fMCK | 10/fMCK | — | 10/fMCK | — | ns |
| | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | 20 MHz < fMCK ≤ 24 MHz | 16/fMCK | — | — | — | — | — | — | ns | |
| | | 16 MHz < fMCK ≤ 20 MHz | 14/fMCK | — | — | — | — | — | — | ns | |
| | | 8 MHz < fMCK ≤ 16 MHz | 12/fMCK | — | — | — | — | — | — | ns | |
| | | 4 MHz < fMCK ≤ 8 MHz | 8/fMCK | — | 16/fMCK | — | — | — | — | ns | |
| | 1.8 V ≤ EVDD < 2.7 V, 1.6 V ≤ Vb ≤ 2.0 V <small>Note 2</small> | 20 MHz < fMCK ≤ 24 MHz | 36/fMCK | — | — | — | — | — | — | ns | |
| | | 16 MHz < fMCK ≤ 20 MHz | 32/fMCK | — | — | — | — | — | — | ns | |
| | | 8 MHz < fMCK ≤ 16 MHz | 26/fMCK | — | — | — | — | — | — | ns | |
| | | 4 MHz < fMCK ≤ 8 MHz | 16/fMCK | — | 16/fMCK | — | — | — | — | ns | |
| | fMCK ≤ 4 MHz | 10/fMCK | — | 10/fMCK | 10/fMCK | — | 10/fMCK | — | ns | | |
| SCKp high-/low-level width | tkH2, tkL2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | tkcy2/2 - 12 | — | tkcy2/2 - 50 | — | tkcy2/2 - 50 | — | tkcy2/2 - 50 | ns | |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | tkcy2/2 - 18 | — | tkcy2/2 - 50 | — | tkcy2/2 - 50 | — | tkcy2/2 - 50 | ns | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <small>Note 2</small> | tkcy2/2 - 50 | — | tkcy2/2 - 50 | — | tkcy2/2 - 50 | — | tkcy2/2 - 50 | ns | |
| Slp setup time (to SCKp1) <small>Note 3</small> | tsIK2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | 1/fMCK + 20 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | ns | |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | 1/fMCK + 20 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | ns | |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <small>Note 2</small> | 1/fMCK + 30 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | — | 1/fMCK + 30 | ns | |
| Slp hold time (from SCKp1) <small>Note 3</small> | tkSI2 | | 1/fMCK + 31 | — | 1/fMCK + 31 | — | 1/fMCK + 31 | — | 1/fMCK + 31 | ns | |
| Delay time from SCKp↓ to SOP output <small>Note 4</small> | tkSO2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | — | 2/fMCK + 120 | — | 2/fMCK + 573 | — | 2/fMCK + 573 | — | 2/fMCK + 573 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | — | 2/fMCK + 214 | — | 2/fMCK + 573 | — | 2/fMCK + 573 | — | 2/fMCK + 573 | ns |
| | | 1.8 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <small>Note 2</small> , Cb = 30 pF, Rb = 5.5 kΩ | — | 2/fMCK + 573 | — | 2/fMCK + 573 | — | 2/fMCK + 573 | — | 2/fMCK + 573 | ns |

(Notes, Caution and Remarks are listed on the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with $EV_{DD} \geq V_b$.
- Note 3.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp setup time becomes “to $SCKp\downarrow$ ” and the Slp hold time becomes “from $SCKp\downarrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
- Note 4.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOp output becomes “from $SCKp\uparrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

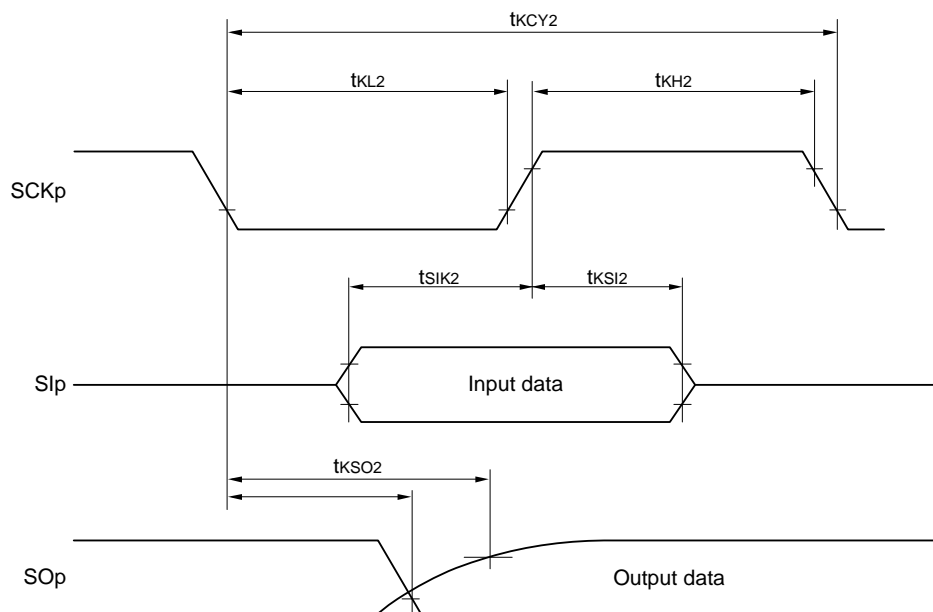
Caution Select the TTL input buffer for the Slp pin and $SCKp$ pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

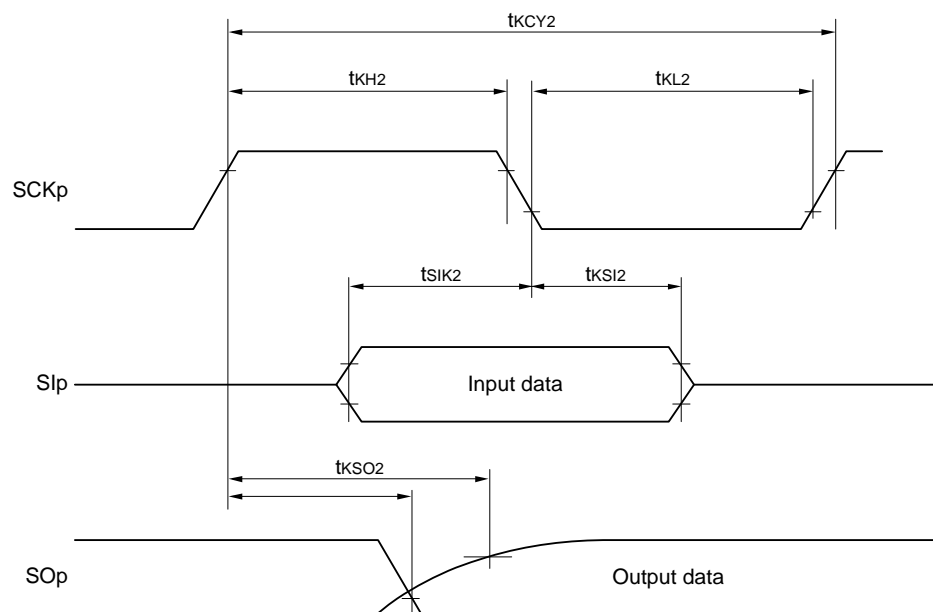


- Remark 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** p: CSI number (p = 00 to 03), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)
- Remark 3.** f_{mck} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

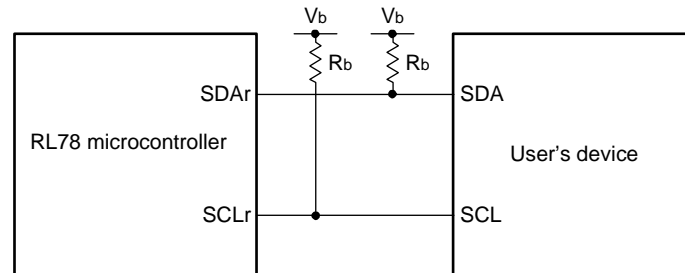
(10) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (simplified I²C mode)(TA = -40 to 85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LP (Low-power main) mode | | LV (low-voltage main) Mode | | Unit |
|-------------------------------|---------------------|---|------------------------------------|----------------|------------------------------------|---------------|------------------------------------|---------------|------------------------------------|---------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | f _{SCL} | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| | | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | | 400 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 250 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = "L" | t _{LOW} | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | 475 | | 1550 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | 475 | | 1550 | | 1550 | | 1550 | | ns |
| | | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | 1150 | | 1550 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | 1150 | | 1550 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ | 1550 | | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = "H" | t _{HIGH} | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | 245 | | 610 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | 200 | | 610 | | 610 | | 610 | | ns |
| | | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | 675 | | 610 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | 600 | | 610 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ | 610 | | 610 | | 610 | | 610 | | ns |
| Data setup time (reception) | t _{SU-DAT} | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 135 Note 3 | | 1/f _{MCK} + 190 Note 2 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 135 Note 3 | | 1/f _{MCK} + 190 Note 2 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | ns |
| | | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | ns |
| | | 1.8 V ≤ EV _{DD} < 4.0 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | 1/f _{MCK} + 190 Note 3 | | ns |
| Data hold time (transmission) | t _{HD-DAT} | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | 0 | 405 | ns |

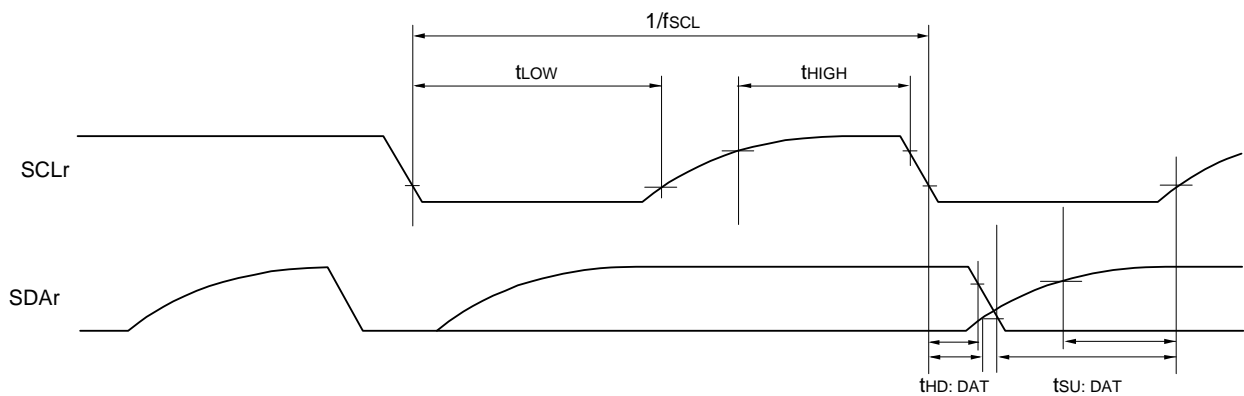
- Note 1.** The value must be equal to or less than $f_{MCK}/4$.
- Note 2.** Use it with $EV_{DD} \geq V_b$.
- Note 3.** Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.

Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



- Remark 1.** R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

2.5.2 Serial interface IICA

(1) I²C standard mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LP (Low-power main) mode | | LV (low-voltage main) mode | | Unit | |
|---|----------------------|--|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|-----|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| SCLA0 clock frequency | f _{SCL} | Standard mode: f _{CLK} ≥ 1 MHz | 2.7 V ≤ EVDD ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ EVDD ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ EVDD ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | t _{SU: STA} | 2.7 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 4.7 | | 4.7 | | 4.7 | | μs | |
| Hold time ^{Note 1} | t _{HD: STA} | 2.7 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 4.0 | | 4.0 | | 4.0 | | μs | |
| Hold time when SCLA0 = "L" | t _{LOW} | 2.7 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 4.7 | | 4.7 | | 4.7 | | μs | |
| Hold time when SCLA0 = "H" | t _{HIGH} | 2.7 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 4.0 | | 4.0 | | 4.0 | | μs | |
| Data setup time (reception) | t _{SU: DAT} | 2.7 V ≤ EVDD ≤ 5.5 V | 250 | | 250 | | 250 | | 250 | | ns | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 250 | | 250 | | 250 | | 250 | | ns | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 250 | | 250 | | 250 | | 250 | | ns | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 250 | | 250 | | 250 | | ns | |
| Data hold time (transmission) ^{Note 2} | t _{HD: DAT} | 2.7 V ≤ EVDD ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs | |
| Setup time of stop condition | t _{SU: STO} | 2.7 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | 4.0 | | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 4.0 | | 4.0 | | 4.0 | | μs | |
| Bus-free time | t _{BUF} | 2.7 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.7 V ≤ EVDD ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | 4.7 | | μs | |
| | | 1.6 V ≤ EVDD ≤ 5.5 V | — | | 4.7 | | 4.7 | | 4.7 | | μs | |

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of t_{HD: DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode**(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LP (Low-power main) mode | | LV (low-voltage main) mode | | Unit | |
|--|----------|------------------------------|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|-----|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| SCLA0 clock frequency | fsCL | Fast mode: fCLK ≥ 3.5 MHz | 2.7 V ≤ EVDD ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ EVDD ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | tsu: STA | 2.7 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| Hold time ^{Note 1} | tHD: STA | 2.7 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| Hold time when SCLA0 = "L" | tLOW | 2.7 V ≤ EVDD ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | 1.3 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | 1.3 | | μs | |
| Hold time when SCLA0 = "H" | tHIGH | 2.7 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| Data setup time (reception) | tsu: DAT | 2.7 V ≤ EVDD ≤ 5.5 V | 100 | | 100 | | 100 | | 100 | | ns | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 100 | | 100 | | 100 | | 100 | | ns | |
| Data hold time (transmission) ^{Note 2} | tHD: DAT | 2.7 V ≤ EVDD ≤ 5.5 V | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs | |
| Setup time of stop condition | tsu: STO | 2.7 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 0.6 | | 0.6 | | 0.6 | | 0.6 | | μs | |
| Bus-free time | tBUF | 2.7 V ≤ EVDD ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | 1.3 | | μs | |
| | | 1.8 V ≤ EVDD ≤ 5.5 V | 1.3 | | 1.3 | | 1.3 | | 1.3 | | μs | |

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IoH1, IoL1, VoH1, VoL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LP (Low-power main) mode | | LV (low-voltage main) mode | | Unit |
|--------------------------------------|----------|--|---------------------------|------|--------------------------|------|--------------------------|------|----------------------------|------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | fsCL | Fast mode plus: fCLK ≥ 10 MHz 2.7 V ≤ EVDD ≤ 5.5 V | 0 | 1000 | — | — | — | — | — | — | kHz |
| Setup time of restart condition | tsU: STA | 2.7 V ≤ EVDD ≤ 5.5 V | 0.26 | | — | — | — | — | — | — | μs |
| Hold time Note 1 | tHD: STA | 2.7 V ≤ EVDD ≤ 5.5 V | 0.26 | | — | — | — | — | — | — | μs |
| Hold time when SCLA0 = "L" | tLOW | 2.7 V ≤ EVDD ≤ 5.5 V | 0.5 | | — | — | — | — | — | — | μs |
| Hold time when SCLA0 = "H" | tHIGH | 2.7 V ≤ EVDD ≤ 5.5 V | 0.26 | | — | — | — | — | — | — | μs |
| Data setup time (reception) | tsU: DAT | 2.7 V ≤ EVDD ≤ 5.5 V | 50 | | — | — | — | — | — | — | ns |
| Data hold time (transmission) Note 2 | tHD: DAT | 2.7 V ≤ EVDD ≤ 5.5 V | 0 | 0.45 | — | — | — | — | — | — | μs |
| Setup time of stop condition | tsU: STO | 2.7 V ≤ EVDD ≤ 5.5 V | 0.26 | | — | — | — | — | — | — | μs |
| Bus-free time | tBUF | 2.7 V ≤ EVDD ≤ 5.5 V | 0.5 | | — | — | — | — | — | — | μs |

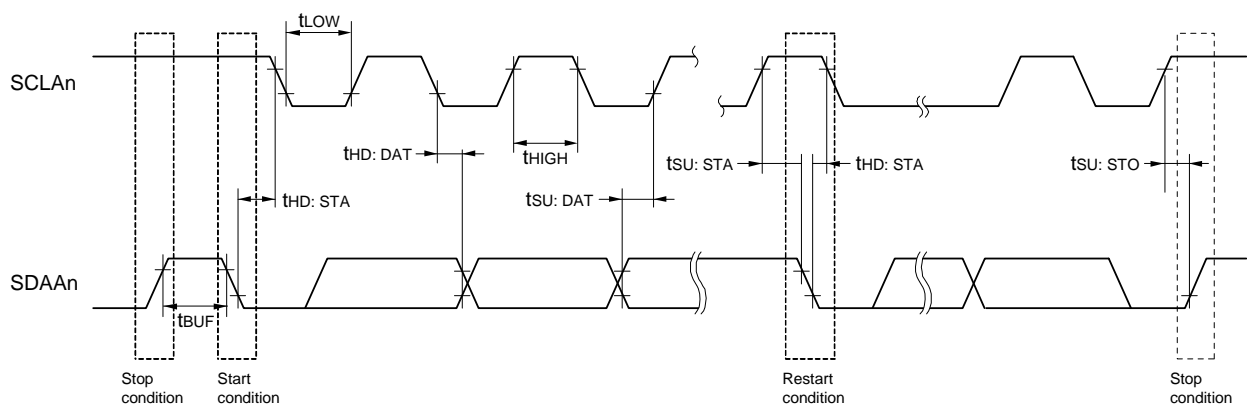
Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

I²C serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM | Reference voltage (+) = VDD Reference voltage (-) = VSS | Reference voltage (+) = VBGR Reference voltage (-) = AVREFM |
|---|-------------------|--|--|--|
| ANI0 to ANI3 | | Refer to 2.6.1 (1). | Refer to 2.6.1 (3). | Refer to 2.6.1 (4). |
| ANI16 to ANI22 | | Refer to 2.6.1 (2). | | |
| Internal reference voltage Temperature sensor output voltage | | Refer to 2.6.1 (1). | | |

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|--------|---|-------------------------------|--------|---------------|------|
| Resolution | RES | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution AVREFP = VDD Note 3 | 1.8 V ≤ AVREFP ≤ 5.5 V | 1.2 | ±3.5 | LSB |
| | | | 1.6 V ≤ AVREFP ≤ 5.5 V Note 4 | 1.2 | ±7.0 | LSB |
| Conversion time | tCONV | 10-bit resolution Target pin: ANI2 and ANI3 | 3.6 V ≤ VDD ≤ 5.5 V | 2.125 | 39 | μs |
| | | | 2.7 V ≤ VDD ≤ 5.5 V | 3.1875 | 39 | μs |
| | | | 1.8 V ≤ VDD ≤ 5.5 V | 17 | 39 | μs |
| | | | 1.6 V ≤ VDD ≤ 5.5 V | 57 | 95 | μs |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage | 3.6 V ≤ VDD ≤ 5.5 V | 2.375 | 39 | μs |
| | | | 2.7 V ≤ VDD ≤ 5.5 V | 3.5625 | 39 | μs |
| Zero-scale error Notes 1, 2 | EzS | 10-bit resolution AVREFP = VDD Note 3 | 1.8 V ≤ AVREFP ≤ 5.5 V | | ±0.25 | %FSR |
| | | | 1.6 V ≤ AVREFP ≤ 5.5 V Note 4 | | ±0.50 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution AVREFP = VDD Note 3 | 1.8 V ≤ AVREFP ≤ 5.5 V | | ±0.25 | %FSR |
| | | | 1.6 V ≤ AVREFP ≤ 5.5 V Note 4 | | ±0.50 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution AVREFP = VDD Note 3 | 1.8 V ≤ AVREFP ≤ 5.5 V | | ±2.5 | LSB |
| | | | 1.6 V ≤ AVREFP ≤ 5.5 V Note 4 | | ±5.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution AVREFP = VDD Note 3 | 1.8 V ≤ AVREFP ≤ 5.5 V | | ±1.5 | LSB |
| | | | 1.6 V ≤ AVREFP ≤ 5.5 V Note 4 | | ±2.0 | LSB |
| Analog input voltage | VAIN | ANI2 and ANI3 | 0 | | AVREFP | V |
| | | Internal reference voltage (1.8 V ≤ VDD ≤ 5.5 V) | | | VBGR Note 5 | V |
| | | Temperature sensor output voltage (1.8 V ≤ VDD ≤ 5.5 V) | | | VTMP25 Note 5 | V |

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 5. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI22

(TA = -40 to +85°C, $1.6\text{ V} \leq EV_{DD} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$,

Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|-------------------------------------|--------|---|--|--------|---------------------------------|-------|------|
| Resolution | RES | | 8 | | 10 | bit | |
| Overall error Note 1 | AINL | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | 1.2 | ±5.0 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | 1.2 | ±8.5 | LSB |
| Conversion time | tCONV | 10-bit resolution Target ANI pin: ANI16 to ANI22 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 17 | 39 | μs |
| | | | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | | 57 | 95 | μs |
| Zero-scale error Notes 1, 2 | EzS | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ±0.35 | %FSR |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ±0.35 | %FSR |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ±3.5 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ±6.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ±2.0 | LSB |
| | | | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5 | | | ±2.5 | LSB |
| Analog input voltage | VAIN | ANI16 to ANI22 | 0 | | AV_{REFP} and EV_{DD} | V | |

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD} \leq AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--|-------------------|---|--|--------|------------------|-------|------|
| Resolution | RES | | 8 | | 10 | bit | |
| Overall error Note 1 | AINL | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V Note 3 | | 1.2 | ±10.5 | LSB |
| Conversion time | t _{CONV} | 10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ V _{DD} ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V | 57 | | 95 | μs |
| | | 10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.5625 | | 39 | μs |
| 1.8 V ≤ V _{DD} ≤ 5.5 V | 17 | | | 39 | μs | | |
| Zero-scale error Notes 1, 2 | E _{zs} | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Full-scale error Notes 1, 2 | E _{fs} | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V Note 3 | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 1.8 V ≤ V _{DD} ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ V _{DD} ≤ 5.5 V Note 3 | | | ±2.5 | LSB |
| Analog input voltage | V _{AIN} | ANI0 to ANI3 | 0 | | V _{DD} | V | |
| | | ANI16 to ANI22 | 0 | | EV _{DD} | V | |
| | | Internal reference voltage (1.8 V ≤ V _{DD} ≤ 5.5 V) | V _{BGR} Note 4 | | | V | |
| | | Temperature sensor output voltage (1.8 V ≤ V _{DD} ≤ 5.5 V) | V _{TMPS25} Note 4 | | | V | |

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 4. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 and ANI3, ANI16 to ANI22

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD ≤ VDD, VSS = 0 V, Reference voltage (+) = VBGR Note 3, Reference voltage (-) = AVREFM = 0 V Note 4)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|--------|------------|------|------|-------------|-------|
| Resolution | RES | | 8 | | | bit |
| Conversion time | tCONV | | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | Ezs | | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | | | | ±1.0 | LSB |
| Analog input voltage | VAIN | | 0 | | VBGR Note 3 | V |

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|---------|--|------|------|------|-------|
| Temperature sensor output voltage | VTMPS25 | Setting ADS register = 80H, TA = +25°C | | 1.05 | | V |
| Internal reference voltage | VBGR | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | FVTMPS | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | tAMP | 2.4 V ≤ VDD ≤ 5.5 V | 5 | | | μs |
| | | 1.8 V ≤ VDD < 2.4 V | 10 | | | μs |

2.6.3 D/A converter (channel 1)

(TA = -40 to +85°C, 1.6 V ≤ EVSS ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------|---------------------|------|------|------|------|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 1.8 V ≤ VDD ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 1.8 V ≤ VDD ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | tSET | Cload = 20 pF | 2.7 V ≤ VDD ≤ 5.5 V | | | 3 | μs |
| | | | 1.6 V ≤ VDD < 2.7 V | | | 6 | μs |

2.6.4 Comparator

(Comparator 0: TA = -40 to +85°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(Comparator 1: TA = -40 to +85°C, 1.6 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|--------|---|--|---------------|------|------------------------------|------|
| Input voltage range | VIREF0 | IVREF0 pin | | 0 | | V _{DD} - 1.4 Note 1 | V |
| | VIREF1 | IVREF1 pin | | 1.4 Note 1 | | V _{DD} | V |
| | VICMP | IVCMP0 pin | | -0.3 | | V _{DD} + 0.3 | V |
| | | IVCMP1 pin | | -0.3 | | EV _{DD} + 0.3 | V |
| Output delay | td | V _{DD} = 3.0 V Input slew rate > 50 mV/μs | Comparator high-speed mode, standard mode | | | 1.2 | μs |
| | | | Comparator high-speed mode, window mode | | | 2.0 | μs |
| | | | Comparator low-speed mode, standard mode | | 3 | | μs |
| | | | Comparator low-speed mode, window mode | | 4 | | μs |
| Operation stabilization wait time | tcMP | | | 100 | | | μs |
| Reference voltage declination in channel 0 of internal DAC Note 2 | ΔVIDAC | | | | | ± 2.5 | LSB |

Note 1. In window mode, make sure that VREF1 - VREF0 ≥ 0.2 V.

Note 2. Only in CMP0

2.6.5 PGA

(TA = -40 to +85°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---------------------|--|---|------------------------|------|-----------------------------|------|
| Input offset voltage | V _{IOPGA} | | | | | ±10 | mV |
| Input voltage range | V _{IPGA} | | | 0 | | 0.9 × V _{DD} /Gain | V |
| Output voltage range | V _{IOHPGA} | | | 0.93 × V _{DD} | | | V |
| | V _{IOHPGA} | | | | | 0.07 × V _{DD} | V |
| Gain error | | x4, x8 | | | | ±1 | % |
| | | x16 | | | | ±1.5 | % |
| | | x32 | | | | ±2 | % |
| Slew rate | SR _{RPGA} | Rising When V _{IN} = 0.1V _{DD} /gain to 0.9V _{DD} /gain. 10 to 90% of output voltage amplitude | 4.0 V ≤ V _{DD} ≤ 5.5 V (Other than x32) | 3.5 | | | V/μs |
| | | | 4.0 V ≤ V _{DD} ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ V _{DD} ≤ 4.0V | 0.5 | | | |
| | SR _{FPGA} | Falling When V _{IN} = 0.1V _{DD} /gain to 0.9V _{DD} /gain. 90 to 10% of output voltage amplitude | 4.0 V ≤ V _{DD} ≤ 5.5 V (Other than x32) | 3.5 | | | |
| | | | 4.0 V ≤ V _{DD} ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ V _{DD} ≤ 4.0V | 0.5 | | | |
| Reference voltage stabilization wait time ^{Note} | t _{PGA} | x4, x8 | | | | 5 | μs |
| | | x16, x32 | | | | 10 | μs |

Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

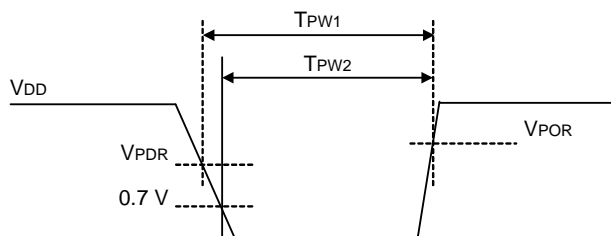
2.6.6 POR circuit characteristics

(TA = -40 to +85°C, Vss = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|------------------|--|------|------|------|------|
| Detection voltage | V _{POR} | The power supply voltage is rising. | 1.47 | 1.51 | 1.55 | V |
| | V _{PDR} | The power supply voltage is falling. <i>Note 1</i> | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width <i>Note 2</i> | T _{PW1} | Other than STOP/SUB HALT/SUB RUN | 300 | | | μs |
| | T _{PW2} | STOP/SUB HALT/SUB RUN | 300 | | | μs |

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +85°C, VPDR ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|--------------------------------------|--------|--------------------------------------|------|------|------|------|
| Detection voltage | Supply voltage level | VLVD0 | The power supply voltage is rising. | 3.98 | 4.06 | 4.14 | V |
| | | | The power supply voltage is falling. | 3.90 | 3.98 | 4.06 | V |
| | | VLVD1 | The power supply voltage is rising. | 3.68 | 3.75 | 3.82 | V |
| | | | The power supply voltage is falling. | 3.60 | 3.67 | 3.74 | V |
| | | VLVD2 | The power supply voltage is rising. | 3.07 | 3.13 | 3.19 | V |
| | | | The power supply voltage is falling. | 3.00 | 3.06 | 3.12 | V |
| | | VLVD3 | The power supply voltage is rising. | 2.96 | 3.02 | 3.08 | V |
| | | | The power supply voltage is falling. | 2.90 | 2.96 | 3.02 | V |
| | | VLVD4 | The power supply voltage is rising. | 2.86 | 2.92 | 2.97 | V |
| | | | The power supply voltage is falling. | 2.80 | 2.86 | 2.91 | V |
| | | VLVD5 | The power supply voltage is rising. | 2.76 | 2.81 | 2.87 | V |
| | | | The power supply voltage is falling. | 2.70 | 2.75 | 2.81 | V |
| | | VLVD6 | The power supply voltage is rising. | 2.66 | 2.71 | 2.76 | V |
| | | | The power supply voltage is falling. | 2.60 | 2.65 | 2.70 | V |
| | | VLVD7 | The power supply voltage is rising. | 2.56 | 2.61 | 2.66 | V |
| | | | The power supply voltage is falling. | 2.50 | 2.55 | 2.60 | V |
| | | VLVD8 | The power supply voltage is rising. | 2.45 | 2.50 | 2.55 | V |
| | | | The power supply voltage is falling. | 2.40 | 2.45 | 2.50 | V |
| | | VLVD9 | The power supply voltage is rising. | 2.05 | 2.09 | 2.13 | V |
| | | | The power supply voltage is falling. | 2.00 | 2.04 | 2.08 | V |
| | | VLVD10 | The power supply voltage is rising. | 1.94 | 1.98 | 2.02 | V |
| | | | The power supply voltage is falling. | 1.90 | 1.94 | 1.98 | V |
| | | VLVD11 | The power supply voltage is rising. | 1.84 | 1.88 | 1.91 | V |
| | | | The power supply voltage is falling. | 1.80 | 1.84 | 1.87 | V |
| | | VLVD12 | The power supply voltage is rising. | 1.74 | 1.77 | 1.81 | V |
| | | | The power supply voltage is falling. | 1.70 | 1.73 | 1.77 | V |
| VLVD13 | The power supply voltage is rising. | 1.64 | 1.67 | 1.70 | V | | |
| | The power supply voltage is falling. | 1.60 | 1.63 | 1.66 | V | | |
| Minimum pulse width | | tLW | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

(2) LVD Detection Voltage of Interrupt & Reset Mode

(TA = -40 to +85°C, VPDR ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------------|--|--|------------------------------|------|------|------|---|
| Interrupt and reset mode | VLVDA0 | VPOC0, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage | 1.60 | 1.63 | 1.66 | V | |
| | VLVDA1 | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | VLVDA2 | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | VLVDA3 | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | VLVDB0 | VPOC0, VPOC1, VPOC2 = 0, 0, 1, falling reset voltage | 1.80 | 1.84 | 1.87 | V | |
| | VLVDB1 | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | VLVDB2 | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | VLVDB3 | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | VLVDC0 | VPOC0, VPOC1, VPOC2 = 0, 1, 0, falling reset voltage | 2.40 | 2.45 | 2.50 | V | |
| | VLVDC1 | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | VLVDC2 | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| Falling interrupt voltage | | | 2.60 | 2.65 | 2.70 | V | |
| VLVDC3 | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V | |
| | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V | |
| VLVDD0 | VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage | 2.70 | 2.75 | 2.81 | V | | |
| VLVDD1 | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V | |
| | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V | |
| VLVDD2 | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V | |
| | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V | |
| VLVDD3 | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V | |
| | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V | |

2.6.8 Power supply voltage rising slope characteristics

(TA = -40 to +85°C, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------|------------|------|------|------|------|
| Power supply voltage rising slope | SVDD | | | | 54 | V/ms |

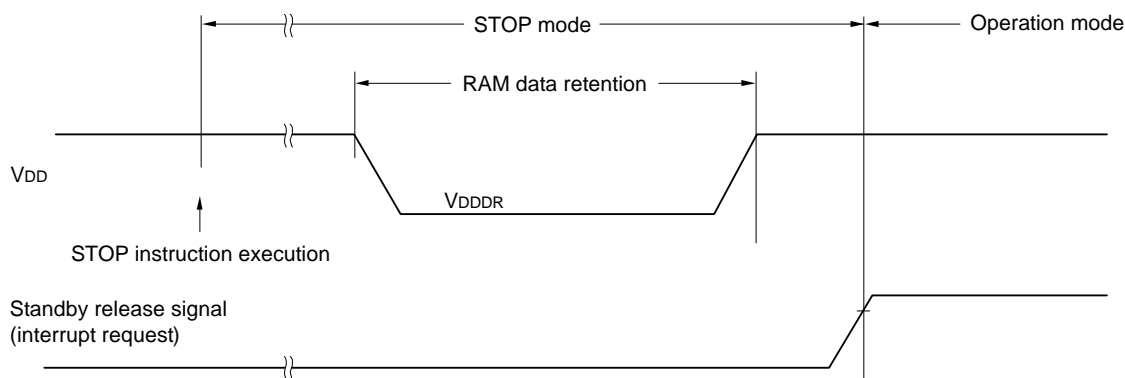
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------|------------|-----------|------|------|------|
| Data retention supply voltage | VDDDR | | 1.46 Note | | 5.5 | V |

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-------------------|-----------------------|-----------|---------|-----------|------|-------|
| System clock frequency | fCLK | 1.8 V ≤ VDD ≤ 5.5 V | | 1 | | 24 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | C _{erwr} | Retained for 20 years | TA = 85°C | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year | TA = 25°C | | 1,000,000 | | |
| | | Retained for 5 years | TA = 85°C | 100,000 | | | |
| | | Retained for 20 years | TA = 85°C | 10,000 | | | |

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|-----------|------|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

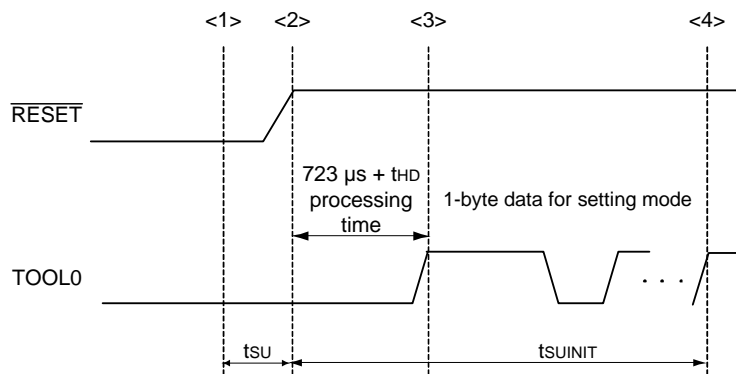
2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +85°C, 1.8 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|--|------|------|------|------|
| How long from when an external reset ends until the initial communication settings are specified ^{Note 1} | tsUNIT | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends ^{Note 1} | tsu | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) ^{Notes 1, 2} | tHD | POR and LVD reset must end before the external reset ends. | 1 | | | ms |

Note 1. Deassertion of the POR and LVD reset signals must precede deassertion of the pin reset signal.

Note 2. This excludes the flash firmware processing time (723 μs).



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsUNIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (TA = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications (TA = -40 to +105°C)

R5F105xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G11 User's Manual.

Caution 3. Please contact Renesas Electronics sales office for derating of operation under TA = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Caution 4. When operating temperature exceeds 85°C, only HS (high-speed main) mode can be used as the flash operation mode. Regulator mode should be used with the normal setting (MCSEL = 0).

Caution 5. The EVDD pin is not present on products with 24 or less pins. Accordingly, replace EVDD with VDD and the voltage condition $1.6 \leq EVDD \leq VDD \leq 5.5 \text{ V}$ with $1.6 \leq VDD \leq 5.5 \text{ V}$.

Remark When the products "G: Industrial applications" is used in the range of TA = -40 to +85°C, see 2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C).

| Fields of application | A: Consumer applications | G: Industrial applications |
|--|--|---|
| Operating ambient temperature | TA = -40 to +85°C | TA = -40 to +105°C |
| Operating mode Operating Voltage Range | HS (High-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 24 MHz 2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz LS (Low-speed main) mode: 1.8 V ≤ VDD ≤ 5.5 V @ 1 MHz to 8 MHz LV (Low-voltage main) mode: 1.8 V ≤ VDD ≤ 5.5 V @ 1 MHz to 4 MHz | Only in HS (High-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 24 MHz 2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz |
| High-speed on-chip oscillator clock to an accuracy | 1.8 V ≤ VDD ≤ 5.5 V: ±1.0% @ TA = -20 to +85°C ±1.5% @ TA = -40 to -20°C 1.6 V ≤ VDD < 1.8 V: ±5.0% @ TA = -20 to +85°C ±5.5% @ TA = -40 to -20°C | 2.4 V ≤ VDD ≤ 5.5 V: ±2.0% @ TA = +85 to +105°C ±1.0% @ TA = -20 to +85°C ±1.5% @ TA = -40 to -20°C |
| Serial array unit | UART CSI: fCLK/2 (12 Mbps are supported), fCLK/4 Simplified I ² C | UART CSI: fCLK/4 Simplified I ² C |
| IICA | Standard mode Fast mode Fast mode plus | Standard mode Fast mode |
| Voltage Detector | <ul style="list-style-type: none"> • Rising: 1.67 V to 4.06 V (14 levels) • Falling: 1.63 V to 3.98 V (14 levels) | <ul style="list-style-type: none"> • Rising: 2.61 V to 4.06 V (8 levels) • Falling: 2.55 V to 3.98 V (8 levels) |

Remark The electrical characteristics for "G: Industrial applications" differ from those for "A: Consumer applications" when the product is in use in an ambient temperature over 85°C. For details, see 3.1 to 3.10 in the following pages.

3.1 Absolute Maximum Ratings

(1/2)

| Parameter | Symbols | Conditions | Ratings | Unit |
|------------------------|---------------------|--|--|------|
| Supply voltage | V _{DD} | | -0.5 to +6.5 | V |
| | EV _{DD} | | -0.5 to +6.5 | V |
| | AV _{REFP} | | 0.3 to V _{DD} + 0.3 Note 2 | V |
| | AV _{REFM} | | -0.3 to V _{DD} + 0.3 Note 2 and AV _{REFM} ≤ AV _{REFP} | V |
| REGC pin input voltage | V _I REGC | REGC | -0.3 to +2.8 and -0.3 to V _{DD} + 0.3 Note 1 | V |
| Input voltage | V _{I1} | P00, P01, P30 to P33, P40, and P51 to P56 | -0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 Note 2 | V |
| | V _{I2} | P20 to P23, P121, P122, P125, P137, EXCLK, RESET | -0.3 to V _{DD} + 0.3 Note 2 | V |
| Output voltage | V _{O1} | P00, P01, P30 to P33, P40, and P51 to P56 | -0.3 to EV _{DD} + 0.3 and -0.3 to V _{DD} + 0.3 Note 2 | V |
| | V _{O2} | P20 to P23 | -0.3 to V _{DD} + 0.3 Note 2 | V |
| Analog input voltage | V _{A11} | ANI16 to ANI22 | -0.3 to EV _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 Notes 2, 3 | V |
| | V _{A12} | ANI0 to ANI3 | -0.3 to V _{DD} + 0.3 and -0.3 to AV _{REF} (+) + 0.3 Notes 2, 3 | V |

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(2/2)

| Parameter | Symbols | Conditions | | Ratings | Unit |
|-------------------------------|---------|----------------------------------|---------------------------------------|-------------|------|
| Output current, high | IOH1 | Per pin | P00, P01, P30 to P33, P40, P51 to P56 | -40 | mA |
| | | Total of all pins -170 mA | P00, P01, P40 | -70 | mA |
| | | | P30 to P33, P51 to P56 | -100 | mA |
| | IOH2 | Per pin | P20 to P23 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | IOL1 | Per pin | P00, P01, P30 to P33, P40, P51 to P56 | 40 | mA |
| | | Total of all pins 170 mA | P00, P01, P40 | 70 | mA |
| | | | P30 to P33, P51 to P56 | 100 | mA |
| | IOL2 | Per pin | P20 to P23 | 1 | mA |
| | | Total of all pins | | 4 | mA |
| Operating ambient temperature | TA | In normal operation mode | | -40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | Tstg | | | -65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1 characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Resonator | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---------------------|------|------|------|------|
| X1 clock oscillation frequency (fx) ^{Note} | Ceramic resonator/ crystal resonator | 2.7 V ≤ VDD ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ VDD < 2.7 V | 1.0 | | 16.0 | |

Note Indicates only permissible oscillator frequency ranges. Refer to **3.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

3.2.2 On-chip oscillator characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Oscillators | Parameters | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-----------------|----------------------|------|-------|------|------|
| High-speed on-chip oscillator clock frequency ^{Notes 1, 2} | f _{IH} | 2.7 V ≤ VDD ≤ 5.5 V | 1 | | 24 | MHz |
| | | 2.4 V ≤ VDD ≤ 5.5 V | 1 | | 16 | |
| High-speed on-chip oscillator clock frequency accuracy | | TA = +85°C to +105°C | -2 | | 2 | % |
| | | TA = -20°C to +85°C | -1 | | 1 | % |
| | | TA = -40°C to -20°C | -1.5 | | 1.5 | % |
| Middle-speed on-chip oscillator oscillation frequency ^{Note 2} | f _{IM} | | 1 | | 4 | MHz |
| Middle-speed on-chip oscillator oscillation frequency accuracy | | | -12 | | +12 | % |
| Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy | DIMT | | | 0.008 | | %/°C |
| Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy | DIMV | TA = 25°C | | 0.02 | | %/V |
| Low-speed on-chip oscillator clock frequency ^{Note 2} | f _{IL} | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | -15 | | +15 | % |

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **3.4 AC Characteristics** for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------------|---|---|----------------------|-------|----------------|------|
| Output current, high Note 1 | IOH1 | Per pin for P00, P01, P30 to P33, P40, and P51 to P56 | | | -3.0 Note 2 | mA |
| | | Total of P00, P01, and P40 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | -12.5 | mA |
| | | | 2.7 V ≤ EVDD < 4.0 V | | -10.0 | mA |
| | | | 2.4 V ≤ EVDD < 2.7 V | | -5.0 | mA |
| | | Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | -30.0 | mA |
| | | | 2.7 V ≤ EVDD < 4.0 V | | -19.0 | mA |
| | | | 2.4 V ≤ EVDD < 2.7 V | | -10.0 | mA |
| | Total of all pins (When duty ≤ 70% Note 3) | | | -42.5 | mA | |
| | IOH2 | Per pin for P20 to P23 | | | -0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2.4 V ≤ VDD ≤ 5.5 V | | -0.4 | mA |

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)
 <Example> Where n = 80% and IOH = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|----------------------|------|---------------|------|
| Output current, low Note 1 | IOL1 | Per pin for P00, P01, P30 to P33, P40, and P51 to P56 | | | 8.5 Note 2 | mA |
| | | Total of P00, P01, and P40 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | 36.0 | mA |
| | | | 2.7 V ≤ EVDD < 4.0 V | | 15.0 | mA |
| | | | 2.4 V ≤ EVDD < 2.7 V | | 9.0 | mA |
| | | Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3) | 4.0 V ≤ EVDD ≤ 5.5 V | | 40.0 | mA |
| | | | 2.7 V ≤ EVDD < 4.0 V | | 35.0 | mA |
| | 2.4 V ≤ EVDD < 2.7 V | | | 20.0 | mA | |
| | Total of all pins (When duty ≤ 70% Note 3) | | | 76.0 | mA | |
| | IOL2 | Per pin for P20 to P23 | | | 0.4 Note 2 | mA |
| Total of all pins (When duty ≤ 70% Note 3) | | 2.4 V ≤ VDD ≤ 5.5 V | | 1.6 | mA | |

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(3/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|---------------------|------------------|--|--|----------------------|------|----------------------|---|
| Input voltage, high | V _{IH1} | P00, P01, P30 to P33, P40, and P51 to P56 | Normal mode | 0.8 EV _{DD} | | EV _{DD} | V |
| | V _{IH2} | P00, P30 to P32, P40, P51 to P56 | TTL mode 4.0 V ≤ EV _{DD} ≤ 5.5 V | 2.2 | | EV _{DD} | V |
| | | | TTL mode 3.3 V ≤ EV _{DD} < 4.0 V | 2.0 | | EV _{DD} | V |
| | | | TTL mode 2.4 V ≤ EV _{DD} < 3.3 V | 1.5 | | EV _{DD} | V |
| | V _{IH3} | P20 to P23 (digital input) | | 0.7 V _{DD} | | V _{DD} | V |
| | V _{IH4} | P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$ | | 0.8 V _{DD} | | V _{DD} | V |
| Input voltage, low | V _{IL1} | P00, P01, P30 to P33, P40, and P51 to P56 | Normal mode | 0 | | 0.2 EV _{DD} | V |
| | V _{IL2} | P00, P30 to P32, P40, P51 to P56 | TTL mode 4.0 V ≤ EV _{DD} ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL mode 3.3 V ≤ EV _{DD} < 4.0 V | 0 | | 0.5 | V |
| | | | TTL mode 2.4 V ≤ EV _{DD} < 3.3 V | 0 | | 0.32 | V |
| | V _{IL3} | P20 to P23 (digital input) | | 0 | | 0.3 V _{DD} | V |
| | V _{IL4} | P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$ | | 0 | | 0.2 V _{DD} | V |

Caution The maximum value of V_{IH} of pins P00, P01, P20, P30 to P33, P40 and P51 to P56 is V_{DD} or EV_{DD}, even in the N-ch open-drain mode.

(P20: V_{DD})

(P00, P01, P30 to P33, P40, P51 to P56: EV_{DD})

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(4/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------|--------|--|--|------------|------|------|
| Output voltage, high | VOH1 | P00, P01, P30 to P33, P40, and P51 to P56 | 4.0 V ≤ EVDD ≤ 5.5 V, IOH = -3.0 mA | EVDD - 0.7 | | V |
| | | | 2.7 V ≤ EVDD ≤ 5.5 V, IOH = -2.0 mA | EVDD - 0.6 | | V |
| | | | 2.4 V ≤ EVDD ≤ 5.5 V IOH = -1.5 mA | EVDD - 0.5 | | V |
| | VOH2 | P20 to P23 | 2.4 V ≤ VDD ≤ 5.5 V, IOH = -100 μA | VDD - 0.5 | | V |
| Output voltage, low | VOL1 | P00, P01, P30 to P33, P40, and P51 to P56 | 4.0 V ≤ EVDD ≤ 5.5 V, IOL = 8.5 mA | | 0.7 | V |
| | | | 2.7 V ≤ EVDD ≤ 5.5 V, IOL = 3.0 mA | | 0.6 | V |
| | | | 2.7 V ≤ EVDD ≤ 5.5 V, IOL = 1.5 mA | | 0.4 | V |
| | | | 2.4 V ≤ EVDD ≤ 5.5 V, IOL = 0.6 mA | | 0.4 | V |
| | VOL2 | P20 to P23 | 2.4 V ≤ VDD ≤ 5.5 V, IOL = 400 μA | | 0.4 | V |

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(5/5)

| Items | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | | |
|-----------------------------|--------|---|-------------------------|---------------------------------------|------|------|-----|----|
| Input leakage current, high | ILI1 | P00, P01, P30 to P33, P40, and P51 to P56 | VI = EVDD | | 1 | μA | | |
| | ILI2 | P20 to P23, P125, P137, RESET | VI = VDD | | 1 | μA | | |
| | ILI3 | P121, P122, X1, X2, EXCLK | VI = VDD | In input port or external clock input | | 1 | μA | |
| | | | | In resonator connection | | 10 | μA | |
| Input leakage current, low | ILIL1 | P00, P01, P30 to P33, P40, and P51 to P56 | VI = VSS | | -1 | μA | | |
| | ILIL2 | P20 to P23, P125, P137, RESET | VI = VSS | | -1 | μA | | |
| | ILIL3 | P121, P122, X1, X2, EXCLK | VI = VSS | In input port or external clock input | | -1 | μA | |
| | | | | In resonator connection | | -10 | μA | |
| On-chip pull-up resistance | Ru | P00, P01, P30 to P33, P40, P51 to P56, P125 | VI = VSS, In input port | | 10 | 20 | 100 | kΩ |

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/3)

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit | | | | | |
|--------------------------|---------------------------|--|---|---------------------------|--|---------------------------|--------------------------------|-------------|----------------------|----|----|-----|-----|----|
| Supply current Note 1 | IDD1 | Operating mode | Basic operation | HS (high-speed main) mode | fHOCO = 48 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 1.7 | | mA | | | | |
| | | | | | | VDD = 3.0 V | | 1.7 | | | | | | |
| | | | | | fHOCO = 24 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 1.4 | | | | | | |
| | | | | | | VDD = 3.0 V | | 1.4 | | | | | | |
| | | | Normal operation | HS (high-speed main) mode | fHOCO = 48 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 3.5 | 7.3 | | mA | | | |
| | | | | | | VDD = 3.0 V | | 3.5 | 7.3 | | | | | |
| | | | | | fHOCO = 24 MHz ^{Note 3} fIH = 24 MHz ^{Note 3} | VDD = 5.0 V | | 3.2 | 6.7 | | | | | |
| | | | | | | VDD = 3.0 V | | 3.2 | 6.7 | | | | | |
| | | Normal operation | | HS (high-speed main) mode | fHOCO = 16 MHz ^{Note 3} fIH = 16 MHz ^{Note 3} | VDD = 5.0 V | | 2.4 | 4.9 | | | | | |
| | | | | | | VDD = 3.0 V | | 2.4 | 4.9 | | | | | |
| | | | | | Normal operation | HS (high-speed main) mode | fMX = 20 MHz ^{Note 2} | VDD = 5.0 V | Square wave input | | | 2.7 | 5.7 | mA |
| | | | | | | | | | Resonator connection | | | 2.8 | 5.8 | |
| | | VDD = 3.0 V | Square wave input | | | | 2.7 | 5.7 | | | | | | |
| | | | Resonator connection | | | | 2.8 | 5.8 | | | | | | |
| | | fMX = 10 MHz ^{Note 2} | VDD = 5.0 V | Square wave input | | 1.8 | 3.4 | | | | | | | |
| | | | | Resonator connection | | 1.9 | 3.5 | | | | | | | |
| VDD = 3.0 V | Square wave input | | 1.8 | 3.4 | | | | | | | | | | |
| | Resonator connection | | 1.9 | 3.5 | | | | | | | | | | |
| Normal operation | Subsystem clock operation | fIL = 15 kHz, TA = -40°C ^{Note 4} | | | 1.8 | 5.9 | μA | | | | | | | |
| | | | fIL = 15 kHz, TA = +25°C ^{Note 4} | | 1.9 | 5.9 | | | | | | | | |
| | | | fIL = 15 kHz, TA = +85°C ^{Note 4} | | 2.3 | 8.7 | | | | | | | | |
| | | | fIL = 15 kHz, TA = +105°C ^{Note 4} | | 3.0 | 20.9 | | | | | | | | |

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fIH: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. fIM: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. fIL: Low-speed on-chip oscillator clock frequency

Remark 5. fSUB: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/3)

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit | | |
|--|----------------------------|--------------|---------------------------|---|-------------------------|----------------------|------|------|------|----|
| Supply current Note 1 | I _{DD2} Note 2 | HALT mode | HS (high-speed main) mode | f _{HOCO} = 48 MHz Note 3 | V _{DD} = 5.0 V | | 0.59 | 3.45 | mA | |
| | | | | f _{HH} = 24 MHz Note 4 | V _{DD} = 3.0 V | | 0.59 | 3.45 | | |
| | | | | f _{HOCO} = 24 MHz Note 3 | V _{DD} = 5.0 V | | 0.41 | 2.85 | | |
| | | | | f _{HH} = 16 MHz Note 4 | V _{DD} = 3.0 V | | 0.41 | 2.85 | | |
| | | | | f _{HOCO} = 16 MHz Note 3 | V _{DD} = 5.0 V | | 0.39 | 2.08 | | |
| | | | | f _{HH} = 16 MHz Note 4 | V _{DD} = 3.0 V | | 0.39 | 2.08 | | |
| | | | HS (high-speed main) mode | f _{MX} = 20 MHz Note 3 | V _{DD} = 5.0 V | Square wave input | | 0.20 | 2.45 | mA |
| | | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | | V _{DD} = 3.0 V | Square wave input | | 0.20 | 2.45 | |
| | | | | f _{MX} = 10 MHz Note 3 | V _{DD} = 5.0 V | Square wave input | | 0.15 | 1.28 | |
| | | | | | | Resonator connection | | 0.30 | 1.36 | |
| | | | | | V _{DD} = 3.0 V | Square wave input | | 0.15 | 1.28 | |
| | | | Subsystem clock operation | f _{IL} = 15 kHz, T _A = -40°C Note 5 | | | 0.48 | 1.22 | μA | |
| | | | | f _{IL} = 15 kHz, T _A = +25°C Note 5 | | | 0.55 | 1.22 | | |
| f _{IL} = 15 kHz, T _A = +85°C Note 5 | | | | 0.80 | 3.30 | | | | | |
| f _{IL} = 15 kHz, T _A = +105°C Note 5 | | | | 2.00 | 17.3 | | | | | |

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{HM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(3/3)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--------------------------|----------------|---------------------|-------------|------|------|------|------|
| Supply current Note 1 | IDD3 Note 2 | STOP mode Note 3 | TA = -40°C | | 0.19 | 0.51 | μA |
| | | | TA = +25°C | | 0.25 | 0.51 | |
| | | | TA = +50°C | | 0.28 | 1.10 | |
| | | | TA = +70°C | | 0.38 | 1.90 | |
| | | | TA = +85°C | | 0.60 | 3.30 | |
| | | | TA = +105°C | | 1.5 | 17.0 | |

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. The values do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

Peripheral Functions (Common to all products)

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|--------------------------------|--|---|------|------|-------|------|
| Low-speed on-chip oscillator operating current | IFIL Note 1 | | | | 0.22 | | μA |
| 12-bit interval timer operating current | ITMKA Notes 1, 3, 4 | fIL = 15 kHz fMAIN stopped (per unit) | | | 0.02 | | μA |
| 8-bit interval timer operating current Notes 1, 9 | ITMT | fIL = 15 kHz fMAIN stopped (per unit) | 8-bit counter mode × 2-channel operation | | 0.04 | | μA |
| | | | 16-bit counter mode operation | | 0.03 | | μA |
| Watchdog timer operating current | IWD _T Notes 1, 3, 5 | fIL = 15 kHz fMAIN stopped (per unit) | | | 0.22 | | μA |
| A/D converter operating current | IADC Notes 1, 6 | During maximum-speed conversion | Normal mode, AVREFP = VDD = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, AVREFP = VDD = 3.0 V | | 0.5 | 0.7 | mA |
| Internal reference voltage (1.45 V) current Notes 1, 10 | IADREF | | | | 85.0 | | μA |
| Temperature sensor operating current | ITMPS Note 1 | | | | 85.0 | | μA |
| D/A converter operating current | IDAC Note 1 | Per channel | | | | 1.5 | mA |
| PGA operating current | IPGA Notes 1, 2 | | | | 480 | 700 | μA |
| Comparator operating current | ICMP Note 8 | VDD = 5.0 V, Regulator output voltage = 2.1 V | Comparator high-speed mode Window mode | | 12.5 | | μA |
| | | | Comparator low-speed mode Window mode | | 3.0 | | |
| | | | Comparator high-speed mode Standard mode | | 6.5 | | |
| | | | Comparator low-speed mode Standard mode | | 1.9 | | |
| | | VDD = 5.0 V, Regulator output voltage = 1.8 V | Comparator high-speed mode Window mode | | 8.0 | | |
| | | | Comparator low-speed mode Window mode | | 2.2 | | |
| | | | Comparator high-speed mode Standard mode | | 4.0 | | |
| | | | Comparator low-speed mode Standard mode | | 1.3 | | |
| LVD operating current | ILVD Notes 1, 7 | | | | 0.10 | | μA |
| Self-programming operating current | IFSP Notes 1, 12 | | | | 2.0 | 12.20 | mA |
| BGO current | IBGO Notes 1, 11 | | | | 2.0 | 12.20 | mA |
| SNOOZE operating current | ISNOZ Note 1 | ADC operation fIH = 24 MHz, AVREFP = VDD = 3.0 V | Mode transition Note 13 | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed | | 1.20 | 2.04 | mA |
| | | CSI/UART operation fIH = 24 MHz | | 0.70 | 1.54 | mA | |
| | ISNOZM Note 1 | ADC operation fIM = 4 MHz, AVREFP = VDD = 3.0 V | Mode transition Note 13 | | 0.05 | 0.13 | mA |
| | | | The A/D conversion operations are performed | | 0.67 | 0.84 | mA |
| | | CSI operation, fIM = 4 MHz | | 0.06 | 0.15 | mA | |

(Notes and Remarks are listed on the next page.)

- Note 1.** Current flowing to VDD.
- Note 2.** Operable range is 2.7 to 5.5 V.
- Note 3.** When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock, and high-speed system clock are stopped.
- Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- Note 8.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.
- Note 9.** Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 8-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
- Note 10.** Current consumed by generating the internal reference voltage (1.45 V).
- Note 11.** Current flowing during programming of the data flash.
- Note 12.** Current flowing during self-programming.
- Note 13.** For transition time to the SNOOZE mode, see **24.3.3 SNOOZE mode** in the RL78/G11 User's Manual.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. Temperature condition of the TYP. value is TA = 25°C

3.4 AC Characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

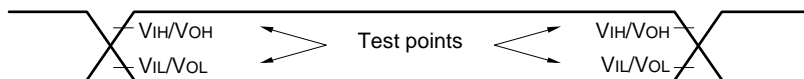
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|--|--|------------------------------|----------------------|---------|------|------|
| Instruction cycle (minimum instruction execution time) | TCY | Main system clock (fMAIN) operation | HS (high-speed main) mode | 2.7 V ≤ VDD ≤ 5.5 V | 0.04167 | 1 | μs |
| | | | | 2.4 V ≤ VDD < 2.7 V | 0.0625 | 1 | μs |
| | | Subsystem clock (fSUB) operation | fil | 2.4 V ≤ VDD ≤ 5.5 V | | 66.7 | μs |
| | | In the self- programming mode | HS (high-speed main) mode | 2.7 V ≤ VDD ≤ 5.5 V | 0.04167 | 1 | μs |
| 2.4 V ≤ VDD < 2.7 V | 0.0625 | | | 1 | μs | | |
| External system clock frequency | fEX | 2.7 V ≤ VDD ≤ 5.5 V | | 1 | | 20 | MHz |
| | | 2.4 V ≤ VDD < 2.7 V | | 1 | | 16 | MHz |
| External system clock input high-/low- level width | tEXH, tEXL | 2.7 V ≤ VDD ≤ 5.5 V | | 24 | | | ns |
| | | 2.4 V ≤ VDD < 2.7 V | | 30 | | | ns |
| TI00 to TI03 input high-/low-level width | tTIH, tTIL ^{Note 1} | | | 1/fMCK + 10 | | | ns |
| TO00 to TO03, TKBO0, and TKBO1 output frequency ^{Note 2} | fTO | TO00 to TO03, TKBO0, and TKBO1 (in the case of output from port pins other than P20) | HS (high-speed main) mode | 4.0 V ≤ EVDD ≤ 5.5 V | | 12 | MHz |
| | | | | 2.7 V ≤ EVDD < 4.0 V | | 8 | |
| | | | | 2.4 V ≤ EVDD < 2.7 V | | 4 | |
| | TKBO1 (in the case of output from P20) | HS (high-speed main) mode | 4.0 V ≤ VDD ≤ 5.5 V | | 1.5 | MHz | |
| | | | 2.7 V ≤ VDD < 4.0 V | | 1.2 | | |
| | | | 2.4 V ≤ VDD < 2.7 V | | 1 | | |
| PCLBUZ0, PCLBUZ1 output frequency | fPCL | HS (high-speed main) mode | | 4.0 V ≤ EVDD ≤ 5.5 V | | 16 | MHz |
| | | | | 2.7 V ≤ EVDD < 4.0 V | | 8 | |
| | | | | 2.4 V ≤ EVDD < 2.7 V | | 4 | |
| Interrupt input high- /low-level width | tINTH, tINTL | INTP0 to INTP2, INTP9 | | 2.4 V ≤ VDD ≤ 5.5 V | 1 | | μs |
| | | INTP3 to INTP8, INTP10, INTP11 | | 2.4 V ≤ VDD ≤ 5.5 V | 1 | | |
| Key interrupt input low-level width | tKR | KR0 to KR7 | | 2.4 V ≤ EVDD ≤ 5.5 V | 250 | | ns |
| RESET low-level width | tRSL | | | | 10 | | μs |

Note 1. Following conditions must be satisfied on low level interface of EVDD < VDD.
2.4 V ≤ EVDD ≤ 2.7 V: MIN.125 ns

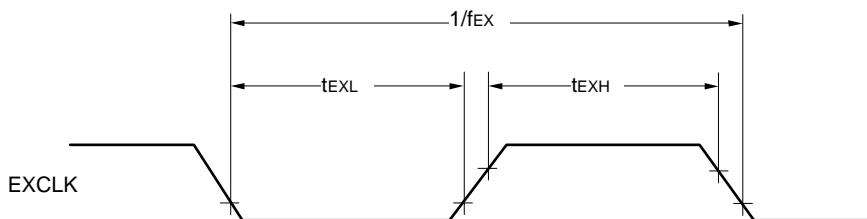
Note 2. When duty is 50%.

Remark fMCK: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

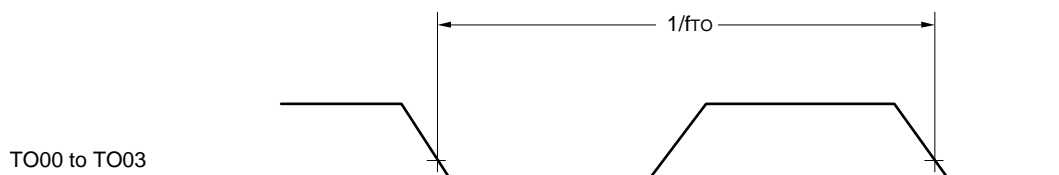
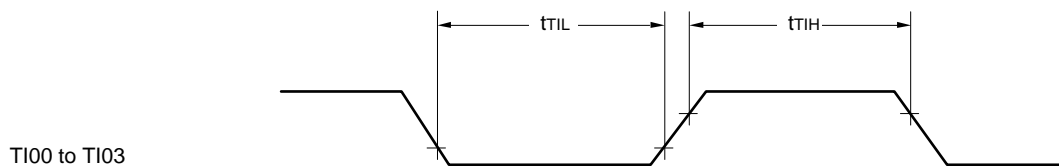
AC Timing Test Points



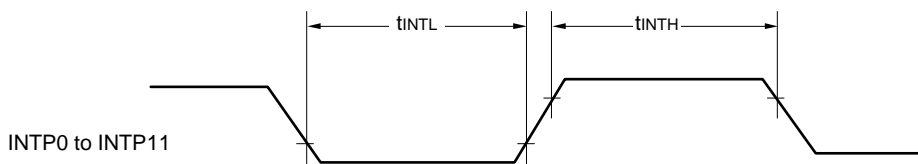
External System Clock Timing



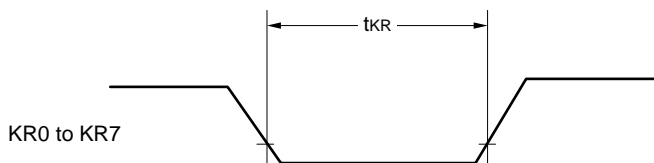
TI/TO Timing



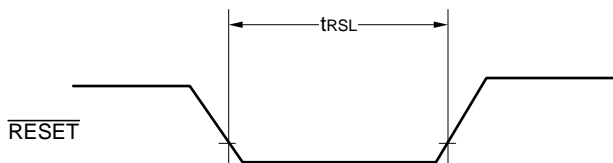
Interrupt Request Input Timing



Key Interrupt Input Timing

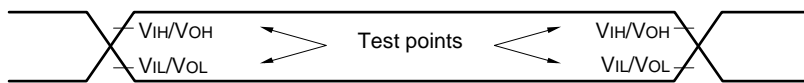


$\overline{\text{RESET}}$ Input Timing



3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) during communication at same potential (UART mode)

When P01, P30, P31 and P54 are used as TxDq pin

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------|--------|--|---------------------------|-------------------------------|------|
| | | | MIN. | MAX. | |
| Transfer rate | | Theoretical value of the maximum transfer rate fMCK = fCLK = 24 MHz | | fMCK/12 ^{Notes 1, 2} | bps |
| | | | | 2.0 | Mbps |

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode:

2.4 V ≤ EVDD ≤ 2.7 V: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

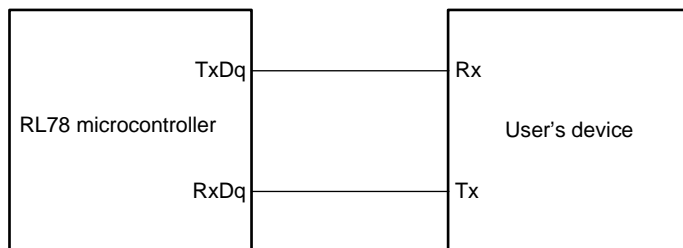
When P20 is used as TxD1 pin

(TA = -40 to +105°C, 2.4 V ≤ EVDD = VDD ≤ 5.5 V, VSS = 0 V)

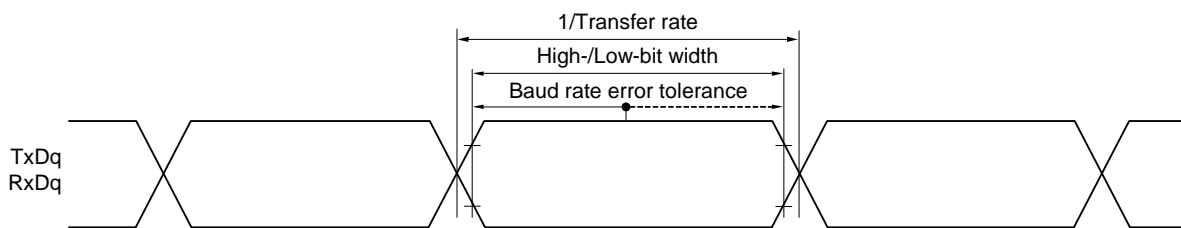
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------|--------|---------------------|--|-------------------------|------|
| | | | MIN. | MAX. | |
| Transfer rate | | 4.0 V ≤ VDD ≤ 5.5 V | | fMCK/16 ^{Note} | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK = 24 MHz | | 1.5 |
| | | 2.7 V ≤ VDD ≤ 5.5 V | | fMCK/20 ^{Note} | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK = 24 MHz | | 1.2 |
| | | 2.4 V ≤ VDD ≤ 5.5 V | | fMCK/16 ^{Note} | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK = 16 MHz | | 1.0 |

Note Transfer rate in the SNOOZE mode is 4800 bps only. When fhoco = 48 MHz, SNOOZE mode is not supported.

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3 and 5)

Remark 2. f_{MC}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

When P01, P32, P53, P54 and P56 are used as SOMn pins

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|--|------------|----------------------|---------------------------|------|------|
| | | | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 4/fCLK | 2.7 V ≤ EVDD ≤ 5.5 V | 250 | ns |
| | | | 2.4 V ≤ EVDD ≤ 5.5 V | 500 | ns |
| SCKp high-/low-level width | tkH1, tkL1 | 4.0 V ≤ EVDD ≤ 5.5 V | tkCY1/2 - 24 | ns | |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | tkCY1/2 - 36 | ns | |
| | | 2.4 V ≤ EVDD ≤ 5.5 V | tkCY1/2 - 76 | ns | |
| Slp setup time (to SCKp↑) Note 1 | tSIK1 | 4.0 V ≤ EVDD ≤ 5.5 V | 66 | ns | |
| | | 2.7 V ≤ EVDD ≤ 5.5 V | | ns | |
| | | 2.4 V ≤ EVDD ≤ 5.5 V | 133 | ns | |
| Slp hold time (from SCKp↑) Note 2 | tKSI1 | | 38 | ns | |
| Delay time from SCKp↓ to SOp output Note 3 | tKSO1 | C = 30 pF Note 4 | | 50 | ns |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin**(TA = -40 to +105°C, 2.4 V ≤ EVDD = VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|--|------------|---------------------|---------------------------|------|------|----|
| | | | MIN. | MAX. | | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 4/fCLK | 2.7 V ≤ VDD ≤ 5.5 V | 1000 | | ns |
| | | | 2.4 V ≤ VDD ≤ 5.5 V | 1200 | | ns |
| SCKp high-/low-level width | tkH1, tkL1 | 4.0 V ≤ VDD ≤ 5.5 V | tkCY1/2 - 24 | | ns | |
| | | 2.7 V ≤ VDD ≤ 5.5 V | tkCY1/2 - 36 | | ns | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | tkCY1/2 - 76 | | ns | |
| Slp setup time (to SCKp↑) Note 1 | tSIK1 | 2.7 V ≤ VDD ≤ 5.5 V | 66 | | ns | |
| | | 2.4 V ≤ VDD ≤ 5.5 V | 133 | | ns | |
| Slp hold time (from SCKp↑) Note 2 | tKS11 | | 38 | | ns | |
| Delay time from SCKp↓ to SOp output Note 3 | tkSO1 | C = 30 pF Note 4 | | 180 | ns | |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**When P01, P32, P53, P54 and P56 are used as SOMn pins****(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|------------|-----------------------------|---------------------------|--------------|------|
| | | | MIN. | MAX. | |
| SCKp cycle time ^{Note 4} | tkCY2 | 4.0 V ≤ EVDD ≤ 5.5 V | fMCK > 20 MHz | 16/fMCK | ns |
| | | | fMCK ≤ 20 MHz | 12/fMCK | ns |
| | | 2.7 V ≤ EVDD < 4.0 V | fMCK > 16 MHz | 16/fMCK | ns |
| | | | fMCK ≤ 16 MHz | 12/fMCK | ns |
| | | 2.4 V ≤ EVDD < 2.7 V | 12/fMCK and 1000 | ns | |
| SCKp high-/low-level width | tkH2, tkL2 | 4.0 V ≤ EVDD ≤ 5.5 V | tkCY2/2 - 14 | ns | |
| | | 2.7 V ≤ EVDD < 4.0 V | tkCY2/2 - 16 | ns | |
| | | 2.4 V ≤ EVDD < 2.7 V | tkCY2/2 - 36 | ns | |
| Slp setup time (to SCKp↑) ^{Note 1} | tsIK2 | 2.7 V ≤ EVDD ≤ 5.5 V | 1/fMCK + 40 | ns | |
| | | 2.4 V ≤ EVDD < 2.7 V | 1/fMCK + 60 | ns | |
| Slp hold time (from SCKp↑) ^{Note 1} | tkSI2 | | 1/fMCK + 62 | ns | |
| Delay time from SCKp↓ to SOp output ^{Note 2} | tkSO2 | C = 30 pF ^{Note 3} | 2.7 V ≤ EVDD ≤ 5.5 V | 2/fMCK + 66 | ns |
| | | | 2.4 V ≤ EVDD < 2.7 V | 2/fMCK + 113 | ns |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” and the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|--------------------------------------|--------|------------|---------------------------|--------------|------|----|
| | | | MIN. | MAX. | | |
| $\overline{\text{SSI00}}$ setup time | tSSIK | DAPmn = 0 | 2.7 V ≤ VDD ≤ 3.6 V | 240 | | ns |
| | | | 2.4 V ≤ VDD < 2.7 V | 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ VDD ≤ 3.6 V | 1/fMCK + 240 | | ns |
| | | | 2.4 V ≤ VDD < 2.7 V | 1/fMCK + 400 | | ns |
| $\overline{\text{SSI00}}$ hold time | tKSSI | DAPmn = 0 | 2.7 V ≤ VDD ≤ 3.6 V | 1/fMCK + 240 | | ns |
| | | | 2.4 V ≤ VDD < 2.7 V | 1/fMCK + 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ VDD ≤ 3.6 V | 240 | | ns |
| | | | 2.4 V ≤ VDD < 2.7 V | 400 | | ns |

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5, 12)

When P20 is used as SO10 pin**(TA = -40 to +105°C, 2.4 V ≤ EVDD = VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|------------|-----------------------------|---------------------------|------------------|------|
| | | | MIN. | MAX. | |
| SCKp cycle time ^{Note 4} | tkCY2 | 4.0 V ≤ VDD ≤ 5.5 V | fMCK > 20 MHz | 20/fMCK | ns |
| | | | fMCK ≤ 20 MHz | 18/fMCK | ns |
| | | 2.7 V ≤ VDD < 4.0 V | fMCK > 16 MHz | 20/fMCK and 1000 | ns |
| | | | fMCK ≤ 16 MHz | 18/fMCK | ns |
| | | 2.4 V ≤ VDD < 2.7 V | 18/fMCK and 1200 | ns | |
| SCKp high-/low-level width | tkH2, tkL2 | 4.0 V ≤ VDD ≤ 5.5 V | tkCY2/2 - 14 | ns | |
| | | 2.7 V ≤ VDD < 4.0 V | tkCY2/2 - 16 | ns | |
| | | 2.4 V ≤ VDD < 2.7 V | tkCY2/2 - 36 | ns | |
| Slp setup time (to SCKp↑) ^{Note 1} | tsIK2 | 2.7 V ≤ VDD ≤ 5.5 V | 1/fMCK + 40 | ns | |
| | | 2.4 V ≤ VDD < 2.7 V | 1/fMCK + 60 | ns | |
| Slp hold time (from SCKp↑) ^{Note 1} | tkSI2 | | 1/fMCK + 62 | ns | |
| Delay time from SCKp↓ to SOp output ^{Note 2} | tkSO2 | C = 30 pF ^{Note 3} | 2.7 V ≤ VDD ≤ 5.5 V | 2/fMCK + 190 | ns |
| | | | 2.4 V ≤ VDD < 2.7 V | 2/fMCK + 250 | ns |

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” and the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

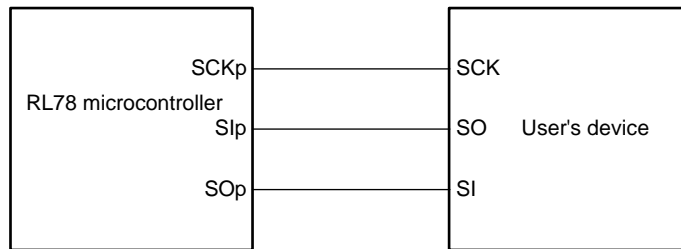
Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

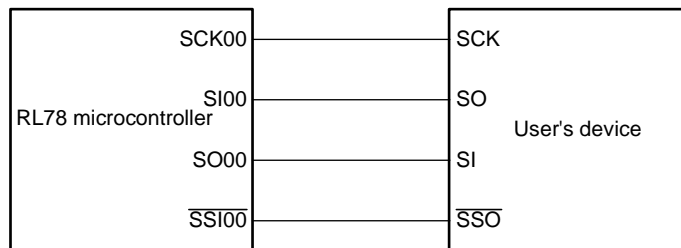
Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00 to 03))

CSI mode connection diagram (during communication at same potential)

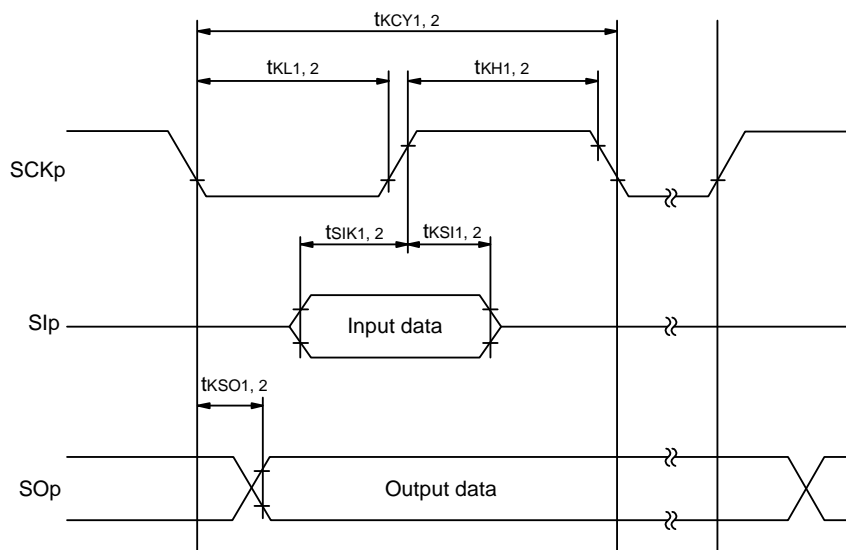


**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))**

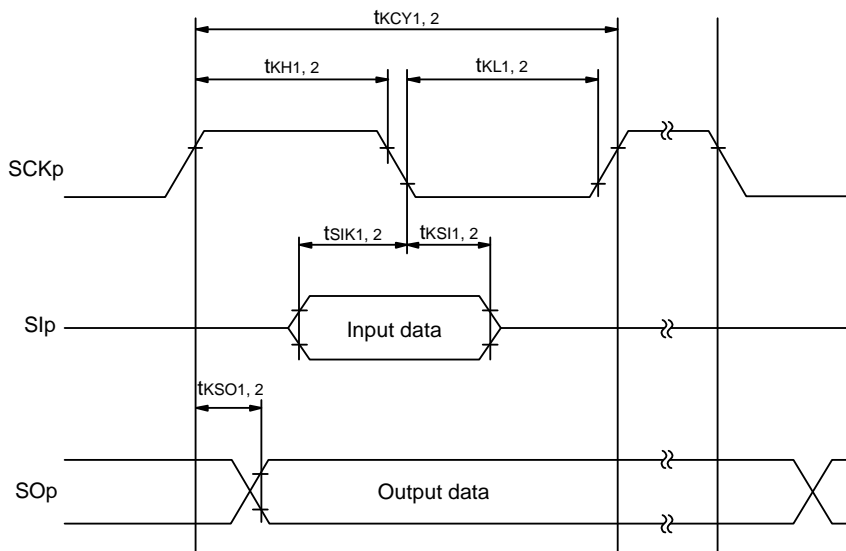


Remark p: CSI number (p = 00, 01, 10 and 11)

**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark 1. p: CSI number (p = 00, 01, 10 and 11)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(4) During communication at same potential (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)**

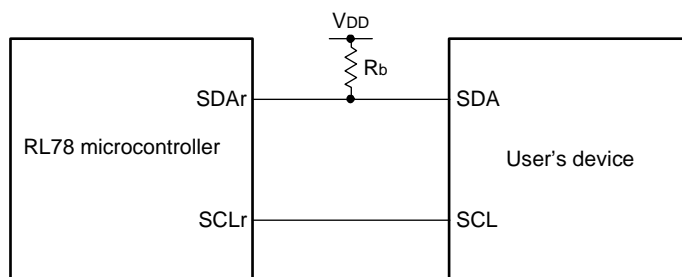
| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|-------------------------------|----------|--|---------------------------|------------|------|
| | | | MIN. | MAX. | |
| SCLr clock frequency | fscl | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.4 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | | 100 Note 1 | |
| Hold time when SCLr = "L" | tLOW | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 4600 | | |
| Hold time when SCLr = "H" | tHIGH | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 4600 | | |
| Data setup time (reception) | tsu: DAT | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 1/fMCK + 220 Note 2 | | ns |
| | | 2.4 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 1/fMCK + 580 Note 2 | | |
| Data hold time (transmission) | thd: DAT | 2.7 V ≤ EVDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ EVDD ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ | 0 | 1420 | |

Note 1. The value must be equal to or less than fMCK/4.

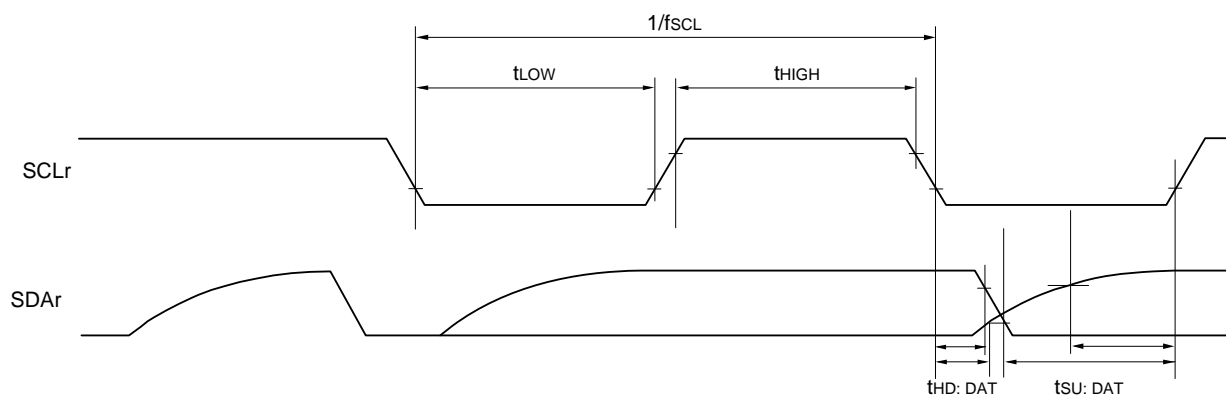
Note 2. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (EVDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- Remark 1.** R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
- Remark 2.** r: IIC number (r = 00, 01, 10 and 11), g: PIM number (g = 0, 3 and 5), h: POM number (h = 0, 3 and 5)
- Remark 3.** f_{mck}: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
 n: Channel number (n = 0 to 3), mn = 00 to 03)

(5) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (UART mode) (dedicated baud rate generator output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---------------|--------|--|--|--------------------|------|
| | | | MIN. | MAX. | |
| Transfer rate | | Reception 4.0 V ≤ EVDD ≤ 5.5 V, 2.3 V ≤ Vb ≤ 4.0 V | | fMCK/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 2.0 |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | | fMCK/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 2.0 |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V | | fMCK/12 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 1.3 |

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.**Note 2.** Use it with EVDD ≥ Vb.**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EVDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Vb[V]: Communication line voltage**Remark 2.** q: UART number (q = 0 and 1), g: PIM and POM numbers (g = 0, 2, 3, 5, 12)**Remark 3.** fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03))

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|---------------|--------|--------------|---|------|------------------------|------|
| | | | MIN. | MAX. | | |
| Transfer rate | | Transmission | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V | | 2.6 ^{Note 2} | Mbps |
| | | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V | | 1.2 ^{Note 4} | Mbps |
| | | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V | | Notes 5, 6 | bps |
| | | | Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V | | 0.43 ^{Note 7} | Mbps |

Note 1. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ and $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $2.7\text{ V} \leq EV_{DD} \leq 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $2.4\text{ V} \leq E_{VDD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

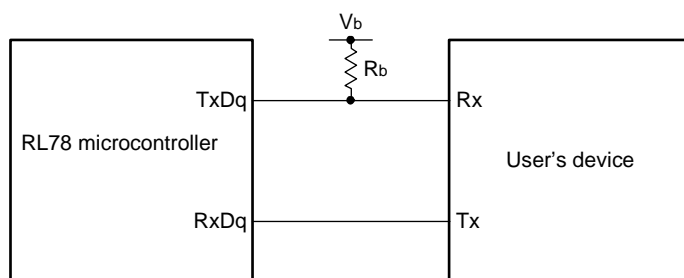
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

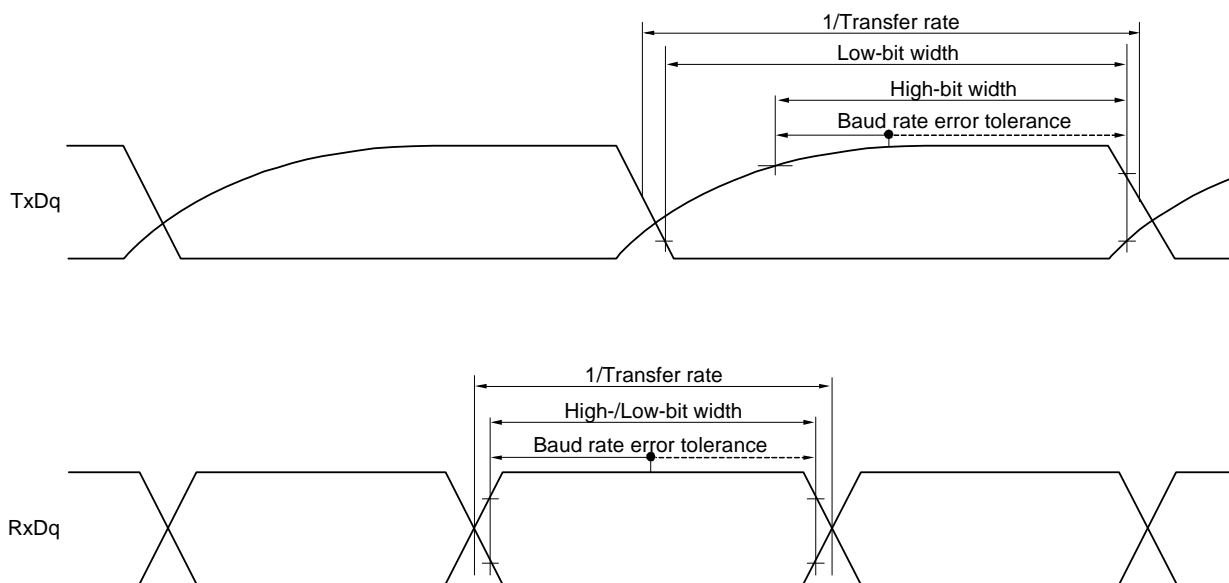
Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EVDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3, 5 and 12)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(6) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)****(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|-----------------------|--------|--|---------------------------|------|------|
| | | | MIN. | MAX. | |
| SCKp cycle time | tkCY1 | tkCY1 ≥ 4/fCLK 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 600 | | ns |
| | | | 1000 | | ns |
| | | | 2300 | | ns |
| SCKp high-level width | tkH1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | tkCY1/2 - 150 | | ns |
| | | | tkCY1/2 - 340 | | ns |
| | | | tkCY1/2 - 916 | | ns |
| SCKp low-level width | tkL1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | tkCY1/2 - 24 | | ns |
| | | | tkCY1/2 - 36 | | ns |
| | | | tkCY1/2 - 100 | | ns |

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (EVDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|--|--------|---|---------------------------|------|------|
| | | | MIN. | MAX. | |
| Slp setup time (to SCKp↑) Note 1 | tSIK1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | 958 | | ns |
| Slp hold time (from SCKp↑) Note 1 | tSIH1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | tKSO1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | 966 | ns |
| Slp setup time (to SCKp↓) Note 2 | tSIK1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | 220 | | ns |
| Slp hold time (from SCKp↓) Note 2 | tSIH1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | tKSO1 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ | | | |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ | | | ns |

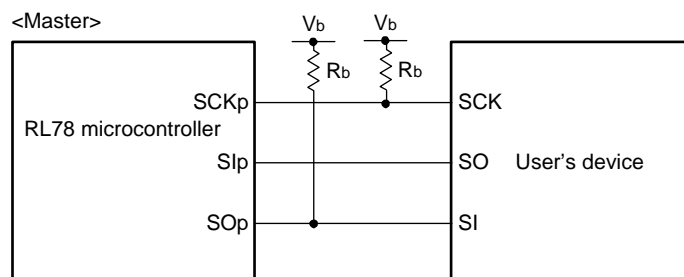
Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. Use it with EVDD ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EVDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

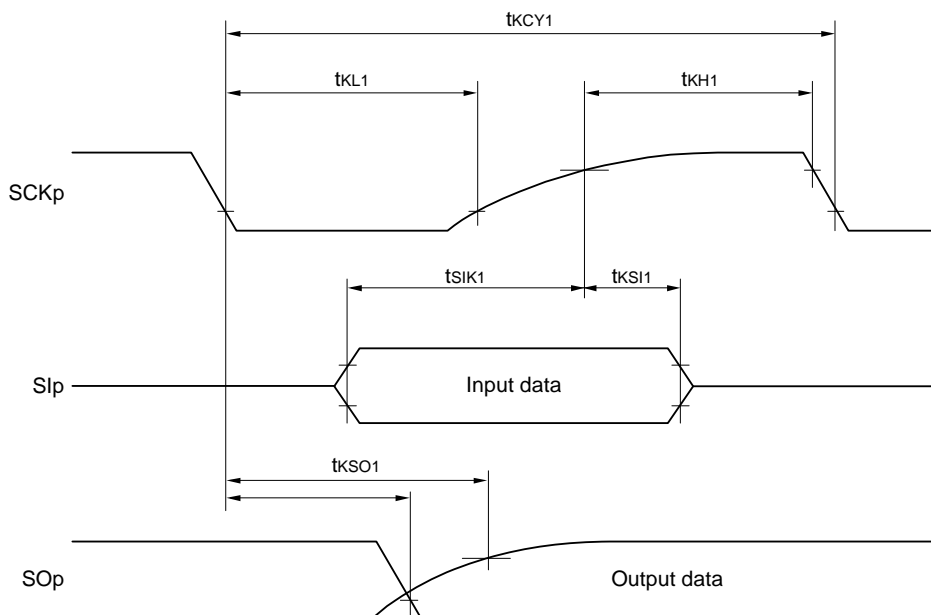
CSI mode connection diagram (during communication at different potential)

Remark 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

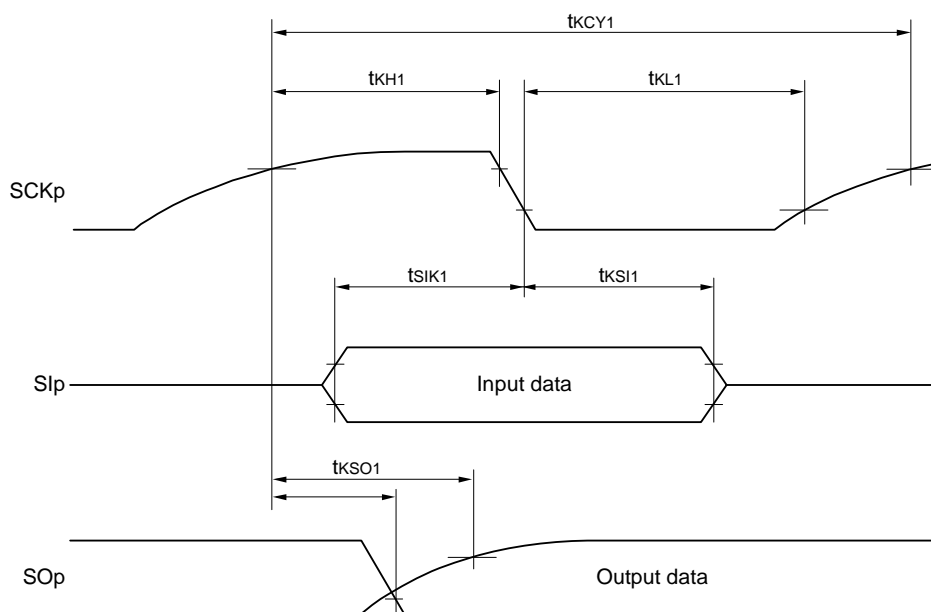
Remark 2. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{mck} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

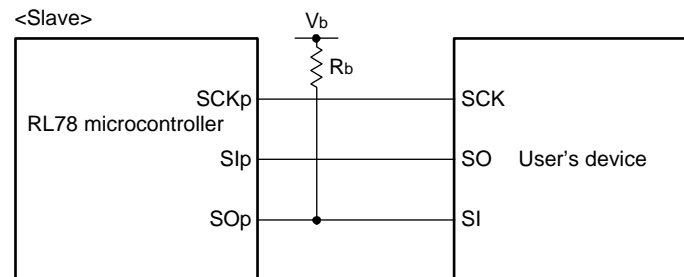
(7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit | |
|---|------------|---|---------------------------|---------------|------|----|
| | | | MIN. | MAX. | | |
| SCKp cycle time ^{Note 1} | tkCY2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | 20 MHz < fMCK ≤ 24 MHz | 24/fMCK | | ns |
| | | | 8 MHz < fMCK ≤ 20 MHz | 20/fMCK | | ns |
| | | | 4 MHz < fMCK ≤ 8 MHz | 16/fMCK | | ns |
| | | | fMCK ≤ 4 MHz | 12/fMCK | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | 20 MHz < fMCK ≤ 24 MHz | 32/fMCK | | ns |
| | | | 16 MHz < fMCK ≤ 20 MHz | 28/fMCK | | ns |
| | | | 8 MHz < fMCK ≤ 16 MHz | 24/fMCK | | ns |
| | | | 4 MHz < fMCK ≤ 8 MHz | 16/fMCK | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note 2} | 20 MHz < fMCK ≤ 24 MHz | 72/fMCK | | ns |
| | | | 16 MHz < fMCK ≤ 20 MHz | 64/fMCK | | ns |
| | | | 8 MHz < fMCK ≤ 16 MHz | 52/fMCK | | ns |
| | | | 4 MHz < fMCK ≤ 8 MHz | 32/fMCK | | ns |
| | | fMCK ≤ 4 MHz | 20/fMCK | | ns | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| SCKp high-/low-level width | tkH2, tkL2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V | tkCY2/2 - 24 | | ns | |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V | tkCY2/2 - 36 | | ns | |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note 2} | tkCY2/2 - 100 | | ns | |
| Slp setup time (to SCKp↑) ^{Note 3} | tsIK2 | 2.7 V ≤ EVDD ≤ 5.5 V, 2.3 V ≤ Vb ≤ 4.0 V | 1/fMCK + 40 | | ns | |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note 2} | 1/fMCK + 60 | | ns | |
| Slp hold time (from SCKp↑) ^{Note 4} | tkSI2 | | 1/fMCK + 62 | | ns | |
| Delay time from SCKp↓ to SOP output ^{Note 5} | tkSO2 | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V Cb = 30 pF, Rb = 1.4 kΩ | | 2/fMCK + 240 | ns | |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V Cb = 30 pF, Rb = 2.7 kΩ | | 2/fMCK + 428 | ns | |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note 2} Cb = 30 pF, Rb = 5.5 kΩ | | 2/fMCK + 1146 | ns | |

(Notes, Caution and Remarks are listed on the next page.)

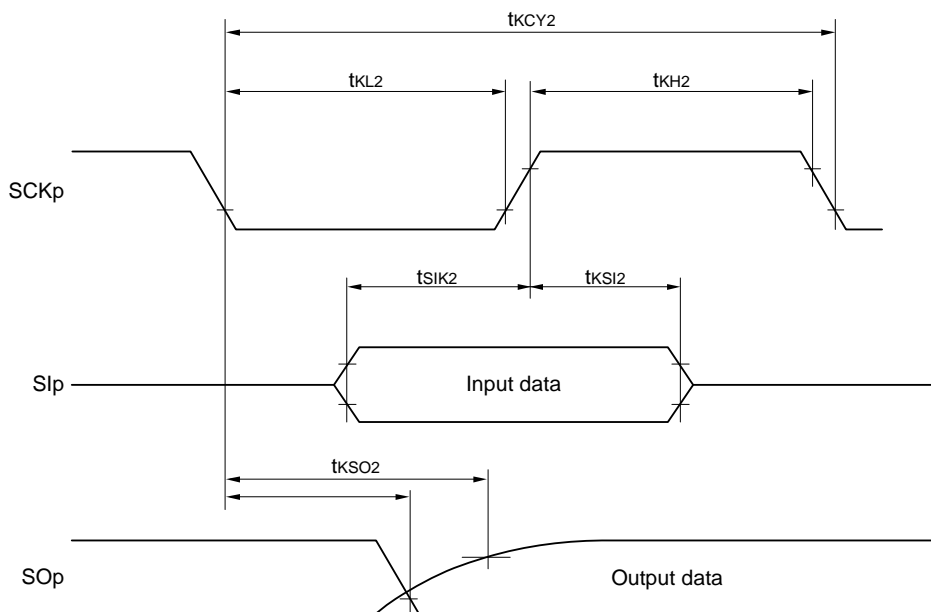
- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with $EV_{DD} \geq V_b$.
- Note 3.** When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to $SCKp\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
- Note 4.** When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from $SCKp\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
- Note 5.** When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from $SCKp\uparrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
- Caution** Select the TTL input buffer for the Slp pin and $SCKp$ pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

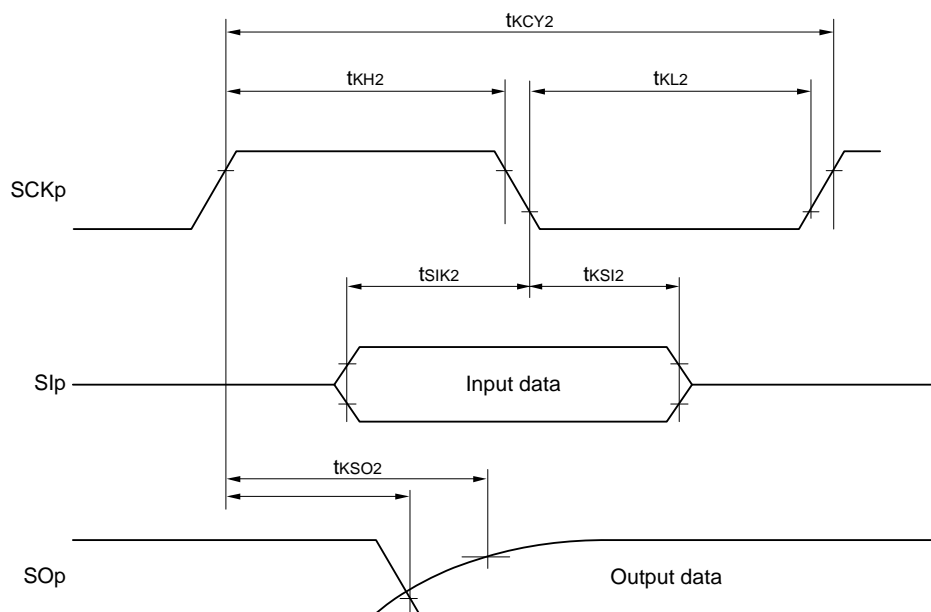


- Remark 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)
- Remark 3.** f_{mck} : Serial array unit operation clock frequency
(Operation clock to be set by the $CKSmn$ bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

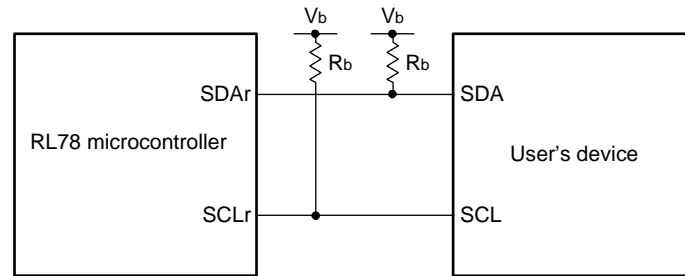
(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|-------------------------------|---------------------|--|---------------------------------|------------|------|
| | | | MIN. | MAX. | |
| SCLr clock frequency | f _{SCL} | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | | 100 Note 1 | kHz |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = "L" | t _{LOW} | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | 1200 | | ns |
| | | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | 4600 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = "H" | t _{HIGH} | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | 620 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | 500 | | ns |
| | | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | 2700 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ | 1830 | | ns |
| Data setup time (reception) | t _{SU-DAT} | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | 1/f _{MCK} + 340 Note 3 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | 1/f _{MCK} + 340 Note 3 | | ns |
| | | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | 1/f _{MCK} + 760 Note 3 | | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | 1/f _{MCK} + 760 Note 3 | | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ | 1/f _{MCK} + 570 Note 3 | | ns |
| Data hold time (transmission) | t _{HD-DAT} | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ | 0 | 770 | ns |
| | | 4.0 V ≤ EVDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ EVDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ EVDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ | 0 | 1215 | ns |

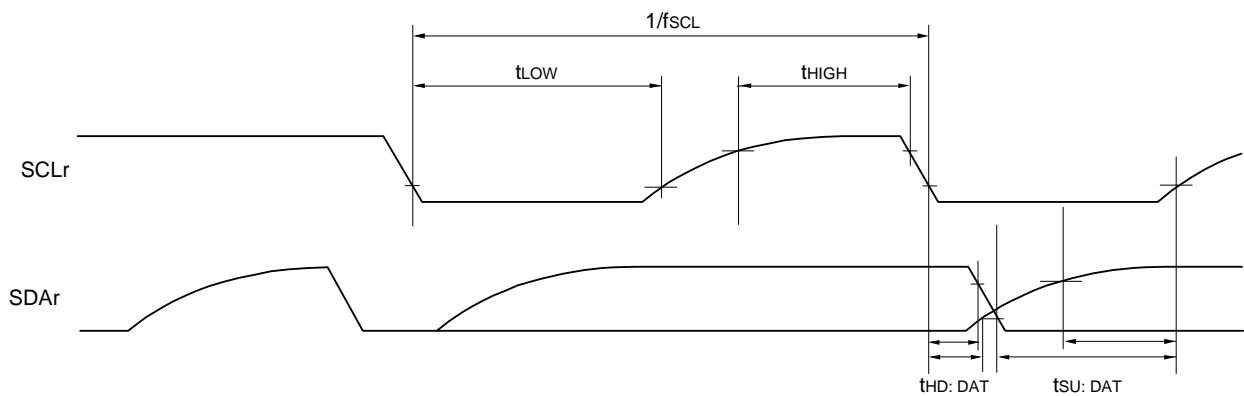
- Note 1.** The value must be equal to or less than $f_{MCK}/4$.
- Note 2.** Use it with $EV_{DD} \geq V_b$.
- Note 3.** Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.

Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



- Remark 1.** $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | | | Unit |
|--------------------------------------|----------|-----------------------------|---------------------------|------|-----------|------|------|
| | | | Standard mode | | Fast mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | fSCL | Fast mode: fCLK ≥ 3.5 MHz | — | — | 0 | 400 | kHz |
| | | Standard mode: fCLK ≥ 1 MHz | 0 | 100 | — | — | |
| Setup time of restart condition | tSU: STA | | 4.7 | | 0.6 | | μs |
| Hold time Note 1 | tHD: STA | | 4.0 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | tLOW | | 4.7 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | tHIGH | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | tSU: DAT | | 250 | | 100 | | ns |
| Data hold time (transmission) Note 2 | tHD: DAT | | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time of stop condition | tSU: STO | | 4.0 | | 0.6 | | μs |
| Bus-free time | tBUF | | 4.7 | | 1.3 | | μs |

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

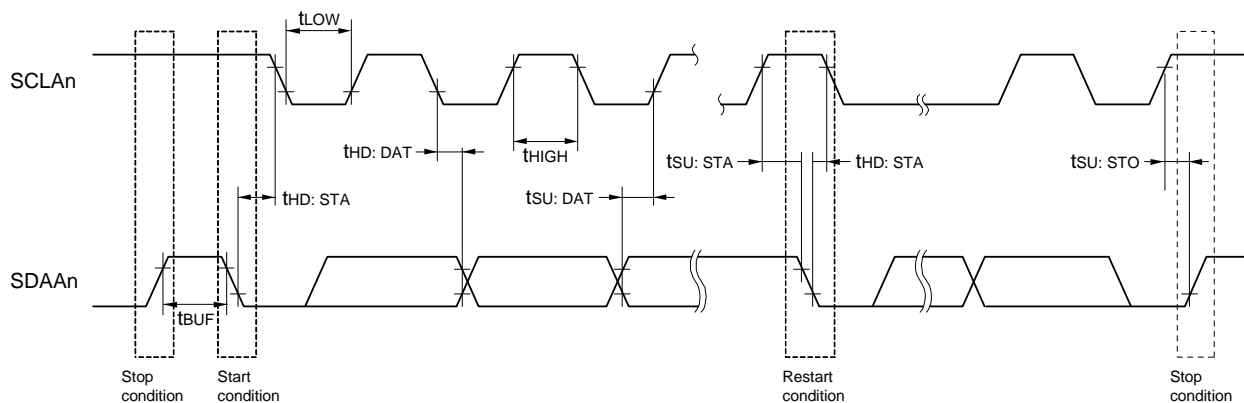
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM} | Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS} | Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM} |
|---|-------------------|--|--|--|
| ANI0 to ANI3 | | Refer to 3.6.1 (1). | Refer to 3.6.1 (3). | Refer to 3.6.1 (4). |
| ANI16 to ANI22 | | Refer to 3.6.1 (2). | | |
| Internal reference voltage Temperature sensor output voltage | | Refer to 3.6.1 (1). | | |

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-------------------|---|------------------------------------|--------|----------------------------|------|
| Resolution | RES | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution AV _{REFP} = V _{DD} Note 3 | 2.4 V ≤ AV _{REFP} ≤ 5.5 V | 1.2 | ±3.5 | LSB |
| Conversion time | t _{CONV} | 10-bit resolution Target pin: ANI2 and ANI3 | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.125 | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.1875 | 39 | μs |
| | | | 2.4 V ≤ V _{DD} ≤ 5.5 V | 17 | 39 | μs |
| | | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.375 | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.5625 | 39 | μs |
| | | | 2.4 V ≤ V _{DD} ≤ 5.5 V | 17 | 39 | μs |
| Zero-scale error Notes 1, 2 | EzS | 10-bit resolution AV _{REFP} = V _{DD} Note 3 | 2.4 V ≤ AV _{REFP} ≤ 5.5 V | | ±0.25 | %FSR |
| Full-scale error Notes 1, 2 | EFS | 10-bit resolution AV _{REFP} = V _{DD} Note 3 | 2.4 V ≤ AV _{REFP} ≤ 5.5 V | | ±0.25 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution AV _{REFP} = V _{DD} Note 3 | 2.4 V ≤ AV _{REFP} ≤ 5.5 V | | ±2.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution AV _{REFP} = V _{DD} Note 3 | 2.4 V ≤ AV _{REFP} ≤ 5.5 V | | ±1.5 | LSB |
| Analog input voltage | V _{AIN} | ANI2 and ANI3 | 0 | | AV _{REFP} | V |
| | | Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V) | | | V _{BGR} Note 4 | V |
| | | Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V) | | | V _{TMPS25} Note 4 | V |

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
 Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
 Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI22

(TA = -40 to +105°C, $2.4\text{ V} \leq EV_{DD} \leq V_{DD} \leq 5.5\text{ V}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$,

Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|--------|---|---|--------|------|---------------------------------|---------------|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | 1.2 | ± 5.0 | LSB |
| Conversion time | tCONV | 10-bit resolution Target ANI pin: ANI16 to ANI22 | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 2.125 | | 39 | μs |
| | | | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 3.1875 | | 39 | μs |
| | | | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | Ezs | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.35 | %FSR |
| Full-scale error Notes 1, 2 | Efs | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 0.35 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution $EV_{DD} \leq AV_{REFP} = V_{DD}$ Notes 3, 4 | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ | | | ± 2.0 | LSB |
| Analog input voltage | VAIN | ANI16 to ANI22 | | 0 | | AV_{REFP} and EV_{DD} | V |

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD} \leq AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,

Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---|---------------------------------|----------------------------|------|------------------|------|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 2.4 V ≤ V _{DD} ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | t _{CONV} | 10-bit resolution Target pin: ANI0 to ANI3, ANI16 to ANI22 | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ V _{DD} ≤ 5.5 V | 17 | | 39 | μs |
| | | 10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage | 3.6 V ≤ V _{DD} ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ V _{DD} ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ V _{DD} ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | E _{ZS} | 10-bit resolution | 2.4 V ≤ V _{DD} ≤ 5.5 V | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | E _{FS} | 10-bit resolution | 2.4 V ≤ V _{DD} ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 2.4 V ≤ V _{DD} ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 2.4 V ≤ V _{DD} ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | V _{AIN} | ANI0 to ANI3 | | 0 | | V _{DD} | V |
| | | ANI16 to ANI22 | | 0 | | EV _{DD} | V |
| | | Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V) | | V _{BGR} Note 3 | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V) | | V _{TMPS25} Note 3 | | | V |

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0 to ANI3, ANI16 to ANI22

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, 2.4 V ≤ EVDD ≤ VDD = 0 V,

Reference voltage (+) = VBGR Note 3, Reference voltage (-) = AVREFM = 0 V Note 4)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|--------|------------------|------|------|-------------|-------|
| Resolution | RES | | 8 | | | bit |
| Conversion time | tCONV | | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | Ezs | | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | | | ±1.0 | LSB |
| Analog input voltage | VAIN | | 0 | | VBGR Note 3 | V |

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = Vss, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|---------|--|------|------|------|-------|
| Temperature sensor output voltage | VTMPS25 | Setting ADS register = 80H, TA = +25°C | | 1.05 | | V |
| Internal reference voltage | VBGR | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | FVTMPS | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | tAMP | 2.4 V ≤ VDD ≤ 3.6 V | 5 | | | μs |

3.6.3 D/A converter (channel 1)

(TA = -40 to +105°C, 2.4 V ≤ EVSS ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------|---------------------|------|------|------|------|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 2.4 V ≤ VDD ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 2.4 V ≤ VDD ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | tSET | Cload = 20 pF | 2.7 V ≤ VDD ≤ 5.5 V | | | 3 | μs |
| | | | 2.4 V ≤ VDD < 2.7 V | | | 6 | μs |

3.6.4 Comparator

(Comparator 0: TA = -40 to +105°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

(Comparator 1: TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------|---|---|------|------------------|------|
| Input voltage range | VIREF0 | IVREF0 pin | 0 | | VDD - 1.4 Note 1 | V |
| | VIREF1 | IVREF1 pin | 1.4 Note 1 | | VDD | V |
| | VICMP | IVCMP0 pin | -0.3 | | VDD + 0.3 | V |
| | | IVCMP1 pin | -0.3 | | EVDD + 0.3 | V |
| Output delay | td | VDD = 3.0 V Input slew rate > 50 mV/μs | Comparator high-speed mode, standard mode | | 1.2 | μs |
| | | | Comparator high-speed mode, window mode | | 2.0 | μs |
| | | | Comparator low-speed mode, standard mode | | 3 | μs |
| | | | Comparator low-speed mode, window mode | | 4 | μs |
| Operation stabilization wait time | tcMP | | 100 | | | μs |
| Reference voltage declination in channel 0 of internal DAC Note 2 | ΔVIDAC | | | | ±2.5 | LSB |

Note 1. In window mode, make sure that VREF1 - VREF0 ≥ 0.2 V.

Note 2. Only in CMP0

3.6.5 PGA

(TA = -40 to +105°C, 2.7 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---------------------|--|---|------------------------|------|-----------------------------|------|
| Input offset voltage | V _{IOPGA} | | | | | ±10 | mV |
| Input voltage range | V _{IPGA} | | | 0 | | 0.9 × V _{DD} /Gain | V |
| Output voltage range | V _{IOHPGA} | | | 0.93 × V _{DD} | | | V |
| | V _{IOHPGA} | | | | | 0.07 × V _{DD} | V |
| Gain error | | x4, x8 | | | | ±1 | % |
| | | x16 | | | | ±1.5 | % |
| | | x32 | | | | ±2 | % |
| Slew rate | SR _{RPGA} | Rising When V _{IN} = 0.1V _{DD} /gain to 0.9V _{DD} /gain. 10 to 90% of output voltage amplitude | 4.0 V ≤ V _{DD} ≤ 5.5 V (Other than x32) | 3.5 | | | V/μs |
| | | | 4.0 V ≤ V _{DD} ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ V _{DD} ≤ 4.0V | 0.5 | | | |
| | SR _{FPGA} | Falling When V _{IN} = 0.1V _{DD} /gain to 0.9V _{DD} /gain. 90 to 10% of output voltage amplitude | 4.0 V ≤ V _{DD} ≤ 5.5 V (Other than x32) | 3.5 | | | |
| | | | 4.0 V ≤ V _{DD} ≤ 5.5 V (x32) | 3.0 | | | |
| | | | 2.7 V ≤ V _{DD} ≤ 4.0V | 0.5 | | | |
| Reference voltage stabilization wait time ^{Note} | t _{PGA} | x4, x8 | | | | 5 | μs |
| | | x16, x32 | | | | 10 | μs |

Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

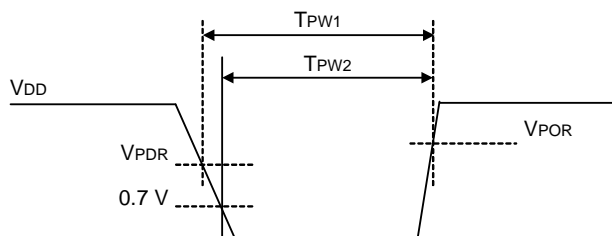
3.6.6 POR circuit characteristics

(TA = -40 to +105°C, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|------------------|--|------|------|------|------|
| Detection voltage | V _{POR} | The power supply voltage is rising. | 1.45 | 1.51 | 1.57 | V |
| | V _{PDR} | The power supply voltage is falling. <i>Note 1</i> | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width <i>Note 2</i> | T _{PW1} | Other than STOP/SUB HALT/SUB RUN | 300 | | | μs |
| | T _{PW2} | STOP/SUB HALT/SUB RUN | 300 | | | μs |

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|-------------------|----------------------|----------------------|--------------------------------------|------|------|------|------|----|
| Detection voltage | Supply voltage level | VLVD0 | The power supply voltage is rising. | 3.90 | 4.06 | 4.22 | V | |
| | | | The power supply voltage is falling. | 3.83 | 3.98 | 4.13 | V | |
| | | VLVD1 | The power supply voltage is rising. | 3.60 | 3.75 | 3.90 | V | |
| | | | The power supply voltage is falling. | 3.53 | 3.67 | 3.81 | V | |
| | | VLVD2 | The power supply voltage is rising. | 3.01 | 3.13 | 3.25 | V | |
| | | | The power supply voltage is falling. | 2.94 | 3.06 | 3.18 | V | |
| | | VLVD3 | The power supply voltage is rising. | 2.90 | 3.02 | 3.14 | V | |
| | | | The power supply voltage is falling. | 2.85 | 2.96 | 3.07 | V | |
| | | VLVD4 | The power supply voltage is rising. | 2.81 | 2.92 | 3.03 | V | |
| | | | The power supply voltage is falling. | 2.75 | 2.86 | 2.97 | V | |
| | | VLVD5 | The power supply voltage is rising. | 2.71 | 2.81 | 2.92 | V | |
| | | | The power supply voltage is falling. | 2.64 | 2.75 | 2.86 | V | |
| | | VLVD6 | The power supply voltage is rising. | 2.61 | 2.71 | 2.81 | V | |
| | | | The power supply voltage is falling. | 2.55 | 2.65 | 2.75 | V | |
| | | VLVD7 | The power supply voltage is rising. | 2.51 | 2.61 | 2.71 | V | |
| | | | The power supply voltage is falling. | 2.45 | 2.55 | 2.65 | V | |
| | | Minimum pulse width | tlw | | 300 | | | μs |
| | | Detection delay time | | | | | 300 | μs |

(2) LVD Detection Voltage of Interrupt & Reset Mode

(TA = -40 to +105°C, VPDR ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--------------------------|--------|--|------------------------------|------|------|------|---|
| Interrupt and reset mode | VLVDD0 | VPOC0, VPOC1, VPOC2 = 0, 1, 1, falling reset voltage | 2.64 | 2.75 | 2.86 | V | |
| | VLVDD1 | LVIS0, LVIS1 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | VLVDD2 | LVIS0, LVIS1 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | VLVDD3 | LVIS0, LVIS1 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

3.6.8 Power supply voltage rising slope characteristics

(TA = -40 to +105°C, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-----------------------------------|--------|------------|------|------|------|------|
| Power supply voltage rising slope | SVDD | | | | 54 | V/ms |

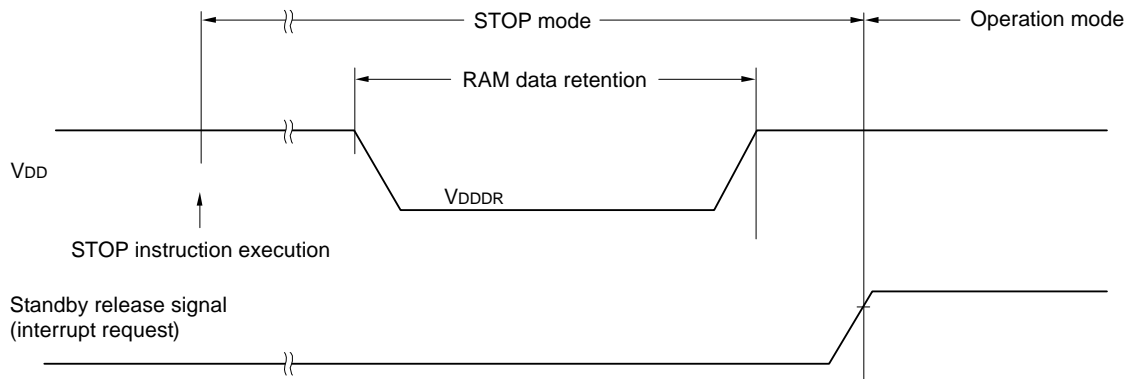
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------|--------|------------|-----------|------|------|------|
| Data retention supply voltage | VDDDR | | 1.44 Note | | 5.5 | V |

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|--------|-----------------------|-----------|---------|-----------|------|-------|
| System clock frequency | fCLK | 2.4 V ≤ VDD ≤ 5.5 V | | 1 | | 24 | MHz |
| Number of code flash rewrites Notes 1, 2, 3 | Cerwr | Retained for 20 years | TA = 85°C | 1,000 | | | Times |
| Number of data flash rewrites Notes 1, 2, 3 | | Retained for 1 year | TA = 25°C | | 1,000,000 | | |
| | | Retained for 5 years | TA = 85°C | 100,000 | | | |
| | | Retained for 20 years | TA = 85°C | 10,000 | | | |

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|---------------------------|---------|------|-----------|------|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

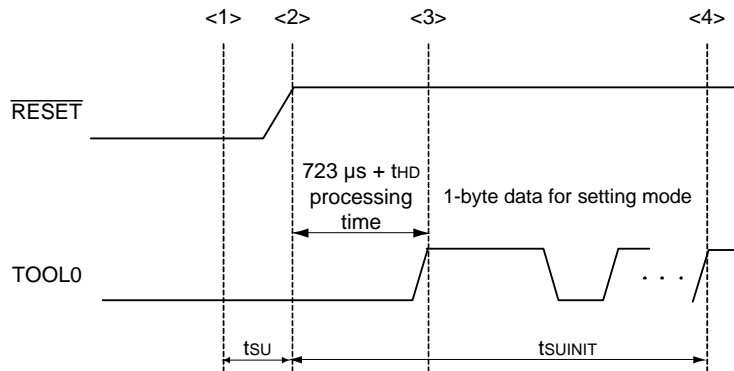
3.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +105°C, 2.4 V ≤ EVDD ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---------|--|------|------|------|------|
| How long from when an external reset ends until the initial communication settings are specified ^{Note 1} | tsuINIT | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends ^{Note 1} | tsu | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) ^{Notes 1, 2} | tHD | POR and LVD reset must end before the external reset ends. | 1 | | | ms |

Note 1. Deassertion of the POR and LVD reset signals must precede deassertion of the pin reset signal.

Note 2. This excludes the flash firmware processing time (723 μs).



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

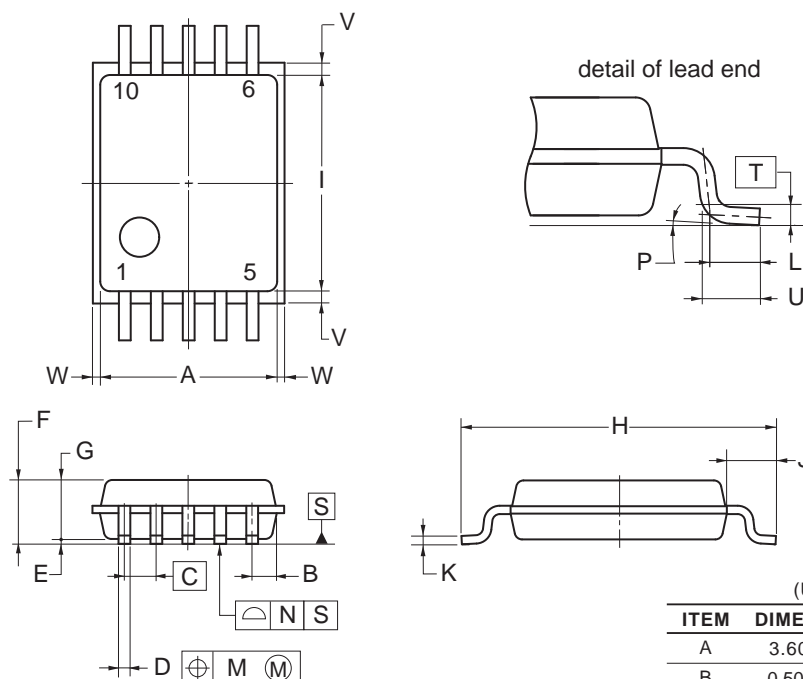
tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 10-pin package

| | | | |
|------------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LSSOP10-4.4x3.6-0.65 | PLSP0010JA-A | P10MA-65-CAC-2 | 0.05 |



(UNIT:mm)

| ITEM | DIMENSIONS |
|------|--|
| A | 3.60±0.10 |
| B | 0.50 |
| C | 0.65 (T.P.) |
| D | 0.24±0.08 |
| E | 0.10±0.05 |
| F | 1.45 MAX. |
| G | 1.20±0.10 |
| H | 6.40±0.20 |
| I | 4.40±0.10 |
| J | 1.00±0.20 |
| K | 0.17 ^{+0.08} _{-0.07} |
| L | 0.50 |
| M | 0.13 |
| N | 0.10 |
| P | 3° ^{+5°} _{-3°} |
| T | 0.25 (T.P.) |
| U | 0.60±0.15 |
| V | 0.25 MAX. |
| W | 0.15 MAX. |

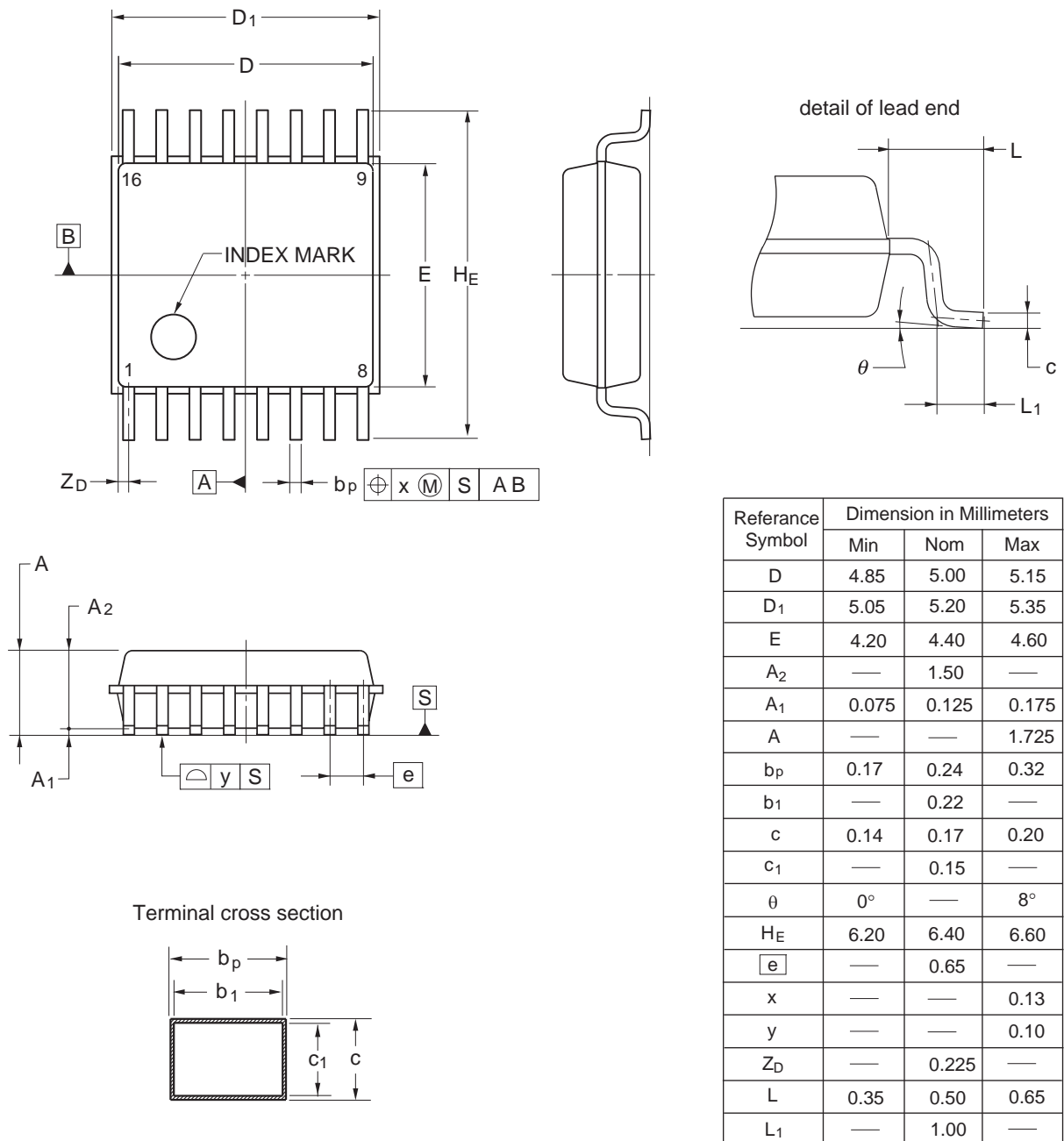
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

©2012 Renesas Electronics Corporation. All rights reserved.

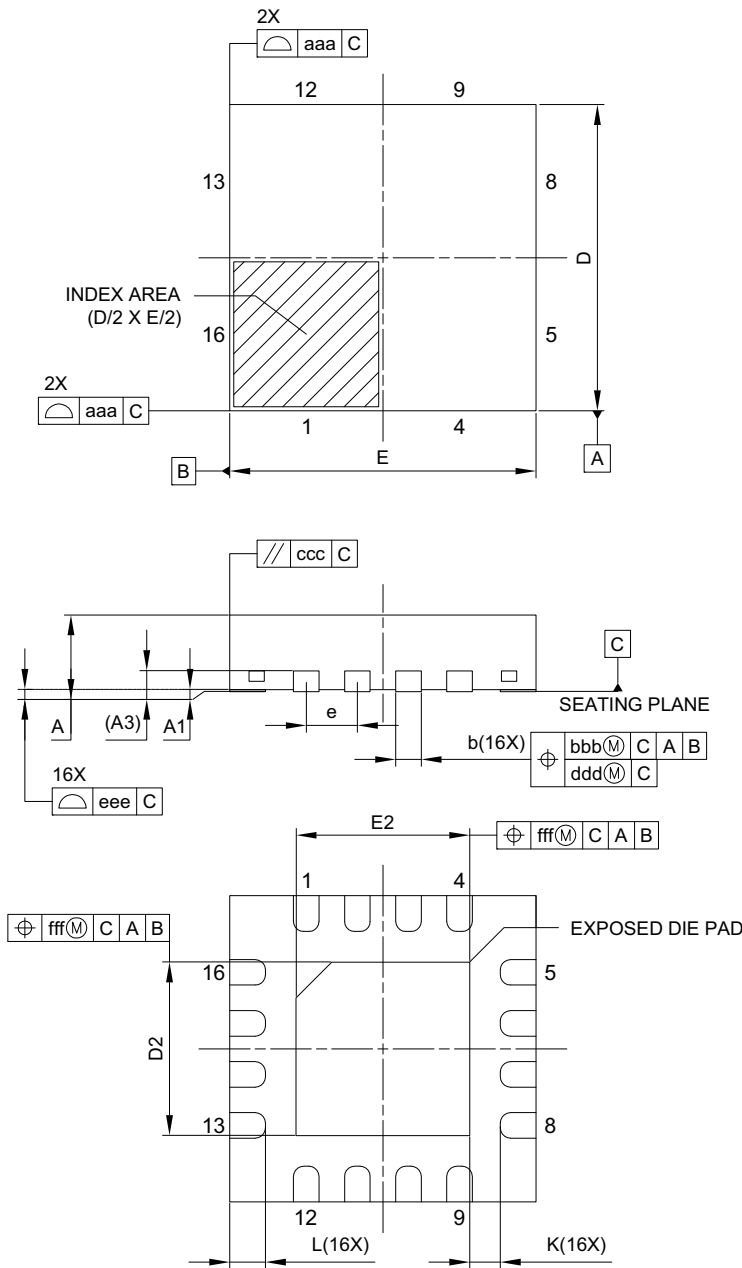
4.2 16-pin package

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---------------------|--------------|---------------|---------------|
| P-SSOP16-4.4x5-0.65 | PRSP0016JC-B | P16MA-65-FAB | 0.08 |



<R>

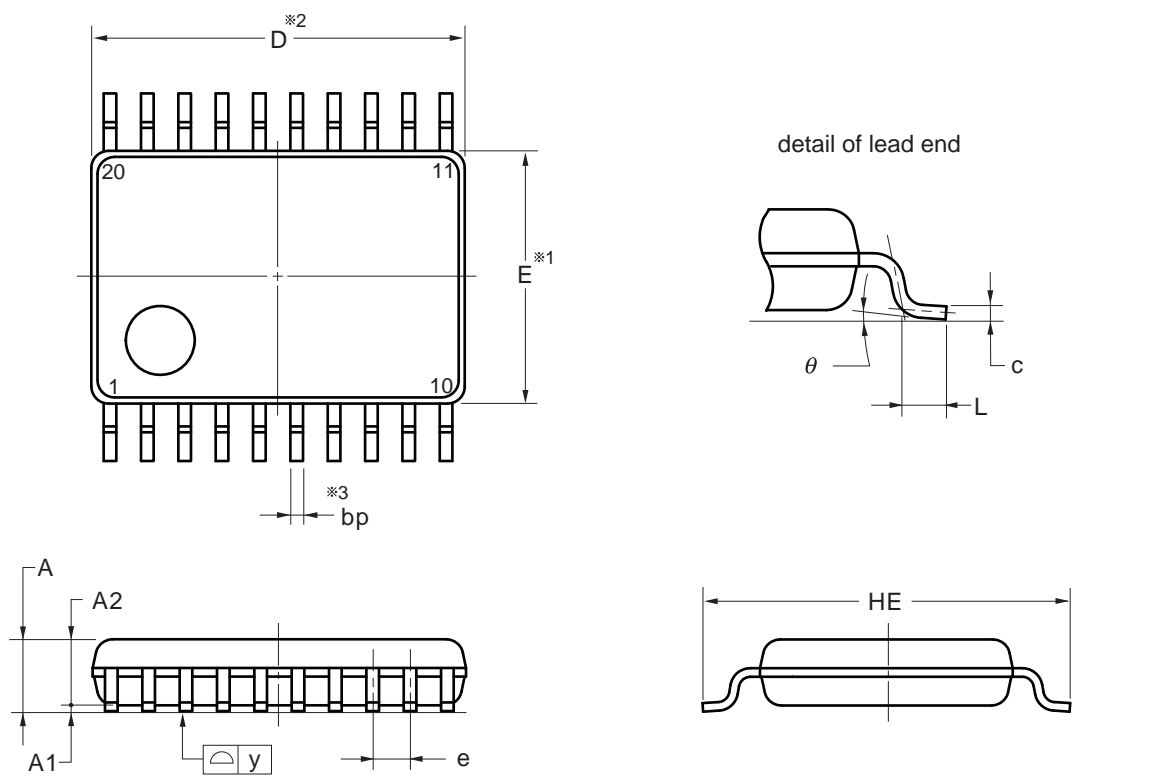
| | | |
|---------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-HWQFN016-3x3-0.50 | PWQN0016KD-A | 0.02 |



| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 3.00 BSC | | |
| E | 3.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.30 | 0.35 | 0.40 |
| K | 0.20 | — | — |
| D2 | 1.65 | 1.70 | 1.75 |
| E2 | 1.65 | 1.70 | 1.75 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

4.3 20-pin package

| | | | |
|------------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1 |



NOTE

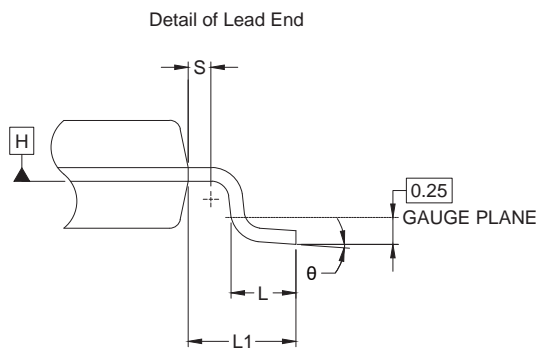
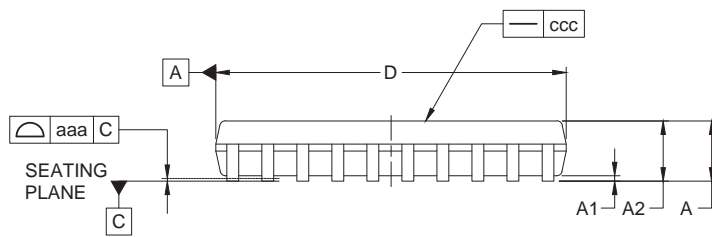
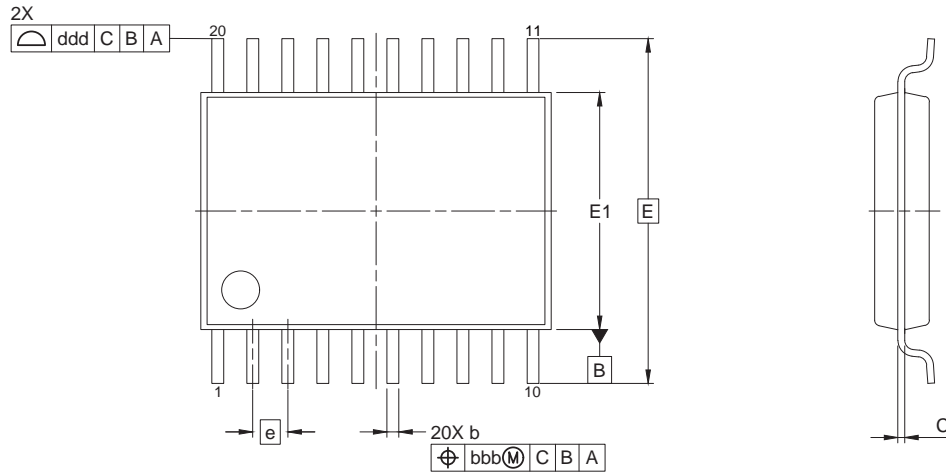
- 1. Dimensions "※1" and "※2" do not include mold flash.
- 2. Dimension "※3" does not include trim offset.

(UNIT:mm)

| ITEM | DIMENSIONS |
|------|--|
| D | 6.50±0.10 |
| E | 4.40±0.10 |
| HE | 6.40±0.20 |
| A | 1.45 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.15 |
| e | 0.65±0.12 |
| bp | 0.22 ^{+0.10} _{-0.05} |
| c | 0.15 ^{+0.05} _{-0.02} |
| L | 0.50±0.20 |
| y | 0.10 |
| θ | 0° to 10° |

©2012 Renesas Electronics Corporation. All rights reserved.

| | | |
|--------------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-TSSOP20-4.40x6.50-0.65 | PTSP0020JI-A | 0.08 |

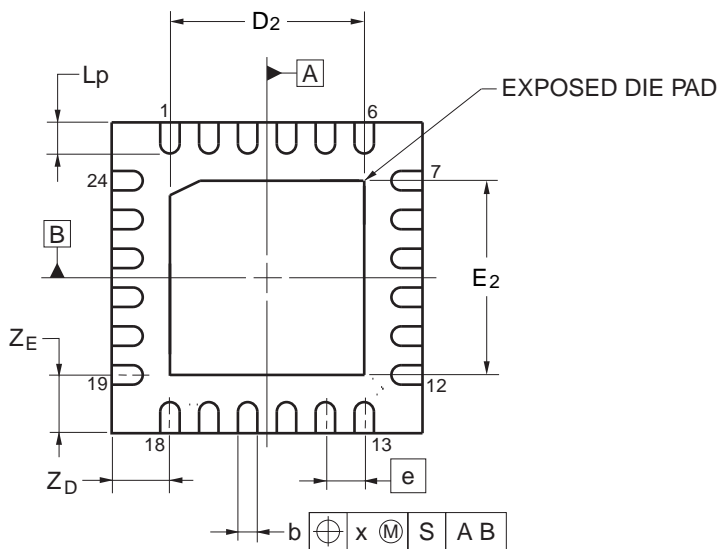
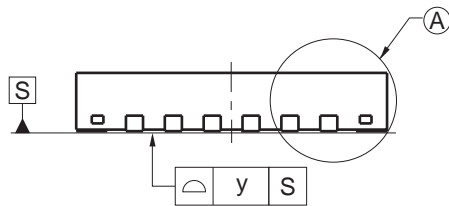
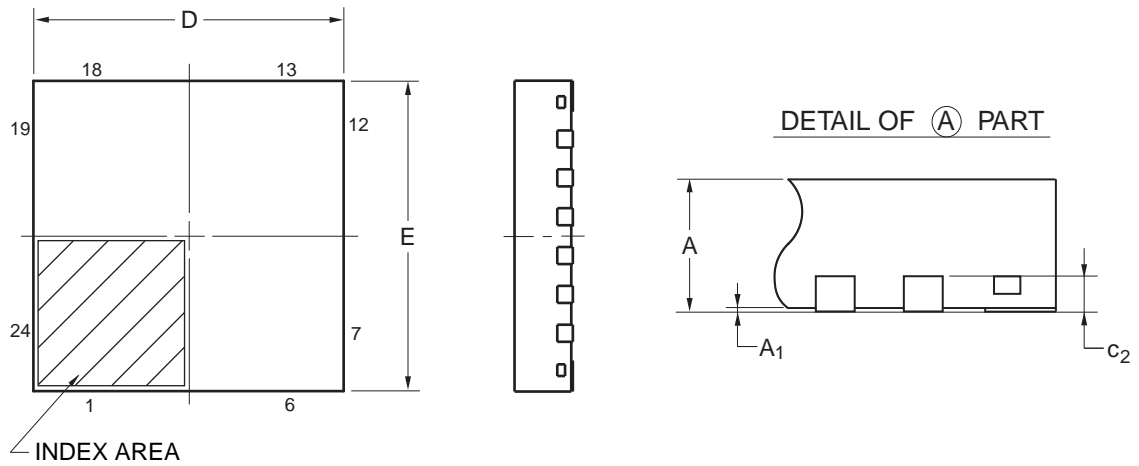


| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min. | Nom. | Max. |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | - | 0.30 |
| C | 0.09 | 0.127 | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.50 | 0.60 | 0.75 |
| S | 0.20 | - | - |
| θ | 0° | - | 8° |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.05 | | |
| ddd | 0.20 | | |

NOTES:
 1. DIMENSION 'D' AND 'E1' DOES NOT INCLUDE MOLD FLASH.
 2. DIMENSION 'b' DOES NOT INCLUDE TRIM OFFSET.
 3. DIMENSION 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE [H].

4.4 24-pin package

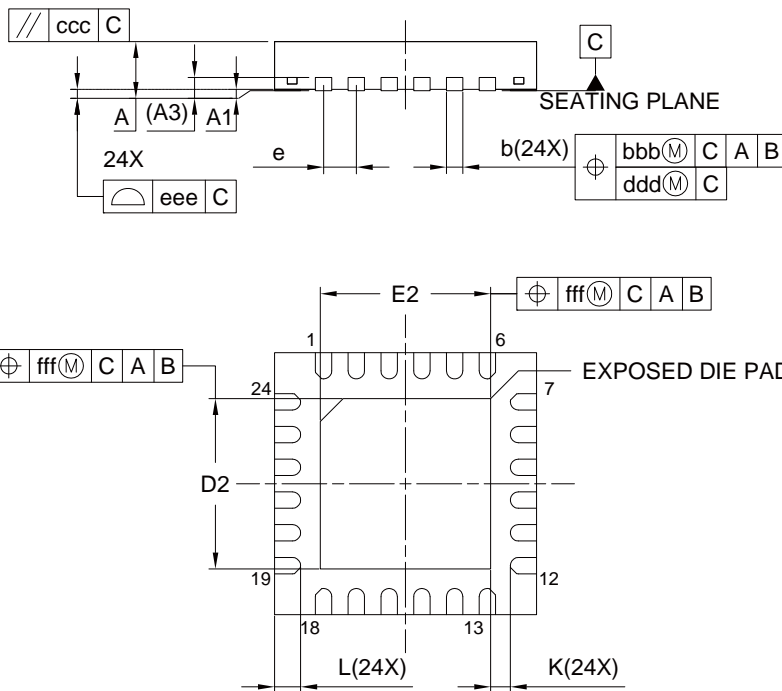
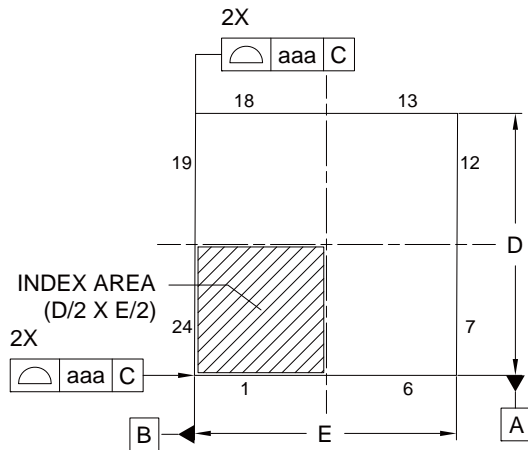
| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|--------------------|--------------|----------------|---------------|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-3 | 0.04 |



| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| D | 3.95 | 4.00 | 4.05 |
| E | 3.95 | 4.00 | 4.05 |
| A | — | — | 0.80 |
| A ₁ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| L _p | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| Z _D | — | 0.75 | — |
| Z _E | — | 0.75 | — |
| C ₂ | 0.15 | 0.20 | 0.25 |
| D ₂ | — | 2.50 | — |
| E ₂ | — | 2.50 | — |

©2013 Renesas Electronics Corporation. All rights reserved.

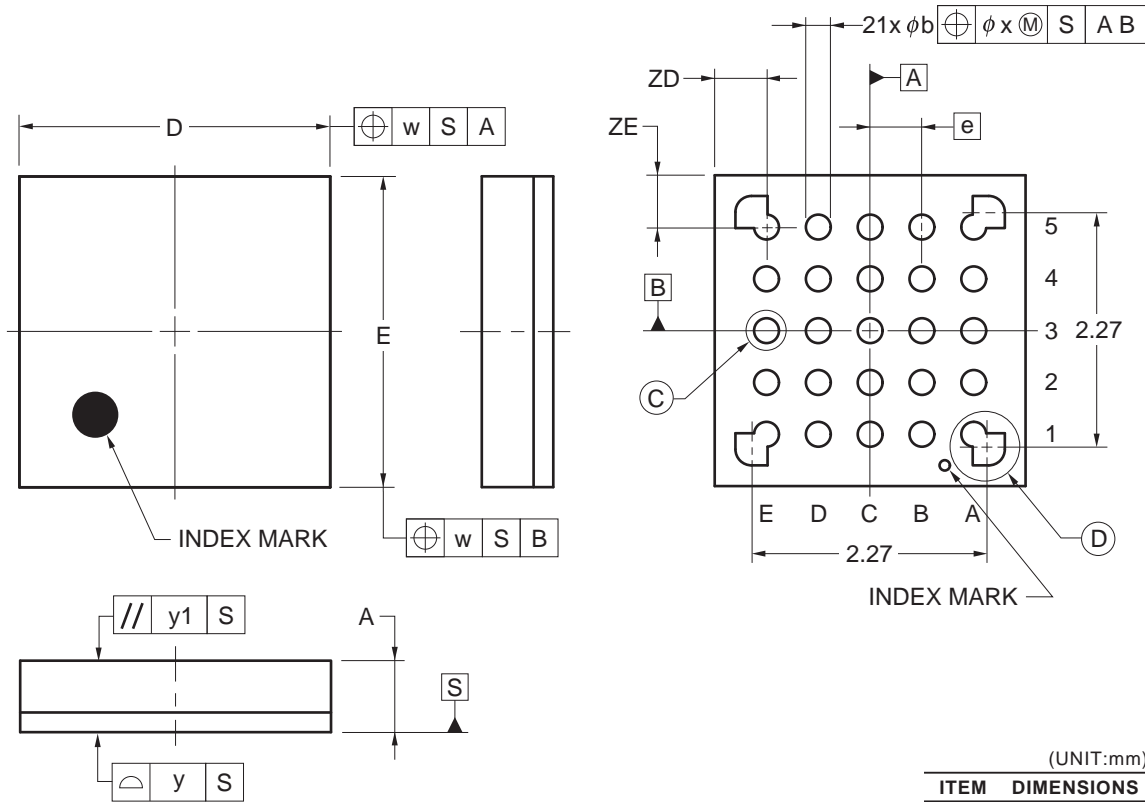
| | | |
|---------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-HWQFN024-4x4-0.50 | PWQN0024KF-A | 0.04 |



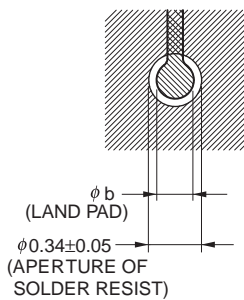
| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min. | Nom. | Max. |
| A | - | - | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.00 BSC | | |
| E | 4.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | - | - |
| D2 | 2.55 | 2.60 | 2.65 |
| E2 | 2.55 | 2.60 | 2.65 |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

4.5 25-pin package

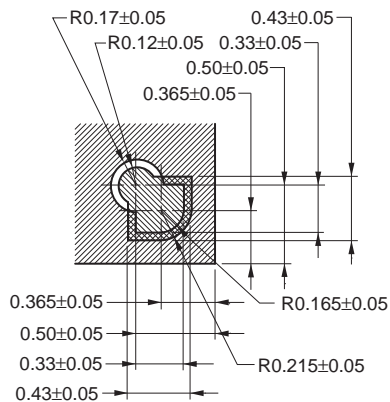
| | | | |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
| P-WFLGA25-3x3-0.50 | PWLG0025KA-A | P25FC-50-2N2-2 | 0.01 |



DETAIL OF \textcircled{C} PART



DETAIL OF \textcircled{D} PART



(UNIT:mm)

| ITEM | DIMENSIONS |
|------|------------|
| D | 3.00±0.10 |
| E | 3.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.50 |
| ZE | 0.50 |

©2012 Renesas Electronics Corporation. All rights reserved.

REVISION HISTORY

RL78/G11 Datasheet

| Rev. | Date | Description | |
|------------|--|----------------------|--|
| | | Page | Summary |
| 0.50 | Mar 31 2016 | — | First Edition issued |
| 1.00 | Sep 28 2016 | p.7 | Modification of Pin Configuration in 1.3.3 25-pin products |
| | | p.9 | Addition of 1.5.1 20-pin products |
| | | p.10 | Addition of product name and Modification of Block Diagram in 1.5.2 24-pin, 25-pin products |
| | | p.12 | Addition of I ² C bus in 1.6 Outline of Functions |
| | | p.15 | Modification of Conditions of I _{OH1} , I _{OL1} in 2.1 Absolute Maximum Ratings |
| | | p.16 | Modification of High-speed on-chip oscillator clock frequency accuracy and addition of D _{IMT} , D _{IMV} in 2.2.2 On-chip oscillator characteristics |
| | | p.17 | Modification of Caution in 2.3.1 Pin characteristics |
| | | p.19 | Modification of Input voltage, high and Input voltage, low in 2.3.1 Pin characteristics |
| | | p.19, 20 | Modification of Caution in 2.3.1 Pin characteristics |
| | | p.22, 23, 24, 26, 27 | Modification of specifications in 2.3.2 Supply current characteristics |
| | | p.29, 30 | Modification of specification in 2.4 AC Characteristics |
| | | p.35 | Modification of specifications in 2.5.1 Serial array unit (1) |
| | | p.39 | Modification of specifications in 2.5.1 Serial array unit (3) |
| | | p.40, 42 | Modification of specification in 2.5.1 Serial array unit (4) |
| | | p.62 | Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (1) |
| | | p.64 | Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (2) |
| | | p.65 | Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (3) |
| | | p.70 | Modification of Conditions in 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic |
| | | p.79 | Addition of description in 3 ELECTRICAL SPECIFICATIONS (TA = -40 to +105°C) |
| | | p.82 | Modification of High-speed on-chip oscillator clock frequency accuracy and addition of D _{IMT} , D _{IMV} in 3.2.2 On-chip oscillator characteristics |
| | | p.83 | Modification of Caution in 3.3.1 Pin characteristics |
| | | p.85 | Modification of Input voltage, high and Input voltage, low in 3.3.1 Pin characteristics |
| | | p.85, 86 | Modification of Caution in 3.3.1 Pin characteristics |
| p.88 to 91 | Modification of specifications in 3.3.2 Supply current characteristics | | |
| p.97 | Modification of specifications and specification table in 3.5.1 Serial array unit (1) | | |
| p.103 | Modification of specifications in 3.5.1 Serial array unit (3) | | |
| p.125 | Modification of Conditions in 3.6.1 A/D converter characteristics (4) | | |
| p.126 | Modification of Conditions in 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic | | |
| 1.10 | Dec 28 2016 | p.4 | Modification of 1.2 Ordering Information |
| 2.00 | Feb 15, 2018 | Throughout | Addition of specifications of 10-pin and 16-pin products |
| | | p.2 | Modification of description in 1.1 Features |
| | | p.6 | Modification of figure in 1.3.4 24-pin products |
| | | p.11 | Modification of figure in 1.5.3 20-pin products |
| | | p.12 | Modification of figure in 1.5.4 24-pin, 25-pin products |

| Rev. | Date | Description | |
|----------|--|--------------|---|
| | | Page | Summary |
| 2.00 | Feb 15, 2018 | p.13, 14 | Modification of table in 1.6 Outline of Functions |
| | | p.18 | Modification of 2.2.2 On-chip oscillator characteristics |
| | | p.19, 21 | Modification of 2.3.1 Pin characteristics |
| | | p.24 | Modification of 2.3.2 Supply current characteristics |
| | | p.32 | Modification of 2.4 AC Characteristics |
| | | p.79 | Modification of figure in 2.10 Timing of Entry to Flash Memory Programming Modes |
| | | p.84 | Modification of 3.2.1 X1 characteristics |
| | | p.84 | Modification of 3.2.2 On-chip oscillator characteristics |
| | | p.85, 86, 87 | Modification of 3.3.1 Pin characteristics |
| | | p.95 | Modification of 3.4 AC Characteristics |
| | | p.99 | Modification of note in 3.5.1 Serial array unit (1) |
| | | p.134 | Modification of figure in 3.10 Timing of Entry to Flash Memory Programming Modes |
| 2.20 | Apr 26, 2019 | p.3 | Addition of note in Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11 |
| | | p.5 | Modification of figure in 1.3.1 10-pin products |
| | | p.5 | Modification of figure in 1.3.2 16-pin products |
| | | p.5 | Modification of figure in 1.3.3 20-pin products |
| | | p.6 | Modification of figure in 1.3.4 24-pin products |
| | | p.13, 14 | Modification of table in 1.6 Outline of Functions |
| | | p.16 | Modification of specification in 2.1 Absolute Maximum Ratings |
| | | p.19, 22 | Modification of specification in 2.3.1 Pin characteristics |
| | | p.25, 27 | Modification of note 1 in 2.3.2 Supply current characteristics |
| | | p.29, 30 | Modification of specification and addition of note 14 in 2.3.2 Supply current characteristics, Peripheral Functions (Common to all products) |
| | | p.32 | Modification of specification in 2.4 AC Characteristics |
| | | p.36 | Modification of note 2 in 2.5.1 Serial array unit, (1) During communication at same potential (UART mode) |
| | | p.41 | Modification of specification in 2.5.1 Serial array unit, (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output), When P20 is used as SO10 pin |
| | | p.43 | Modification of specification in 2.5.1 Serial array unit, (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input), When P01, P32, P53, P54 and P56 are used as SOMn pins |
| | | p.44 | Modification of specification in 2.5.1 Serial array unit, (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input), When P20 is used as SO10 pin |
| p.47 | Modification of specification in 2.5.1 Serial array unit, (5) During communication at same potential (simplified I ² C mode) | | |
| p.53, 54 | Modification of specification in 2.5.1 Serial array unit, (7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) | | |
| p.60 | Modification of note 3 in 2.5.1 Serial array unit, (9) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input) | | |

| Rev. | Date | Description | |
|-------|--|--------------|---|
| | | Page | Summary |
| 2.20 | Apr 26, 2019 | p.69 | Modification of note 3 in 2.6.1 A/D converter characteristics, (2) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI16 to ANI22 |
| | | p.70 | Modification of specification in 2.6.1 A/D converter characteristics, (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI3, ANI16 to ANI22, internal reference voltage, and temperature sensor output voltage |
| | | p.71 | Modification of specification in 2.6.1 A/D converter characteristics, (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI0, ANI2 and ANI3, ANI16 to ANI22 |
| | | p.72 | Modification of title in 2.6.3 D/A converter (channel 1) |
| | | p.73 | Modification of specification in 2.6.4 Comparator |
| | | p.82 | Modification of specification in 3.1 Absolute Maximum Ratings |
| | | p.84 | Modification of specification in 3.2.1 X1 characteristics |
| | | p.85, 87, 88 | Modification of specification in 3.3.1 Pin characteristics |
| | | p.93 | Modification of specification in 3.3.2 Supply current characteristics, Peripheral Functions (Common to all products) |
| | | p.99 | Modification of specification in 3.5.1 Serial array unit, (1) during communication at same potential (UART mode), When P20 is used as TxD1 pin |
| | | p.101 | Modification of specification in 3.5.1 Serial array unit, (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output), When P01, P32, P53, P54 and P56 are used as Somn pins |
| | | p.102 | Modification of specification in 3.5.1 Serial array unit, (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output), When P20 is used as SO10 pin |
| | | p.103 | Modification of note 1 in 3.5.1 Serial array unit, (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input), When P01, P32, P53, P54 and P56 are used as SOMn pins |
| | | p.105 | Modification of specification and note 1 in 3.5.1 Serial array unit, (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input), When P20 is used as SO10 pin |
| | | p.124 | Modification of specification in 3.6.1 A/D converter characteristics, (1) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage |
| | | p.125 | Modification of note 3 in 3.6.1 A/D converter characteristics, (2) When reference voltage (+) = $AV_{REFP}/ANI0$ (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI16 to ANI22 |
| | | p.127 | Modification of specification in 3.6.1 A/D converter characteristics, (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin: ANI0 to ANI3, ANI16 to ANI22 |
| | | p.128 | Modification of title in 3.6.3 D/A converter (channel 1) |
| | | p.129 | Modification of specification in 3.6.4 Comparator |
| | | p.131 | Modification of specification in 3.6.6 POR circuit characteristics |
| p.132 | Modification of specification in 3.6.7 LVD circuit characteristics, (1) LVD Detection Voltage of Reset Mode and Interrupt Mode | | |

| Rev. | Date | Description | |
|------|---------------|-------------|--|
| | | Page | Summary |
| 2.30 | June 30, 2020 | p.3 | Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11 |
| | | p.4 | Modification of table in 1.2 Ordering Information |
| | | p.5 | Modification of description in 1.3.3 20-pin products |
| | | p.26 | Modification of specification in 2.3.2 Supply current characteristics |
| | | p.138 | Addition of package drawing in 4.3 20-pin package |
| | | p.140 | Addition of package drawing in 4.4 24-pin package |
| 2.40 | Oct 30, 2020 | p.3 | Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G11 |
| | | p.4 | Modification of table in 1.2 Ordering Information |
| | | p.6 | Addition of description and figure in 1.3.2 16-pin products |
| | | p.138 | Addition of package drawing in 4.2 16-pin package |

SuperFlash is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics Corporation

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc. Milpitas Campus

1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.

Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics America Inc. San Jose Campus

6024 Silver Creek Valley Road, San Jose, CA 95138, USA

Tel: +1-408-284-8200, Fax: +1-408-284-2775

Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3

Tel: +1-905-237-2004

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany

Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 101-T01, Floor 1, Building 7, Yard No. 7, 8th Street, Shangdi, Haidian District, Beijing 100085, China

Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai 200333, China

Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong

Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan

Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, #06-02 Singapore 339949

Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit No 3A-1 Level 3A Tower 8 UOA Business Park, No 1 Jalan Pengerutcara U1/51A, Seksyen U1, 40150 Shah Alam, Selangor, Malaysia

Tel: +60-3-5022-1288, Fax: +60-3-5022-1290

Renesas Electronics India Pvt. Ltd.

No.77C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India

Tel: +91-80-67208700

Renesas Electronics Korea Co., Ltd.

17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea

Tel: +82-2-558-3737, Fax: +82-2-558-5338