

LOW-JITTER SAW OSCILLATOR (SPSO)

OUTPUT : LV-PECL, LVDS, HCSSL



Product Number
 EG-2121CA: Q3805CAx0xxxx00
 : X1M000101xxxx00
 EG-2102CA: Q3806CA00xxxx00
 : X1M000091xxxx00

EG-2121CA
EG-2102CA

- Frequency range : 53.125 MHz to 700 MHz
- Supply voltage : 2.5 V ... EG-2121CA
3.3 V ... EG-2102CA
- Output : LV-PECL or LVDS or HCSSL
- Function : Output enable (OE)
- External dimensions : 7.0 × 5.0 × 1.2 mm



•Very low jitter and low phase noise by SAW unit.

Specifications (characteristics)

► Differential LV-PECL Output

Item	Symbol	EG-2121CA		EG-2102CA		Conditions / Remarks
		LV-PECL				
Output frequency range	f _o	53.125 MHz to 500 MHz		100 MHz to 700 MHz		Please contact us about available frequencies.
Supply voltage	V _{CC}	2.5 V ± 0.125 V		3.3 V ± 0.3 V		
Storage temperature	T _{stg}	-40 C to +100 C				Storage as single product.
Operating temperature	T _{use}	P: 0 C to +70 C, R: -5 C to +85 C, S: -20 C to +70 C				
Frequency tolerance	f _{tol}	G: ± 50 × 10 ⁻⁶ , H: ± 100 × 10 ⁻⁶				
Current consumption	I _{CC}	80 mA Max.		100 mA Max.		OE=V _{CC} , L ECL=50 Ω
Disable current	I _{dis}	20 mA Max.		32 mA Max.		OE=GND
Symmetry	SYM	P: 40 % to 60 % (f _o > 350 MHz)		P: 45 % to 55 %		at outputs crossing point
		P: 45 % to 55 % (f _o ≤ 350 MHz)				
		D: 48 % to 52 % (f _o ≤ 175 MHz)				
Output voltage	V _{OH}	1.55 V Typ.		2.35 V Typ.		DC characteristics
	V _{CC} -1.025 V to V _{CC} -0.88 V					
	V _{OL}	0.8 V Typ.		1.6 V Typ.		
Output load condition (ECL)	L _{ECL}	50 Ω				Terminated to V _{CC} -2.0 V
Input voltage	V _{IH}	70 % V _{CC} Min.				OE terminal
	V _{IL}	30 % V _{CC} Max.				
Rise time / Fall time	t _r / t _f	400 ps Max.				Between 20 % and 80 % of (V _{OH} -V _{OL})
Start-up time	t _{str}	10 ms Max.				Time at minimum supply voltage to be 0 s
Phase Jitter	t _{pj}	0.8 ps Max.				f _o < 100 MHz
		0.5 ps Max.				100 MHz ≤ f _o < 200 MHz
		0.3 ps Max.				200 MHz ≤ f _o
Frequency aging	f _{aging}	± 10 × 10 ⁻⁶ / year Max.				+25 C, First year, V _{CC} =2.5 V, 3.3 V

► LVDS Output

Item	Symbol	EG-2121CA		EG-2102CA		Conditions / Remarks
		LVDS				
Output frequency range	f _o	53.125 MHz to 700 MHz				Please contact us about available frequencies.
Supply voltage	V _{CC}	2.5 V ± 0.125 V		3.3 V ± 0.3 V		
Storage temperature	T _{stg}	-40 C to +100 C				Storage as single product.
Operating temperature	T _{use}	P: 0 C to +70 C, R: -5 C to +85 C, S: -20 C to +70 C				
Frequency tolerance	f _{tol}	G: ± 50 × 10 ⁻⁶ , H: ± 100 × 10 ⁻⁶				
Current consumption	I _{CC}	30 mA Max.		45 mA Max.		OE=V _{CC} , L LVDS= 100 Ω
Disable current	I _{dis}	20 mA Max.		30 mA Max.		OE=GND
Symmetry	SYM	L: 40 % to 60 % (f _o > 350 MHz)		L: 40 % to 60 % (f _o > 350 MHz)		at outputs crossing point
		L: 45 % to 55 % (f _o ≤ 350 MHz)				
		V: 48 % to 52 % (f _o ≤ 175 MHz)				
Output voltage	V _{OD}	350 mV Typ. 247 mV to 454 mV				DC characteristics
	dV _{OD}	50 mV Max.				
	V _{OS}	1.25 V Typ. 1.125 V to 1.375 V				
	dV _{OS}	150 mV Max.				
Output load condition (LVDS)	L _{LVDS}	100 Ω				Connected between OUT to $\overline{\text{OUT}}$
Input voltage	V _{IH}	70 % V _{CC} Min.				OE terminal
	V _{IL}	30 % V _{CC} Max.				
Rise time / Fall time	t _r / t _f	400 ps Max.				Between 20 % and 80 % of Differential Output Peak to Peak voltage
Start-up time	t _{str}	10 ms Max.				Time at minimum supply voltage to be 0 s
Phase Jitter	t _{pj}	0.8 ps Max.				f _o < 100 MHz
		0.5 ps Max.				100 MHz ≤ f _o < 200 MHz
		0.3 ps Max.				200 MHz ≤ f _o
Frequency aging	f _{aging}	± 10 × 10 ⁻⁶ / year Max.				+25 C, First year, V _{CC} =2.5 V, 3.3 V

► HCSL Output

Item	Symbol	EG-2121CA		EG-2102CA		Conditions / Remarks
		HCSL				
Output frequency range	fo	100 MHz to 350 MHz				Please contact us about available frequencies.
Supply voltage	V _{CC}	2.5 V ± 0.125 V		3.3 V ± 0.3 V		
Storage temperature	T _{stg}	-40 °C to +125 °C				Storage as single product.
Operating temperature	T _{use}	P: 0 °C to +70 °C, R: -5 °C to +85 °C, S: -20 °C to +70 °C				
Frequency tolerance	f _{tol}	G: ±50 × 10 ⁻⁶ , H: ±100 × 10 ⁻⁶				
Current consumption	I _{CC}	80 mA Max.		85 mA Max.		OE=V _{CC} , L HCSL=50 Ω
Disable current	I _{dis}	20 mA Max.		35 mA Max.		OE=GND
Symmetry	SYM	45 % to 55 %				at outputs crossing point
Output Voltage	V _{OH}	0.75 V Typ.				DC characteristics
	V _{OL}	-0.3 V Typ.				
Output load condition (HCSL)	L HCSL	50 Ω				Terminated to GND
Input voltage	V _{IH}	70 % V _{CC} Min.				OE terminal
	V _{IL}	30 % V _{CC} Max.				
Rise time / Fall time	t _r / t _f	500 ps Max.				Between 0.175 V and 0.525 V of output
Start-up time	t _{str}	10 ms Max.				Time at minimum supply voltage to be 0 s
Phase Jitter	t _{pj}	0.8 ps Max.				fo < 100 MHz
		0.5 ps Max.				100 MHz ≤ fo < 200 MHz
		0.3 ps Max.				200 MHz ≤ fo
Frequency aging *2	f _{aging}	± 10 × 10 ⁻⁶ / year Max.				+25 °C, First year, V _{CC} =2.5 V, 3.3 V

Product Name EG-2121 CA 250.00000MHz P G P A

(Standard form)

- ① Model ② Package type ③ Frequency
 ④ Output/Symmetry ⑤ Frequency tolerance ⑥ Operating temperature
 ⑦ Frequency aging (A*1: Frequency tolerance include aging, N*2: Frequency tolerance exclude aging)

*1 This includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift, and aging(+25 °C, 10 years).

*2 This includes initial frequency tolerance, temperature variation, supply voltage change, and reflow drift(except aging).

(⑤⑥⑦): GRA, GSA are not available)

(⑤⑥): As for LV-PECL and LVDS output, for 53.125 MHz ≤ fo < 100 MHz only HP is available)

④ Symbol	Output	Symmetry	
		EG-2121CA	EG-2102CA
P	LV-PECL	40 % to 60 % (fo > 350 MHz) 45 % to 55 % (fo ≤ 350 MHz)	45 % to 55 %
D	LV-PECL	48 % to 52 % (fo ≤ 175 MHz)	48 % to 52 % (fo ≤ 350 MHz)
L	LVDS	40 % to 60 % (fo > 350 MHz) 45 % to 55 % (fo ≤ 350 MHz)	
V	LVDS	48 % to 52 % (fo ≤ 175 MHz)	
H	HCSL	45 % to 55 %	

⑤ Frequency tolerance	
G	±50 × 10 ⁻⁶
H	±100 × 10 ⁻⁶

⑥ Operating temperature	
P	0 °C to +70 °C
R	-5 °C to +85 °C
S	-20 °C to +70 °C

Table 2 Jitter

Item	Symbol	Specifications	Remarks
Jitter *	t _{DJ}	0.2 ps Typ.	Deterministic Jitter
	t _{RJ}	3 ps Typ.	Random Jitter
	t _{RMS}	3 ps Typ.	σ (RMS of total distribution)
	t _{p-p}	25 ps Typ.	Peak to Peak
	t _{acc}	4 ps Typ.	Accumulated Jitter(σ) n=2 to 50 000 cycles

* Tested using a DTS-2075 Digital timing system made by WAVECREST with jitter analysis software VISI6.

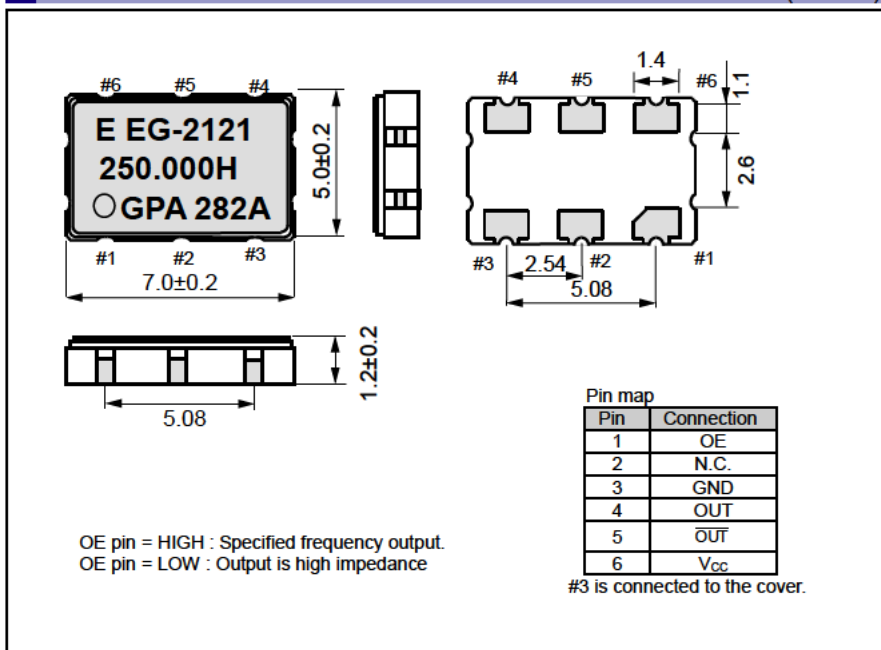
* Based on SIA-3100C signal integrity analyzer made from WAVECREST.

○ : Differential LV-PECL, LVDS output

□ : HCSL output

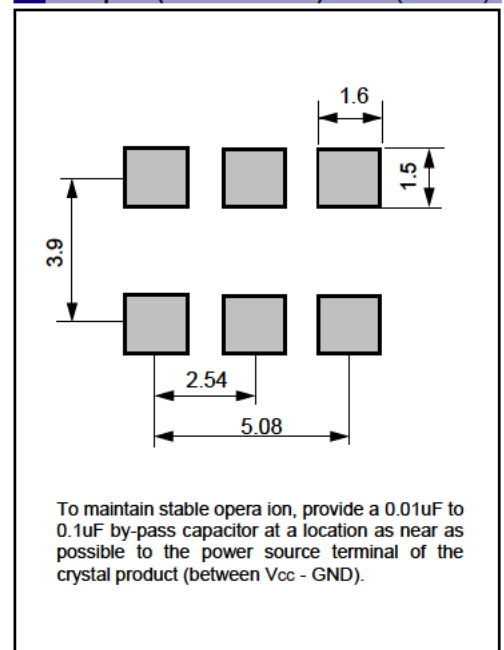
External dimensions

(Unit:mm)



Footprint (Recommended)

(Unit:mm)



PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

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ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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► Explanation of the mark that are using it for the catalog

	► Pb free.
	► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
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