

## Features

- 32.768 kHz μPower oscillator
- ±10 PPM Initial tolerance, ±50 ppm over temperature
- Smallest Footprint: 1.2 mm<sup>2</sup>
  - 1.5 x 0.8 mm CSP
  - No external bypass cap required
  - Output drives multiple loads and eliminates discrete XTALs
- Improved stability reduces system power with fewer network timekeeping updates
- Ultra-low power: 4.5 μA
- Supply voltage range: 1.62V to 3.63V
- Operating temperature ranges: -40°C to +85°C
- Pb-free, RoHS and REACH compliant

## Applications

- Health and wellness monitors
- Wireless connectivity sleep clock
- ULP input devices
- RTC reference clock



## Electrical Specifications

**Table 1. Electrical Characteristics**

Conditions: Min/Max limits are over temperature, Vdd = 1.8V ±10%, unless otherwise stated. Typicals are at 25°C and Vdd = 1.8V.

| Parameter                                     | Symbol                          | Min. | Typ.   | Max. | Unit              | Condition   |
|---|---------------------------------|------|--------|------|-------------------|---|
| <b>Frequency and Stability</b>                |                                 |      |        |      |                   |   |
| Output Frequency                              | F <sub>OUT</sub>                |      | 32.768 |      | kHz               |   |
| Total Frequency Stability <sup>(1)</sup>      | F <sub>stab</sub>               | -10  | 1      | 10   | ppm               | T <sub>A</sub> = 25°C   |
|   |                                 | -50  |        | 50   | ppm               | T <sub>A</sub> = -40°C to +85°C   |
| First Year Frequency Aging                    | F <sub>aging</sub>              |      | ±1     |      | ppm               | T <sub>A</sub> = 25°C   |
| <b>Jitter Performance</b>                     |                                 |      |        |      |                   |   |
| Period Jitter                                 | PJ                              |      | 2.5    | 4    | nS <sub>RMS</sub> | Cycles = 10,000, Per JEDEC standard 65B                                   |
| <b>Supply Voltage and Current Consumption</b> |                                 |      |        |      |                   |   |
| Operating Supply Voltage                      | Vdd                             | 1.62 | 1.8    | 3.63 | V                 |   |
| No Load Supply Current                        | I <sub>dd</sub>                 |      | 4      | 5.3  | μA                | Vdd = 1.8V  |
| Start-up Time at Power-up                     | t <sub>start</sub>              |      | 135    | 300  | ms                | Measured when supply reaches 90% of final Vdd, to the first output pulse. |
| <b>Operating Temperature Range</b>            |                                 |      |        |      |                   |   |
| Operating Temperature Range                   | Op_Temp                         | -40  |        | 85   | °C                |   |
| <b>LVC MOS Output</b>                         |                                 |      |        |      |                   |   |
| Output Rise/Fall Time                         | t <sub>r</sub> , t <sub>f</sub> |      | 9      | 20   | ns                | 10-90% (Vdd), 15 pF Load.   |
| Output Clock Duty Cycle                       | DC                              | 45   |        | 55   | %                 |   |
| Output Voltage High                           | VOH                             | 90%  |        |      | Vdd               | I <sub>OH</sub> = -1 μA   |
| Output Voltage Low                            | VOL                             |      |        | 10%  | Vdd               | I <sub>OL</sub> = 1 μA  |

**Note:**

1. Relative to 32.768 kHz, includes initial tolerance, over temp stability, 3x reflow, Vdd range, board-level underfill, and 20% load variation. Tested with Agilent 53132A frequency counter. Measured with 100 ms gate time for accurate frequency measurement.

Table 2. Pin Description

| CSP Pin | Symbol  | I/O                 | Functionality   |
|---------|---------|---------------------|---|
| 1       | NC      | Internal Test       | No Connect. Leave floating. Pin 1 is for internal testing and is designed to be left floating.  |
| 2       | CLK Out | OUT                 | 32.768 kHz, LVCMOS compatible output. Drive strength is sufficient to drive multiple low-power loads.   |
| 3       | Vdd     | Power Supply        | Operates from nominal supply voltages between 1.8V to 3.3V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). SiT1572 includes on-chip filtering capacitors. |
| 4       | GND     | Power Supply Ground | Connect to ground.  |

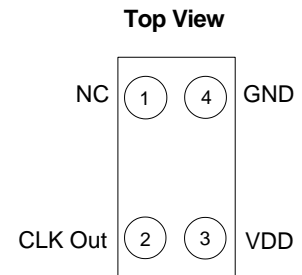


Figure 1. Pin Assignment

Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter  | Test Condition       | Value       | Unit         |
|--|----------------------|-------------|--------------|
| Continuous Power Supply Voltage Range (Vdd)        |                      | -0.5 to 4.0 | V            |
| Continuous Maximum Operating Temperature Range     |                      | 105         | $^{\circ}$ C |
| Short Duration Maximum Operating Temperature Range | $\leq$ 30 minutes    | 125         | $^{\circ}$ C |
| Human Body Model (HBM) ESD Protection              | JESD22-A114          | 2000        | V            |
| Charge-Device Model (CDM) ESD Protection           | JESD22-C101          | 750         | V            |
| Machine Model (MM) ESD Protection                  | JESD22-A115          | 300         | V            |
| Latch-up Tolerance                                 | JESD78 Compliant     |             |              |
| Mechanical Shock Resistance                        | Mil 883, Method 2002 | 20,000      | g            |
| Mechanical Vibration Resistance                    | Mil 883, Method 2007 | 70          | g            |
| 1508 CSP Junction Temperature                      |                      | 150         | $^{\circ}$ C |
| Storage Temperature                                |                      | -65 to 150  | $^{\circ}$ C |

## System Block Diagram

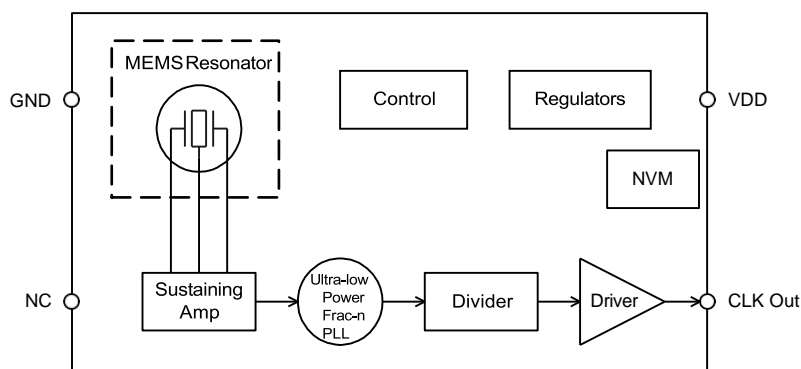


Figure 2. SiT1572 Block Diagram

## Description

The SiT1572 is an ultra-small, micropower, 32.768 kHz oscillator in a CSP-4 package. Typical supply current is 4.5  $\mu$ A under no load condition.

SiTime's MEMS oscillator consists of a MEMS resonator and a programmable analog circuit. SiT1572 MEMS resonator is built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal™ creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal™, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal™ manufacturing processes is the capability to integrate SiTime's MEMS die with a SoC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cost-effective solution to the customer.

## Frequency Stability

The SiT1572 oscillator is Factory trimmed to 32.768 kHz at room temperature and internally compensated over temperature. The result is a very accurate oscillator at room temperature and over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 to 0.06 ppm/°C<sup>2</sup> temperature coefficient, the SiT1572 error is corrected over temperature with an active temperature correction circuit. The result is  $<\pm$ 50 ppm frequency variation over the -40°C to +85°C temperature range.

When measuring the output frequency of SiT1572 with a frequency counter, it is important to make sure the counter's gate time is  $>$ 100 ms. Shorter gate times may lead to inaccurate measurements.

### Typical Operating Curves

( $T_A = 25^\circ\text{C}$ ,  $V_{dd} = 1.8\text{V}$ , unless otherwise stated)



Figure 3. LVCMOS Output Swing ( $V_{dd}=1.8\text{V}$ )

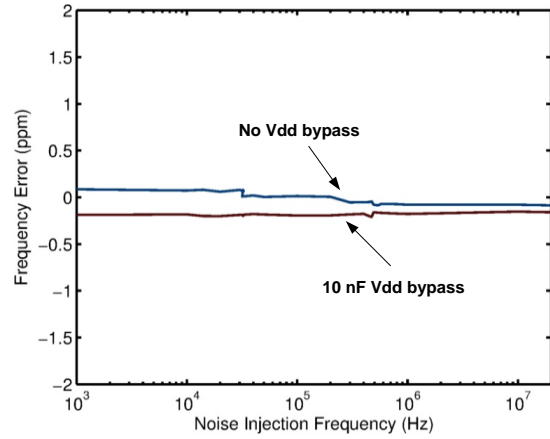
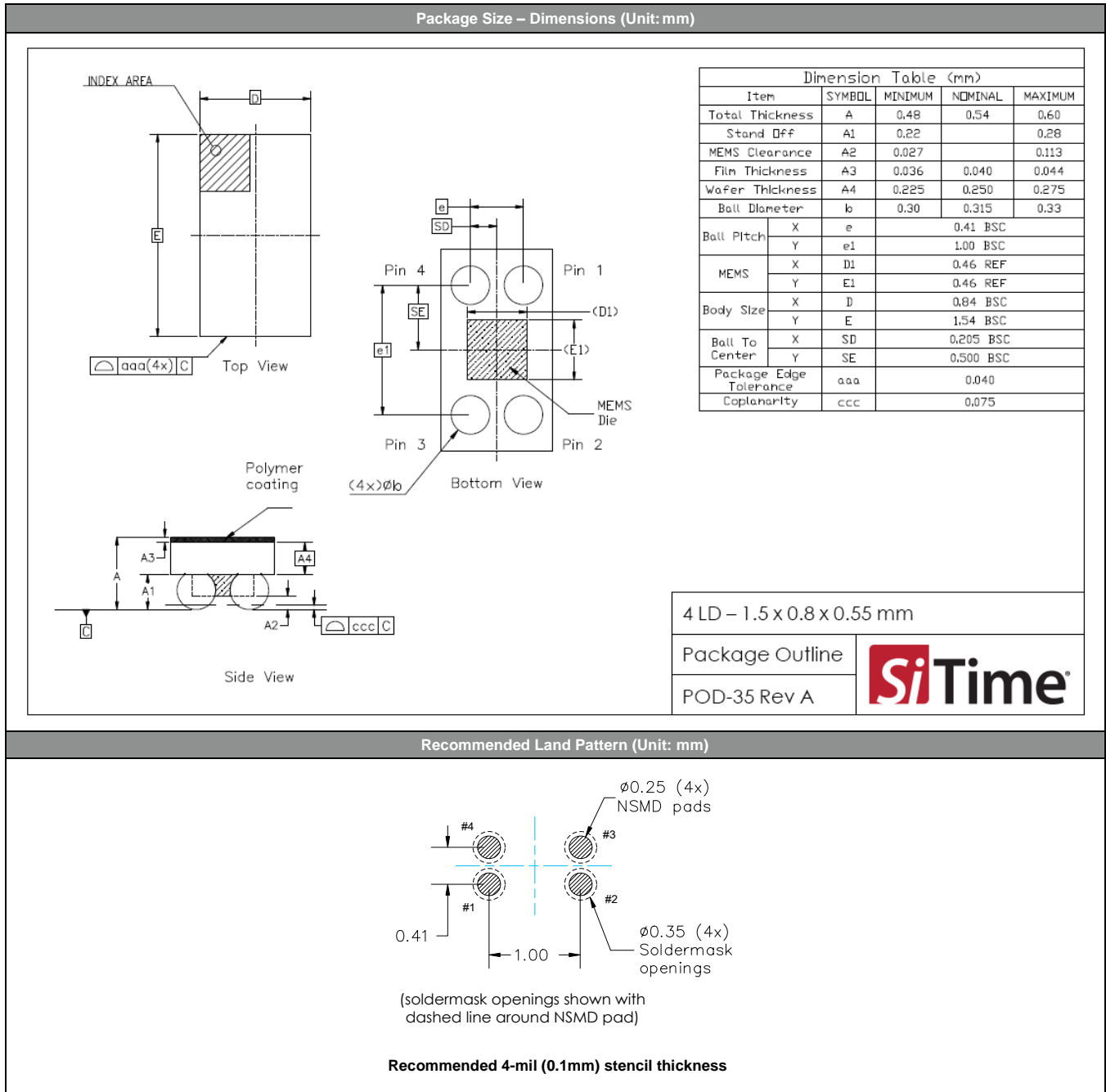


Figure 4. Power Supply Noise rejection (PSNR)

## Dimensions and Patterns

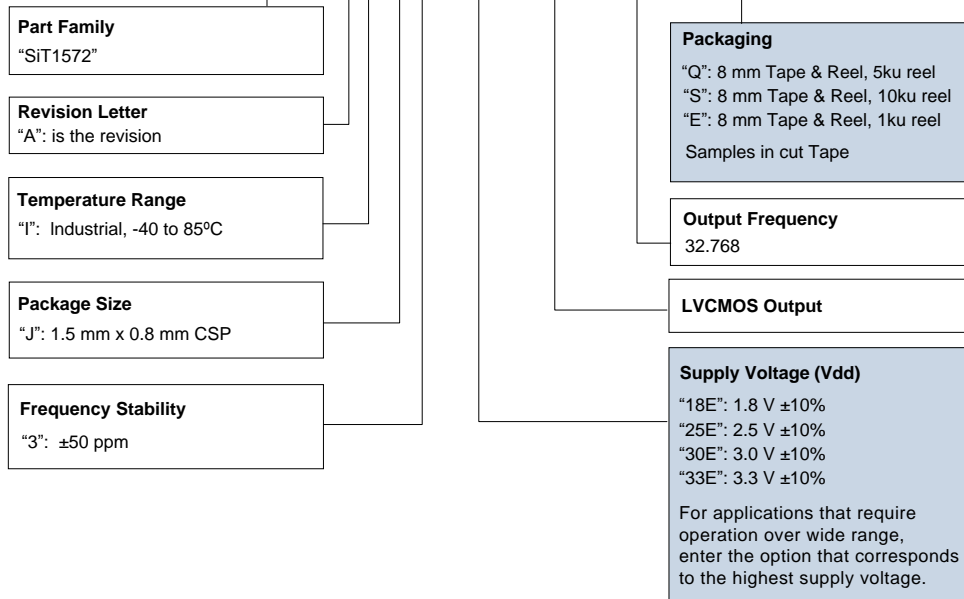


## Manufacturing Guidelines

- 1) No Ultrasonic or Megasonic cleaning: Do not subject SiT1572 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.
- 2) Applying board-level underfill and overmold is acceptable and will not impact the reliability of the device.
- 3) Reflow profile, per JESD22-A113D.
- 4) The SiT1572 CSP includes a protective, opaque polymer top-coat. If the SiT1572 will see intense light, especially in the 1.0-1.2 $\mu$ m IR spectrum, we recommend a protective “glob-top” epoxy or other cover to keep the light from negatively impacting the frequency stability.
- 5) For additional manufacturing guidelines and marking/tape-reel instructions, refer to [SiTime Manufacturing Notes](#).

## Ordering Information

SiT1572AI-J3-33E-DCC-32.768Q



**Table 4. Revision History**

| Version | Release Date | Change Summary      |
|---------|--------------|---------------------|
| 0.9     | 01/24/2018   | Preliminary Release |

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