

DF6F6.8MTU

1. Applications

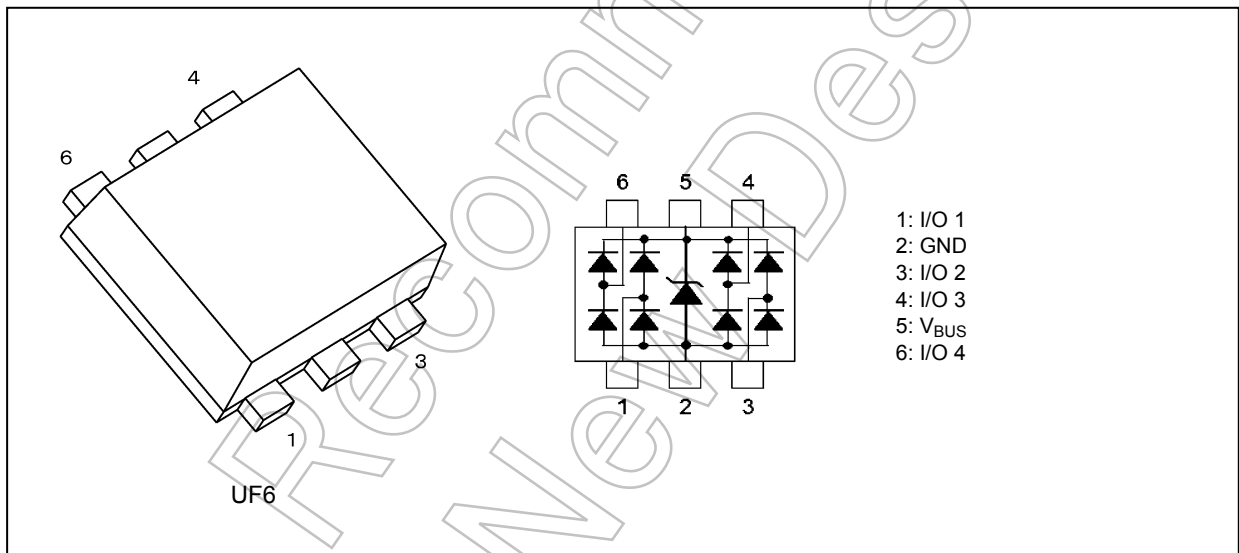
- ESD Protection

Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

2. Features

- (1) ESD protection for up to 4 high-speed data lines and 1 V_{BUS} line.
- (2) Ultra compact packaging for easy configuration in any ESD protection circuits.
- (3) Low Input/output-to-ground capacitance: C_{t(1)} = 0.6 pF (typ.).

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V _{ESD}	±8	kV
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Electrical Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

V_{RWM} : Working peak reverse voltage
 V_{BR} : Reverse breakdown voltage
 I_{BR} : Reverse breakdown current
 I_R : Reverse current
 V_C : Clamp voltage
 I_{PP} : Peak pulse current
 R_{DYN} : Dynamic resistance
 I_F : Forward current
 V_F : Forward voltage

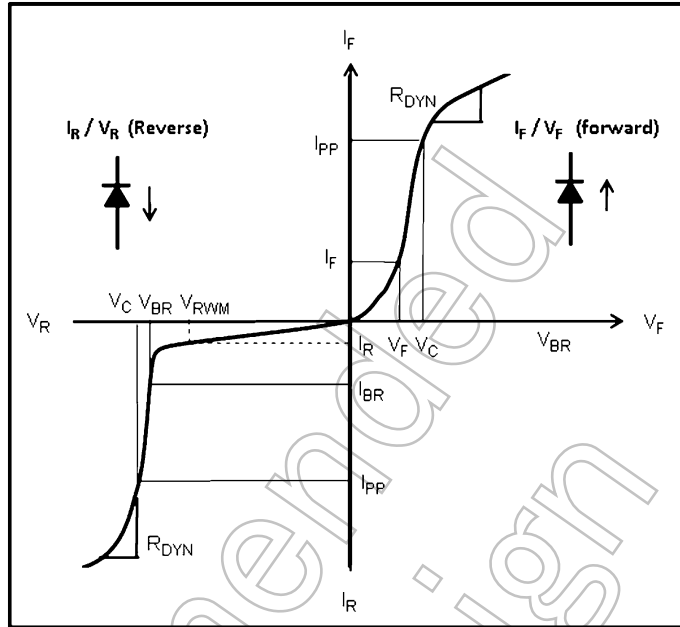


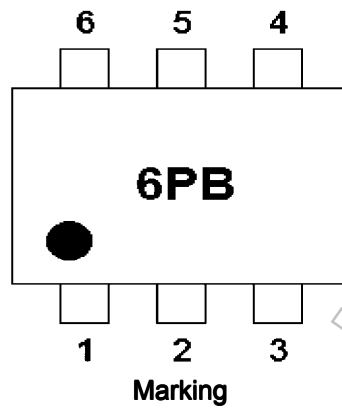
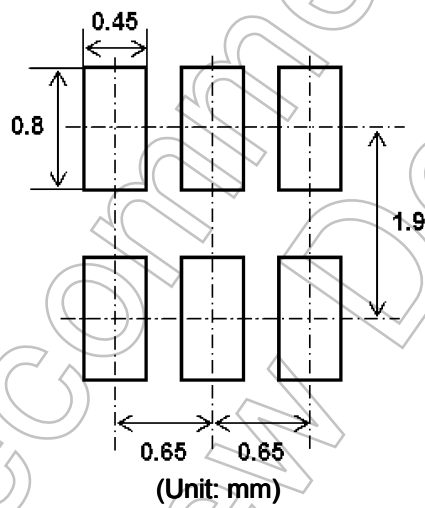
Fig. 5.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}			—	—	5.0	V
Reverse breakdown voltage	$V_{BR(1)}$		$I_{BR} = 5\text{ mA}$ (between I/O and GND)	6.0	—	—	V
	$V_{BR(2)}$		$I_{BR} = 5\text{ mA}$ (between V_{BUS} and GND)	6.8	—	—	V
Reverse current	$I_{R(1)}$		$V_{RWM} = 5\text{ V}$ (between I/O and GND)	—	—	0.5	μA
	$I_{R(2)}$		$V_{RWM} = 5\text{ V}$ (between V_{BUS} and GND)	—	—	0.5	μA
Clamp voltage	$V_{C(1)}$	(Note 1)	$I_{PP} = 1\text{ A}$ (between I/O and GND)	—	15	20	V
	$V_{C(2)}$	(Note 1)	$I_{PP} = 2.5\text{ A}$ (between I/O and GND)	—	18	24	V
	$V_{C(3)}$	(Note 1)	$I_{PP} = 1\text{ A}$ (between V_{BUS} and GND)	—	14	19	V
	$V_{C(4)}$	(Note 1)	$I_{PP} = 9\text{ A}$ (between V_{BUS} and GND)	—	25	30	V
Dynamic resistance	$R_{DYN(1)}$	(Note 2)	(between I/O and GND)	—	0.9	—	Ω
	$R_{DYN(2)}$	(Note 2)	(between V_{BUS} and GND)	—	0.6	—	Ω
Total capacitance	$C_{t(1)}$	(Note 3)	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (between I/O and GND)	—	0.6	1.0	pF
	$C_{t(2)}$		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (between V_{BUS} and GND)	—	67	—	pF
	$C_{t(3)}$		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (between I/O and I/O)	—	0.3	—	pF
Input/output-to-ground capacitance difference	ΔC_{I-GND}		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ (between I/O and GND)	—	0.01	—	pF

Note 1: Based on IEC61000-4-5 8/20 μs pulse.

Note 2: TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using a least-squares fit of TLP characteristics at I_{PP} between 3 A to 8 A.

Note 3: Guaranteed by design.

6. Marking**7. Land Pattern Dimensions (for reference only)**

8. Characteristics Curves (Note)

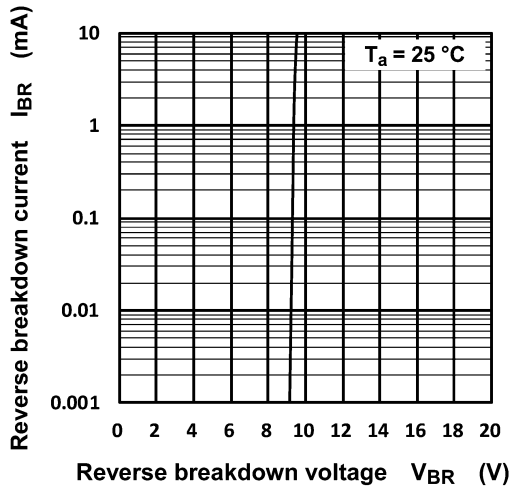


Fig. 8.1 $I_{BR} - V_{BR}$
(I/O to GND)

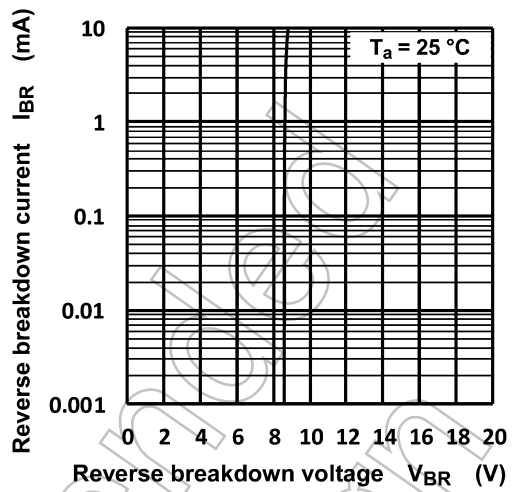


Fig. 8.2 $I_{BR} - V_{BR}$
(V_{BUS} to GND)

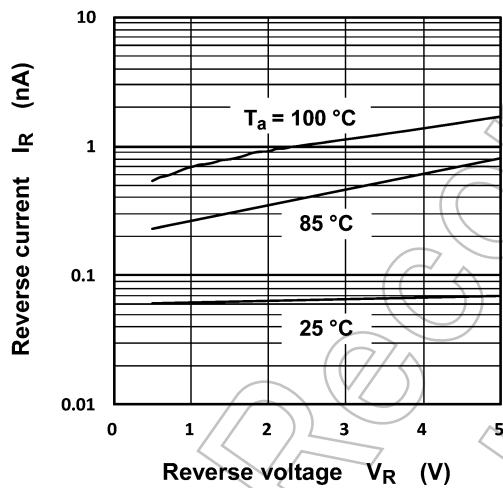


Fig. 8.3 $I_R - V_R$
(I/O to GND)

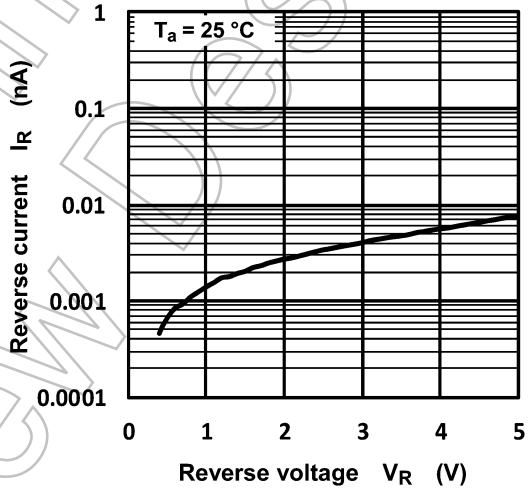


Fig. 8.4 $I_R - V_R$
(V_{BUS} to GND)

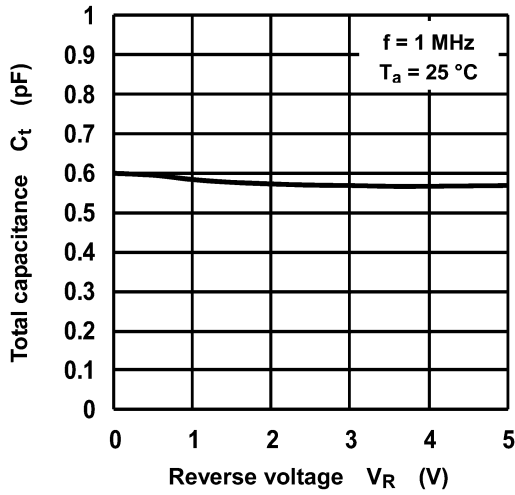


Fig. 8.5 $C_t - V_R$
(I/O to GND)

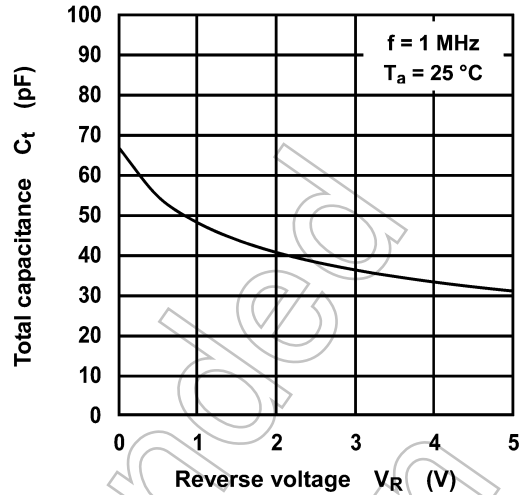


Fig. 8.6 $C_t - V_R$
(VBUS to GND)

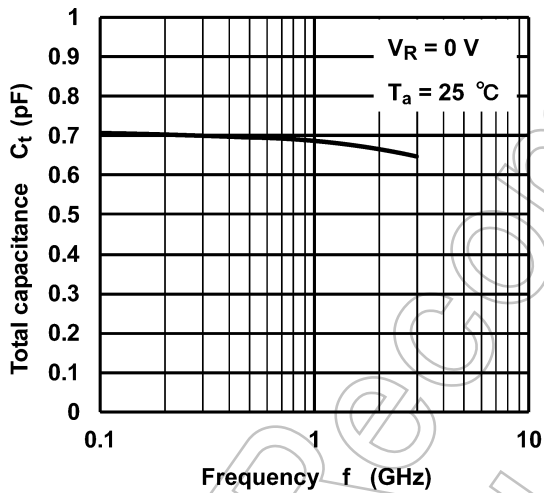
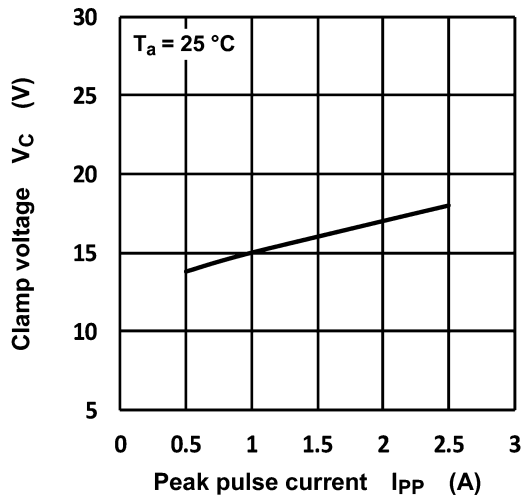


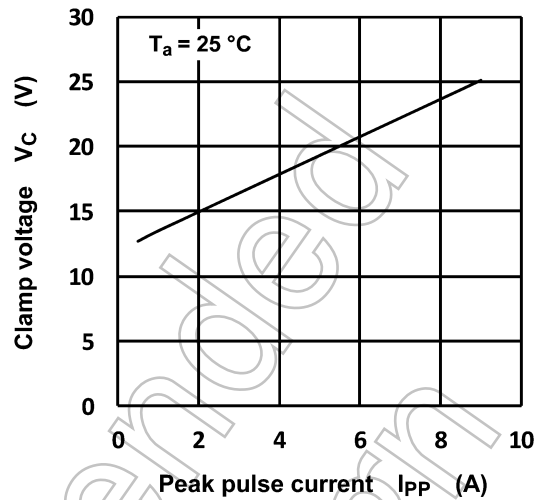
Fig. 8.7 $C_t - f$
(I/O to GND)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

9. Clamp Voltage V_C - Peak Pulse Current (I_{PP}) (Note)



**Fig. 9.1 V_C - I_{PP}
(I/O to GND)**



**Fig. 9.2 V_C - I_{PP}
(VBUS to GND)**

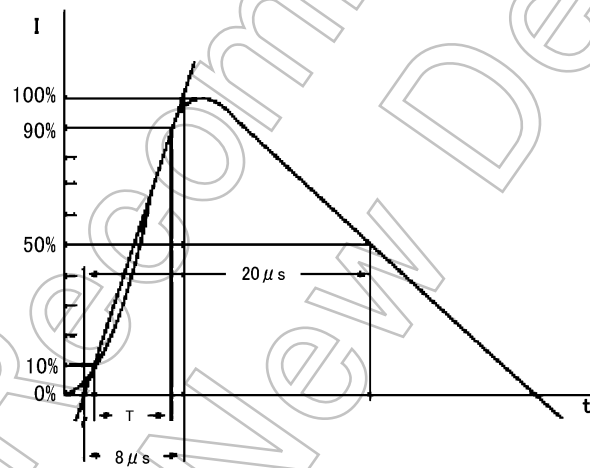


Fig. 9.3 Based on IEC61000-4-5 8/20 μ s pulse

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

10. Insertion Loss (S21) (Note)

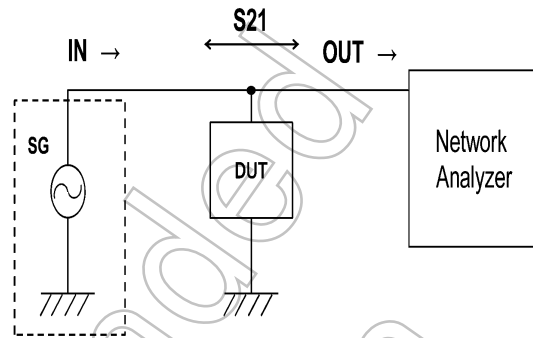
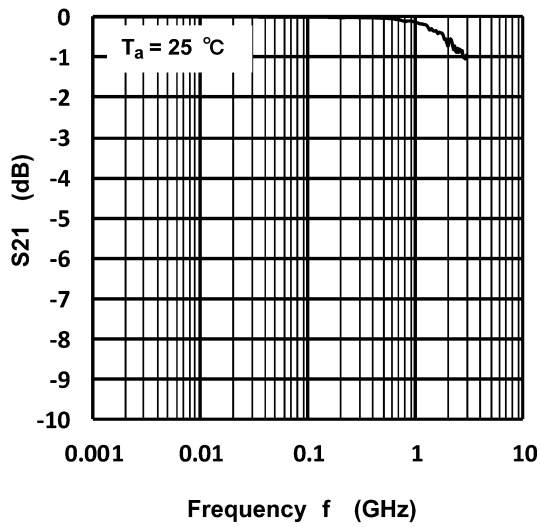
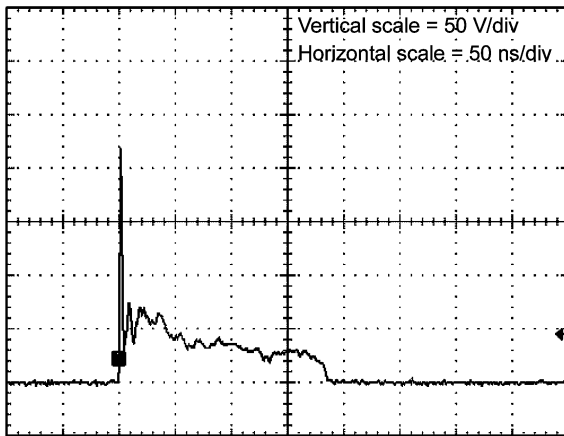


Fig. 10.1 S21 - f
(I/O to GND)

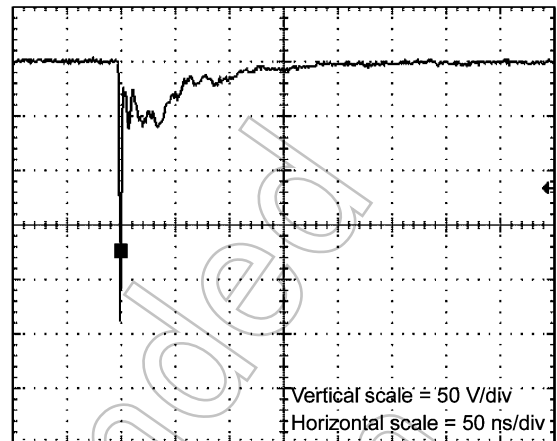
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Not Recommended for New Design

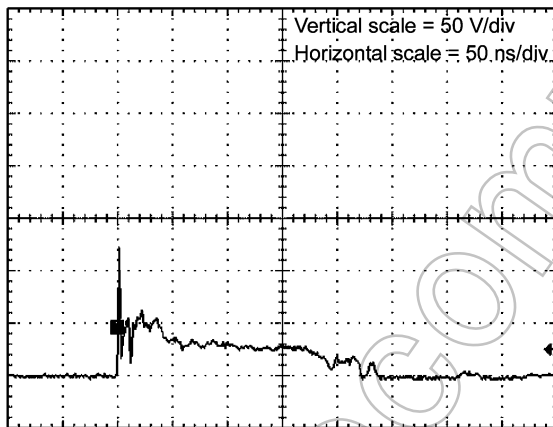
11. ESD Clamp Waveform (Note)



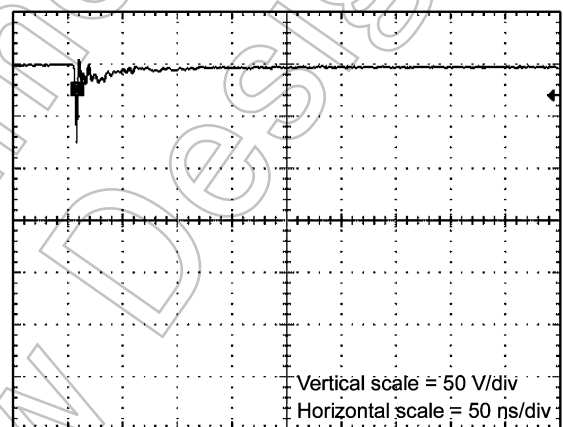
**Fig. 11.1 +8 kV
(I/O to GND)**



**Fig. 11.2 -8 kV
(I/O to GND)**



**Fig. 11.3 +8 kV
(VBUS to GND)**



**Fig. 11.4 -8 kV
(VBUS to GND)**

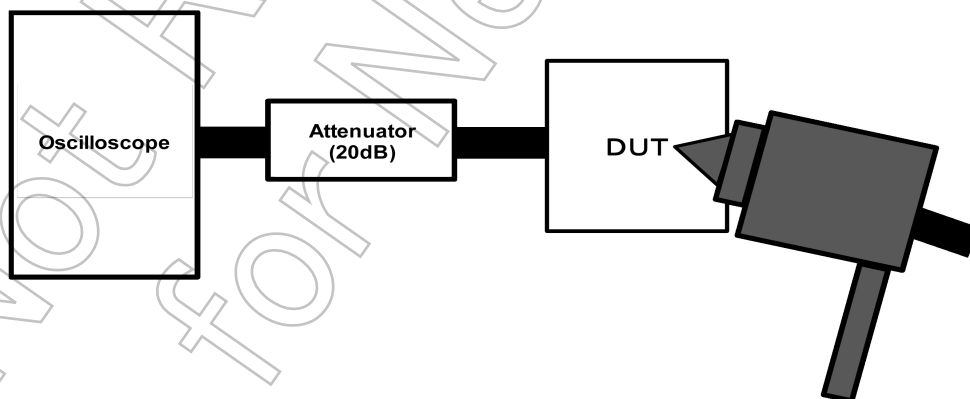
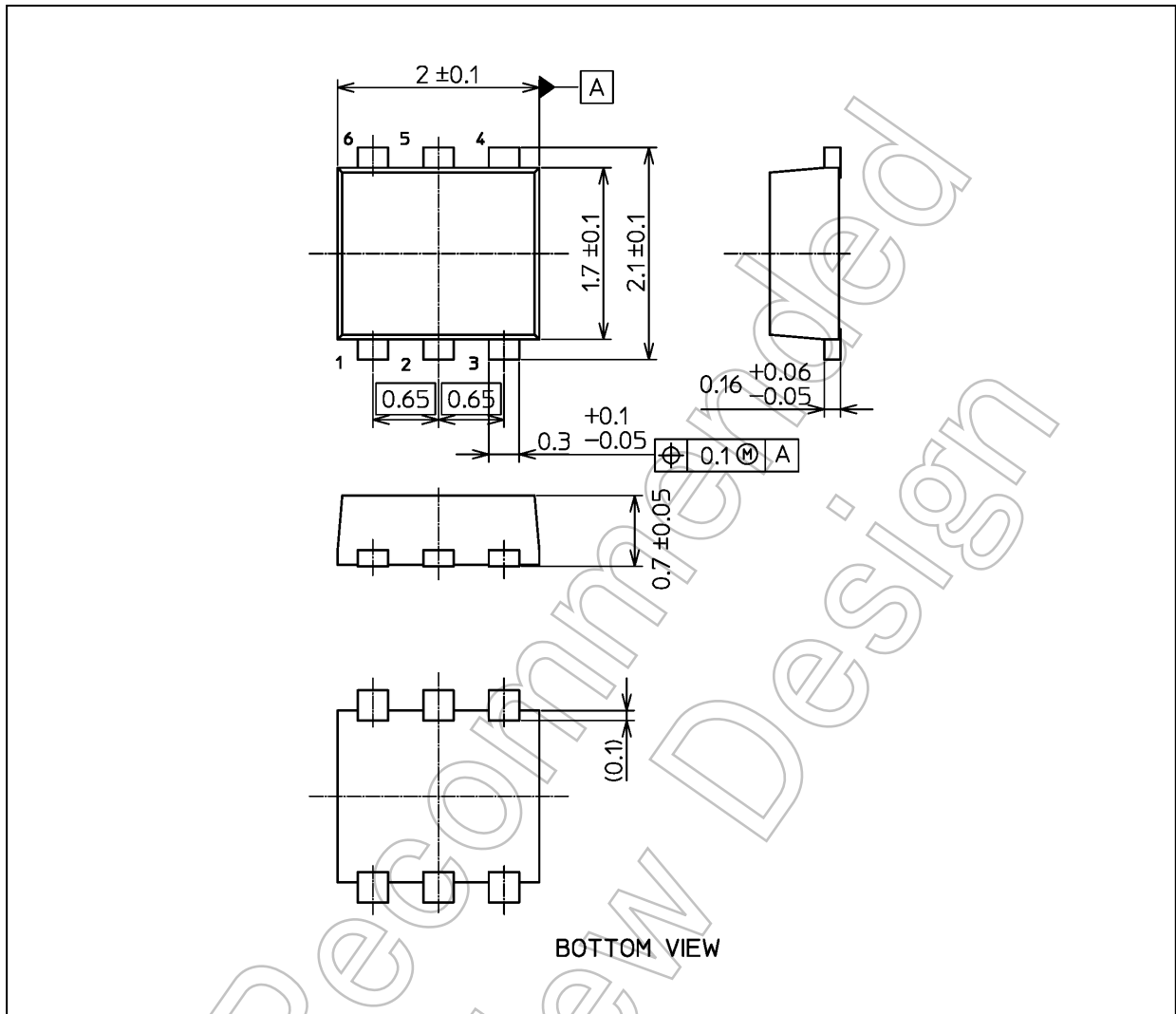


Fig. 11.5 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 7.0 mg (typ.)

Package Name(s)
TOSHIBA: 2-2T1S
Nickname: UF6

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