

ESD Protection Diodes Silicon Epitaxial Planar

DF3D18FU

1. Applications

- ESD Protection

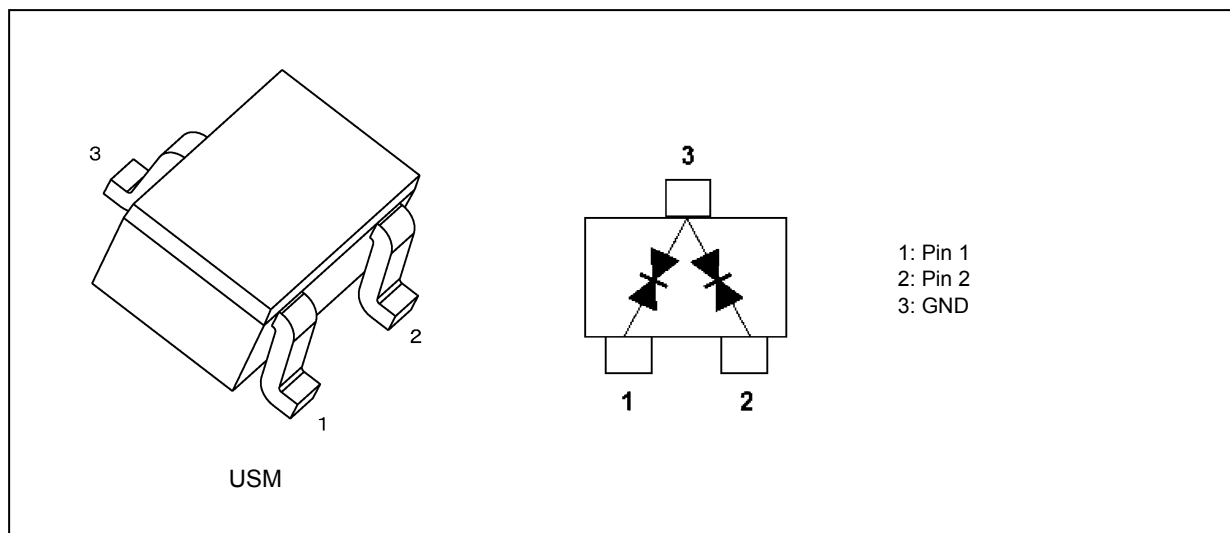
Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

2. Features

- (1) AEC-Q101 qualified (Note 1)

Note 1: For detail information, please contact to our sales.

3. Packaging and Internal Circuit



Start of commercial production
2015-05

4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V_{ESD}	(Note 1)	± 30	kV
Electrostatic discharge voltage(IEC61000-4-2)(Air)				
Electrostatic discharge voltage(ISO10605)(Contact)	V_{ESD}	(Note 2)	± 30	kV
Electrostatic discharge voltage(ISO10605)(Air)				
Peak pulse power	P_{PK}		80	W
Peak pulse current	I_{PP}	(Note 3)	2.5	A
Junction temperature	T_j		150	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to ISO10605. (@ $C = 330\text{ pF}$, $R = 2\text{ k}\Omega$)

Note 3: According to IEC61000-4-5.

5. Electrical Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

V_{RWM} : Working peak reverse voltage
 V_{BR} : Reverse breakdown voltage
 I_{BR} : Reverse breakdown current
 I_R : Reverse current
 V_C : Clamp voltage
 I_{PP} : Peak pulse current
 R_{DYN} : Dynamic resistance

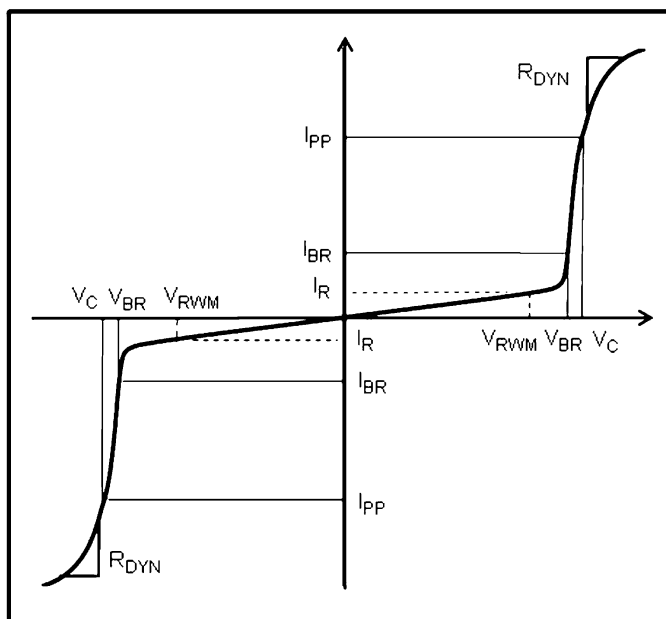


Fig. 5.1 Definitions of Electrical Characteristics

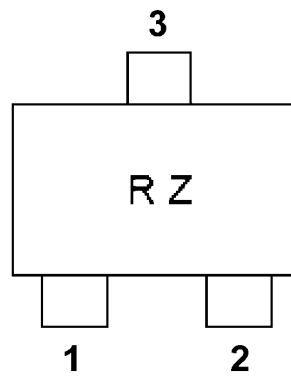
Characteristics	Symbol	Note	Test Condition	Min	Typ.	Max	Unit
Working peak reverse voltage	V_{RWM}		—	—	—	12	V
Reverse breakdown voltage	V_{BR}		$I_{BR} = 1\text{ mA}$	16.2	—	20.5	V
Reverse current	I_R		$V_{RWM} = 12\text{ V}$	—	—	0.1	μA
Clamp voltage	V_C	(Note 1), (Note 3)	$I_{PP} = 1\text{ A}$	—	19	—	V
			$I_{PP} = 2.5\text{ A}$	—	23	33	
Dynamic resistance	R_{DYN}	(Note 2)	—	—	0.8	—	Ω
Total capacitance	C_t		$V_R = 0\text{ V}$, $f = 1\text{ MHz}$	—	9	10	pF

Note 1: Based on IEC61000-4-5 8/20 μs pulse.

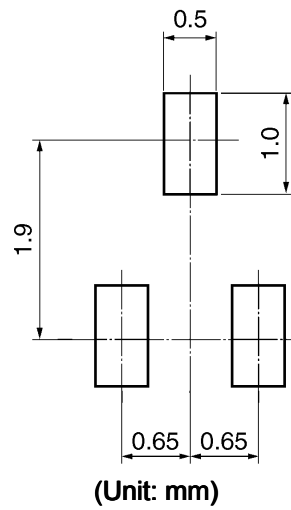
Note 2: TLP parameter: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using a least-squares fit of TLP characteristics at I_{PP} between 8 A to 16 A.

Note 3: Guaranteed by design.

6. Marking



7. Land Pattern Dimensions (for reference only)



8. Characteristics Curves (Note)

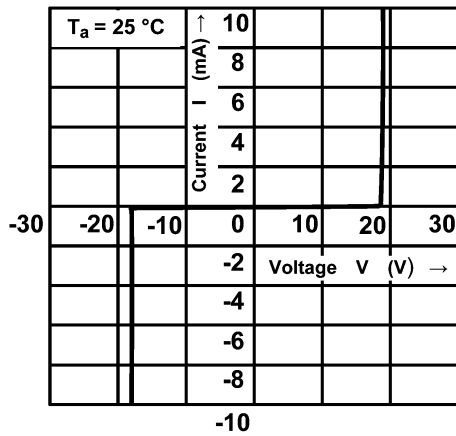


Fig. 8.1 I - V

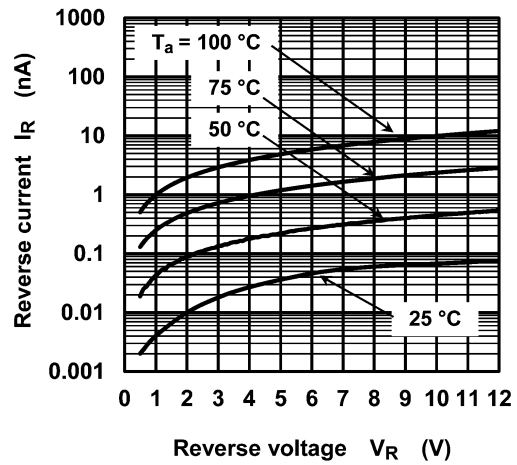


Fig. 8.2 $I_R - V_R$

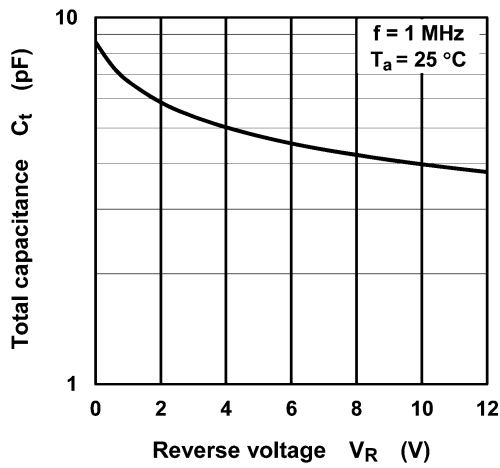


Fig. 8.3 $C_t - V_R$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

9. Clamp Voltage V_C - Peak Pulse Current (I_{PP}) (Note)

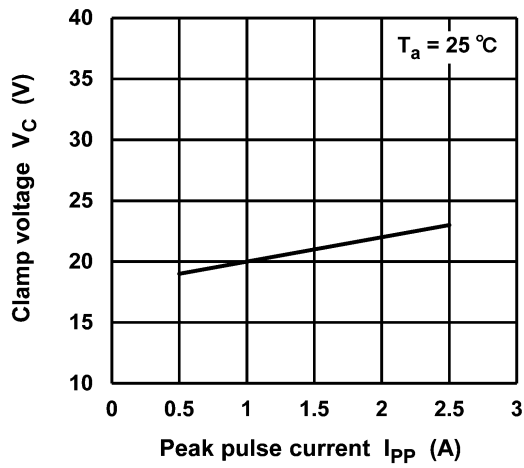


Fig. 9.1 V_C - I_{PP}

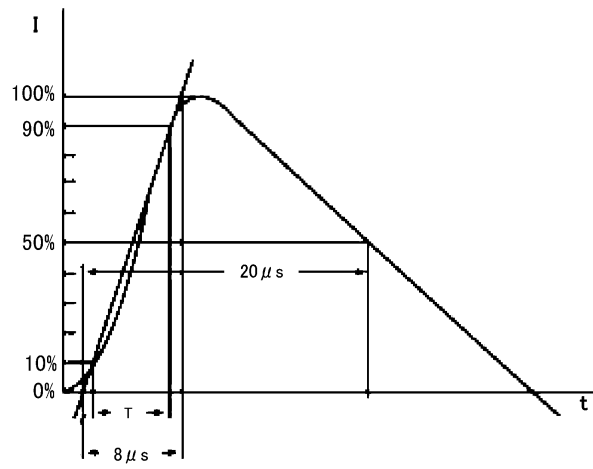
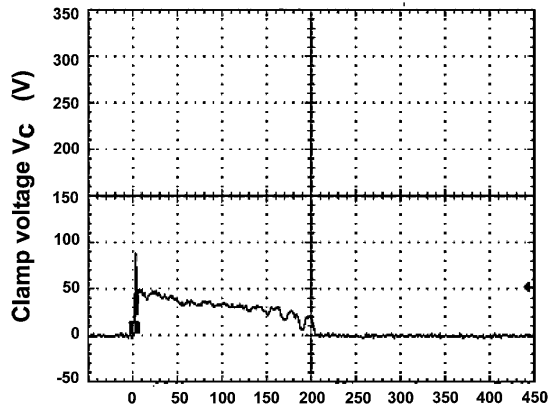


Fig. 9.2 Based on IEC61000-4-5 8/20 μs pulse. (Ed.2)

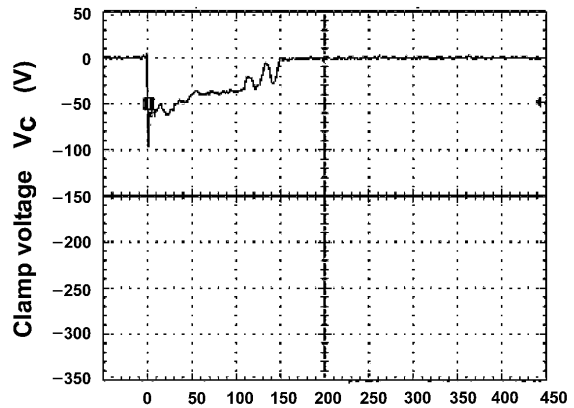
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

10. ESD Clamp Waveform (Note)



Pulse time t_p (ns)

Fig. 10.1 +8 kV



Pulse time t_p (ns)

Fig. 10.2 -8 kV

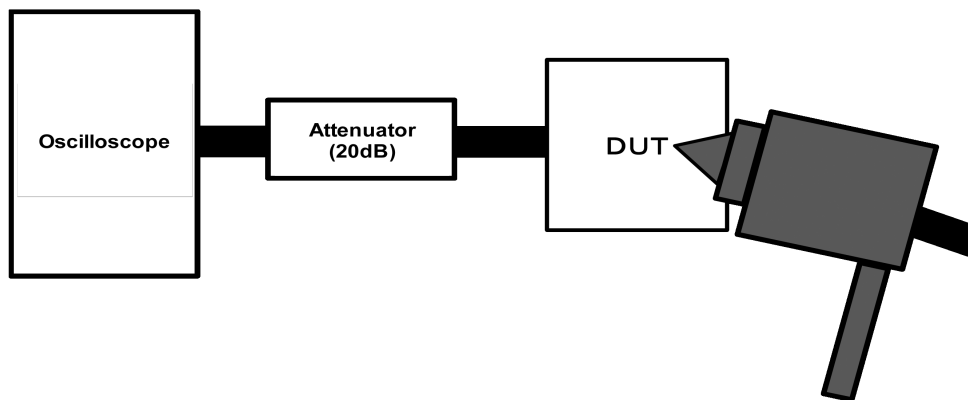


Fig. 10.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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