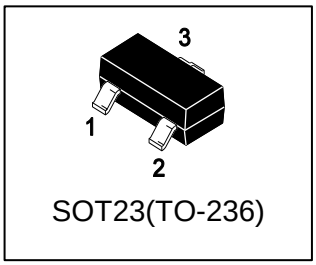
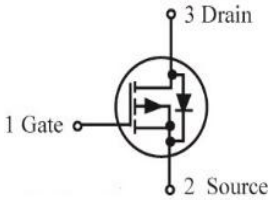
LP3443LT1G
S-LP3443LT1G

20V P-Channel Enhancement-Mode MOSFET



SOT23(TO-236)



1. FEATURES

- VDS = -20V
- RDS(ON)≤70mΩ,@VGS=-4.5V,IDS=-4.7A
- RDS(ON)≤110mΩ,@VGS=-2.5V,IDS=-1.0A
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.
- ESD rating of class 0 (<100V)per Human Body Model

2. APPLICATIONS

- Advanced trench process technology
- High density cell design for ultra low on-resistance.

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3443LT1G	P34	3000/Tape&Reel
LP3443LT3G	P34	10000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	-20	V
Gate–to–Source Voltage – Continuous	VGS	±12	V
Drain Current – Continuous TA = 25°C – Pulsed (Note 1)	 ID IDM	 -4.7 -20	A

5. THERMAL CHARACTERISTICS

Parameter		Symbol	Limits	Unit
Power Dissipation	TA = 25°C	PD	1.1	W
	TA = 75°C		0.7	W
Thermal Resistance, Junction–to–Ambient(Note 2)		RΘJA	110	ºC/W
Junction and Storage temperature		TJ,Tstg	−55~+150	° C

1.Repetitive Rating: Pulse width limited by the maximum junction temperature.

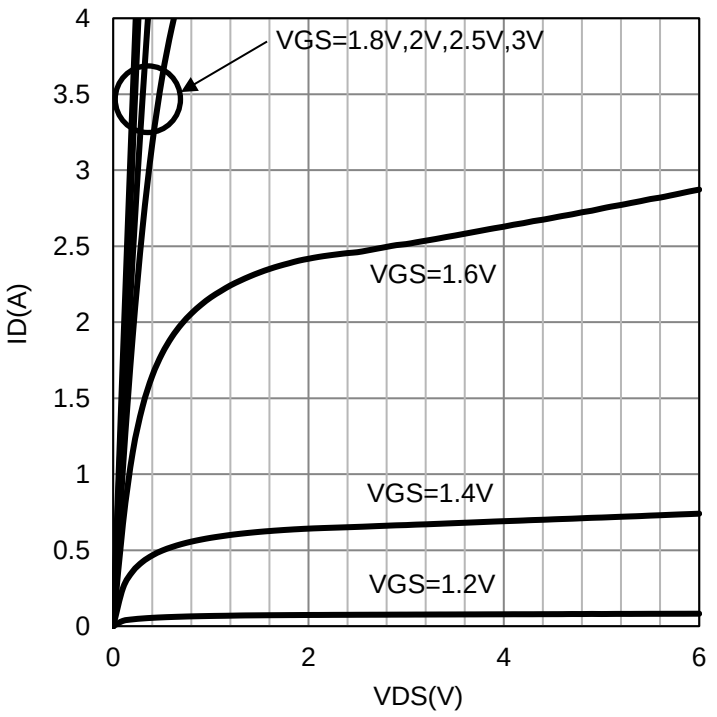
2.1-in² 2oz Cu PCB board.

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

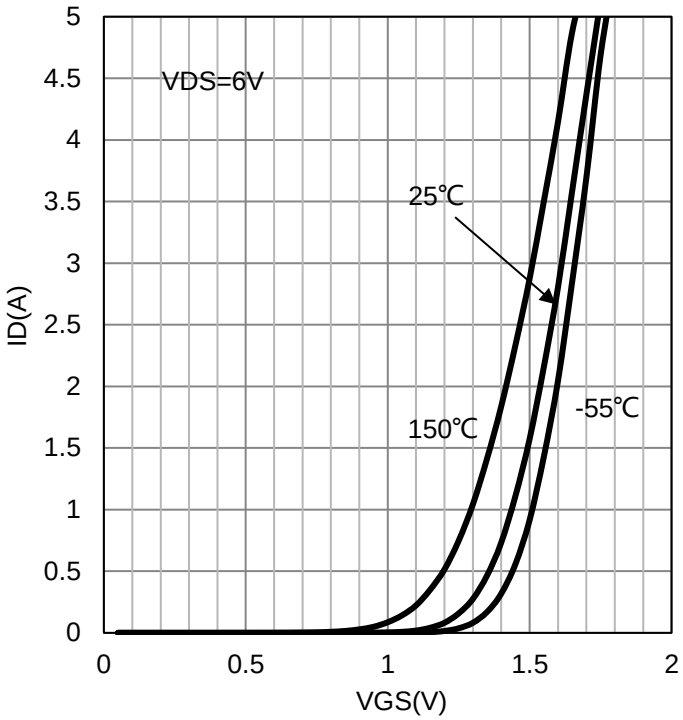
Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)		VBRDSS	-20	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = -250μA)		VGS(th)	-0.6	-0.85	-1.4	V
Zero Gate Voltage Drain Current (VGS = 0, VDS = -20 V)		IDSS	-	-	-1	μA
Gate−to−Source Leakage Current (VDS = 0 V, VGS = ±12 V)		IGSS	-	-	±100	nA
Static Drain–Source On–State Resistance(Note 3)		RDS(on)				mΩ
(VGS = -4.5V, ID = -4.7A)			-	58	70	
(VGS = -2.7V, ID = -3.8A)			-	63	90	
(VGS = -2.5V, ID = -1.0A)			-	75	110	
Diode Forward Voltage (VGS = 0 V, ISD = -1.7 A)		VSD	-	-	-1.2	V
DYNAMIC						
Total Gate Charge@10V	(VDS = -10V, ID = -1.5A)	Qg	-	16.6	-	nC
Total Gate Charge@4.5V		Qg	-	8	-	
Gate−to−Source Gate Charge		Qgs	-	0.9	-	
Gate−to−Drain Charge		Qgd	-	2.7	-	
Turn-On Delay Time	(VDD = -10V, RL =10Ω,ID = −1A, VGEN = -4.5V,RG = 6Ω)	td(on)	-	15.7	-	ns
Rise Time		tr	-	13	-	
Turn-Off Delay Time		td(off)	-	70	-	
Fall Time		tf	-	17.5	-	
Input Capacitance	(f = 200kHz,VDS= -10 V)	Ciss	-	797.3	-	pF
Output Capacitance		Coss	-	88.5	-	
Reverse Transfer Capacitanc		Crss	-	74.8	-	
Forward Transconductance (VDS = -10V, ID = -4.7A)		gfs	-	8	-	S
Body Diode Reverse Recovery Time (IF=-4A,dl/dt=80A/μs)		trr	-	22.15	-	ns
Body Diode Reverse Recovery Charge (IF=-4A,dl/dt=80A/μs)		Qrr	-	6.61	-	nC
Gate-Resistance (VDS = 0 V, VGS = 0 V,f =1MHz)		Rg	-	8.6	-	Ω

3.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

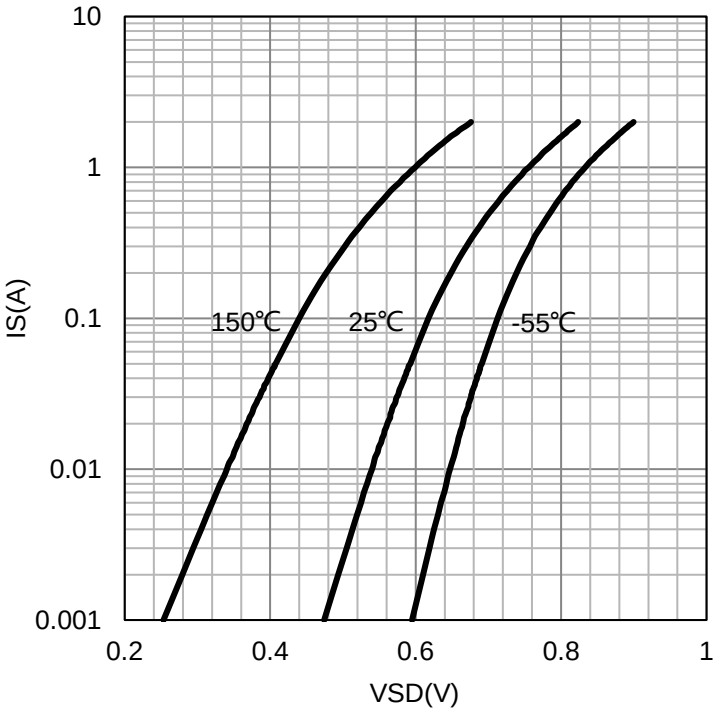
7. ELECTRICAL CHARACTERISTICS CURVES



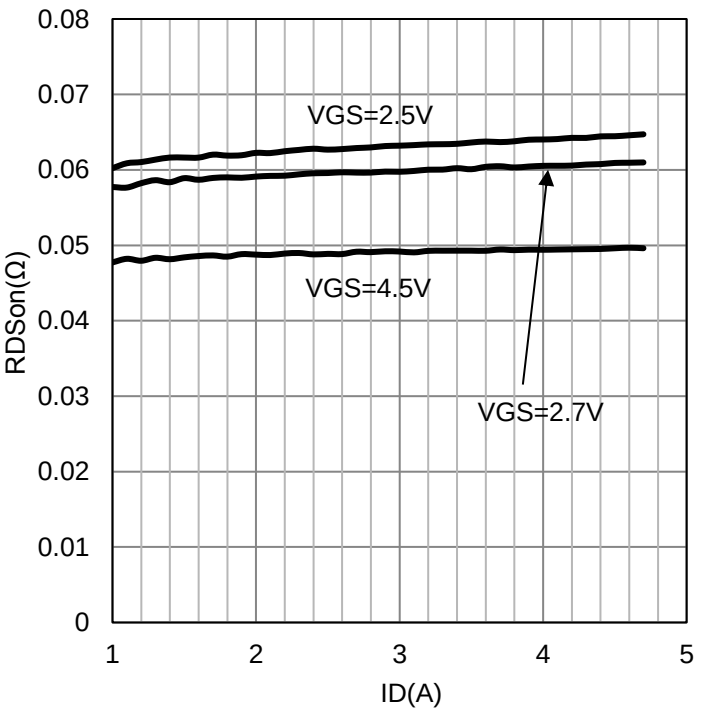
ID vs. VDS



ID vs. VGS

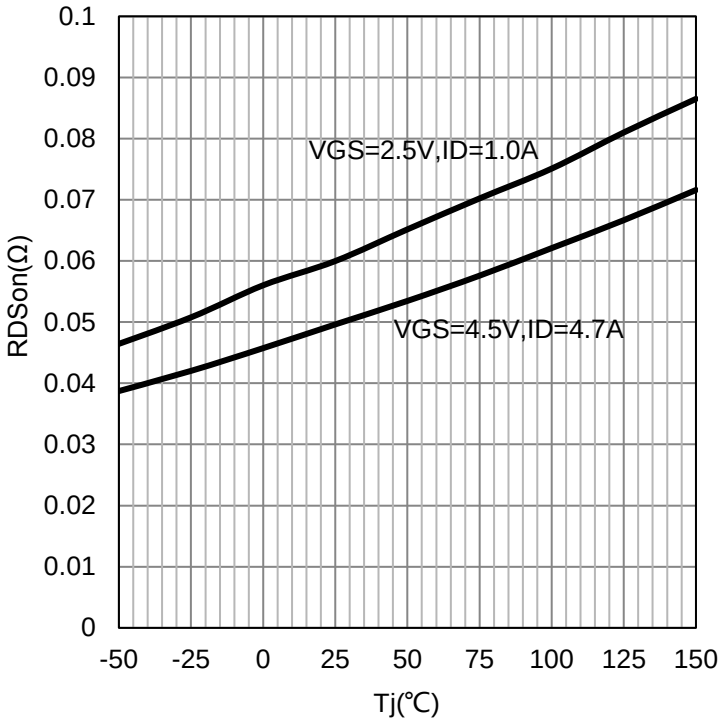


IS vs. VSD

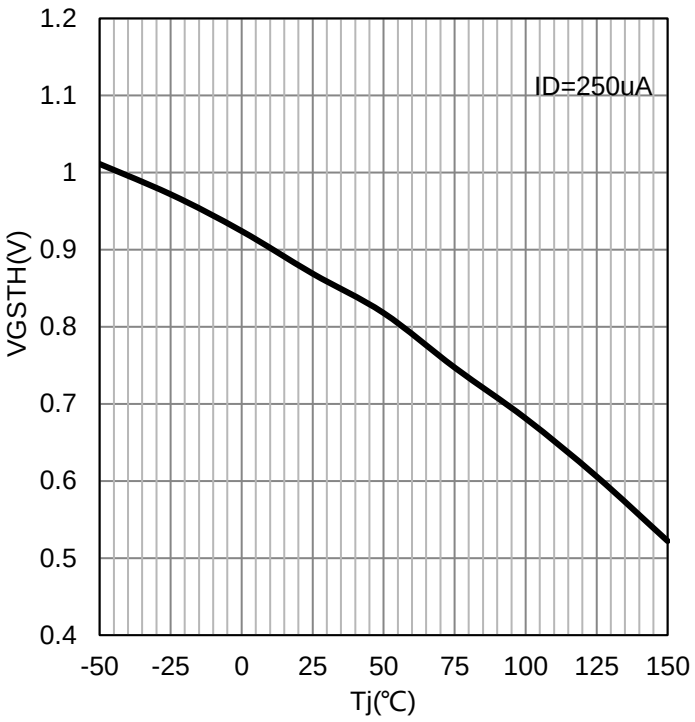


RDS(on) vs. ID

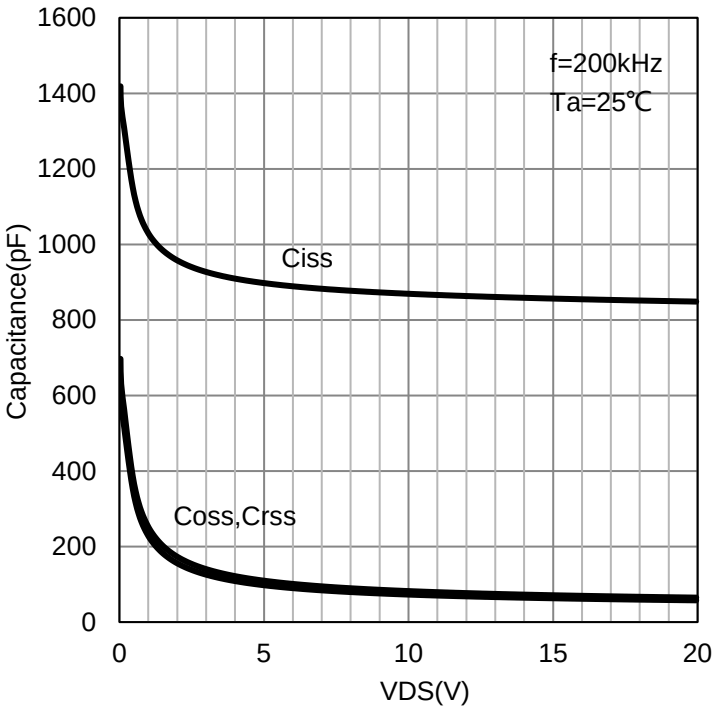
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



RDS(on) vs. Tj

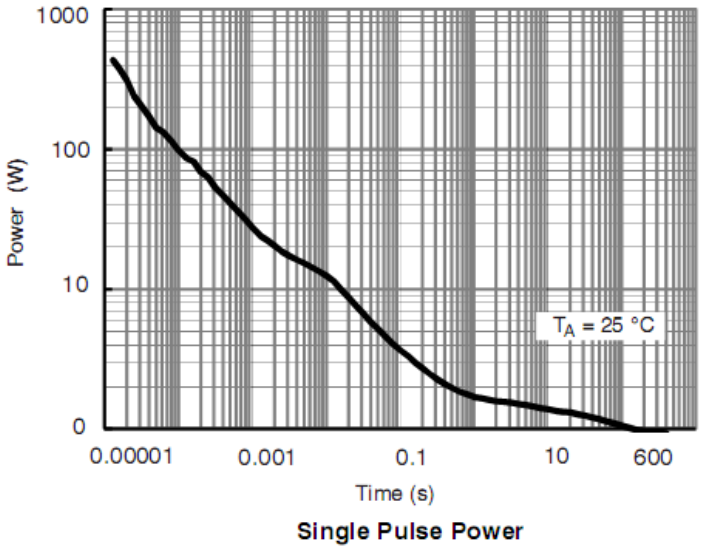


VGSTH vs. Tj

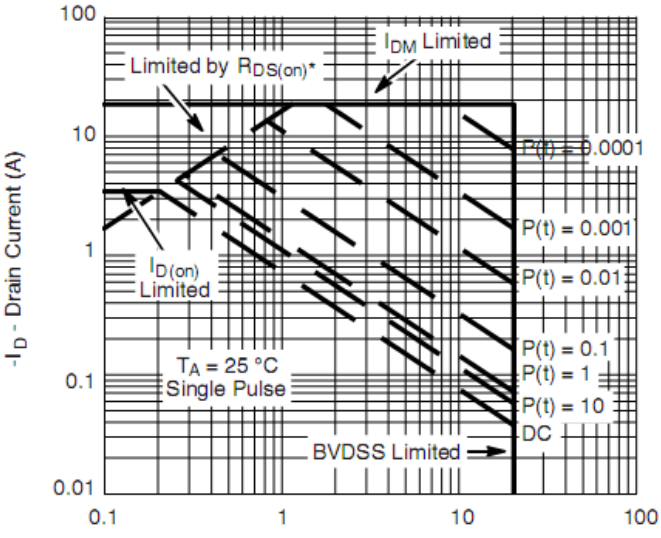


Capacitance

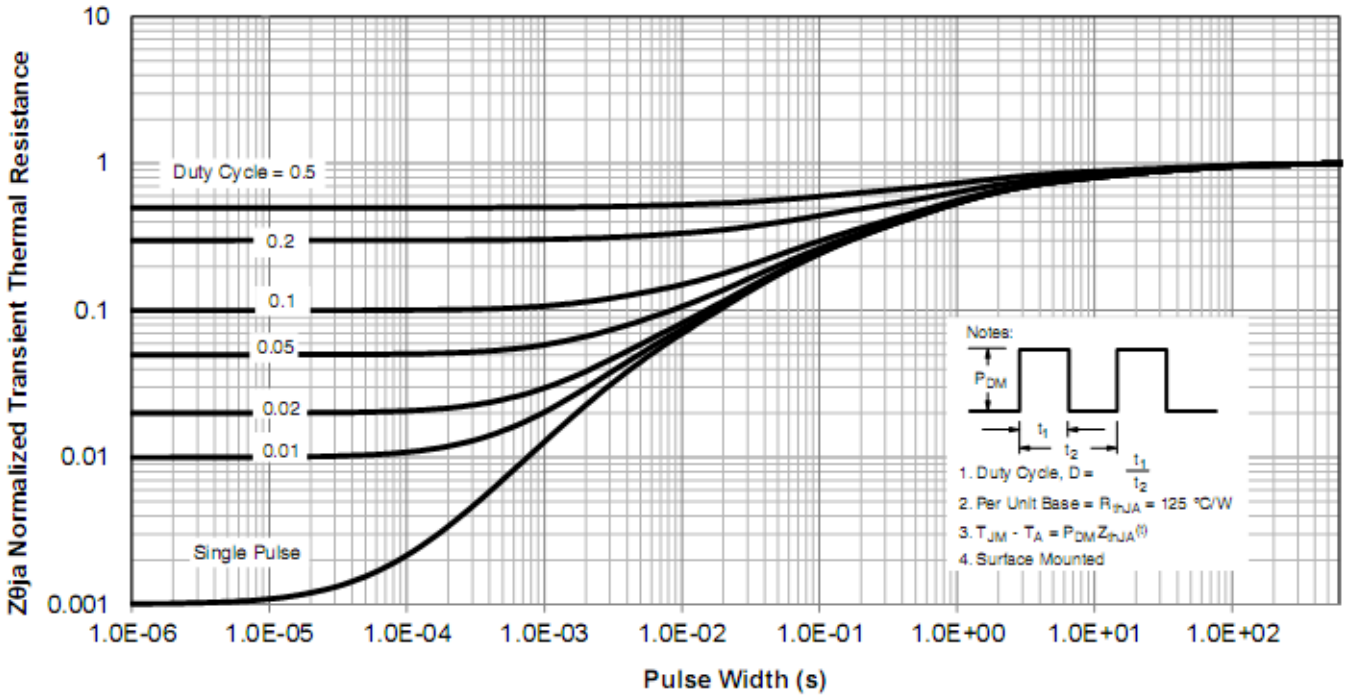
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



Single Pulse Power

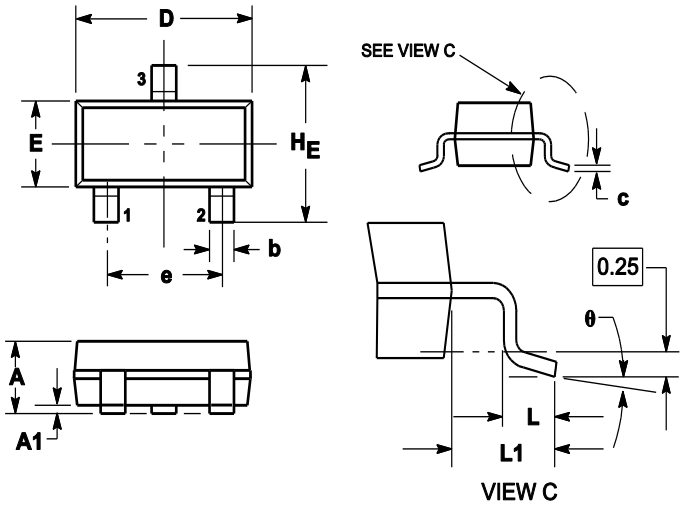


Safe Operating Area



Normalized Maximum Transient Thermal Impedance

8.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT