CW2015CHBD

Low-Cost Fuel Gauge IC with Low-SOC Alert

Features

- System-Side or Pack-Side Fuel Gauging
- 3% Maximum Total SOC Measurement Error
- 14-bit Sigma-Delta ADC for Temperature and Cell Voltage Measurement
- Precision Voltage Measurement
- No Offset Accumulation During Life Time
- No Full-to-Empty Battery Learning Cycles Necessary
- No Sense Resistor Required
- SOC and RRT available
- External Alarm/Interrupt for Low-Battery Warning Available
- Patented “FastCali” gas gauging algorithm
- Calibration After Quick Soft-Reset
- Very Low Active and Sleep Power Consumption
  - Normal mode 15μA
  - Sleep mode <1μA
- General I^2C interface
- Tiny, Lead(Pb)-Free, TDFN Package

Applications

- Smartphone
- Tablet PCs
- Handheld and Portable Applications

General Description

The CW2015 is an ultra-compact, low-cost, host-side/pack-side, sensing resistor free, fuel gauging system IC for Lithium-ion(Li+) based batteries in handheld and portable devices.

CW2015 tracks Li+ battery’s operational condition and uses state-of-art algorithm to report the relative State-of-Charge (SOC) of very different battery chemistry systems (LiCoOx, polymer Li-ion, LiMnOx etc.).

CW2015 includes a 14-bit Sigma-Delta ADC, a precision voltage reference and build-in accurate temperature sensor. The IC allows the end-user to eliminate the expensive sensing resistor which occupies large board area. And the IC also sends out the alarm signal if the battery SOC level reaches pre-programmed threshold.

Quick start function offers the possibility to make an initial estimation of the battery’s SOC, which also enables the IC to be located on system side or pack side, giving the flexibility to system maker on pack selection.

CW2015 uses a 2-wire I^2C compatible serial interface that operates in standard (100 kHz) or fast (400 kHz) mode.

Typical Application

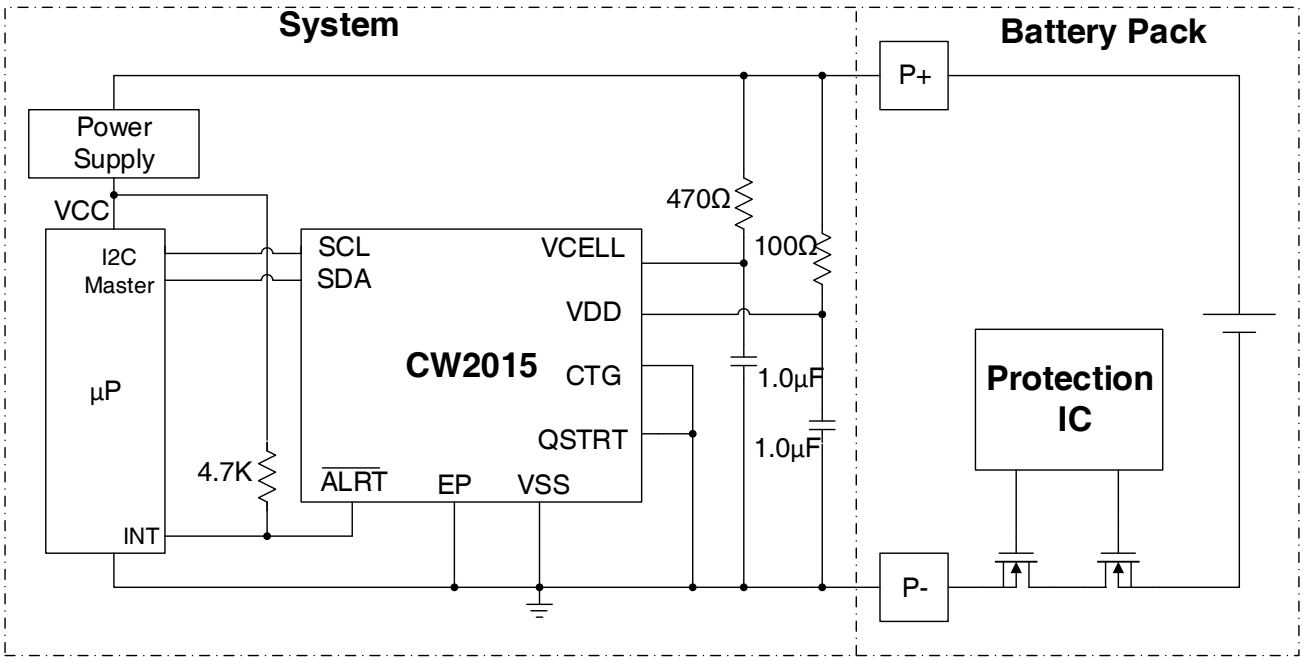


Figure 1. Typical Application Diagram (System Side)

Figure1 is a typical application diagram of CW2015 used in system side, recommended value of the external components is mark on the figure.

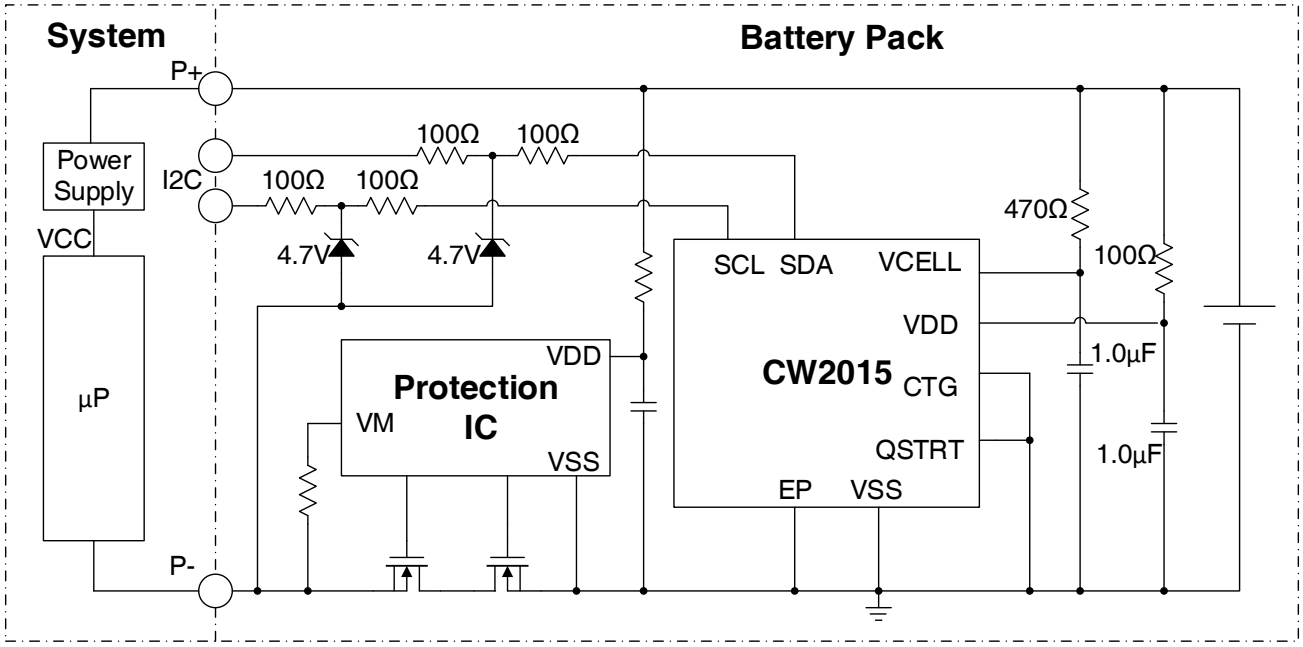


Figure 2. Typical Application Diagram (Pack Side)

Figure 2 is a typical application diagram of CW2015 used in pack side, recommended value of the external components is mark on the figure.

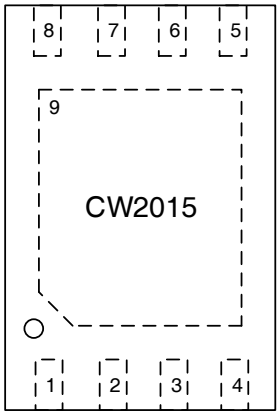
CW2015 can be also used in the 2 batteries connected in series, or several cells connected in parallel. More detailed application information please refers to the application notes or contacts support@cellwise-semi.com for more support.

Ordering Information

PART	OPERATING TEMPERATURE	PACKAGE	TOP MARK
CW2015CHBD	-20ºC to 70ºC	TDFN8	2015CHBD

Pin Configuration

TDFN Package Top view
2mm*3mm – 8pin
(Pad Side Down)

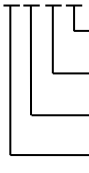


Pin Description

TDFN PIN	NAME	DESCRIPTION
1	CTG	Connect to ground
2	CELL	Battery voltage monitor I/O
3	VDD	System power supply
4	GND	General purpose ground connection
5	$\overline{\text{ALRT}}$	Low SOC alarm signal for MCU interrupt controller
6	QSTRT	Quick start, allows to do a quick SOC estimate
7	SCL	Serial clock input
8	SDA	Serial data Input/output
9	EP	Exposed pad, connect to GND or let floating

Type Number

CW2015XXXX



Package type	D: TDFN8;
Parameter generation	B: Standard firmware and parameter, B version
Embedded Battery profile type	H: Supporting Battery status profile
Function and revision	C: C generation product

Absolute Maximum Ratings

		VALUE		UNITS
		MIN	MAX	
PIN voltage range respect to GND	CTG, CELL, VDD, $\overline{ALRT}$, QSTRT, SCL, SDA to GND	-0.3	6	V
Operation Temperature	T_A	-20	70	°C
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{STG}	-50	150	°C
ESD	All pins. HBM model.		±2	kV
Moisture Sensitivity Level	MSL	Level 3		

Caution:

Stresses beyond "Absolute Maximum Ratings" condition may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

$2.5 \leq V_{DD} \leq 4.5$, T_A= -20 to 70°C, unless otherwise specified.

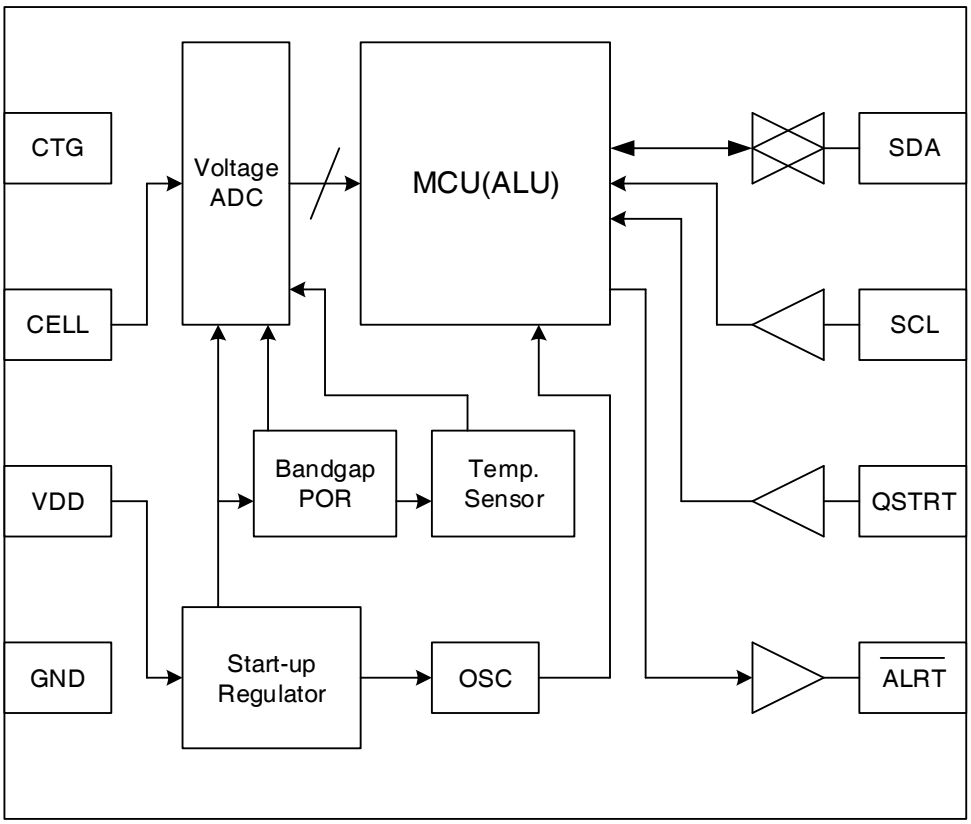
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		+2.5		+4.5	V
Data I/O Pins	SCL, SDA, QSTRT, $\overline{ALRT}$		-0.3		+5.5	V
Analog I/O	CELL, CTG		-0.3		+5.5	V

Electrical Characteristics

$2.5 \leq V_{DD} \leq 4.5$, T_A= -20 to 70°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNITS
Active Current	I_{ACTIVE}	Normal Operation		15	20	μA
Sleep-Mode Current	I_{SLEEP}	$V_{DD} \leq 2.0V$		0.5	1	μA
Time-Based Accuracy	t_{ERR}	V_{DD}=3.7V	-3		3	%
ADC input resistor	R_{ADIN}	$V_{DD}=V_{CELL}$=3.7V	10			MΩ
ADC resolution				14		bits
ADC conversion time	t_{ADCON}	$V_{DD}=V_{CELL}$=3.7V		10		ms
Battery Voltage update time	$t_{VUPDATE}$	$V_{DD}=V_{CELL}$=3.7V		250		ms
Input Logic-High SCL, SDA, QSTRT	V_{IH}	V_{DD}=3.7V	1.4			V
Input Logic-Low SCL, SDA, QSTRT	V_{IL}	V_{DD}=3.7V			0.6	V
Input Hysteresis	V_{IHYS}		0.2			V
Output Logic-Low: SDA, $\overline{ALRT}$	V_{OL}	I_{OL}=4mA		0.2	0.4	V
Pull down current: SDA, $\overline{ALRT}$				4		mA

Function Block Diagram



Detailed Description

Function

CW2015 is an ultra-compact, high precise gas gauging IC that embed new generational battery SOC estimate algorithm.

CW2015 provide the battery voltage, SOC and RRT estimate to user by measuring the cell voltage and temperature.

FastCali algorithm

From battery OCV (open circuits voltage), we deduce the SOC (state of charge) of this battery. Obtains OCV from two ways: idle battery voltage that has been relaxed at least half an hour; battery voltage adds the internal resistor voltage drop when charging or discharging.

Creative “equipment current track” technology precisely calculates the present voltage drop of the internal resistor, combine with the FastCali algorithm, CW2015 promptly infer the OCV value no matter the battery is in charging, relaxing or discharging state.

First SOC Estimate after Power Up

CW2015 considers the battery as a free one that has been relaxed more than 0.5 hours when power up.

CW2015 treats the battery voltage measured by the 14bits ADC as an OCV voltage. According to this voltage, CW2015 deduces the first SOC value.

Error in the first SOC value will be calibrated during the normal use.

RRT

RRT offers the system remaining run time to user for reference. RRT is determined by the present SOC and battery discharging current, i.e. total system power dissipation. Battery remaining capacitor divide the current is the run time. Base on the “equipment current track” technology, CW2015 obtains the discharging current only through measure the battery voltage.

RRT updates all the time and vary according to the present current. Minimum scale of the RRT is 1min.

Quick Start

Quick start allows CW2015 to restart fuel gauge calculations in the same manner as an initial power-up by pull up the quick start pin or set the MODE register [0x0A].

This action used to reduce the large error in the SOC value.

Low SOC Alert

When battery SOC lower than or equal to the setting threshold [0x08], low SOC alert triggered. CW2015 set the ALRT flag to 1, and pull down the ALRT pin to inform the external host. The ALRT pin remains logic-low until the host reset the ALRT flag to logic 0 by I^2C bus.

Cleared ALRT don’t generate another alert signal while the SOC remains below the alert threshold. The SOC must rise above and then fall below or equal to the alert threshold value before another interrupt is generated.

Sleep Mode

All the function will be halt in the sleep mode, power dissipation of CW2015 reduced to the lowest level. Set the MODE register bit Sleep to 11 to enter into the sleep mode. All the data update stop, when recover from sleep mode, SOC algorithm begins from the stop point. When the battery voltage is lower than 2.5V, CW2015 enter into the sleep mode automatically.

POR

Power on reset. Set the MODE register bit POR to 1111 to reset the device, all the registers and date except flash will reset to zero.

Register Map

Below table shows the I²C register map for the CW2015.

Table 1. Register Map

REGISTER NAME	ADDRESS	DESCRIPTION	READ/WRITE	DEFAULT VALUE
VERSION	0x00	Returns IC version, software version	R	0x73
VCELL	0x02-0x03	Reports 14-bit A/D measurement of battery voltage	R	0x00
SOC	0x04-0x05	Reports 16-bit SOC result calculated	R	0x00
RRT_Alert	0x06-0x07	13 bits remaining run time and low SOC alert bit	W/R	0x00
CONFIG	0x08	Configure register, alert threshold set	W/R	0x18
MODE	0x0A	Special command for IC state	W/R	0xC0

VCELL Register(0x02~0x03)

The VCELL register is a read-only register that updates continuously the battery terminal voltage. Battery voltage is measured at the CELL pin with GND pin as a ground reference. A 14bit sigma-delta A/D converter is used and the voltage resolution is 305uV for CW2015. This A/D converter updates the cell voltage for a period of <10ms after IC POR and then four times a second afterwards.

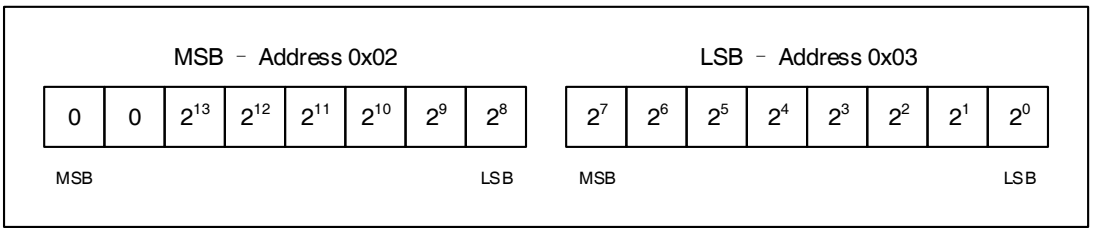


Figure 3. VCELL Register Format

SOC Register(0x04~0x05)

The SOC register is also a read-only register that indicates the State-of-Charge of the battery cell. SOC value is a relative concept which display as a percentage of the cell's total capacity. This register intrinsically adjusts itself to the change of battery cell's parameter due to aging, poor cell parameter distribution control or rapid change in total capacity.

In this register, the high 8bit part contains the SOC information in % units which can be directly used by end user if this accuracy is already good enough for application. The low 8bit part provides more accurate part of the SOC information until 1/256%.

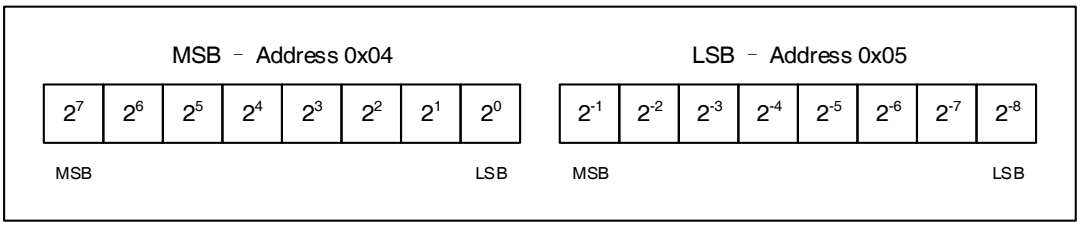


Figure 4. SOC Register Format

RRT_ALRT Register(0x06~0x07)

ALRT, Flag register bit. This bit is set by the IC when the SOC register value falls below or equal to the alert threshold setting and an interrupt is generated. This bit can only be cleared by the host through I²C bus. The power-up default value for ALRT is logic 0.

The read-only register RRT indicates the remaining run time (RRT) of the battery according to the present SOC and the discharge current. RRT is not a linear variation value, and updates once per second.

Register RRT provides 13 bits to record the remaining time, and 1 LSB represents one minute.

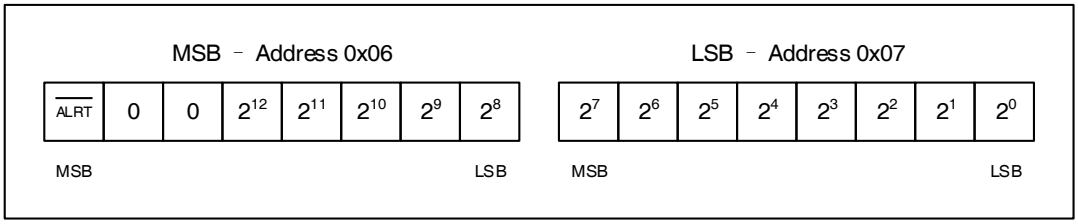


Figure 5. RRT_ALRT Register Format

CONFIG Register(0x08)

ATHD is low SOC alert threshold setting register. The alert threshold is a 5-bit value that sets the state of charge level where an interrupt is generated on the ALRT pin. The alert threshold has an LSB weight of 1% and can be programmed from 0% up to 31%. The power-up default value for ATHD is 3%.

UFG is a flag bit used to indicator the battery information update state.

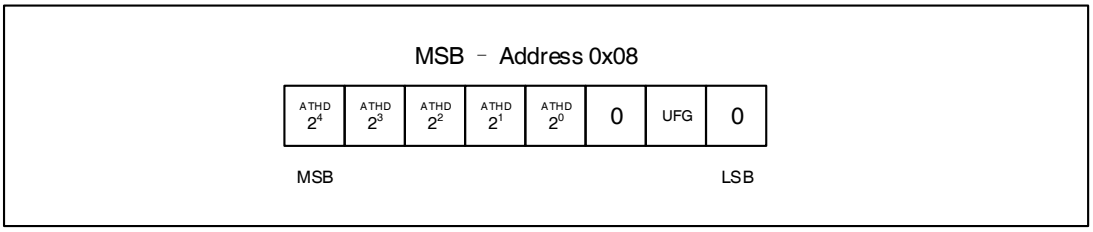


Figure 6. CONFIG Register Format

MODE Register(0x0A)

Mode register is used for Master to control the IC.

Sleep mode, two bits to control. Default value 11, write 11 to force the CW2015 enter the sleep mode; write 00 to wake up.

QSTRT, quick start, two bits to control. Default value 00, write 11 to start.

Quick-start allows the IC to restart fuel-gauge calculations in the same manner as initial power-up of the IC. For example, if an application's power-up sequence is exceedingly noisy such that excess error is introduced into the IC's "first guess" of SOC, the host can issue a quick-start to reduce the error. A quick-start is also initiated by a rising edge on the QSTRT pin.

POR, power of reset, four bits to control. Default value 0000, write 1111 to completely restart the IC as if power removed.

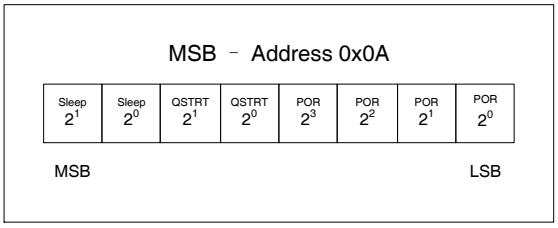


Figure 7. MODE Register Format

I²C Interface

The CW2015 communicates through an I²C interface. I²C is a two-wire open-drain interface supporting multiple devices and masters on a single bus. Some I²C devices can act as masters or slaves, but the CW2015 can only act as a slave device that only pull the bus wires LOW and never drive the bus HIGH. Data on the I²C-bus can be transferred at rates of up to 100kbps in standard mode. I2C fast mode (400kbps) or fast mode plus (1 Mbps) are also supported.

Device Address

I²C device address is consisted of 7bits slave address and 1 read/write control bit.

ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R/W

Figure 8. I2C address structure

Address of CW2015 is fixed on 0b1100010. Combine with de R/W bit:
Read command of CW2015 is 0xC5;
Write command of CW2015 is 0xC4.

START and STOP Conditions

When the bus is idle, both SCL and SDA must be HIGH. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from HIGH to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Read and Write Command

Figure 9 shows an overview of the read and write command on the I²C bus.

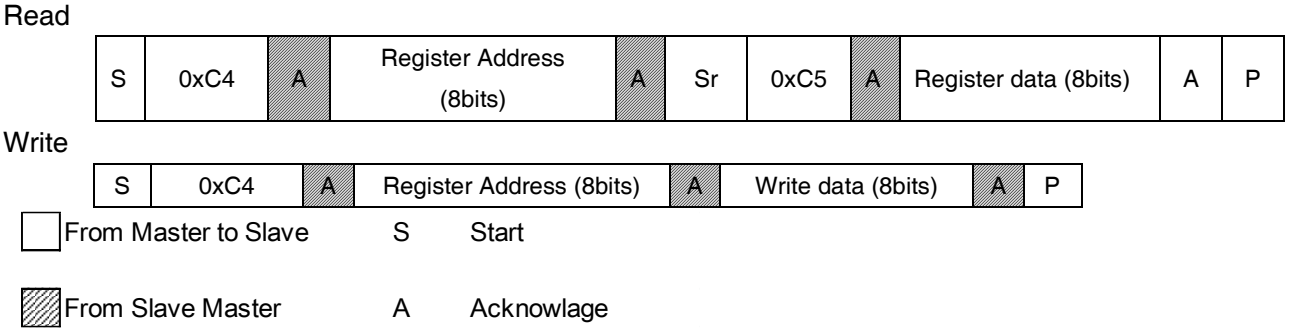
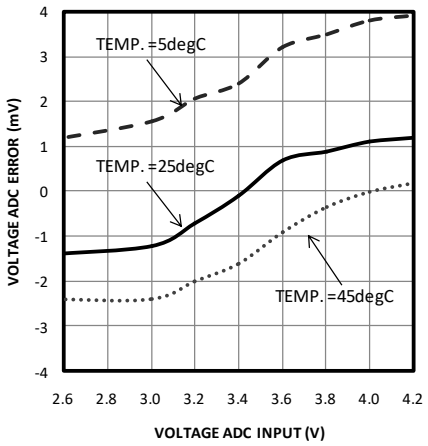


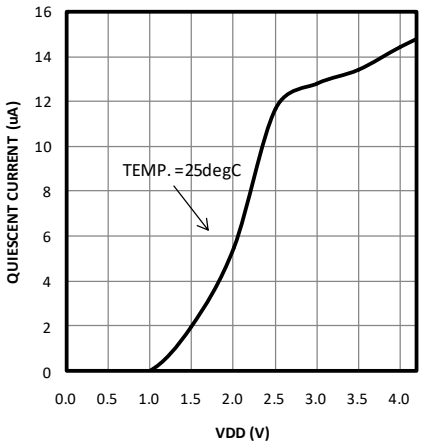
Figure 9. Read and Write Command

Typical Operation Parameter

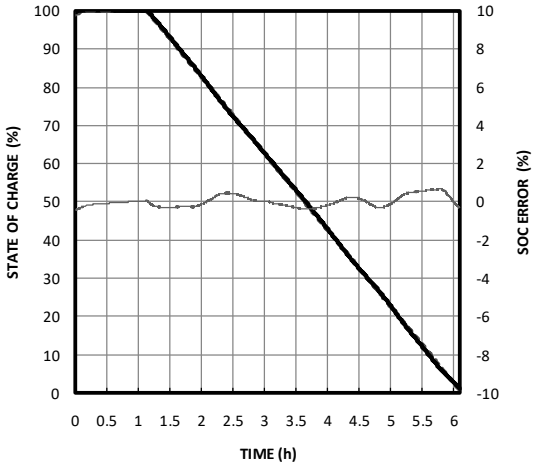
CW2015 VOLTAGE ADC ERROR vs. TEMPERATURE



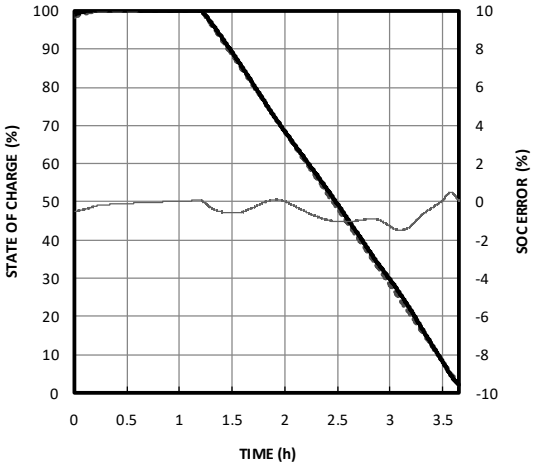
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



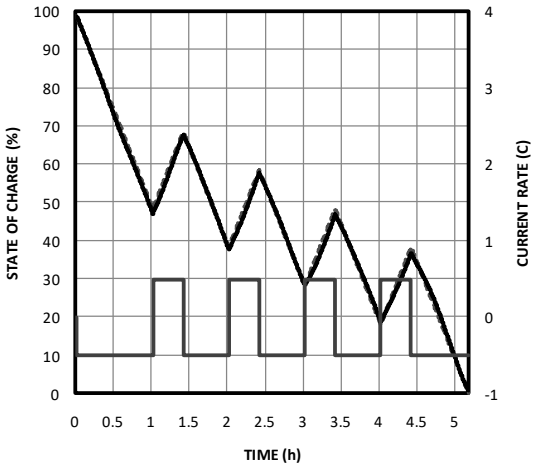
SIMPLE C/5 RATE DISCHARGE SOC ACCURACY



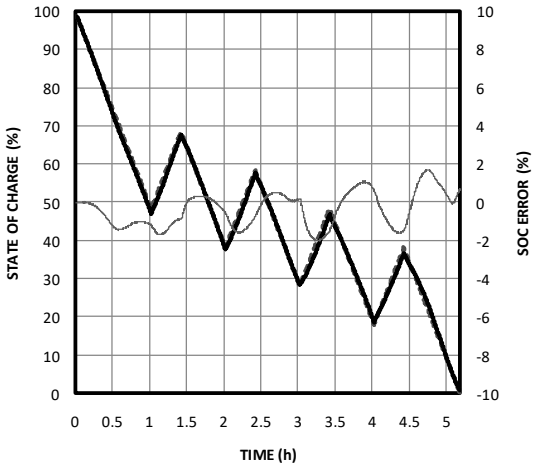
SIMPLE C/2 RATE DISCHARGE SOC ACCURACY



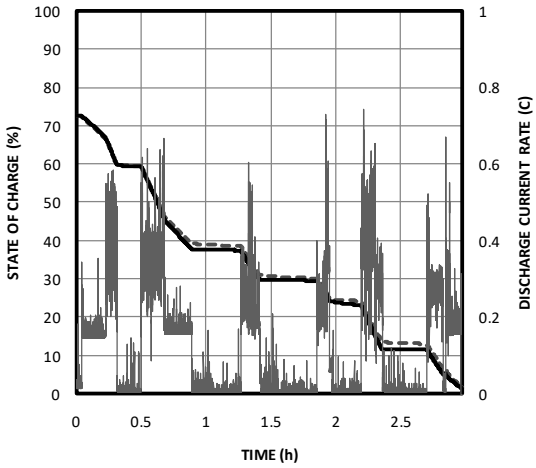
C/2 RATE ZIGZAG PATTERN SOC ACCURACY 1



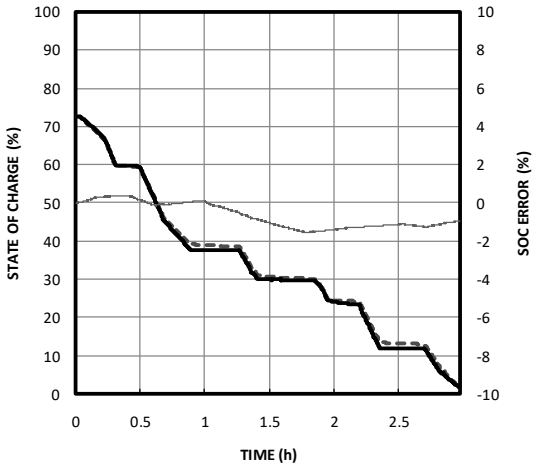
C/2 RATE ZIGZAG PATTERN SOC ACCURACY 2



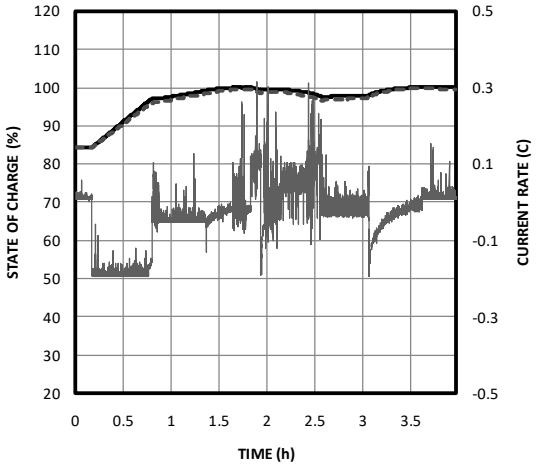
REAL APPLICATION/DISCHARGE SOC ACCURACY 1



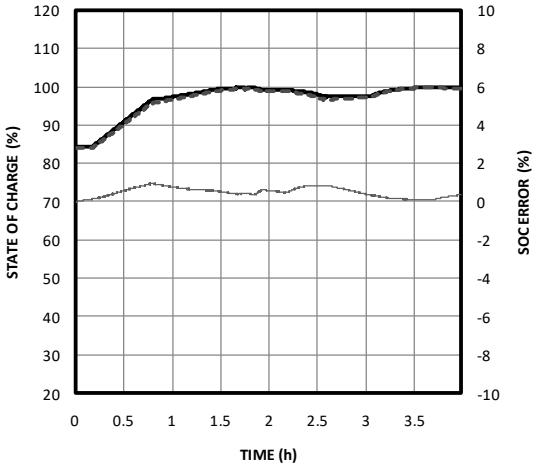
REAL APPLICATION/DISCHARGE SOC ACCURACY 2



REAL APPLICATION UNDER CV MODE SOC ACCURACY 1

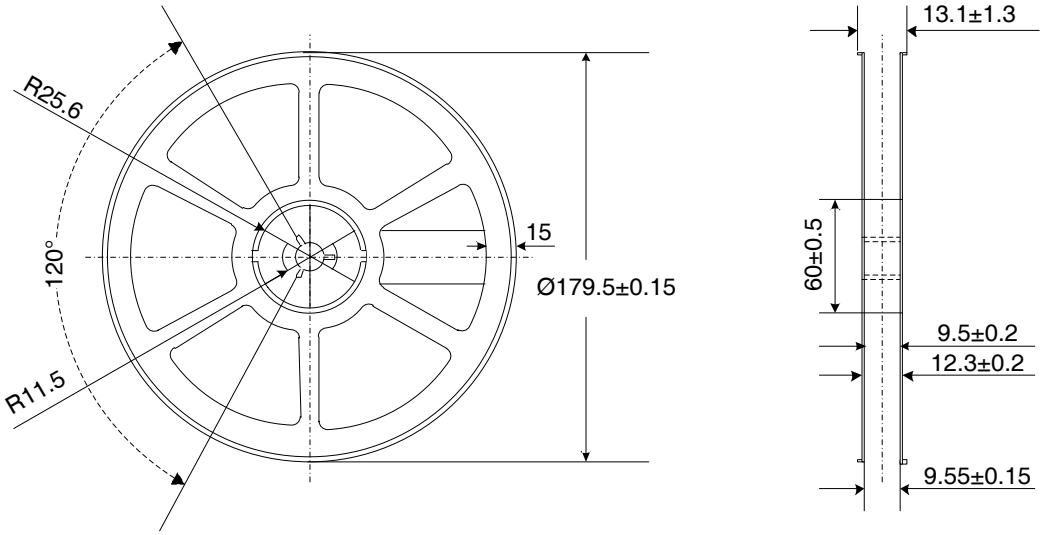


REAL APPLICATION UNDER CV MODE SOC ACCURACY 2



Tape and Reel Information

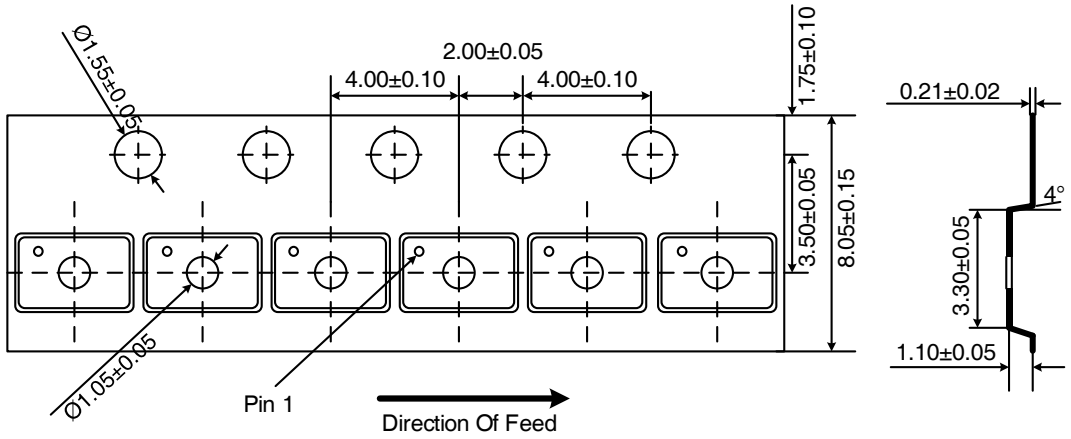
TDFN Package Reel Information



Color: Blue

All DIM in mm

TDFN Package Tape Information



Carrier Tape Color: Black

Cover Tape Width: 5.30±0.10

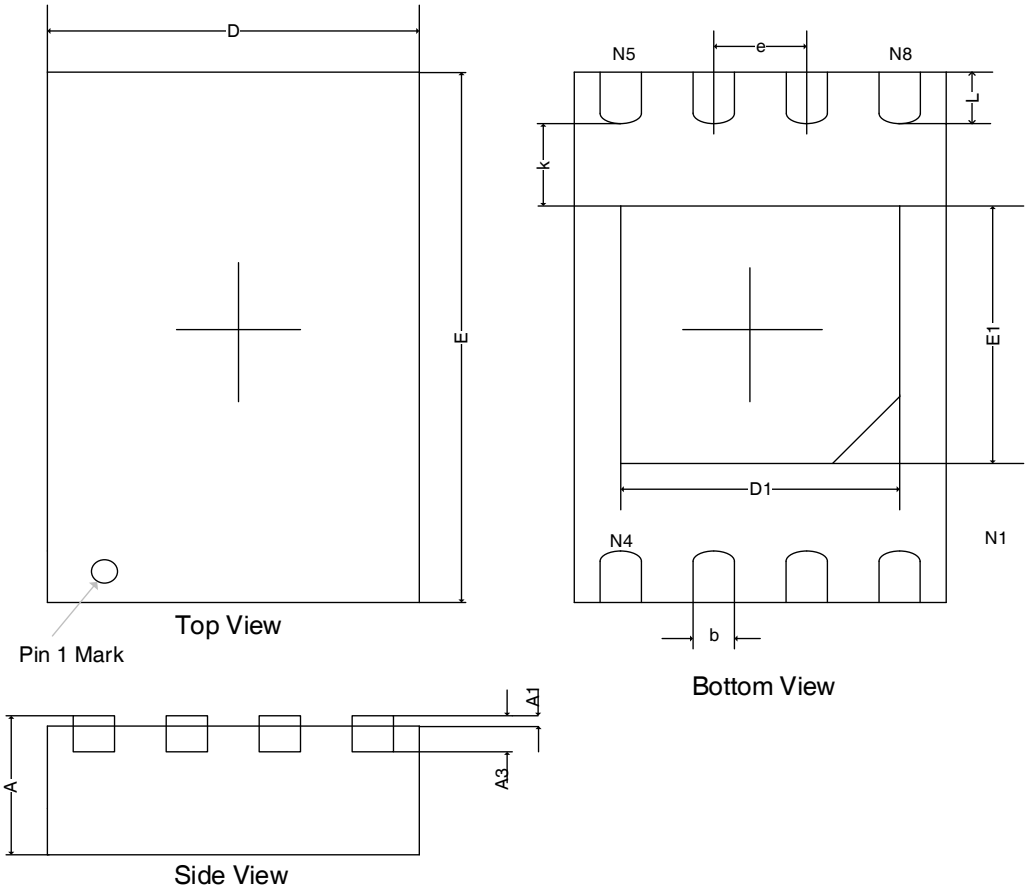
Cover Tape Color: Transparent

All DIM in mm

All the package materials are Pb free and Halogen free.

Package Information

TDFN 2x3-8L(P0.50T0.75/0.85) PACKAGE OUTLINE DIMENSIONS



SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
K	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

Revision History

DATE	VERSION	CHANGED ITEM	WRITTEN BY	APPROVED BY
2017-08-01	1.0	Initial Release	Ark	Jun
2018-01-19	1.1	Add MSL rating on page 4	Richard	Jun
2018-06-29	1.2	Update register default value	Richard	Jun

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.