NTGS3446

Power MOSFET 20 V, 5.1 A Single N-Channel, TSOP6

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} Specified at Elevated Temperature
- Pb−Free Package is Available

Applications

- Power Management in portable and battery−powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	20	V
Gate−to−Source Voltage	V_{GS}	±12	V
Thermal Resistance Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 244 0.5 2.5 10	 °C/W W A A
Thermal Resistance Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 128 1.0 3.6 14	 °C/W W A A
Thermal Resistance Junction−to−Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Drain Current − Continuous @ T_A = 25°C − Pulsed Drain Current (t_p < 10 μs)	 $R_{\theta JA}$ P_d I_D I_{DM}	 62.5 2.0 5.1 20	 °C/W W A A
Source Current (Body Diode)	I_S	5.1	A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Minimum FR−4 or G−10PCB, operating to steady state.
2. Mounted onto a 2" square FR−4 board (1" sq. 2 oz. cu. 0.06" thick single−sided), operating to steady state.
3. Mounted onto a 2" square FR−4 board (1" sq. 2 oz. cu. 0.06" thick single−sided), t < 5.0 seconds.

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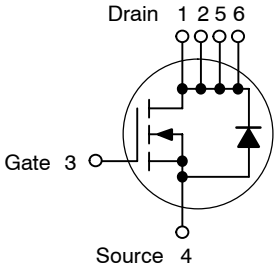
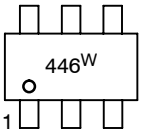
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	36 mΩ @ 4.5 V	5.1 A

N−Channel



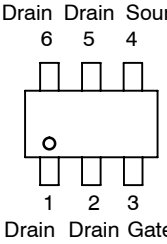
MARKING DIAGRAM

TSOP−6
CASE 318G
STYLE 1



446 = Device Code
W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS3446T1	TSOP−6	3000/Tape & Reel
NTGS3446T1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	20 –	– 22	– –	Vdc mV/°C
Zero Gate Voltage Collector Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 85°C)		I_{DSS}	 – –	 – –	 1.0 25	μAdc
Gate−Body Leakage Current (V_{GS} = ±12 Vdc, V_{DS} = 0)		$I_{GSS(f)}$ $I_{GSS(r)}$	– –	– –	100 −100	nAdc
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage I_D = 0.25 mA, V_{DS} = V_{GS} Temperature Coefficient (Negative)		$V_{GS(th)}$	0.6 –	0.85 −2.5	1.2 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (V_{GS} = 4.5 Vdc, I_D = 5.1 Adc) (V_{GS} = 2.5 Vdc, I_D = 4.4 Adc)		$R_{DS(on)}$	 – –	 36 44	 45 55	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 5.1 Adc)		g_{FS}	–	12	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	510	750	pF
Output Capacitance		C_{oss}	–	200	350	
Transfer Capacitance		C_{rss}	–	60	100	
SWITCHING CHARACTERISTICS (Note 5)						
Turn−On Delay Time	(V_{DD} = 10 Vdc, I_D = 1.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	9.0	16	ns
Rise Time		t_r	–	12	20	
Turn−Off Delay Time		$t_{d(off)}$	–	35	60	
Fall Time		t_f	–	20	35	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 5.1 Adc, V_{GS} = 4.5 Vdc)	Q_T	–	8.0	15	nC
		Q_{gs}	–	2.0	–	
		Q_{gd}	–	2.0	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage (Note 4)	(I_S = 1.7 Adc, V_{GS} = 0 Vdc) (I_S = 1.7 Adc, V_{GS} = 0 Vdc, T_J = 85°C)	V_{SD}	 –	0.74 0.66	1.1 –	Vdc
Reverse Recovery Time	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, di_S/dt = 100 A/μs)	t_{rr}	–	20	–	ns
		t_a	–	11	–	
		t_b	–	9.0	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.01	–	μC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

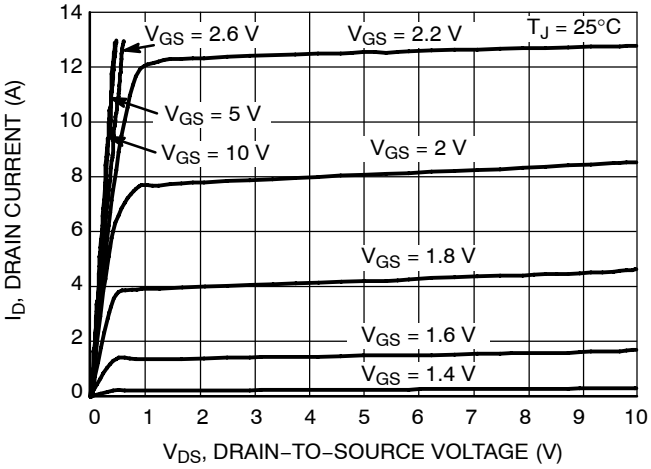


Figure 1. On−Region Characteristics

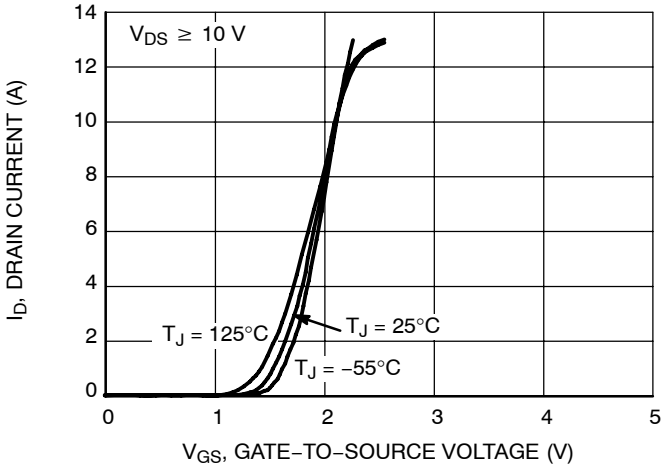


Figure 2. Transfer Characteristics

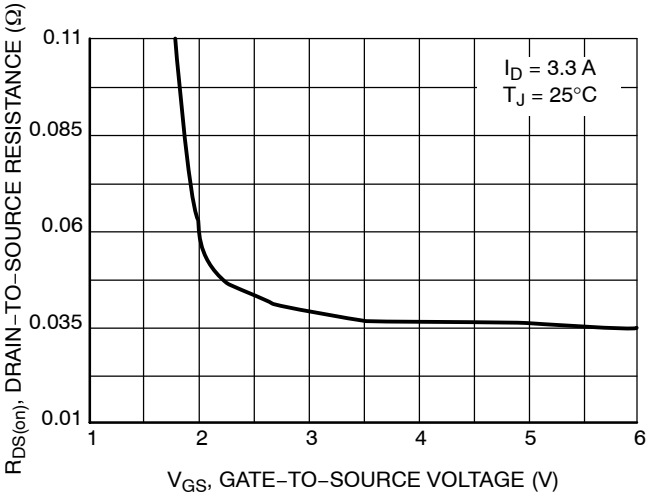


Figure 3. On−Resistance versus Gate−To−Source Voltage

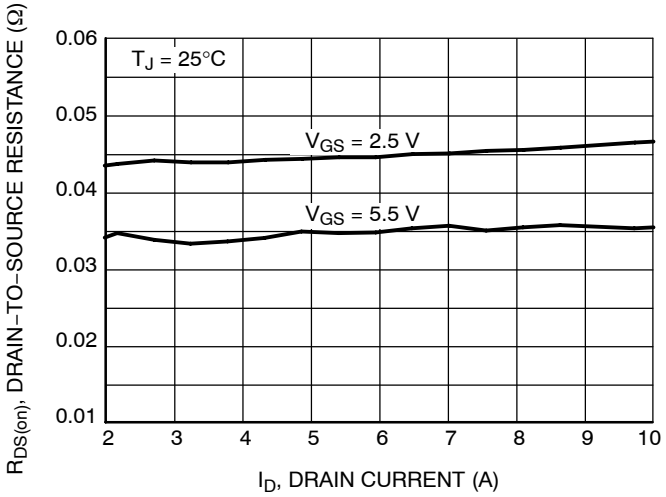


Figure 4. On−Resistance versus Drain Current and Gate Voltage

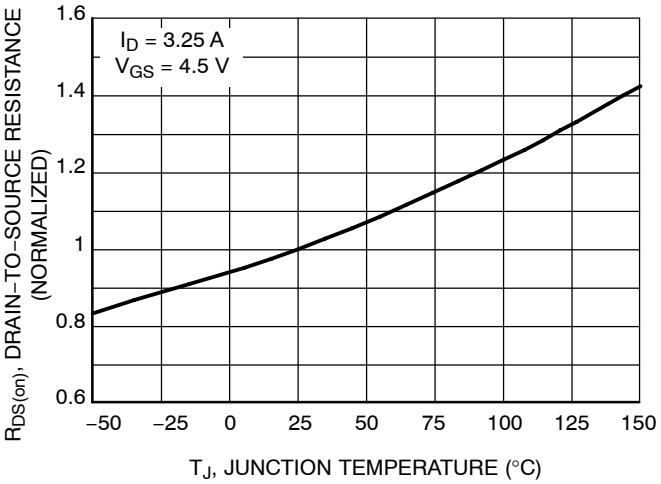


Figure 5. On−Resistance Variation with Temperature

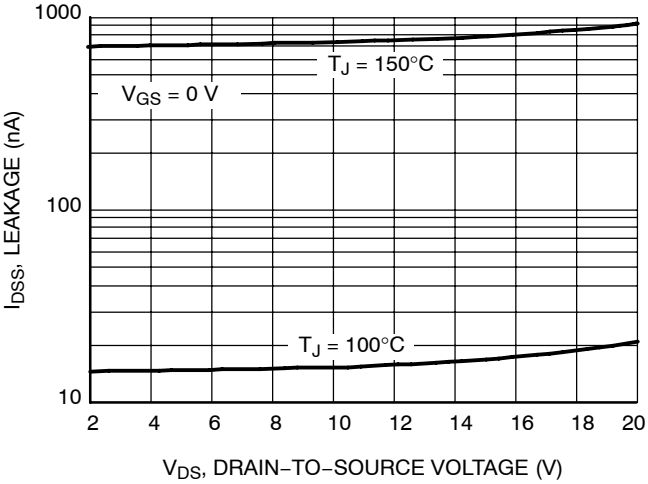


Figure 6. Drain−to−Source Leakage Current versus Voltage

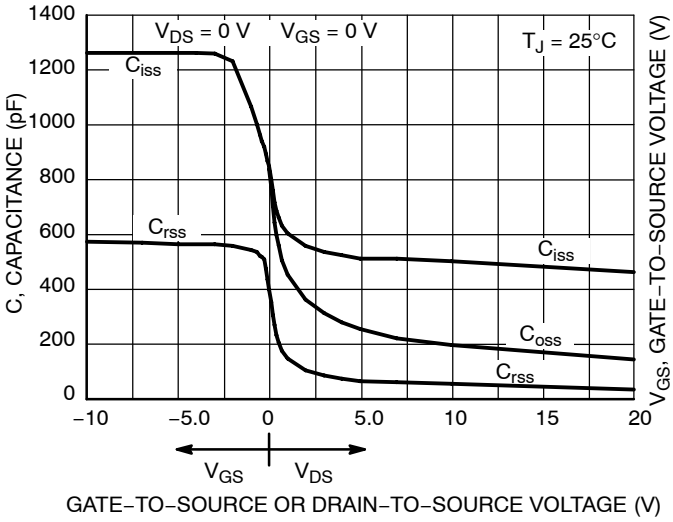


Figure 7. Capacitance Variation

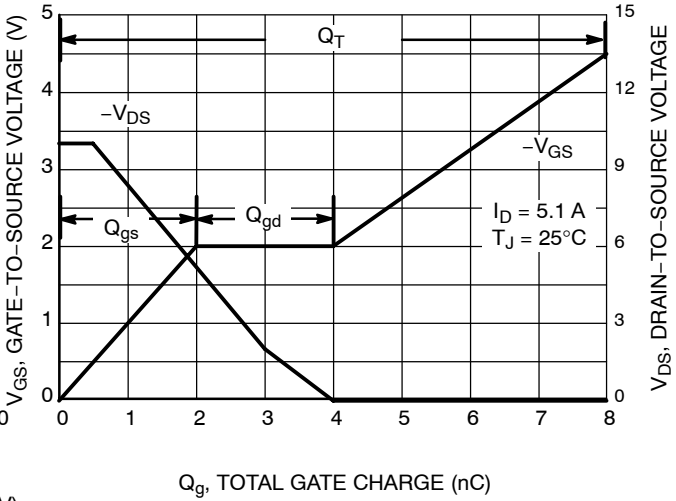


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

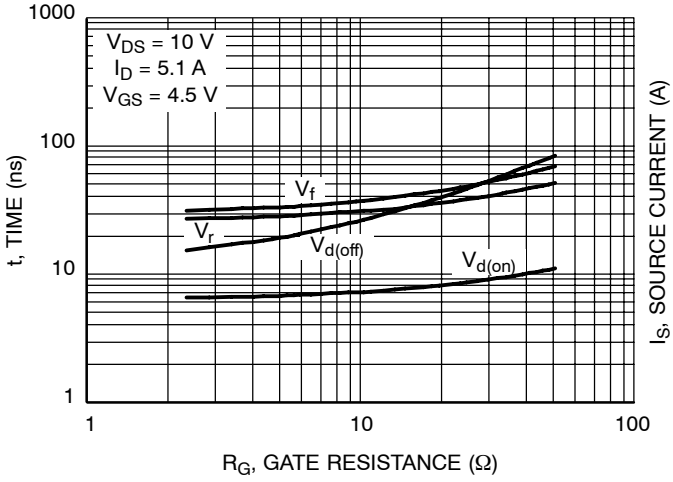


Figure 9. Resistive Switching Time Variation versus Gate Resistance

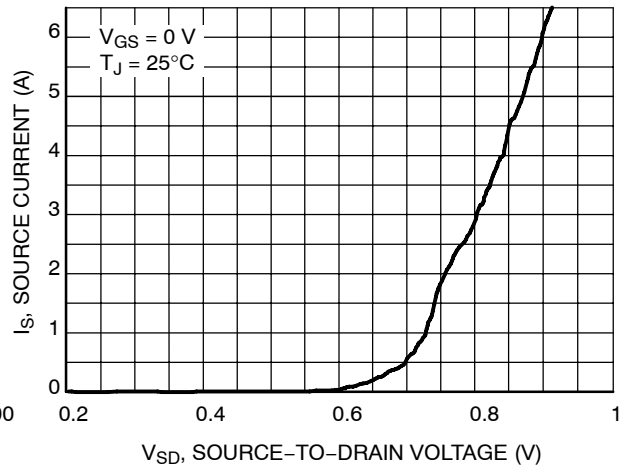


Figure 10. Diode Forward Voltage versus Current

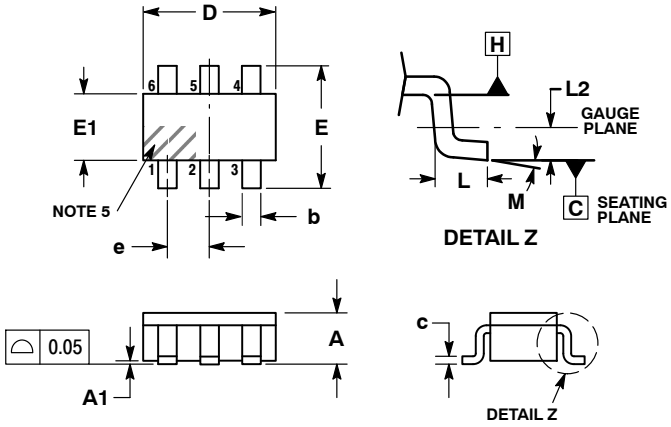
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

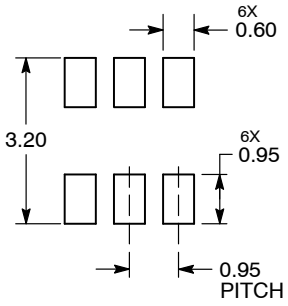
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

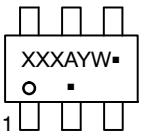
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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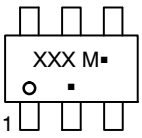

STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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