

Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. ("LAPIS Technology") and LAPIS Technology succeeded LAPIS Semiconductor's LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ML630Q464/Q466

Ultra Low Power 32-bit Microcontroller

■ GENERAL DESCRIPTION

This LSI is a high-performance low power 32-bit microcontroller. Equipped with a 32-bit CPU core Cortex™-M0+, it implements a 128 KB flash memory, 16 KB RAM, rich peripheral circuits, such as USB Full speed device, synchronous serial port, UART, I²C bus interface, supply voltage level detect circuit, RC oscillation type A/D converter, successive approximation type A/D converter, and LCD driver. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) is most suitable for battery-driven applications.

■ FEATURES

- CPU
 - 32-bit RISC CPU (CPU name: ARM Cortex™-M0+)
 - Thumb[®]/Thumb[®]-2 instruction supported
 - Serial Wire Debug Port
 - Minimum instruction execution time
 30.5 μs (@32.768 kHz system clock)
 41.7ns (@24 MHz system clock)

- Internal memory
 - Re-writing the program memory area by software
 - Number of segments

| Product name | Flash memory | | SRAM |
|--------------|---------------------|--------------------|-------------------|
| | Program area | Data area | |
| ML630Q464 | 64KB (16K × 32bit) | 2KB (0.5K × 32bit) | 8KB (2K × 32bit) |
| ML630Q466 | 128KB (32K × 32bit) | 2KB (0.5K × 32bit) | 16KB (4K × 32bit) |

- Interrupt controller (NVIC)
 - 1 non-maskable interrupt source (Internal source: 1)
 - 31 maskable interrupt sources (Internal sources: 30, External sources: 1)
 - Priority level (4-level) can be set for each interrupt
- DMA controller (DMAC)
 - 2 channels
 - Enable to allocate multiple DMA transfer request sources for each channel.
 - Channel priority: fixed mode/round robin mode
 - DMA transfer mode: cycle steal mode/burst mode
 - DMA request type: software requests/hardware requests
 - Maximum transfer count: 65,536
 - Data transfer size: 8 bits/16 bits/32 bits
 - Transfer request source: SSIOF, UART, UARTF, I2CF, RC-ADC, SA-ADC
- Time base counter (TBC)
 - Low-speed time base counter ×1 channel
- 1 kHz Timer
 - 10 Hz / 1 Hz interrupt function

- Timers (TMR)
 - 8 bits × 8 channels
(Timer0-7: 16-bit x 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
 - Selection of one shot timer mode is possible
 - External clock can be selected as timer clock.
- Function Timers (FTM)
 - 16-bit × 4 channels
 - Equipped with the timer/capture/PWM functions using a 16-bit counter
 - An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3φ)
 - 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input selectable as timer clock
 - Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.
- Real Time Clock (RTC)
 - 1 channels (99 years calendar, alarm, revision of the clock)
- Watchdog timer (WDT)
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)
- Synchronous serial port (SSIOF/SSIO)
 - without FIFOs (SSIO) : 1 channel
 - with 16-byte transmits and receives FIFOs (SSIOF) : 1 channel
 - Master/slave selectable
 - LSB first/MSB first selectable
 - Clock polarity (data out at rising edge and data in at falling edge/data out at falling edge and data in at rising edge) selectable
 - 8-bit length/16-bit length selectable
 - Initial clock level (High start/Low start) selectable
 - supports slave-select signal (only SSIOF)
- UART (UARTF/UART)
 - without FIFOs (UART) : 1 channel
 - with 16-byte transmits and receives FIFOs (UARTF) : 1 channels
 - Full duplex buffer system
 - Communication speed: Settable within the range of 2400bps to 115200bps.
 - Programmable interface (data length, parity, stop bits selectable)
- I²C bus interface (I²CF/I²C)
 - without FIFOs(I²C) :1 channel
 - with 16-byte transmits and receives FIFOs (I²CF) : 1 channels
 - Master/slave function (only I2CF)
 - Fast mode (400 kHz), standard mode (100 kHz)
- USB full-speed device
 - Compliant with Universal Serial Bus (USB)
 - Full speed (12 Mbps) 1 port.
 - End points: 5 or 6
 - Supports all data transfer types (control transfer, bulk transfer, interrupt transfer, isochronous transfer).
 - Built-in SOF generation and CRC5/16 generation functions
 - Access size to data transfer FIFOs: 8 bits/16 bits/32 bits
- General-purpose ports (PORT)
 - Input/output port × 38 channels (including secondary or tertiary or quaternary or quinary functions).
(ML630Q464 and ML630Q466: including LCD com/seg ports (each 20 ports))

- RC oscillation type A/D converter (RC-ADC)
 - Time division × 2 channels
 - Starting by trigger of Timer/FTM function.
 - 24-bit counter
- Successive approximation type A/D converter (SA-ADC)
 - Input × 12 channels
 - 12-bit A/D converter
 - Starting by trigger of Timer/FTM function.
 - Capacitive touch sense function
- Analog Comparator (CMP)
 - Input × 2ch
 - Common mode input voltage: 0.2V to $V_{DD}-0.2V$
 - Input offset voltage: 30mV(max)
 - Interrupt allow edge selection and sampling selection
- Voltage Level Supervisor (VLS)
 - Threshold voltages: One of 64 levels
 - Accuracy: ±3%
 - Interrupt or Reset generation are selectable
 - Voltage measurement with voltage input pin or V_{DD} pin
- Low Level Detector(LLD)
 - Judgment Voltage: 1.8V±0.2V
 - Can be used as low level detection reset.
- LCD driver
 - Maximum 400 dots (50 segment x 8 common)
 - 1/1 to 1/8 duty
 - 1/2, 1/3 bias (built-in bias generation circuit)
 - Frame frequency selectable
 - Bias voltage multiplying clock selectable (5 types)
 - Contrast adjustment (32 steps)
 - 4 operating mode: LCD drive stop, LCD display, all LCDs on, all LCDs off
 - Programmable display allocation function
- Random number generator (RANDOM)
 - Generates 8-bit random numbers
- AES
 - 128-bit Common key
 - Supports key sizes of 128, 192, and 256 bits
 - Supports ECB, CBC, and CTR modes
- Reset
 - Reset by the RESET_N pin input
 - Reset by power-on detection
 - Reset by overflow of watchdog timer (WDT)
 - Reset by threshold detection in Voltage Level Supervisor(VLS)
 - Reset by low level detection in Low Level Detector(LLD)
 - Reset by the low-speed crystal oscillation stop detection
 - Reset by SYSRESETREQ of Cortex™-M0+ (software reset)

- Clock
 - Low-speed clock:
 - Crystal oscillation (32.768 kHz)
 - Built-in RC oscillation (32.768kHz)
 - High-speed clock:
 - PLL (24 MHz) generated from Crystal oscillation (32.768 kHz)
 - Built-in RC oscillation (16MHz)
- Power management
 - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
 - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
 - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states.
 - ULTRA-DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states, at $V_{DD} > 2.5V$.
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of the oscillation clock)
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
- Guaranteed operating range
 - Operating temperature (ambient) : $-40^{\circ}C$ to $+85^{\circ}C$
 - Operating voltage: $V_{DD} = 1.8V$ to $3.6V$
- Supply current (Typ)
 - High-speed operation (24 MHz) : 250uA/MHz
 - ULTRA-DEEP-HALT : 0.80uA
- Package
 - 100-pin plastic TQFP
 - Tray
 - ML630Q464-xxxTBZWAX
 - ML630Q466-xxxTBZWAX

■ BLOCK DIAGRAM

ML630Q464/Q466 Block Diagram

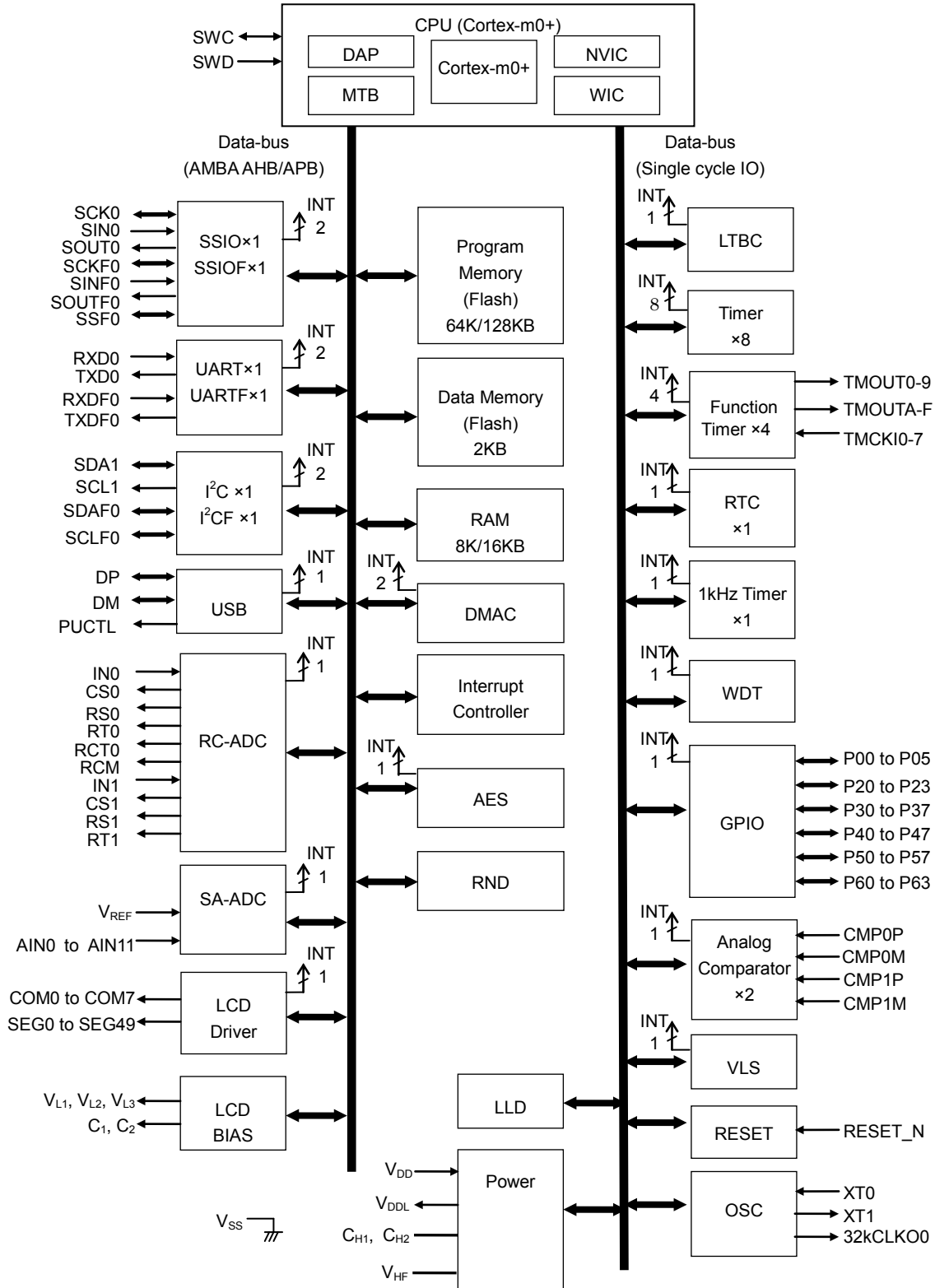


Figure 1. ML630Q464/Q466 Block Diagram

■ PIN CONFIGURATION

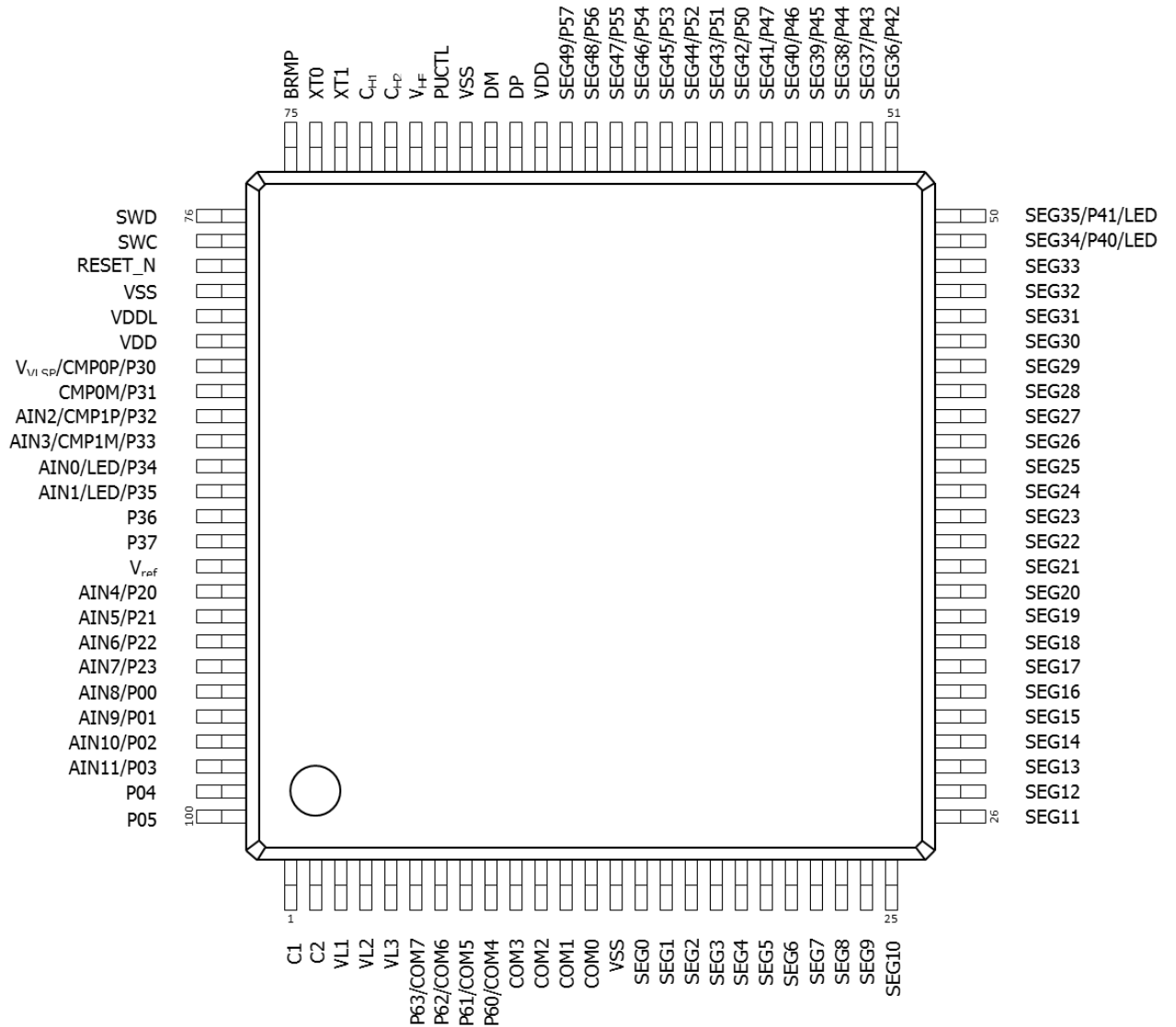


Figure 2. Pin Layout of ML630Q464/Q466

■ PIN LIST

| PIN No. | .Reset State | Primary Function | | Secondary Function | | Tertiary Function | | Quaternary Function | | Quinary Function | |
|----------------|------------------|---|-----|--------------------|-----|-------------------|-----|---------------------|-----|------------------|-----|
| | | Pin name | I/O | Pin name | I/O | pin name | I/O | pin name | I/O | pin name | I/O |
| 14 68 79 | - | V _{SS} | - | - | - | - | - | - | - | - | - |
| 65 81 | - | V _{DD} | - | - | - | - | - | - | - | - | - |
| 80 | - | V _{DDL} | - | - | - | - | - | - | - | - | - |
| 70 | - | V _{HF} | - | - | - | - | - | - | - | - | - |
| 90 | - | V _{REF} | - | - | - | - | - | - | - | - | - |
| 74 | - | XT0 | - | - | - | - | - | - | - | - | - |
| 73 | - | XT1 | - | - | - | - | - | - | - | - | - |
| 78 | Pull-up Input | RESET_N | I | - | - | - | - | - | - | - | - |
| 77 | Pull-up Input | SWC | I | - | - | - | - | - | - | - | - |
| 76 | Pull-up Input | SWD | I/O | - | - | - | - | - | - | - | - |
| 75 | Pull-down Input | BRMP | I | - | - | - | - | - | - | - | - |
| 95 | Hi-Z output | P00/ EX100/ AIN8 | I/O | IN0 | I | SOUT0 | O | RXDF0 | I | - | - |
| 96 | Hi-Z output | P01/ EX101/ AIN9 | I/O | CS0 | O | SIN0 | I | TXDF0 | O | - | - |
| 97 | Hi-Z output | P02/ EX102/ AIN10 | I/O | RCT0 | O | SCK0 | I/O | TMOUT0 | O | - | - |
| 98 | Hi-Z output | P03/ EX103/ AIN11 | I/O | RS0 | O | - | - | TMOUT1 | O | - | - |
| 99 | Hi-Z output | P04/ EX104 | I/O | RT0 | O | - | - | - | - | - | - |
| 100 | Hi-Z output | P05/ EX105 | I/O | RCM | O | - | - | - | - | - | - |
| 91 | Hi-Z output | P20/ EX120/ AIN4 | I/O | IN1 | I | SOUTF0 | O | - | - | - | - |
| 92 | Hi-Z output | P21/ EX121/ AIN5 | I/O | CS1 | O | SINF0 | I | - | - | - | - |
| 93 | Hi-Z output | P22/ EX122/ AIN6 | I/O | RS1 | O | SCKF0 | I/O | TMOUT2 | O | - | - |
| 94 | Hi-Z output | P23/ EX123/ AIN7 | I/O | RT1 | O | SSF0 | I/O | TMOUT3 | O | - | - |
| 82 | Hi-Z output | P30/ EX130/ CMP0P V _{LS} SP | I/O | SDAF0 | I/O | SOUT0 | O | - | - | - | - |
| 83 | Hi-Z output | P31/ EX131/ CMP0M | I/O | SCLF0 | I/O | SIN0 | I | - | - | - | - |
| 84 | Hi-Z output | P32/ EX132/ CMP1P/ AIN2 | I/O | RXDF0 | I | SCK0 | I/O | TMOUT4 | O | - | - |
| 85 | Hi-Z output | P33/ EX133/ CMP1M/ AIN3 | I/O | TXDF0 | O | 32kCLKO | O | TMOUT5 | O | - | - |
| 86 | Hi-Z output | P34/ EX134/ AIN0 LED | I/O | SDA1 | I/O | SOUTF0 | O | - | - | - | - |
| 87 | Hi-Z output | P35/ EX135/ AIN1 LED | I/O | SCL1 | O | SINF0 | I | - | - | - | - |
| 88 | Hi-Z output | P36/ EX136/ TMCK14 | I/O | RXD0 | I | SCKF0 | I/O | TMOUT6 | O | - | - |
| 89 | Hi-Z output | P37/ EX137/ TMCK15 | I/O | TXD0 | O | SSF0 | I/O | TMOUT7 | O | - | - |
| 13 to 10 | Low Level Output | COM0 to COM3 | O | - | - | - | - | - | - | - | - |
| 9 | Hi-Z output | P60/ EX160 | I/O | COM4 | O | - | - | - | - | - | - |
| 8 | Hi-Z output | P61/ EX161 | I/O | COM5 | O | - | - | - | - | - | - |
| 7 | Hi-Z output | P62/ EX162 | I/O | COM6 | O | - | - | - | - | - | - |
| 6 | Hi-Z output | P63/ EX163 | I/O | COM7 | O | - | - | - | - | - | - |
| 15 to 48 | Low Level Output | SEG0 to SEG33 | O | - | - | - | - | - | - | - | - |
| 49 | Hi-Z output | P40/ EX140/ LED | I/O | SDAF0 | I/O | SOUT0 | O | - | - | SEG34 | O |

| PIN No. | .Reset State | Primary Function | | Secondary Function | | Tertiary Function | | Quaternary Function | | Quinary Function | |
|---------|--------------|--------------------------|-----|--------------------|-----|-------------------|-----|---------------------|-----|------------------|-----|
| | | Pin name | I/O | Pin name | I/O | pin name | I/O | pin name | I/O | pin name | I/O |
| 50 | Hi-Z output | P41/ EXI41/ LED | I/O | SCLF0 | I/O | SIN0 | I | - | - | SEG35 | O |
| 51 | Hi-Z output | P42/ EXI42/ TMCKI0 | I/O | RXDF0 | I | SCK0 | I/O | TMOUT8 | O | SEG36 | O |
| 52 | Hi-Z output | P43/ EXI43/ TMCKI1 | I/O | TXDF0 | O | 32kCLKO | O | TMOUT9 | O | SEG37 | O |
| 53 | Hi-Z output | P44/ EXI44 | I/O | SDA1 | I/O | SOUTF0 | O | - | - | SEG38 | O |
| 54 | Hi-Z output | P45/ EXI45 | I/O | SCL1 | O | SINF0 | I | - | - | SEG39 | O |
| 55 | Hi-Z output | P46/ EXI46/ TMCKI2 | I/O | RXD0 | I | SCKF0 | I/O | TMOUTA | O | SEG40 | O |
| 56 | Hi-Z output | P47/ EXI47/ TMCKI3 | I/O | TXD0 | O | SSF0 | I/O | TMOUTB | O | SEG41 | O |
| 57 | Hi-Z output | P50/ EXI50 | I/O | SDAF0 | I/O | SOUT0 | O | - | - | SEG42 | O |
| 58 | Hi-Z output | P51/ EXI51 | I/O | SCLF0 | I/O | SIN0 | I | - | - | SEG43 | O |
| 59 | Hi-Z output | P52/ EXI52 | I/O | RXDF0 | I | SCK0 | I/O | TMOUTC | O | SEG44 | O |
| 60 | Hi-Z output | P53/ EXI53 | I/O | TXDF0 | O | 32kCLKO | O | TMOUTD | O | SEG45 | O |
| 61 | Hi-Z output | P54/ EXI54 | I/O | SDA1 | I/O | SOUTF0 | O | - | - | SEG46 | O |
| 62 | Hi-Z output | P55/ EXI55 | I/O | SCL1 | O | SINF0 | I | - | - | SEG47 | O |
| 63 | Hi-Z output | P56/ EXI56/ TMCKI6 | I/O | RXD0 | I | SCKF0 | I/O | TMOUTE | O | SEG48 | O |
| 64 | Hi-Z output | P57/ EXI57/ TMCKI7 | I/O | TXD0 | O | SSF0 | I/O | TMOUTF | O | SEG49 | O |
| 66 | Hi-Z output | DP | I/O | - | - | - | - | - | - | - | - |
| 67 | Hi-Z output | DM | I/O | - | - | - | - | - | - | - | - |
| 69 | Low output | PUCTL | O | - | - | - | - | - | - | - | - |
| 3 | - | V _{L1} | - | - | - | - | - | - | - | - | - |
| 4 | - | V _{L2} | - | - | - | - | - | - | - | - | - |
| 5 | - | V _{L3} | - | - | - | - | - | - | - | - | - |
| 1 | - | C ₁ | - | - | - | - | - | - | - | - | - |
| 2 | - | C ₂ | - | - | - | - | - | - | - | - | - |
| 71 | - | C _{H1} | - | - | - | - | - | - | - | - | - |
| 72 | - | C _{H2} | - | - | - | - | - | - | - | - | - |

■ PIN DESCRIPTION

In the table below indicates the functional pin description.

The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.

(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quaternary function, 5th:quinary function)

| Pin name | I/O | Description | LSI pin name | Pin mode | Logic |
|--|-----|---|--|-----------------|-------|
| System | | | | | |
| RESET_N | I | Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected. | RESET_N | - | L |
| BRMP | I | Remapping control input (for firmware update) Based on the BRMP pin setting at the time of the reset release, Bank0 is remapped. | BRMP | - | H |
| XT0 | I | Crystal connection pin for low-speed clock. | XT0 | - | - |
| XT1 | O | Capacitors C _{DL} and C _{GL} are connected across this pin and V _{SS} as required. | XT1 | - | - |
| 32kCLKO | O | Low-speed clock output pin | P33,P43,P53 | 2 nd | |
| General-purpose input/output port | | | | | |
| P00-P05 | I/O | General-purpose input/output port. | P00-P05 | 1 st | - |
| P20-P23 | I/O | General-purpose input/output port. | P20-P23 | 1 st | - |
| P30-P37 | I/O | General-purpose input/output port. | P30-P37 | 1 st | - |
| P40-P47 | I/O | General-purpose input/output port. | P40-P47 | 1 st | - |
| P50-P57 | I/O | General-purpose input/output port. | P50-P57 | 1 st | - |
| P60-P63 | I/O | General-purpose input/output port. | P60-P63 | 1 st | - |
| External interrupt | | | | | |
| EXI00-05 EXI20-23 EXI30-37 EXI40-47 EXI50-57 EXI60-63 | I | External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. | P00-P05 P20-P23 P30-P37 P40-P47 P50-P57 P60-P63 | 1 st | H/L |
| LED | | | | | |
| LED | O | N-channel open drain output pins to drive LED. | P34,P35,P40,P41 | 1 st | - |
| UART | | | | | |
| TXD0 | O | UART data output pin. | P37,P47,P57 | 2 nd | - |
| RXD0 | I | UART data input pin. | P36,P46,P56 | 2 nd | - |
| TXDF0 | O | UARTF with FIFO data output pin. | P01,P33,P43,P53 | 2 nd | - |
| RXDF0 | I | UARTF with FIFO data input pin. | P00,P32,P42,P52 | 2 nd | - |
| I²C bus interface | | | | | |
| SDA1 | I/O | I2C1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor. | P34,P44,P54 | 2 nd | - |
| SCL1 | O | I2C1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor. | P35,P45,P55 | 2 nd | - |
| SDAF0 | I/O | I2CF0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor. | P30,P40,P50 | 2 nd | - |
| SCLF0 | I/O | I2CF0 clock input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor. | P31,P41,P51 | 2 nd | - |

| Pin name | I/O | Description | LSI pin name | Pin mode | Logic |
|--|-----|---|--|-----------------|-------|
| Synchronous serial | | | | | |
| SCK0 | I/O | Synchronous serial (SSIO) clock input/output pin. | P02,P32,P42,P52 | 3 rd | - |
| SIN0 | I | Synchronous serial (SSIO) data input pin. | P01,P31,P41,P51 | 3 rd | - |
| SOUT0 | O | Synchronous serial (SSIO) data output pin. | P00,P30,P40,P50 | 3 rd | - |
| SCKF0 | I/O | Synchronous serial with FIFO (SSIOF) clock input/output pin. | P22,P36,P46,P56 | 3 rd | - |
| SINF0 | I | Synchronous serial with FIFO (SSIOF) data input pin. | P21,P35,P45,P55 | 3 rd | - |
| SOUTF0 | O | Synchronous serial with FIFO (SSIOF) data output pin. | P20,P34,P44,P54 | 3 rd | - |
| SSF0 | I/O | Synchronous serial with FIFO (SSIOF) select input/output pin. | P23,P37,P47,P57 | 3 rd | L |
| FTM | | | | | |
| TMOUT0-9 TMOUTA-F | O | FTM output pin. | P02,P03,P22,P23 P32,P33,P36,P37 P42,P43,P46,P47 P52,P53,P56,P57 | 4 th | - |
| TMCKI0-7 | I | External clock input pin for FTM. | P42,P43,P46,P47 P36,P37,P56,P57 | 1 st | - |
| RC oscillation type A/D converter | | | | | |
| IN0 | I | Oscillation input pin of Channel 0. | P00 | 2 nd | - |
| CS0 | O | Reference capacitor connection pin of Channel 0. | P01 | 2 nd | - |
| RS0 | O | Reference resistor connection pin of Channel 0. | P03 | 2 nd | - |
| RT0 | O | Resistor sensor connection pin for measurement of Channel 0. | P04 | 2 nd | - |
| RCT0 | O | Resistor/capacitor sensor connection pin of Channel 0 for measurement. | P02 | 2 nd | - |
| RCM | O | RC oscillation monitor pin. | P05 | 2 nd | - |
| IN1 | I | Oscillation input pin of Channel 1. | P20 | 2 nd | - |
| CS1 | O | Reference capacitor connection pin of Channel 1. | P21 | 2 nd | - |
| RS1 | O | Reference resistor connection pin of Channel 1. | P22 | 2 nd | - |
| RT1 | O | Resistor sensor connection pin for measurement of Channel 1. | P23 | 2 nd | - |
| Successive approximation type A/D converter | | | | | |
| V _{REF} | I | Reference power supply pin for successive approximation type A/D converter. | V _{REF} | - | - |
| AIN0-11 | I | Analog input for successive approximation type A/D converter. | (AIN0-3) P32-35, (AIN4-7) P20-23, (AIN8-11) P00-03 | 1 st | - |
| Analog comparator | | | | | |
| CMP0P | I | Comparator0 Non-inverted input pin. | P30 | 1 st | - |
| CMP0M | I | Comparator0 Inverted input pin. | P31 | 1 st | - |
| CMP1P | I | Comparator1 Non-inverted input pin. | P32 | 1 st | - |
| CMP1M | I | Comparator1 Inverted input pin. | P33 | 1 st | - |
| USB FS Device | | | | | |
| DP | I/O | USB dev D+ pin. | DP | - | - |
| DM | I/O | USB dev D- pin. | DM | - | - |
| PUCTL | O | USB dev pull-up control | PUCTL | - | - |
| DEBUG Interface | | | | | |
| SWC | I | Serial clock of Serial Wire Debug Port | SWC | - | - |
| SWD | I/O | Serial I/O data of Serial Wire Debug Port | SWD | - | - |

| Pin name | I/O | Description | LSI pin name | Pin mode | Logic |
|-----------------------------------|-----|---|-----------------------------------|-----------------|-------|
| Power supply | | | | | |
| V _{SS} | - | Negative power supply pin. | V _{SS} | - | - |
| V _{DD} | - | Positive power supply pin. | V _{DD} | - | - |
| V _{DDL} | - | Positive power supply pin (internally generated) for internal logic. Capacitors C _L is connected between this pin and V _{SS} . | V _{DDL} | - | - |
| V _{HF} | - | Positive power supply pin (internally generated) for built-in halver circuit. Capacitor C _{VH} is connected between this pin and V _{SS} . | V _{HF} | - | - |
| C _{H1} – C _{H2} | - | Capacitor pins of built-in halver circuit | C _{H1} – C _{H2} | - | - |
| LCD driver | | | | | |
| COM0 – COM3 | - | Common pins of LCD driver | COM0 – COM3 | - | - |
| COM4 – COM7 | - | Common pins of LCD driver | P60-P63 | 2 nd | - |
| SEG0 – SEG33 | - | Segment pins of LCD driver | SEG0 – SEG33 | - | - |
| SEG34 – SEG49 | - | Segment pins of LCD driver | P40-P47 P50-P57 | 5 th | - |
| C ₁ – C ₂ | - | Capacitor pins of built-in generation bias circuit | C ₁ – C ₂ | - | - |
| V _{L1} – V _{L3} | - | Reference voltage input pins of built-in bias generation circuit | V _{L1} – V _{L3} | - | - |

■ TERMINATION OF UNUSED PINS

Table 1 shows methods of terminating the unused pins.

Table 1 Termination of Unused Pins

| Pin | Recommended pin termination |
|---|-------------------------------|
| RESET_N | open |
| BRMP | Connect a pull-down resistor. |
| SWC | Connect a pull-up resistor. |
| SWD | Connect a pull-up resistor. |
| V _{REF} | Connect to V _{DD} |
| P00 to P05 | open |
| P20 to P23 | open |
| P30 to P37 | open |
| P40 to P47 | open |
| P50 to P57 | open |
| P60 to P63 | open |
| COM0 to COM3 | open |
| SEG0 to SEG33 | open |
| DP, DM, PUCTL | open |
| V _{L1} , V _{L2} , V _{L3} | open |
| C ₁ , C ₂ | open |

[Note]

For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

■ Electrical Characteristics

● ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|-------------------|-----------|--------------------------------|------|
| Power supply voltage 1 | V _{DD} | Ta=25°C | -0.3 to +4.6 | V |
| Power supply voltage 2 | V _{DDL} | Ta=25°C | -0.3 to +2.0 | V |
| Power supply voltage 3 | V _{L1-3} | Ta=25°C | -0.3 to +6.0 | V |
| Input voltage(P00-P05, P20-P23, P30-P35, SWC, SWD, BRMP, RESET_N, DP, DM) | V _{IN} | Ta=25°C | -0.3 to V _{DD} +0.3 | V |
| Input voltage (5 V tolerant) (P36, P37, P40-P47, P50-P57, P60-P63) | V _{INT} | Ta=25°C | -0.3 to +6.0 | V |
| Output voltage 1 | V _{OUT1} | Ta=25°C | -0.3 to V _{DD} +0.3 | V |
| Output voltage 2 (COM0 to COM7 SEG0 to SEG49) | V _{OUT2} | Ta=25°C | -0.3 to V _{L1-3} +0.3 | V |
| Output current 1 | I _{OUT1} | Ta=25°C | -12 to +11 | mA |
| Output current 2 | I _{OUT2} | Ta=25°C | -12 to +20 | mA |
| Power dissipation | PD | Ta=25°C | 0.9 | W |
| Storage temperature | T _{STG} | – | -55 to +150 | °C |

● RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

| Parameter | Symbol | Condition | Range | Unit |
|--|--------------------|-----------------------------|------------------------------------|------|
| Operating temperature (Ambience) | T _{OP} | – | -40 to +85 | °C |
| Operating voltage | V _{DD} | – | 1.8 to 3.6 | V |
| Reference voltage | V _{REF} | – | 1.8 to V _{DD} | V |
| Operating frequency (CPU) | f _{OP} | – | LSCLK:32.768k HSCLK:500k to 24M | Hz |
| Low speed crystal oscillation frequency | f _{XTL} | – | 32.768k | Hz |
| Low speed crystal oscillation external capacitor 1 | C _{DL} | Using VT-200-FL(from SII) | 6.8 to 12 | pF |
| | C _{GL} | | 6.8 to 12 | |
| Low speed crystal oscillation external capacitor 2 | C _{DL} | Using DT-26(from Daishinku) | 12 to 16 | pF |
| | C _{GL} | | 12 to 16 | |
| Low speed crystal ^{*1} oscillation external capacitor 3 | C _{DL} | Using VT-200-F(from SII) | 12 to 22 | pF |
| | C _{GL} | | 12 to 22 | |
| V _{DDL} external capacitor ^{*2} | C _L | ESR ≤500mΩ | 2.2 ± 30% | μF |
| V _{L1,2,3pin} external capacitor | C _{a,b,c} | – | 1.0 ± 30% | μF |
| C ₁ -C ₂ external capacitor | C ₁₂ | – | 1.0 ± 30% | μF |
| C _{H1} , C _{H2} external capacitor | C _{H12} | – | 1.0 ± 30% | μF |
| V _{HF} external capacitor | C _{HF} | – | 1.0 ± 30% | μF |

*1 : Please use this crystal except DEEPHALT mode because this LSI may not be functioning at DEEPHALT mode with the crystal.
Please evaluate the matching when other crystal oscillator/ceramic oscillator is used.

*2 : Please evaluate on user's conditions, put on C_{L0}(= 0.1μF) if necessary.

● Operating Conditions of Flash Memory

(V_{SS}= 0V)

| Parameter | Symbol | Condition | Range | Unit | |
|-------------------------------------|------------------|----------------------------|-----------------|-------|----|
| Operating temperature (Ambience) | T _{OP} | Data area : write/erase | -40 to +85 | °C | |
| | | Program area : write/erase | 0 to +40 | °C | |
| Operating voltage Write time | V _{DD} | Write/erase | 1.8 to 3.6 | V | |
| | C _{EPD} | Data area (1,024B x 2) | 10,000 | times | |
| | C _{EPP} | Program area | 100 | times | |
| Erase unit | - | Block erase | Program area | 8 | KB |
| | | | Data area | 2 | |
| | | Sector erase | 1 | KB | |
| Erase time(Maximum) | - | Block erase/Sector erase | 100 | ms | |
| Write unit | - | - | 1 word (4 byte) | - | |

● AC characteristics (Oscillation, reset)

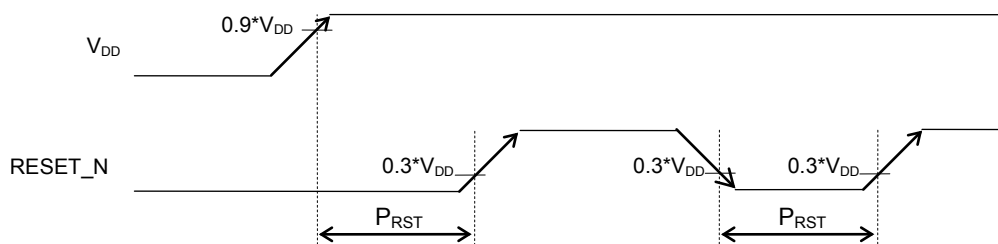
(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|-------------------|-----------------------------|------------|--------|------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Low speed crystal oscillation start time | T _{XTL} | - | - | - | 2 | s | 1 |
| Low speed built-in RC oscillation frequency ^{*1*2*3} | f _{LCR} | Ta=25°C | Typ -1.5% | 32.768 | Typ +1.5% | kHz | |
| | | Ta=-40 to 85°C | typ-5% | 32.768 | typ+5% | | |
| High speed built-in RC oscillation frequency ^{*1*2} | f _{HCR} | Ta=25°C | typ -1% | 16 | typ +1% | MHz | |
| | | Ta=-40 to 85°C | typ -5% | 16 | typ +5% | | |
| PLL frequency | f _{PLL} | f _{XTL} =32.768kHz | typ -0.25% | 24 | typ +0.25% | MHz | |
| Low speed crystal oscillation stop detection time | T _{STOP} | - | - | 600 | - | μs | |
| Reset pulse width | P _{RST} | - | 200 | - | - | μs | |
| Reset noise elimination pulse width | P _{NRST} | - | - | - | 0.3 | μs | |
| Power-on reset activation power rise time | T _{POR} | - | - | - | 10 | ms | |

*1 : Mean value of 1024 cycle.

*2 : Guarantee value at the time of the shipment.

*3 : Except DeepHALT mode and Ultra-DeepHALT mode.



External reset sequence



Power on reset sequence

● DC Characteristics (IDD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating ^{*1} | | | Unit | Measuring circuit |
|---------------------|--------|---|----------------------|------|------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Power consumption 1 | IDD1 | CPU is Stopped Low/High-speed oscillation is stopped | Ta=25°C | – | 0.70 | 2.5 | μA |
| | | | Ta=-40 to 85°C | – | – | 28 | |
| Power consumption 2 | IDD2-1 | ULTRA-DEEP-HALT mode ^{*3*4} (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped. 2.5V ≤ V _{DD} | Ta=25°C | – | 0.80 | 2.5 | μA |
| | | | Ta=-40 to 85°C | – | – | 20 | |
| | IDD2-2 | DEEP-HALT mode ^{*3*4} (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped. | Ta=25°C | – | 1.30 | 3.0 | μA |
| | | | Ta=-40 to 85°C | – | – | 28 | |
| Power consumption 3 | IDD3 | HALT mode ^{*3*4} (LTBC function) Low-speed crystal oscillating (32.768kHz) High speed oscillation is stopped. | Ta=25°C | – | 2.2 | 5.0 | μA |
| | | | Ta=-40 to 85°C | – | – | 32 | |
| Power consumption 4 | IDD4 | CPU Low-speed ^{*2*4} Low-speed crystal oscillating High speed oscillation is stopped. | Ta=25°C | – | 9.0 | 14 | μA |
| | | | Ta=-40 to 85°C | – | – | 45 | |
| Power consumption 5 | IDD5 | CPU High-speed(16MHz) ^{*2*4} High-speed Built-in RC oscillating | Ta=25°C | – | 3.8 | 5.0 | mA |
| | | | Ta=-40 to 85°C | – | – | 5.5 | |
| Power consumption 5 | IDD5 | CPU High-speed(24MHz) ^{*2*4} High-speed PLL oscillating | Ta=25°C | – | 6.0 | 7.0 | mA |
| | | | Ta=-40 to 85°C | – | – | 7.5 | |

*1 : typ.rating is V_{DD}=3.0V

*2 : at CPU activity rate =100% (No HALT state)

*3 : using 32.768KHz crystal oscillator VT-200-FL (from SII)(C_{GL}/C_{DL}= 12pF)using 32.768KHz crystal oscillator DT-26(from Daishinku)(C_{GL}/C_{DL}= 12pF)

*4 : CLKCON valid bits are "0", RSTCON valid bits are "1"

1

● DC Characteristics (VLS)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|------------------|--------------------------------|-------------|-------|-------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| VLS judge voltage (V _{DD} =fall) | V _{VLS} | VLSLV[5:0] = 00H ^{*1} | Typ. -3% | 1.200 | Typ. +3% | V | 1 |
| | | VLSLV[5:0] = 01H ^{*1} | | 1.225 | | | |
| | | VLSLV[5:0] = 02H ^{*1} | | 1.250 | | | |
| | | VLSLV[5:0] = 03H ^{*1} | | 1.275 | | | |
| | | VLSLV[5:0] = 04H ^{*1} | | 1.300 | | | |
| | | VLSLV[5:0] = 05H ^{*1} | | 1.325 | | | |
| | | VLSLV[5:0] = 06H ^{*1} | | 1.350 | | | |
| | | VLSLV[5:0] = 07H ^{*1} | | 1.375 | | | |
| | | VLSLV[5:0] = 08H ^{*1} | | 1.400 | | | |
| | | VLSLV[5:0] = 09H ^{*1} | | 1.425 | | | |
| | | VLSLV[5:0] = 0AH ^{*1} | | 1.450 | | | |
| | | VLSLV[5:0] = 0BH ^{*1} | | 1.475 | | | |
| | | VLSLV[5:0] = 0CH ^{*1} | | 1.500 | | | |
| | | VLSLV[5:0] = 0DH ^{*1} | | 1.525 | | | |
| | | VLSLV[5:0] = 0EH ^{*1} | | 1.550 | | | |
| | | VLSLV[5:0] = 0FH ^{*1} | | 1.575 | | | |
| | | VLSLV[5:0] = 10H ^{*1} | | 1.600 | | | |
| | | VLSLV[5:0] = 11H ^{*1} | | 1.625 | | | |
| | | VLSLV[5:0] = 12H ^{*1} | | 1.650 | | | |
| | | VLSLV[5:0] = 13H ^{*1} | | 1.675 | | | |
| | | VLSLV[5:0] = 14H ^{*1} | | 1.700 | | | |
| | | VLSLV[5:0] = 15H ^{*1} | | 1.725 | | | |
| | | VLSLV[5:0] = 16H ^{*1} | | 1.750 | | | |
| | | VLSLV[5:0] = 17H ^{*1} | | 1.775 | | | |
| | | VLSLV[5:0] = 18H | | 1.800 | | | |
| | | VLSLV[5:0] = 19H | | 1.825 | | | |
| | | VLSLV[5:0] = 1AH | | 1.850 | | | |
| | | VLSLV[5:0] = 1BH | | 1.875 | | | |
| | | VLSLV[5:0] = 1CH | | 1.900 | | | |
| | | VLSLV[5:0] = 1DH | | 1.925 | | | |
| | | VLSLV[5:0] = 1EH | | 1.950 | | | |
| | | VLSLV[5:0] = 1FH | | 1.975 | | | |
| | | VLSLV[5:0] = 20H | | 2.000 | | | |
| VLSLV[5:0] = 21H | 2.050 | | | | | | |
| VLSLV[5:0] = 22H | 2.100 | | | | | | |
| VLSLV[5:0] = 23H | 2.150 | | | | | | |
| VLSLV[5:0] = 24H | 2.200 | | | | | | |
| VLSLV[5:0] = 25H | 2.250 | | | | | | |
| VLSLV[5:0] = 26H | 2.300 | | | | | | |
| VLSLV[5:0] = 27H | 2.350 | | | | | | |
| VLSLV[5:0] = 28H | 2.400 | | | | | | |
| VLSLV[5:0] = 29H | 2.450 | | | | | | |
| VLSLV[5:0] = 2AH | 2.500 | | | | | | |
| VLSLV[5:0] = 2BH | 2.550 | | | | | | |
| VLSLV[5:0] = 2CH | 2.600 | | | | | | |

| | | | | | | | |
|---|------------------|------------------|-------------------------------|-------------------------------|-------------------------------|---|---|
| | | VLSLV[5:0] = 2DH | | 2.650 | | | 1 |
| | | VLSLV[5:0] = 2EH | | 2.700 | | | |
| | | VLSLV[5:0] = 2FH | | 2.750 | | | |
| | | VLSLV[5:0] = 30H | | 2.800 | | | |
| | | VLSLV[5:0] = 31H | | 2.850 | | | |
| | | VLSLV[5:0] = 32H | | 2.900 | | | |
| | | VLSLV[5:0] = 33H | | 2.950 | | | |
| | | VLSLV[5:0] = 34H | | 3.000 | | | |
| | | VLSLV[5:0] = 35H | | 3.050 | | | |
| | | VLSLV[5:0] = 36H | Typ. -3% | 3.100 | Typ. +3% | V | |
| | | VLSLV[5:0] = 37H | | 3.150 | | | |
| | | VLSLV[5:0] = 38H | | 3.200 | | | |
| | | VLSLV[5:0] = 39H | | 3.250 | | | |
| | | VLSLV[5:0] = 3AH | | 3.300 | | | |
| | | VLSLV[5:0] = 3BH | | 3.350 | | | |
| | | VLSLV[5:0] = 3CH | | 3.400 | | | |
| | | VLSLV[5:0] = 3DH | | 3.450 | | | |
| | | VLSLV[5:0] = 3EH | | 3.500 | | | |
| | | VLSLV[5:0] = 3FH | | 3.550 | | | |
| V _{VLS} Hysteresis width (V _{DD} =rise) | H _{VLS} | - | V _{VLS} x 1.0% | V _{VLS} x 2.7% | V _{VLS} x 4.5% | V | |

VLSLV[3:0] are bits of the VLSCON register to change detection voltage level.

*1: Setable only at the time of select to V_{VLS} pin.

● DC characteristics (LLD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|-------------------|--------|-----------|--------|------|------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| LLD judge Voltage | VLLR | - | 1.60 | 1.80 | 2.00 | V | 1 |

● DC/AC characteristics (Analog comparator)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|----------------------------|--------------------|-----------------|--------|------|-------------------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Common Input voltage range | V _{CMPIN} | - | 0.2 | - | V _{DD} -0.2 | V | 1 |
| Input offset voltage | V _{CMPOF} | - | -30 | - | 30 | mV | |
| Comparator judge time | T _{CMP} | CMPP- CPM =40mV | - | - | 2 | μs | |

● DC characteristics (LCD Driver)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, T_a=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit | |
|---|-------------------|---|------------------------------|--------------------|-------------|------|-------------------|---|
| | | | Min. | Typ. | Max. | | | |
| V _{L1} voltage | V _{L1} | V _{DD} = 3.0V, T _j = 25°C | LCN[4:0] = 00H* ₂ | 0.89 | 0.94 | 0.99 | V | 1 |
| | | | LCN[4:0] = 01H* ₂ | 0.91 | 0.96 | 1.01 | | |
| | | | LCN[4:0] = 02H* ₂ | 0.93 | 0.98 | 1.03 | | |
| | | | LCN[4:0] = 03H* ₂ | 0.95 | 1.00 | 1.05 | | |
| | | | LCN[4:0] = 04H* ₂ | 0.97 | 1.02 | 1.07 | | |
| | | | LCN[4:0] = 05H* ₂ | 0.99 | 1.04 | 1.09 | | |
| | | | LCN[4:0] = 06H* ₂ | 1.01 | 1.06 | 1.11 | | |
| | | | LCN[4:0] = 07H* ₂ | 1.03 | 1.08 | 1.13 | | |
| | | | LCN[4:0] = 08H* ₂ | 1.05 | 1.10 | 1.15 | | |
| | | | LCN[4:0] = 09H* ₂ | 1.07 | 1.12 | 1.17 | | |
| | | | LCN[4:0] = 0AH* ₂ | 1.09 | 1.14 | 1.19 | | |
| | | | LCN[4:0] = 0BH* ₂ | 1.11 | 1.16 | 1.21 | | |
| | | | LCN[4:0] = 0CH* ₂ | 1.13 | 1.18 | 1.23 | | |
| | | | LCN[4:0] = 0DH* ₂ | 1.15 | 1.20 | 1.25 | | |
| | | | LCN[4:0] = 0EH* ₂ | 1.17 | 1.22 | 1.27 | | |
| | | | LCN[4:0] = 0FH* ₂ | 1.19 | 1.24 | 1.29 | | |
| | | | LCN[4:0] = 10H | 1.21 | 1.26 | 1.31 | | |
| | | | LCN[4:0] = 11H | 1.23 | 1.28 | 1.33 | | |
| | | | LCN[4:0] = 12H | 1.25 | 1.30 | 1.35 | | |
| | | | LCN[4:0] = 13H | 1.27 | 1.32 | 1.37 | | |
| | | | LCN[4:0] = 14H | 1.29 | 1.34 | 1.39 | | |
| | | | LCN[4:0] = 15H | 1.31 | 1.36 | 1.41 | | |
| | | | LCN[4:0] = 16H | 1.33 | 1.38 | 1.43 | | |
| | | | LCN[4:0] = 17H | 1.35 | 1.40 | 1.45 | | |
| LCN[4:0] = 18H | 1.37 | 1.42 | 1.47 | | | | | |
| LCN[4:0] = 19H | 1.39 | 1.44 | 1.49 | | | | | |
| LCN[4:0] = 1AH | 1.41 | 1.46 | 1.51 | | | | | |
| LCN[4:0] = 1BH | 1.43 | 1.48 | 1.53 | | | | | |
| LCN[4:0] = 1CH | 1.45 | 1.50 | 1.55 | | | | | |
| LCN[4:0] = 1DH | 1.47 | 1.52 | 1.57 | | | | | |
| LCN[4:0] = 1EH | 1.49 | 1.54 | 1.59 | | | | | |
| LCN[4:0] = 1FH | 1.51 | 1.56 | 1.61 | | | | | |
| V _{L1} temperature deviation* ¹ | ΔV _{L1} | V _{DD} = 3.0V | – | -0.06 | – | %/°C | | |
| V _{L1} voltage dependency* ¹ | ΔV _{L1} | V _{DD} = 1.8 to 3.6V | – | 5 | 20 | mV/V | | |
| V _{L2} voltage | V _{L2} | V _{DD} = 3.0V, T _j = 25°C 1MΩ load (V _{L3} -V _{SS}) | Typ. -10% | V _{L1} ×2 | Typ. +4% | V | | |
| V _{L3} voltage | V _{L3} | | Typ. -10% | V _{L1} ×3 | Typ. +4% | | | |
| LCD bias voltage generation time | T _{BIAS} | – | – | – | 600 | ms | | |

*¹: V_{L1} can not exceed V_{DD} level. The maximum V_{L1} becomes V_{DD} level when the V_{L1} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.

*²: 1/3 bias only.

● DC characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|--|--------|---|-------------------------|------|-------------------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Output voltage 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57,, P60-P63, SWD,PUCTL) | VOH1 | IOH=-1.0mA | V _{DD} -0.5 | - | - | V | 2 |
| | VOL1 | IOL=+0.5mA | - | - | 0.4 | | |
| Output voltage 2 (P34, P35, P40, P41) (LED mode is selected) | VOL2 | 2.7V ≤ V _{DD} ≤ 3.6V IOL=+5.0mA | - | - | 0.6 | | |
| | | IOL=+2.0mA | - | - | 0.4 | | |
| Output voltage 3 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I ² C mode is selected) | VOL3 | IOL3= +3mA (I ² Cspec) (V _{DD} ≥ 2V) | - | - | 0.4 | | |
| Output voltage 4 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I ² C mode is selected) | VOL4 | IOL4= +2mA(I ² Cspec) (V _{DD} < 2V) | - | - | V _{DD} ×0.2 | | |
| Output voltage 5 (COM0~7) (SEG00~49) (LCD mode is selected) | VOH5 | 1/3bias, IOH5=-0.02mA, VL1=1.2V | V _{L3} -0.2 | - | - | | |
| | VOM5 | 1/3bias, IOM5=+0.02mA, VL1=1.2V | - | - | V _{L2} +0.2 | | |
| | VOM5S | 1/3bias, IOM5S=-0.02mA, VL1=1.2V | V _{L2} -0.2 | - | - | | |
| | VOML5 | 1/3bias, IOML5=+0.02mA, VL1=1.2V | - | - | V _{L1} +0.2 | | |
| | VOML5S | 1/3bias, IOML5S=-0.02mA, VL1=1.2V | V _{L1} -0.2 | - | - | | |
| | VOL5 | 1/3bias, IOL5=+0.02mA, VL1=1.2V | - | - | 0.2 | | |
| Output voltage 5 (COM0~7) (SEG00~49) (LCD mode is selected) | VOH5 | 1/2bias, IOH5=-0.01mA, VL1=1.4V | V _{L3} -0.3 | - | - | | |
| | VOM5 | 1/2bias, IOM5=+0.01mA, VL1=1.4V | - | - | V _{L2} +0.3 | | |
| | VOM5S | 1/2bias, IOM5S=-0.01mA, VL1=1.4V | V _{L2} -0.3 | - | - | | |
| | VOML5 | 1/2bias, IOML5=+0.01mA, VL1=1.4V | - | - | V _{L1} +0.3 | | |
| | VOML5S | 1/2bias, IOML5S=-0.01mA, VL1=1.4V | V _{L1} -0.3 | - | - | | |
| | VOL5 | 1/2bias, IOL5=+0.01mA, VL1=1.4V | - | - | 0.3 | | |

| | | | | | | | |
|--|-------|---|----|---|----|----|---|
| Output leak 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWD,PUCTL) | IOOH1 | VOH=V _{DD} (at high impedance) | - | - | +1 | μA | 3 |
| | IOOL1 | VOL=V _{SS} (at high impedance) | -1 | - | - | | |

● DC characteristics (IIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit | | |
|---|--------|--|--------|------|------|------|-------------------|--|--|
| | | | Min. | Typ. | Max. | | | | |
| Input current 1 (RESET_N) | I IH1 | V IH1=V _{DD} | - | - | 1 | μA | 4 | | |
| | I IL1 | V IL1=V _{SS} | -900 | -300 | -20 | | | | |
| Input current 3 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWC, SWD, BRMP) | I IH3 | V IH3=V _{DD} (at pull down) | 1 | 15 | 200 | | | | |
| | I IL3 | V IL3=V _{SS} (at pull up) | -200 | -15 | -1 | | | | |
| | I IH3Z | V IH3=V _{DD} (at high impedance) | - | - | 1 | | | | |
| | I IL3Z | V IL3=V _{SS} (at high impedance) | -1 | - | - | | | | |
| Input current 4 (P36, P37, P40-P47, P50-P57, P60-P63) | I IH4Z | V IH4=5.0V (at high impedance) | - | - | 1 | | | | |

*1 : typ.rating is V_{DD}=3.0V, Ta=25°C

● DC characteristics (VIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|--------|--|-------------------------|------|-------------------------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1 (RESET_N, SWD, SWC, BRMP, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63) | V IH1 | - | 0.7 ×V _{DD} | - | V _{DD} | V | 5 |
| | V IL1 | - | 0 | - | 0.3 ×V _{DD} | | |
| Input terminal capacitance (RESET_N, SWD, SWC, BRMP, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63) | C IN | f=10kHz V _{rms} =50mV Ta=25°C | - | - | 10 | pF | - |

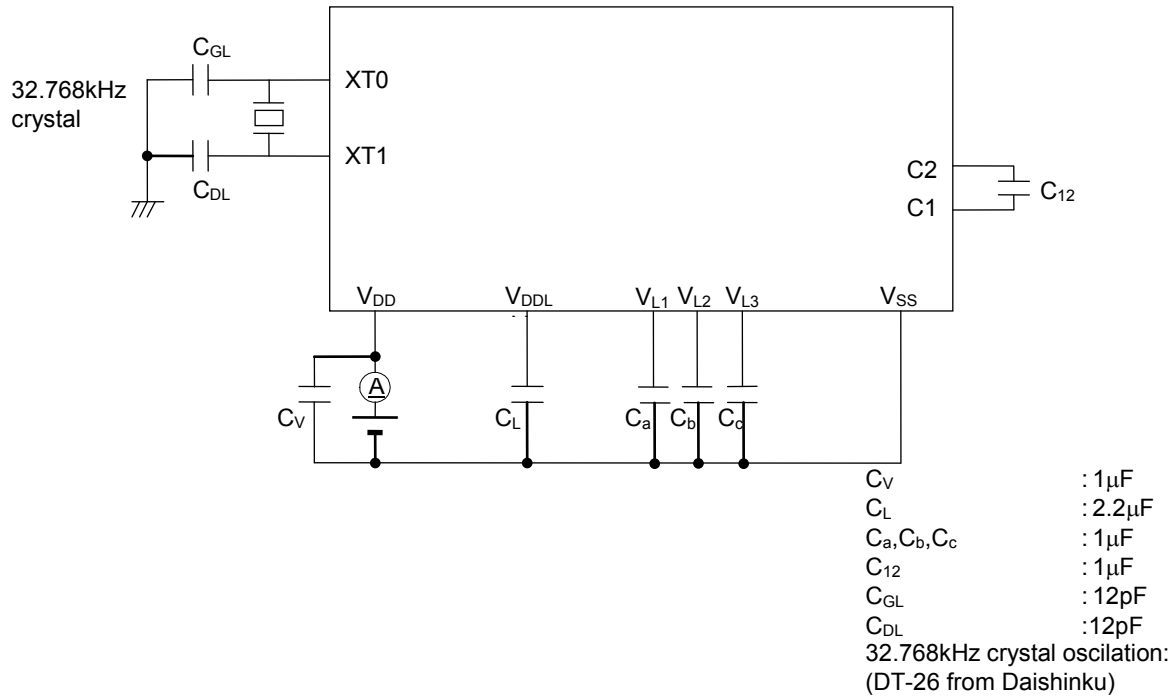
● DC characteristics (USB)

(V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

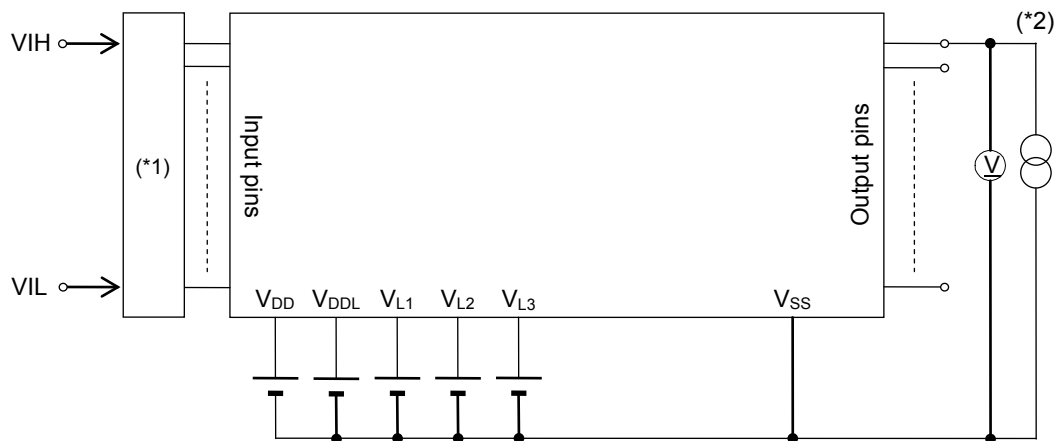
| Parameter | Symbol | Condition | Rating ^{*1} | | | Unit | Measuring circuit |
|---|------------------|---|----------------------|------|------|------|-------------------|
| | | | Min. | Typ. | Max. | | |
| Differential input sensitivity | V _{DI} | Absolute value of the difference between the DP and DM pins | 0.2 | - | - | V | |
| Differential common mode range | V _{CM} | Includes VDI range | 0.8 | - | 2.5 | V | |
| Single end input threshold voltage | V _{SE} | - | 0.8 | - | 2.0 | V | |
| High level output voltage | V _{OH} | 15k W RL is connected to GND | 2.8 | - | - | V | |
| Low level output voltage | V _{OL} | 1.5k W RL to 3.6 V | - | - | 0.3 | V | |
| Hi-Z state input/output leakage current | I _{LO} | 0 V < VIN < 3.3 V | -10 | | 10 | uA | |
| Driver output resistance | Z _{DRV} | Steady state | 28 | | 44 | Ω | |

● MEASURING CIRCUITS

MEASURING CIRCUIT1



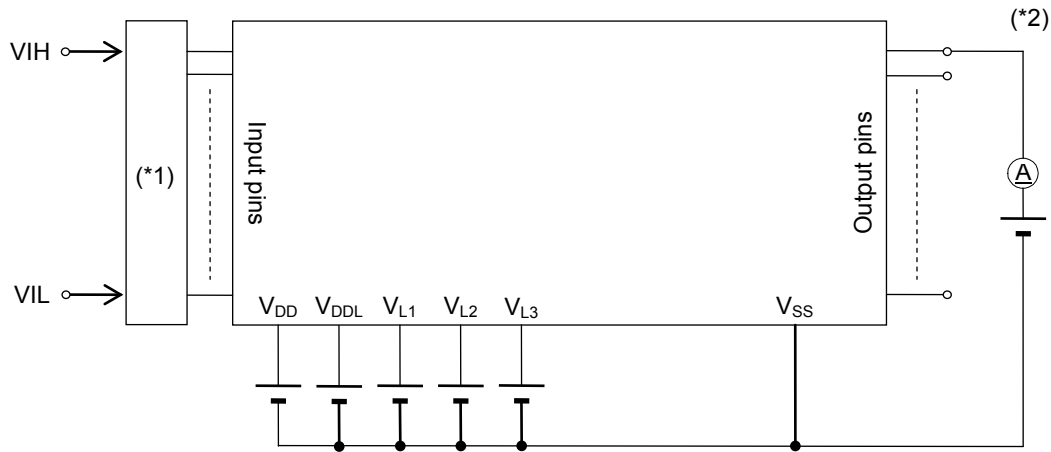
MEASURING CIRCUIT 2



(*1) Input logic circuit to determine the specified measuring conditions.

(*2) Measured at the specified output pins.

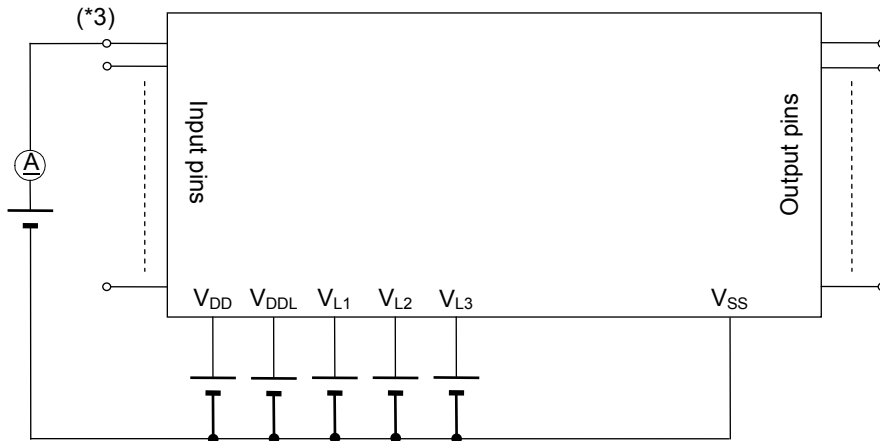
MEASURING CIRCUIT 3



*1: Input logic circuit to determine the specified measuring conditions.

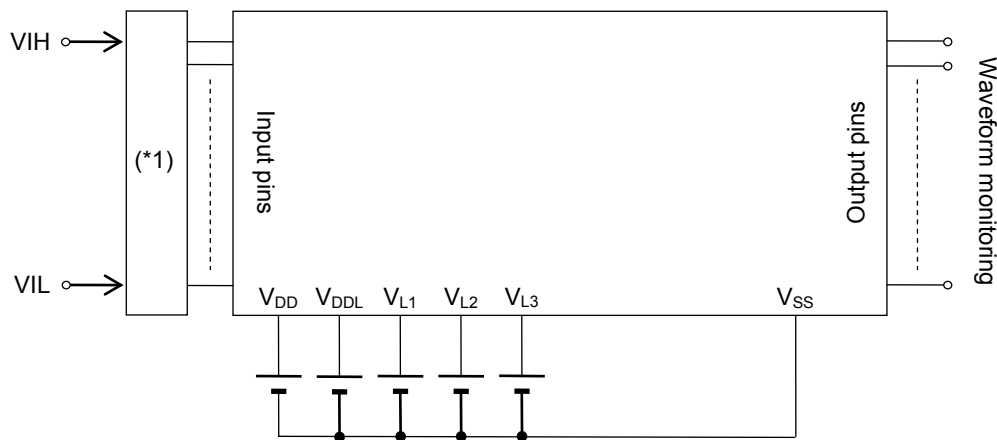
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5



*1: Input logic circuit to determine the specified measuring conditions.

● AC characteristics (USB)

(V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Applied pin |
|---------------------------------|--------------------|-------------------------------------|--------|------|-------|------|-------------|
| | | | Min. | Typ. | Max. | | |
| Rise time (*1) | T _R | CL = 50 pF | 4 | – | 20 | ns | DP, DM |
| Fall time (*1) | T _F | CL = 50 pF | 4 | – | 20 | ns | |
| Output signal crossover voltage | V _{CRS} | CL = 50 pF | 0.8 | – | 2.5 | V | |
| Data rate | T _{DRATE} | Average bit rate (12Mbps ±0.25%) | 11.97 | – | 12.03 | Mbps | |

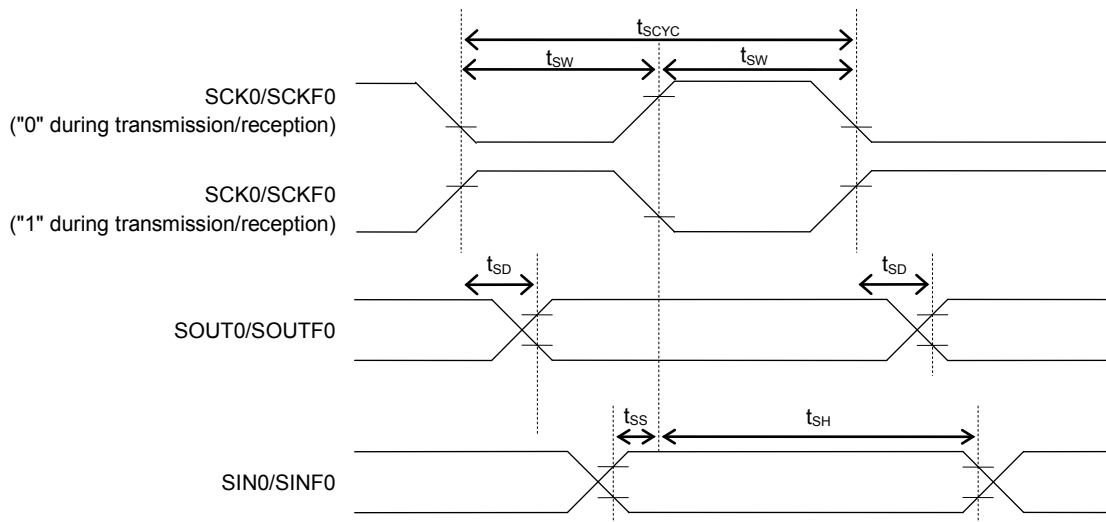
* 1: T_R and T_F: Rise time and fall time between 10% and 90% of the pulse amplitude, respectively

● AC characteristics (synchronous serial port)

($V_{DD}=1.8$ to $3.6V$, $V_{SS}=0V$, $T_a=-40$ to $+85^{\circ}C$, unless otherwise specified)

| Parameter | Symbol | Conditon | Rating | | | Unit |
|--|------------|---|----------------------------|----------------------------|----------------------------|---------|
| | | | Min. | Typ. | Max. | |
| SCK input cycle (slave mode) | t_{SCYC} | High-speed oscillation is not active | 10 | – | – | μs |
| | | High-speed oscillation is active | 500 | – | – | ns |
| SCK output cycle (master mode) | t_{SCYC} | – | – | SCK* ¹ | – | s |
| SCK input pulse width (slave mode) | t_{SW} | High-speed oscillation is not active | 4 | – | – | μs |
| | | High-speed oscillation is active | 200 | – | – | ns |
| SCK output pulse width (master mode) | t_{SW} | – | t_{SCYC} $\times 0.4$ | t_{SCYC} $\times 0.5$ | t_{SCYC} $\times 0.6$ | s |
| SOUT output delay time (slave mode) | t_{SD} | – | – | – | 180 | ns |
| SOUT output delay time (master mode) | t_{SD} | – | – | – | 80 | ns |
| SIN input Setup time (slave mode) | t_{SS} | – | 50 | – | – | ns |
| SIN input Setup time (master mode) | t_{SS} | – | 130 | – | – | ns |
| SINinput Hold time | t_{SH} | – | 50 | – | – | ns |

*¹ : The clock period which is selected by the below registers(min:250ns@ regularly, min:500ns@P02,P22 is used)
 In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).
 In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)



● AC characteristics (I²C Bus interface : Standard mode 100kHz)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

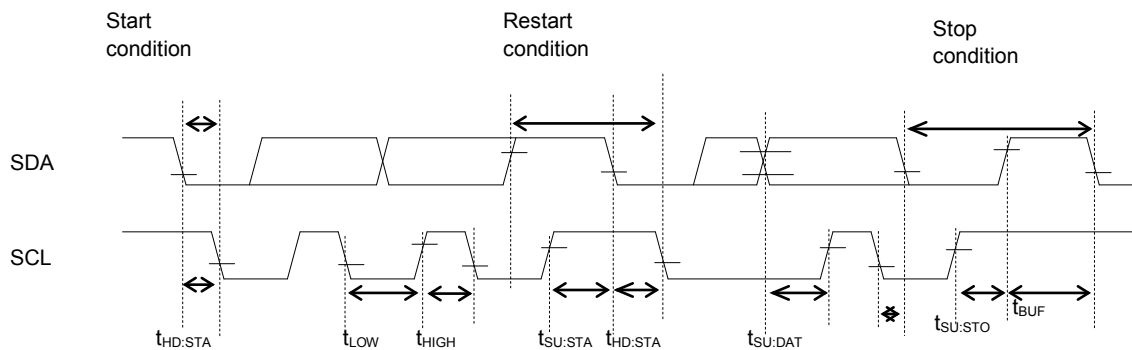
| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---------------------|-----------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f _{SCL} | — | 0 | — | 100 | kHz |
| SCL hold time (Start/restart condition) | t _{HD:STA} | — | 4.0 | — | — | μs |
| SCL "L" level time | t _{LOW} | — | 4.7 | — | — | μs |
| SCL "H" level time | t _{HIGH} | — | 4.0 | — | — | μs |
| SCL setup time (restart condition) | t _{SU:STA} | — | 4.7 | — | — | μs |
| SDA setup time | t _{SU:DAT} | — | 0.25 | — | — | μs |
| SDA setup time (stop condition) | t _{SU:STO} | — | 4.0 | — | — | μs |
| Bus-free time | t _{BUF} | — | 4.7 | — | — | μs |

● AC characteristics (I²C bus interface : fast mode 400kHz)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---------------------|-----------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | f _{SCL} | — | 0 | — | 400 | kHz |
| SCL hold time (start/restart condition) | t _{HD:STA} | — | 0.6 | — | — | μs |
| SCL "L" level time | t _{LOW} | — | 1.3 | — | — | μs |
| SCL "H" level time | t _{HIGH} | — | 0.6 | — | — | μs |
| SCL setup time (restart condition) | t _{SU:STA} | — | 0.6 | — | — | μs |
| SDA setup time | t _{SU:DAT} | — | 0.1 | — | — | μs |
| SDA setup time (stop condition) | t _{SU:STO} | — | 0.6 | — | — | μs |
| Bus-free time | t _{BUF} | — | 1.3 | — | — | μs |

*1: Only at the time of SYSCLK=16MHz or 24MHz



● AC characteristics (RC-ADC)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

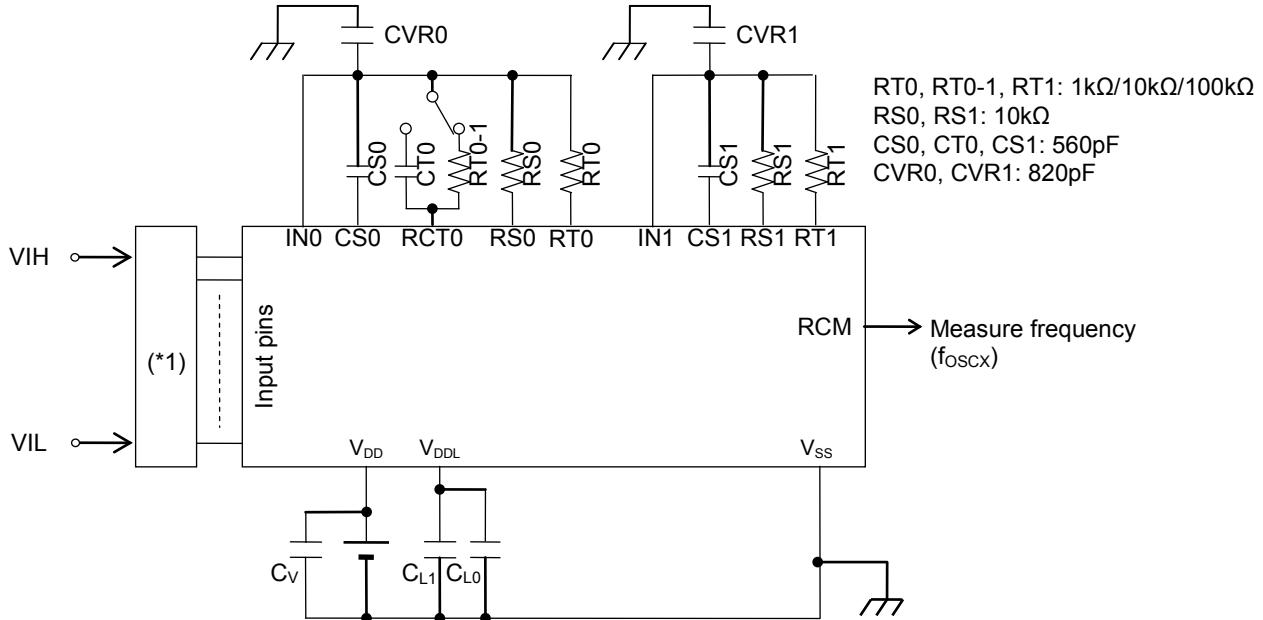
| Parameter | Symbol | Condition | Rating | | | unit |
|--|------------------------|---------------------------------|--------|-------|-------|------|
| | | | Min. | Typ. | Max. | |
| Resister for oscillation | RS0,RS1,RT0, RT0-1,RT1 | - | 1 | - | 400 | kΩ |
| Oscillation frequency V _{DD} = 3.0V CVR=820pF CS=560pF | f _{osc1_0} | Resister for oscillation =1kΩ | - | 528 | - | kHz |
| | f _{osc2_0} | Resister for oscillation =10kΩ | - | 59 | - | kHz |
| | f _{osc3_0} | Resister for oscillation =100kΩ | - | 5.9 | - | kHz |
| RS to RT oscillation frequency ratio *1 V _{DD} = 3.0V CVR=820pF CS=560pF | Kf1_0 | RT0, RT0-1, RT1=1kΩ | 8.225 | 8.94 | 9.655 | - |
| | Kf2_0 | RT0, RT0-1, RT1=10kΩ | 0.99 | 1 | 1.01 | - |
| | Kf3_0 | RT0, RT0-1, RT1=100kΩ | 0.093 | 0.101 | 0.109 | - |

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{oscx} (RT0-CS0 \text{ oscillation})}{f_{oscx} (RS0-CS0 \text{ oscillation})}, \quad \frac{f_{oscx} (RT0-1-CS0 \text{ oscillation})}{f_{oscx} (RS0-CS0 \text{ oscillation})}, \quad \frac{f_{oscx} (RT1-CS1 \text{ oscillation})}{f_{oscx} (RS1-CS1 \text{ oscillation})}$$

(x = 1, 2, 3)

Measuring circuit



(*1) Input logic circuit to determine the specified measuring conditions.

[Note]

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please shield the signal by V_{SS}(GND).
- Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

● AC characteristics (Low speed clock output)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

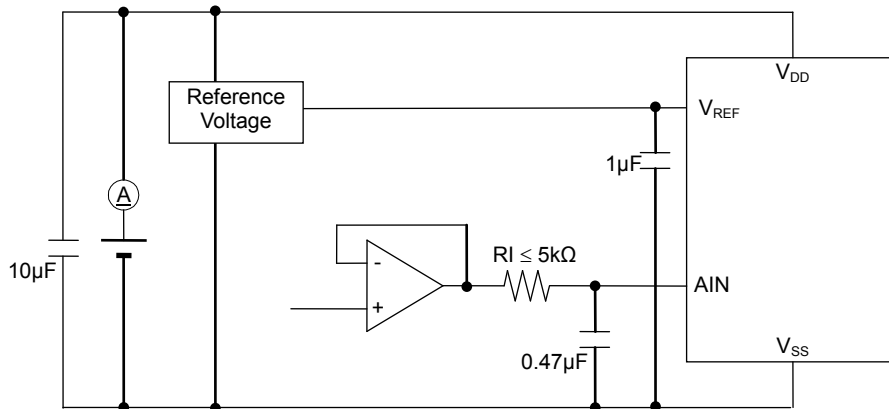
| Parameter | Symbol | Condition | Rating | | | Unit |
|------------------------|--------|-----------|--------|--------|------|------|
| | | | Min. | Typ. | Max. | |
| Clock output frequency | clk | – | – | 32.768 | – | kHz |

● Electrical Characteristics of SA-ADC

($V_{DD}=1.8$ to $3.6V$, $V_{SS}=0V$, $T_a=-40\sim+85^{\circ}C$, unless otherwise specified)

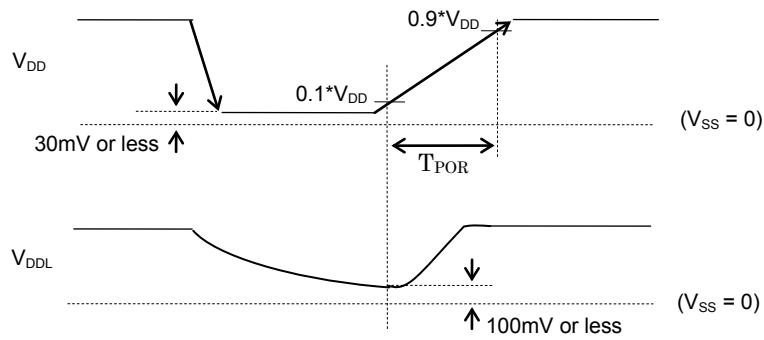
| Parameter | Symbol | Condition | Rating | | | Unit |
|----------------------------------|------------|---|--------|------|----------|----------|
| | | | Min. | Typ. | Max. | |
| Resolution | n | — | — | 12 | — | bit |
| Integral non-linearity error | INL | $2.7V \leq V_{REF} \leq 3.6V$ | -4 | — | +4 | LSB |
| | | $2.2V \leq V_{REF} < 2.7V$ | -6 | — | +6 | |
| | | $1.8V \leq V_{REF} < 2.2V$ (using Low-speed clock) | -10 | — | +10 | |
| Differential non-linearity error | DNL | $2.7V \leq V_{REF} \leq 3.6V$ | -3 | — | +3 | |
| | | $2.2V \leq V_{REF} < 2.7V$ | -5 | — | +5 | |
| | | $1.8V \leq V_{REF} < 2.2V$ (using Low-speed clock) | -9 | — | +9 | |
| Zero-scale error | V_{OFF} | $2.2V \leq V_{REF} \leq 3.6V$ | -6 | — | +6 | |
| | | $1.8V \leq V_{REF} < 2.2V$ (using Low-speed clock) | -10 | — | +10 | |
| Full-scale error | FSE | $2.2V \leq V_{REF} \leq 3.6V$ | -6 | — | +6 | |
| | | $1.8V \leq V_{REF} < 2.2V$ (using Low-speed clock) | -10 | — | +10 | |
| Input impedance | RI | — | — | — | 5k | Ω |
| Reference voltage | V_{REF} | — | 1.8 | — | V_{DD} | V |
| Conversion time | t_{CONV} | Using High-speed clock(max. 4MHz) | — | 170 | — | clk |
| | | Using Low-speed clock | — | 16 | — | |

Measuring circuit



- Power-on and shutdown Procedures

In case of power-on or shutdown of V_{DD} , the procedures and constraints are shown as following.

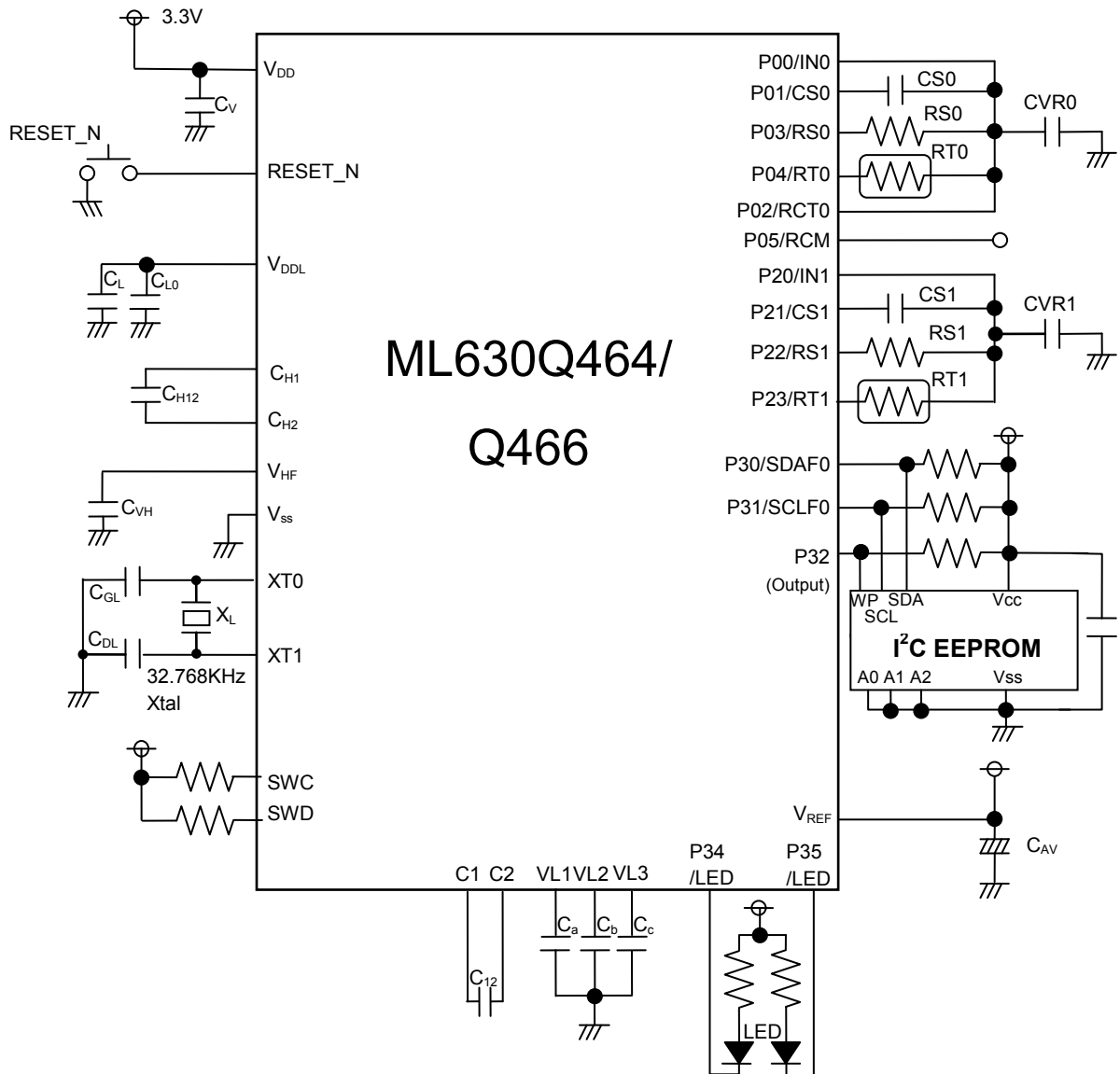


Power down/on and power on reset sequence

Note:

If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.

APPLICATION CIRCUIT EXAMPLE



| | | | |
|------------------|------------------------------|------------|-----------------|
| C_V | : 1 μ F* | C_{L0} | : open* |
| C_L | : 2.2 μ F | C_{12} | : 1 μ F* |
| C_{GL}, C_{DL} | : 12 to 16pF* | C_{VH} | : 1 μ F* |
| $C_a \sim C_c$ | : 1 μ F* | RS0, RS1 | : 10 K Ω |
| C_{H12} | : 1 μ F* | CVR0, CVR1 | : 820 pF |
| C_{AV} | : 1 μ F* | | |
| CS0, CS1 | : 560 pF | | |
| RT0, RT1 | : Thermistor (103AT/Semitec) | | |
| X_L | : DT-26, Daishinku | | |

*: Make a decision the parameters after evaluating on user's conditions when designing circuits for mass production.

PACKAGE DIMENSIONS

ML630Q464/Q466 PACKAGE DIMENSIONS

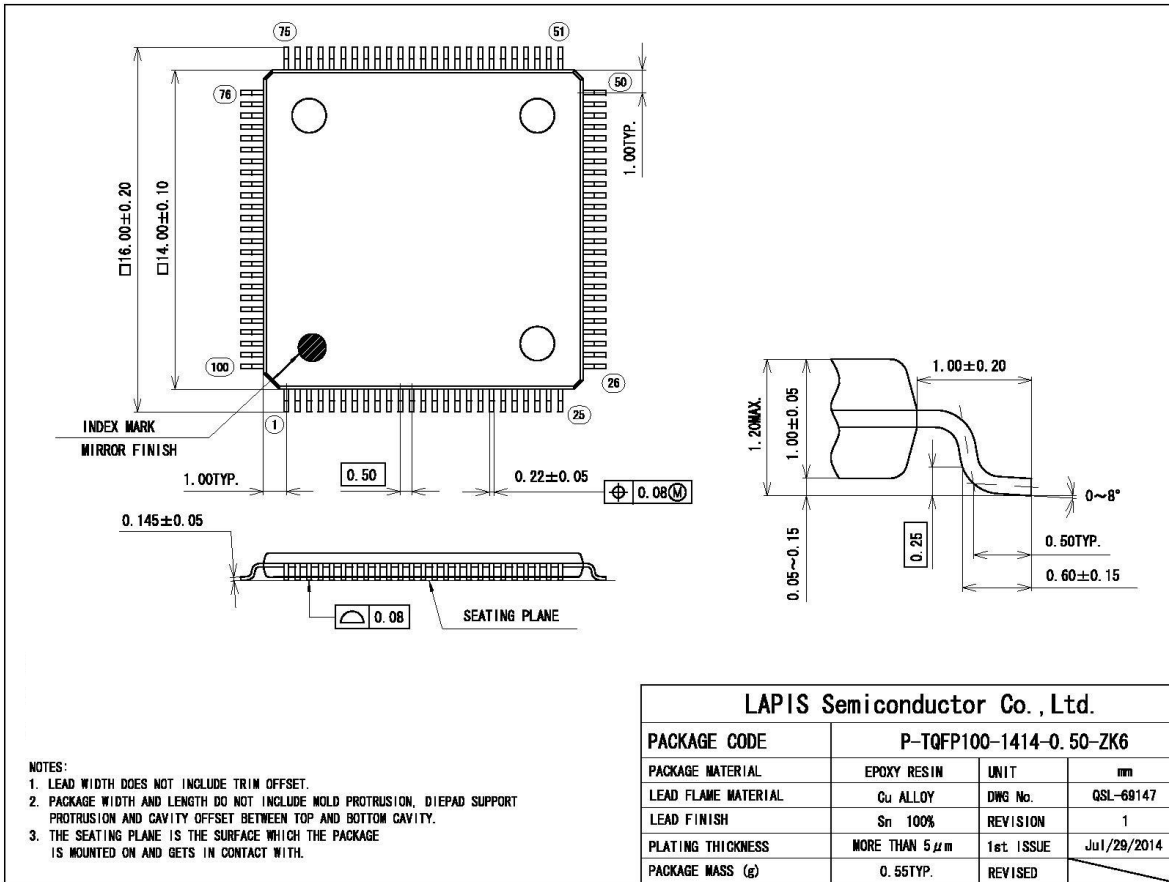


Figure B-1 TQFP100

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions(reflow method, temperature and times).

REVISION HISTORY

| Document No. | Date | Page | | Description |
|----------------|---------------|------------------|-----------------|---------------|
| | | Previous Edition | Current Edition | |
| FEDL630Q464-01 | Oct. 26. 2016 | - | - | Final Edition |

Notes

- 1) The information contained herein is subject to change without notice.
- 2) Although LAPIS Semiconductor is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. LAPIS Semiconductor shall have no responsibility for any damages arising out of the use of our Products beyond the rating specified by LAPIS Semiconductor.
- 3) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.
- 4) The technical information specified herein is intended only to show the typical functions of the Products and examples of application circuits for the Products. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Semiconductor or any third party with respect to the information contained in this document; therefore LAPIS Semiconductor shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.
- 5) The Products are intended for use in general electronic equipment (i.e. AV/OA devices, communication, consumer systems, gaming/entertainment sets) as well as the applications indicated in this document.
- 6) The Products specified in this document are not designed to be radiation tolerant.
- 7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a LAPIS Semiconductor representative: transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.
- 8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.
- 9) LAPIS Semiconductor shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.
- 10) LAPIS Semiconductor has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Semiconductor does not warrant that such information is error-free and LAPIS Semiconductor shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.
- 11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. LAPIS Semiconductor shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.
- 12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.
- 13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Semiconductor.

Copyright 2016 LAPIS Semiconductor Co., Ltd.

LAPIS Semiconductor Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku,
Yokohama 222-8575, Japan
<http://www.lapis-semi.com/en/>