MICROELECTRONICS

PHY6212

Bluetooth LE 5.2 System on Chip

Key Features

- ARM® Cortex™-M0 32-bit processor
- Memory
  - 512KB/2MB in-system flash memory
  - 128KB ROM
  - 138KB SRAM, all programmable retention in sleep mode
  - 8-channel DMA
- 33/19 general purpose I/O pins
  - All pins can be configured as serial interface and programmable IO MUX function mapping
  - All pins can be configured for wake-up
  - 18 pins for triggering interrupt
  - 3 quadrature decoder(QDEC)
  - 6-channel PWM
  - 4-channel I2S
  - 2-channel PDM
  - 2-channel I2C
  - 2-channel SPI
  - 1-channel UART
  - JTAG
- DMIC/AMIC with microphone bias
- 3/8-channel 12bit ADC with low noise voice PGA
- 4-channel 24bit timer, one watchdog timer
- Real timer counter (RTC)
- Power, clock, reset controller
- Flexible power management
  - Supply voltage range 1.8V to 3.6V
  - Embedded buck DC-DC and LDOs
  - Battery monitor: Supports low battery detection
- Power consumption
  - 0.7μA @ OFF Mode (IO wake up only)
  - 2μA @ Sleep Mode with 32KHz RTC
  - Receiver: 6.7mA @sensitivity level
  - Transmitter: 6.7mA @0dBm TX power
- RC oscillator hardware calibrations
  - 32KHz RC osc for RTC with +/-500ppm accuracy
  - 32MHz RC osc for HCLK with 3% accuracy
- High Speed Throughput
  - Support BLE 2Mbps Protocol
  - Support Data Length Extension
  - Throughput up to 1.6Mbps(DLE+2Mbps)
- Support SIG-Mesh Multi-Feature
  - Friend Node
  - Low Power Node
  - Proxy Node
  - Relay Node
- 2.4 GHz transceiver
  - Compliant to Bluetooth 5.2
  - Sensitivity:
    -97dBm@BLE 1Mbps data rate
    -103dBm@BLE 125Kbps data rate
  - TX Power -20 to +10dBm in 3dB steps
  - Single-pin antenna: no RF matching or RX/TX switching required
  - RSSI (1dB resolution)
- AES-128 encryption hardware
- Link layer hardware
  - Automatic packet assembly
  - Automatic packet detection and validation
  - Auto Re-transmit
  - Auto ACK
  - Hardware Address Matching
  - Random number generator
- Operating temperature:
  - -40˚C ~+85 ˚C (Consumer)
  - -40 ˚C ~+105 ˚C (Industrial)
- RoHS Package: QFN48/ QFN32
- Applications: wearables, beacons, appliances, home and building, health and medical, sports and fitness, industrial and manufacturing, retail and payment, security, data transmission, remote control, PC/mobile/TV peripherals, internet of things (IoT)

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Revision History

Date	Version	Description
2018.05	1.0	
2019.06	1.1	Added “GPIO DC Characteristics”
2019.07	1.1	1. Added “Power consumption” in the home page 2. Added information about accuracy of RC osc in the home page
2019.08	1.2	Added “DMIC/AMIC Data Path”
2019.10	1.3	1. Updated the information of “Ordering information” 2. Updated the information of “in-system flash memory” and “Power consumption”
2019.11	1.4	Corrected the information of “PHY6212 (QFN32) Pin Functions – Pin2, 3, 4, 5, 7, 8”
2021.4	1.5	The following content has been added, updated or corrected: • **“Operating Temperature”** on cover: Added the temperature information of “Consumer” and “Industrial". • **“6 Operating Conditions”** on page 63: Added the temperature specification of “Consumer” and “Industrial” in Table 30. • **Message of 2.4GHz transceiver** has been updated to “Compliant to Bluetooth 5.2”, on cover.
2021.7	1.6	The following content has been added, updated or corrected: • **“9 Ordering Information”** and **“10 Chip Marking”** have been consolidated into one, on page 72. • **Maximum MSL** parameter updated: “Moisture Sensitivity Level: 3”.

Table of Contents

1 Introduction

PHY6212 is a System on Chip (SoC) for Bluetooth LE 5.2 applications. PHY6212 has 32-bit ARM® Cortex™-M0 CPU with 138KSRAM/Retention SRAM and an ultra-low power, high performance, multi-mode radio. PHY6212 can support BLE with security, application and over-the-air download update. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

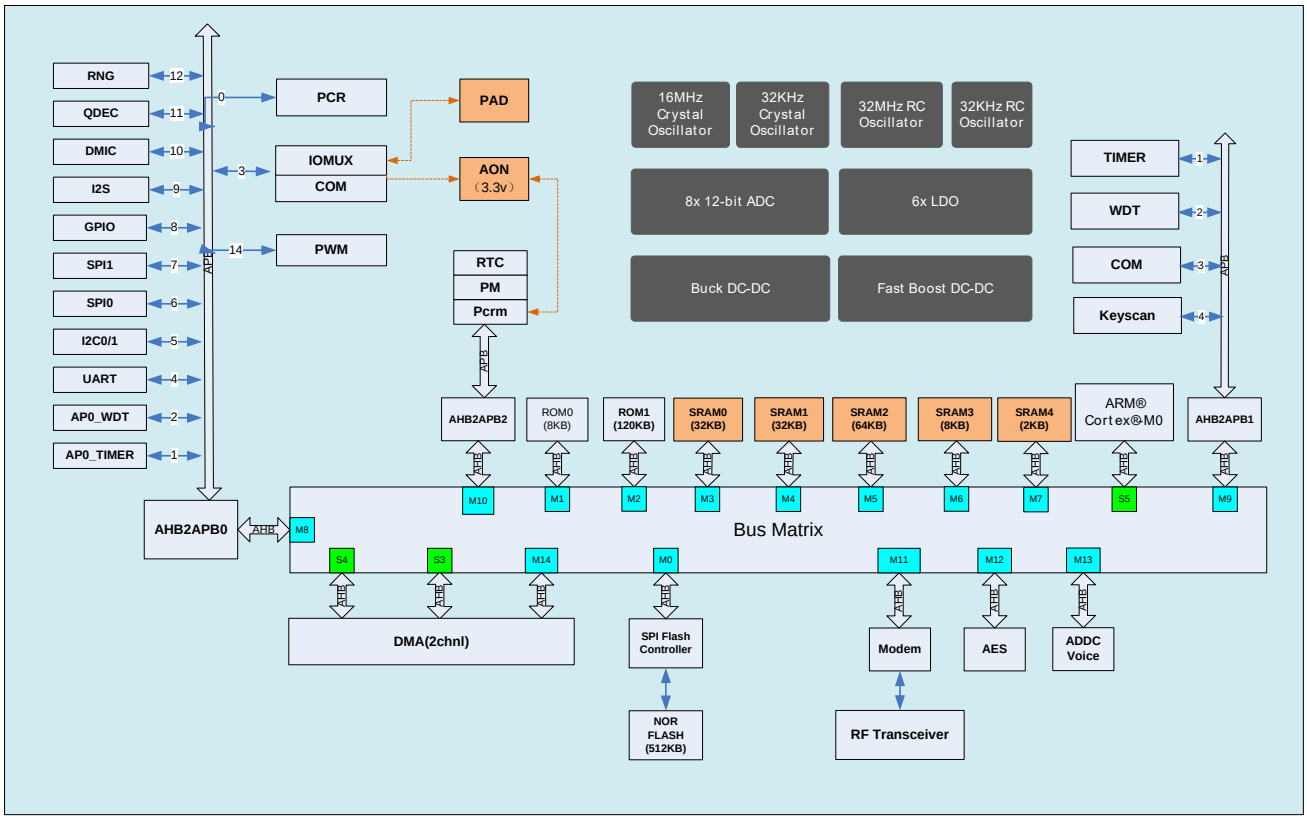


Figure 1: PHY6212 block diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the different package types.

2.2.1 PHY6212 (QFN48)

2.2.1.1 Pin Assignment

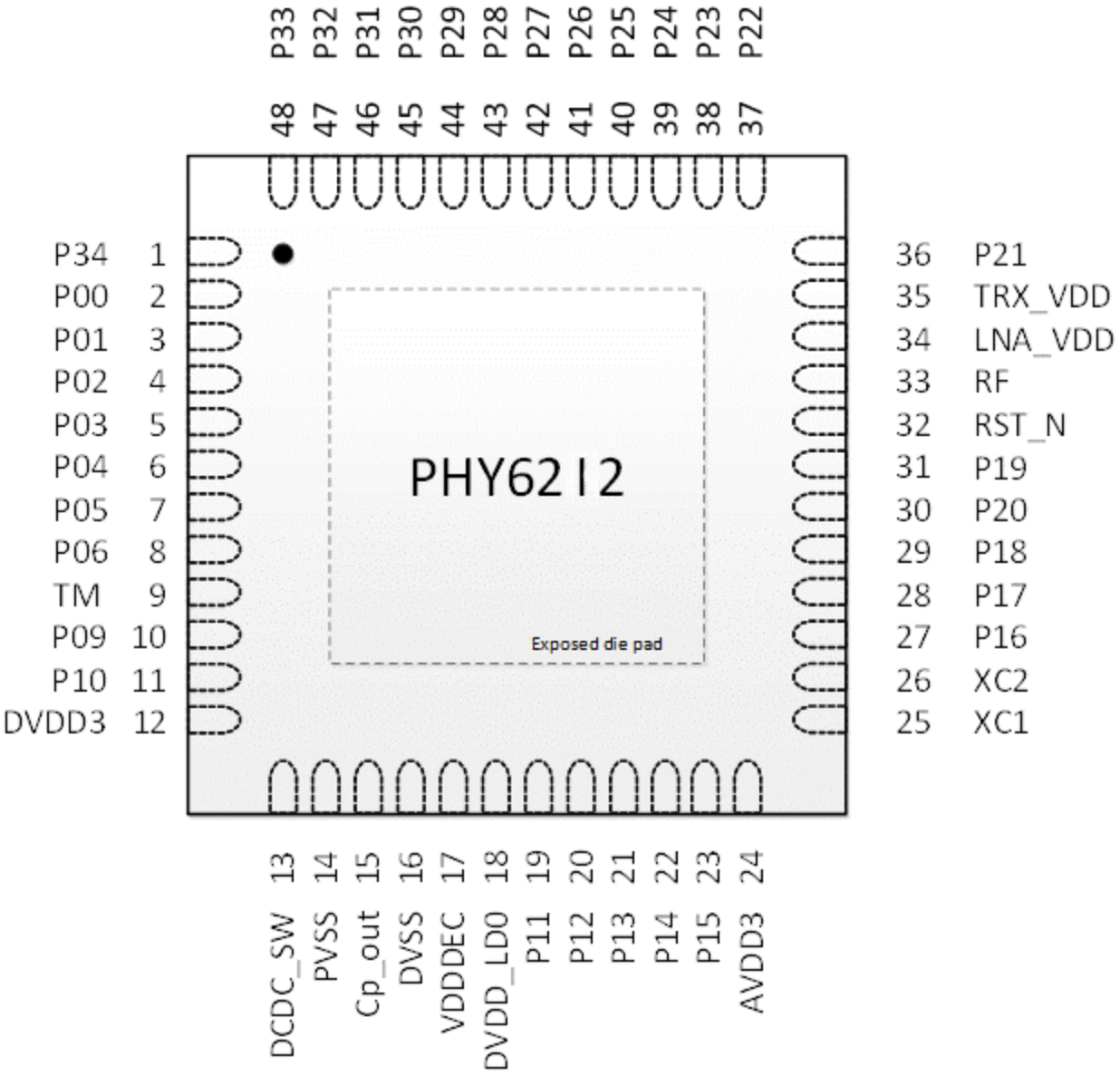


Figure 2: Pin assignment - PHY6212 QFN48 package

2.2.1.2 Pin Function

Pin	Pin name	Description
1	P34	all functions configurable *Note: Not support interrupt and ADC function
2	P00	all functions configurable/ JTAG_TDO *Note: Not support ADC function
3	P01	all functions configurable/ JTAG_TDI *Note: Not support ADC function
4	P02	all functions configurable/JTAG_TMS *Note: Not support ADC function
5	P03	all functions configurable/JTAG_TCK *Note: Not support ADC function
6	P04	all functions configurable *Note: Not support ADC function
7	P05	all functions configurable *Note: Not support ADC function
8	P06	all functions configurable *Note: Not support ADC function
9	TM	Test_Mode
10	P09	all functions configurable *Note: Not support ADC function
11	P10	all functions configurable *Note: Not support ADC function
12	DVDD3	3V power supply for digital IO, DCDC, Charge pump
13	DCDC_SW	Buck dcdc output
14	PVSS	Buck dcdc and charge pump power vss
15	cp_out	charge pump output
16	DVSS	digital vss
17	VDDDEC	1.2V VDD_CORE, digital LDO output
18	DVDD_LDO	digital LDO input
19	P11	all functions configurable/AIO<0>
20	P12	all functions configurable/AIO<1>
21	P13	all functions configurable/AIO<2>
22	P14	all functions configurable/AIO<3>
23	P15	all functions configurable/AIO<4>
24	AVDD3	3V power supply for analog IO, bg, rcosc, etc
25	XC1	16M crystal input
26	XC2	16M crystal output
27	P16	all functions configurable/AIO<5>/32K crystal input
28	P17	all functions configurable/AIO<6>/32k crystal output

Pin	Pin name	Description
29	P18	all functions configurable/AIO<7>/PGA differential positive input *Note: Not support interrupt function
30	P20	all functions configurable/AIO<9>/Micphone bias output *Note: Not support interrupt function
31	P19	all functions configurable/AIO<8>/PGA differential negative input *Note: Not support interrupt function
32	RST_N	reset pin
33	RF	RF antenna
34	LNA_VDD	LNA_VDD
35	TRX_VDD	TRX_VDD
36	P21	all functions configurable *Note: Not support interrupt function and ADC function
37	P22	all functions configurable *Note: Not support interrupt function and ADC function
38	P23	all functions configurable *Note: Not support interrupt function and ADC function
39	P24	all functions configurable/test_mode_select[0] *Note: Not support interrupt function and ADC function
40	P25	all functions configurable/test_mode_select[1] *Note: Not support interrupt function and ADC function
41	P26	all functions configurable *Note: Not support interrupt function and ADC function
42	P27	all functions configurable *Note: Not support interrupt function and ADC function
43	P28	all functions configurable *Note: Not support interrupt function and ADC function
44	P29	all functions configurable *Note: Not support interrupt function and ADC function
45	P30	all functions configurable *Note: Not support interrupt function and ADC function
46	P31	all functions configurable *Note: Not support interrupt function and ADC function
47	P32	all functions configurable *Note: Not support interrupt function and ADC function
48	P33	all functions configurable *Note: Not support interrupt function and ADC function

Table 1: Pin functions PHY6212 QFN48 package

2.2.2 PHY6212 (QFN32)

2.2.2.1 Pin Assignment

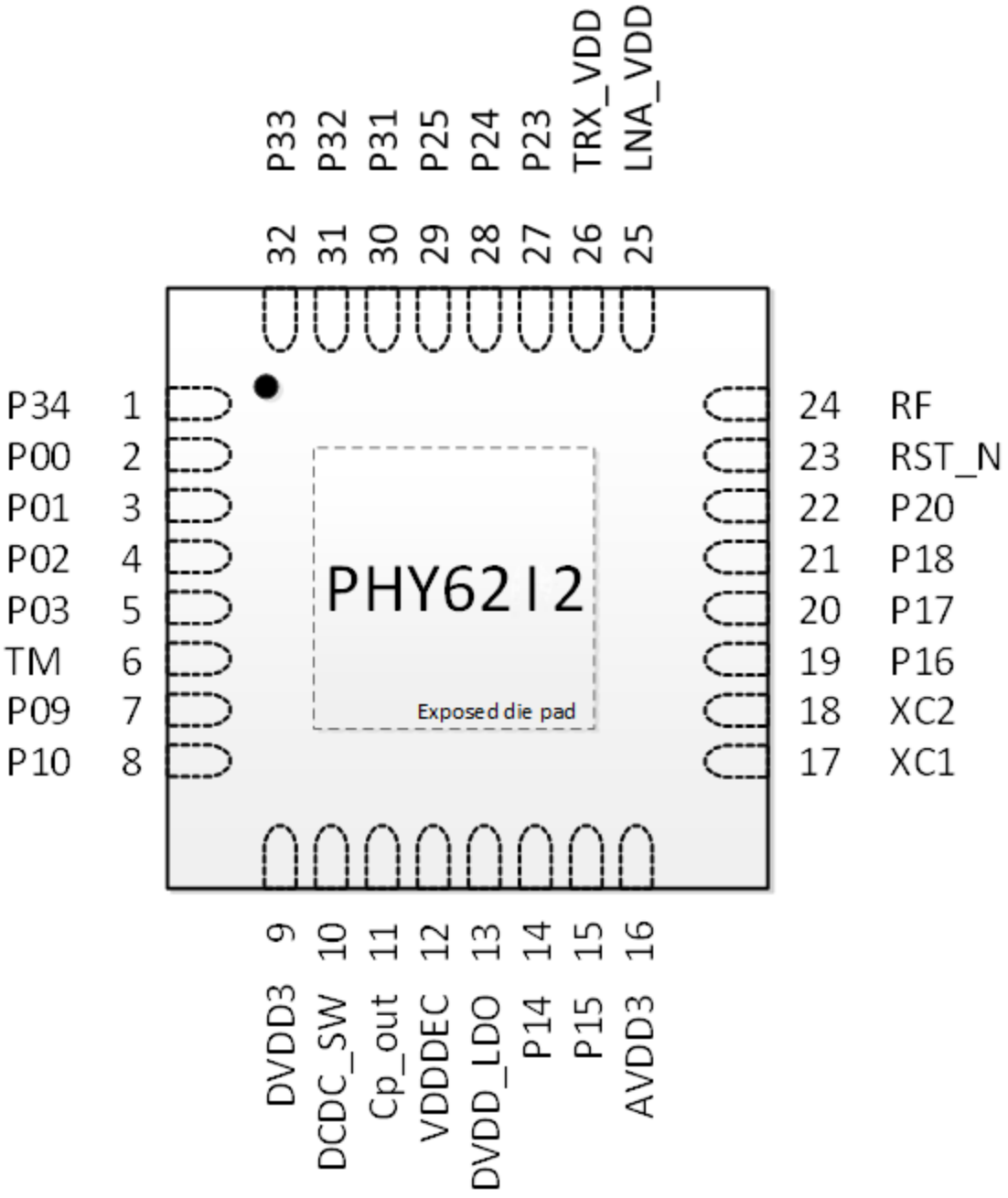


Figure 3: Pin assignment - PHY6212 QFN32 package

2.2.2.2 Pin Functions

Pin	Pin name	Description
1	P34	all functions configurable *Note: Not support interrupt and ADC function
2	P00	all functions configurable/ JTAG_TDO *Note: Not support ADC function
3	P01	all functions configurable/ JTAG_TDI *Note: Not support ADC function
4	P02	all functions configurable/ JTAG_TMS *Note: Not support ADC function
5	P03	all functions configurable/ JTAG_TCK *Note: Not support ADC function
6	TM	Test_Mode
7	P09	all functions configurable *Note: Not support ADC function
8	P10	all functions configurable *Note: Not support ADC function
9	DVDD3	3V power supply for digital IO, DCDC, Charge pump
10	DCDC_SW	Buck dcdc output
11	cp_out	charge pump output
12	VDDDEC	1.2V VDD_CORE, digital LDO output
13	DVDD_LDO	digital LDO input
14	P14	all functions configurable/AIO<3>
15	P15	all functions configurable/AIO<4>
16	AVDD3	3V power supply for analog IO, bg, rcosc, etc
17	XC1	16M crystal input
18	XC2	16M crystal output
19	P16	all functions configurable/AIO<5>/32K crystal input
20	P17	all functions configurable/AIO<6>/32k crystal output
21	P18	all functions configurable *Note: Not support interrupt function
22	P20	all functions configurable/AIO<9>/Micphone bias output
23	RST_N	reset pin
24	RF	RF antenna
25	LNA_VDD	LNA_VDD
26	TRX_VDD	TRX_VDD
27	P23	all functions configurable *Note: Not support interrupt and ADC function
28	P24	all functions configurable/test_mode_select[0] *Note: Not support interrupt and ADC function
29	P25	all functions configurable/test_mode_select[1] *Note: Not support interrupt and ADC function
30	P31	all functions configurable *Note: Not support interrupt and ADC function
31	P32	all functions configurable *Note: Not support interrupt and ADC function
32	P33	all functions configurable *Note: Not support interrupt and ADC function

Table 2: Pin functions PHY6212 QFN32 package

3 System Blocks

The system block diagram of PHY6212 is shown in **Figure 1**.

3.1 CPU

The PHY6212 has an ARM Cortex-M0 CPU. The CPU, memories, and all peripherals are connected by AMBA bus fabrics.

The ARM® Cortex™-M0 CPU has a 16-bit instruction set with 32-bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32-bit multiplier, a 3-stage pipeline and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex™-M0 CPU makes program execution simple and highly efficient.

The main features of ARM® Cortex™-M0 CPU are listed below.

- Up to 96Mhz ARM Cortex™-M0 processor core.
    - Low gate count and high energy efficient.
    - ARMv6M architecture, Thumb ISA but no ARM ISA.
    - No cache and no TCM.
    - Up to 32 interrupts embedded NVIC.
    - SysTick timer.
    - Sleep/deep sleep mode.
    - Support low power WFI and WFE.
- Tight integration of system peripherals reduces area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- power control optimization of system components
- Integrated sleep modes for low power consumption
- Fast code execution permits slower processor clock or increases sleep mode time
- Hardware multiplier
- Deterministic, high-performance interrupt handling for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging.
- APB interface to/from BLE modem.
- Dynamic and static clock gating to save power.
- No TRACE.

Some of these features are shared with the AP subsystem.

3.2 Memory

PHY6212 has total 128KB ROM, 138KB SRAM and up to 512KB FLASH. The physical address space of these memories is shown in **Figure4**.

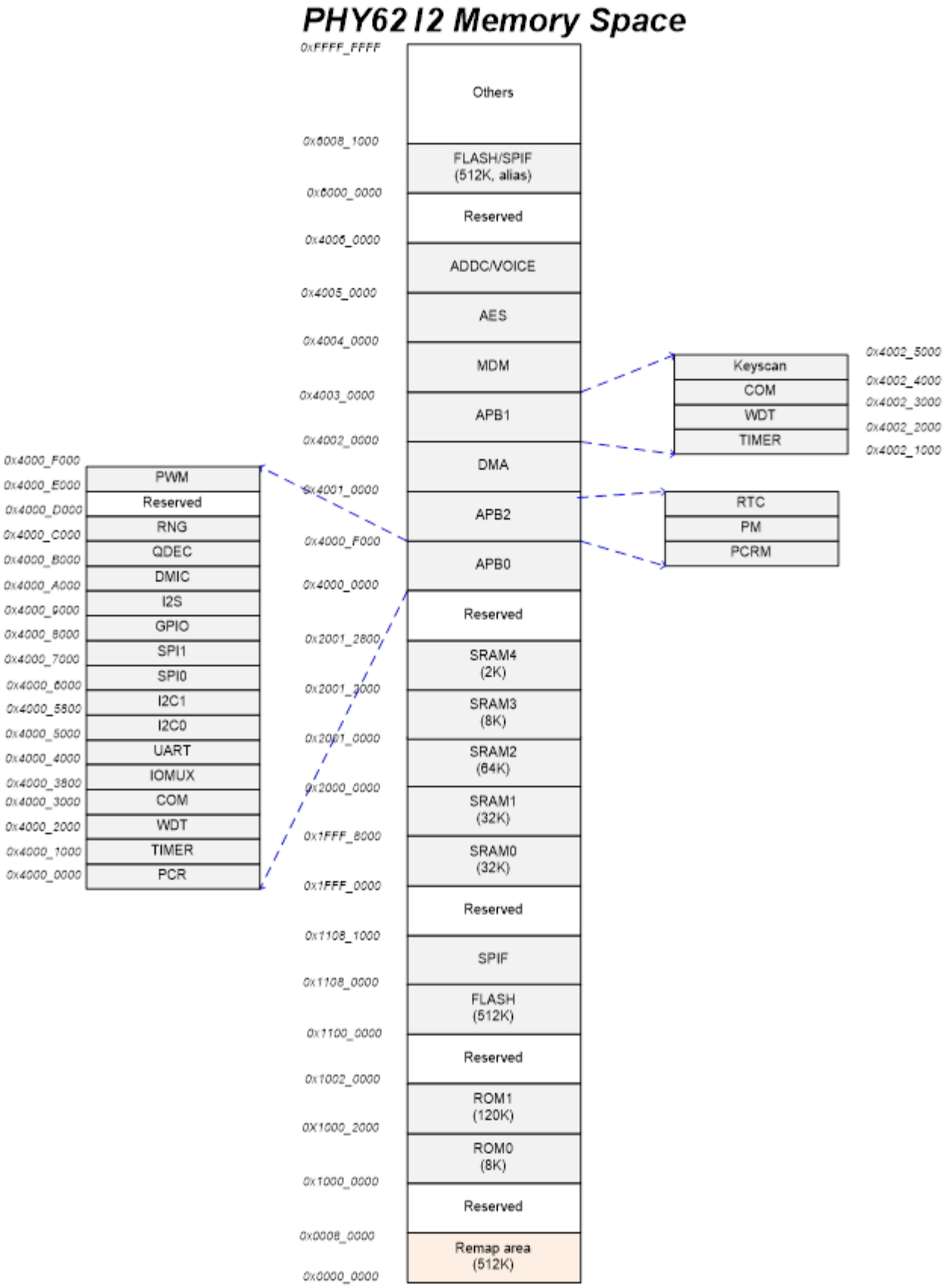


Figure 4: PHY6212 memory space

3.2.1 ROM

PHY6212 has 2 ROMs.

	SIZE	CONTENT
ROM0	8KB	Reserved
ROM1	120KB	Boot ROM for M0. Protocol stack. Common peripheral drivers.

Table 3: List of ROMs

3.2.2 SRAM

PHY6212 has 5 SRAM blocks. All 5 SRAM blocks have retention capability. which can be configured individually. All SRAM blocks can be used to store program or data.

	SIZE	CONTENT
SRAM0	32KB	
SRAM1	32KB	
SRAM2	64KB	
SRAM3	8KB	
SRAM4	2KB	

Table 4: List of SRAMs

3.2.3 FLASH

PHY6212 has FLASH to provide non-volatile program and data storage. The size of the FLASH can be 256KB or 2MB. PHY6212 supports 2-wire reading.

3.2.4 Memory Address Mapping

Name	Size（KB）	Master	Physical Address	CM4 Alias	M0 Remap		
					0	1	2
ROM0	8	M0	1000_0000~1000_1FFF	0x0			
ROM1	120	M0	1000_2000~1001_FFFF		0x0		
RAM0	32	M0	1FFF_0000~1FFF_7FFF				
RAM1	32	M0	1FFF_8000~1FFF_FFFF				
RAM2	64	M0	2000_0000~2000_FFFF			0x0	
RAM3	8	M0	2001_0000~2001_1FFF				
RAM4	2	M0	2001_2000~2001_27FF				
FLASH	512	M0	1100_0000~1107_FFFF				0x0
			6000_0000~6007_FFFF				

Table 5: Memory address mapping

3.3 Boot and Execution Modes

During the boot, the ROM1 is aliased to 0x0 address. The M0 starts to execute the program from the ROM1.

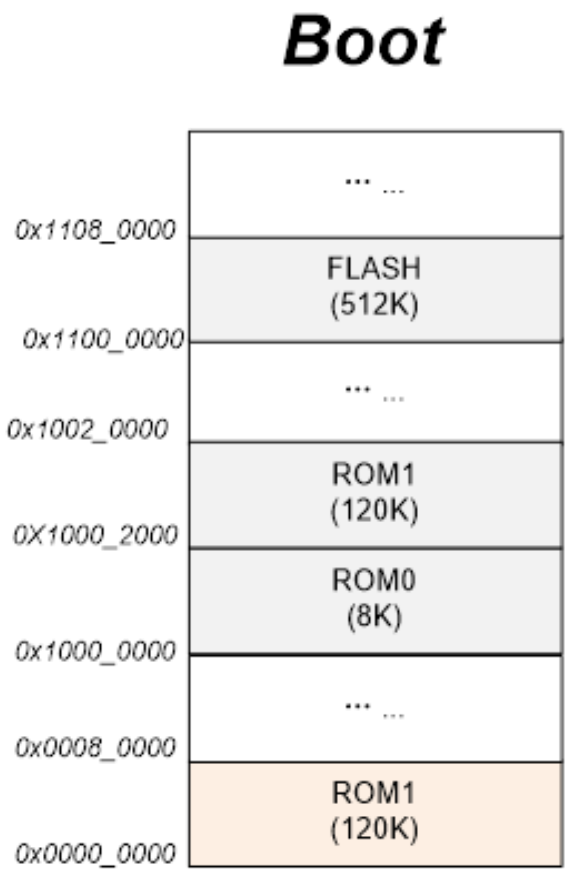


Figure 5: PHY6212 boot mode

3.3.1 Mirror Mode

The mirror mode is not tied to the chip variations. Any chip variation can use mirror mode to execute program. In the mirror mode, the program is copied from the FLASH to the SRAM, then is executed in the SRAM. For the M0 processor, one of the SRAM blocks must be aliased to 0x0 address.

3.3.2 FLASH Mode

The FLASH mode is not tied to the chip variations. Any chip variation can use FLASH mode to execute program. In the FLASH mode, the program is executed in the FLASH. For the M0 processor, the FLASH must be aliased to 0x0 address.

3.3.3 Boot loader

The boot loader in the ROM has the basic structure as shown below. The content in the FLASH should be specifically defined to allow boot loader to identify whether the FLASH content is valid, as shown in the example below. If the FLASH is valid, the ROM boot loader will put the chip in the normal mode and start normal program execution. If the FLASH is not valid, the boot loader will enter FLASH programming mode.

Address	Variable	Content
0	PRODUCT_MODE	Identify the chip mode
4	CODE_BASE	The base address of the code
8	CODE_LEN	The length of the code
C	BOOT_MODE	Identify mirror or FLASH mode

Table 6: Flash content example

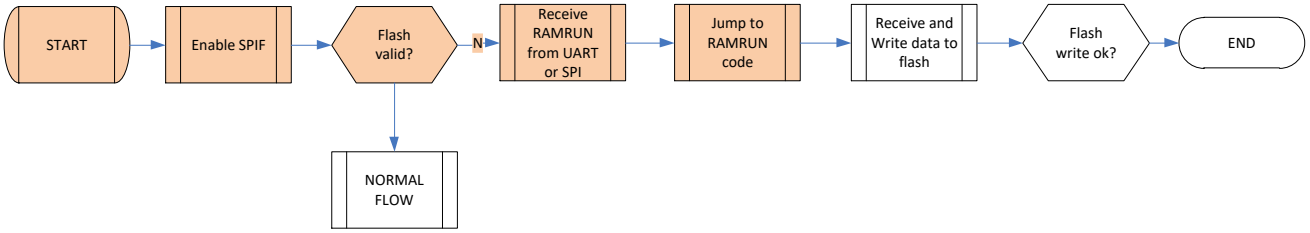


Figure 6: Bootloader flow

3.4 Power, Clock and Reset (PCR)

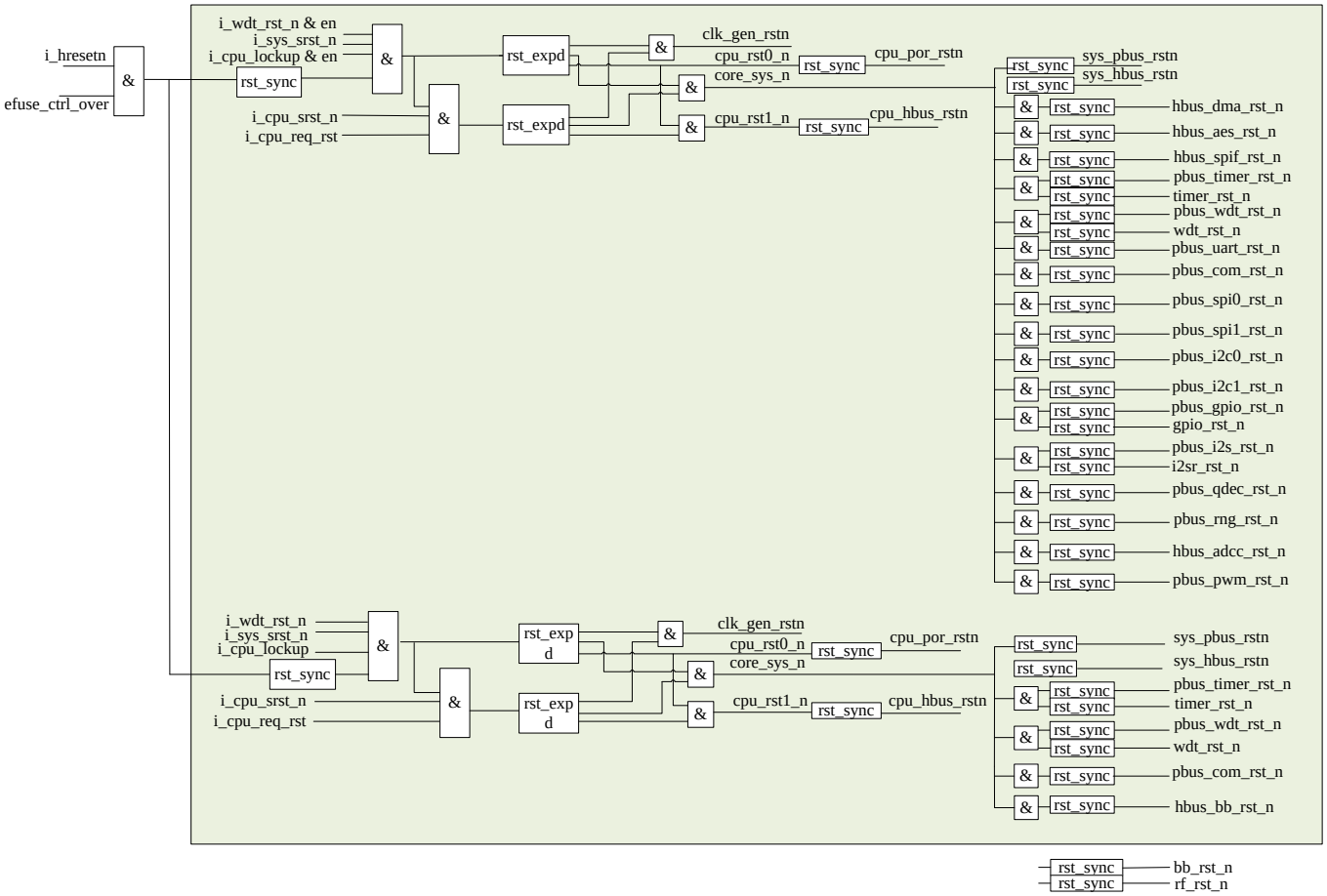


Figure 7: PHY6212 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode

and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

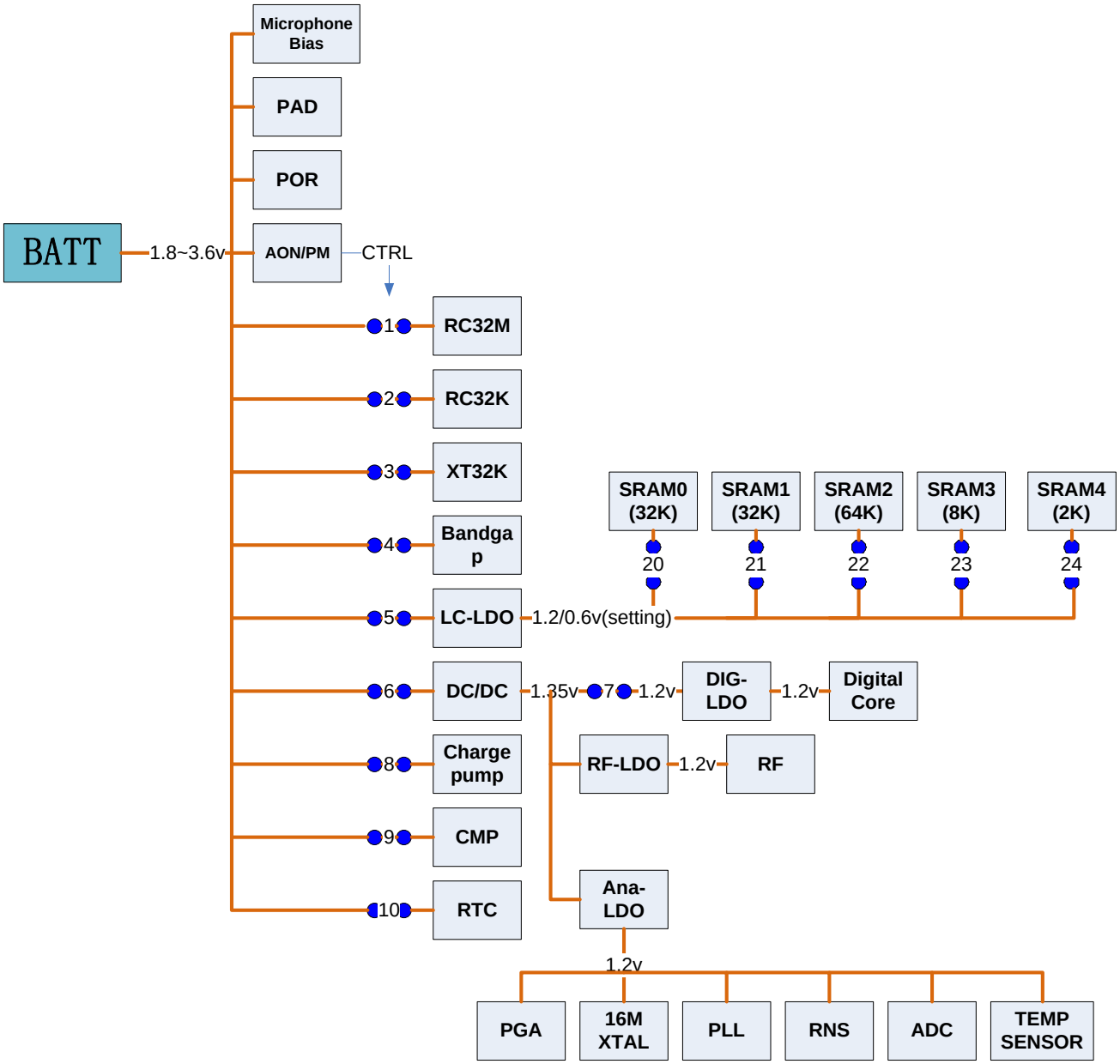


Figure 8: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

Switch	Normal	Sleep	Off
1RC32M	On	Off	Off
2RC32K	On	Optional	Off
3XT32K	On	Optional	Off
4bandgap	On	Off	Off

Switch	Normal	Sleep	Off
5LC-LDO	On	on	Off
6DC/DC	On	Off	Off
7DIG-LDO	On	Off	Off
8charge pump	On	Off	Off
9CMP	On	Optional	Off
10RTC	On	Optional	Off
20SRAM-32K	1.2v	0.6v	0
21SRAM-32K	1.2v	0.6v	0
22SRAM-64K	1.2v	0.6v	0
23SRAM-8K	1.2v	0.6v	0
24SRAM-2K	1.2v	0.6v	0

Table 7: Flash Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include：

- IOs
- RESET
- UVLO reset

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode or FLASH mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep or off mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	M0 Interrupt Number
Reserved	0
Reserved	1
cp_timer_irq	2
cp_wdt_irq	3
bb_irq	4
kscan_irq	5
rtc_irq	6
Reserved	7
Reserved	8
timer_irq	9
wdt_irq	10
uart_irq	11
i2c0_irq	12
i2c1_irq	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
i2s_irq	17
spif_irq	18
dmac_intr	19
dmac_inttc	20
dmac_interr	21
fpidc	22
fpdzc	23
fpioc	24
fpufc	25
fpofc	26
fpixc	27
aes_irq	28
adcc_irq	29
qdec_irq	30
rng_irq	31

Table 8: Interrupts

3.8 Clock Management (CLOCK)

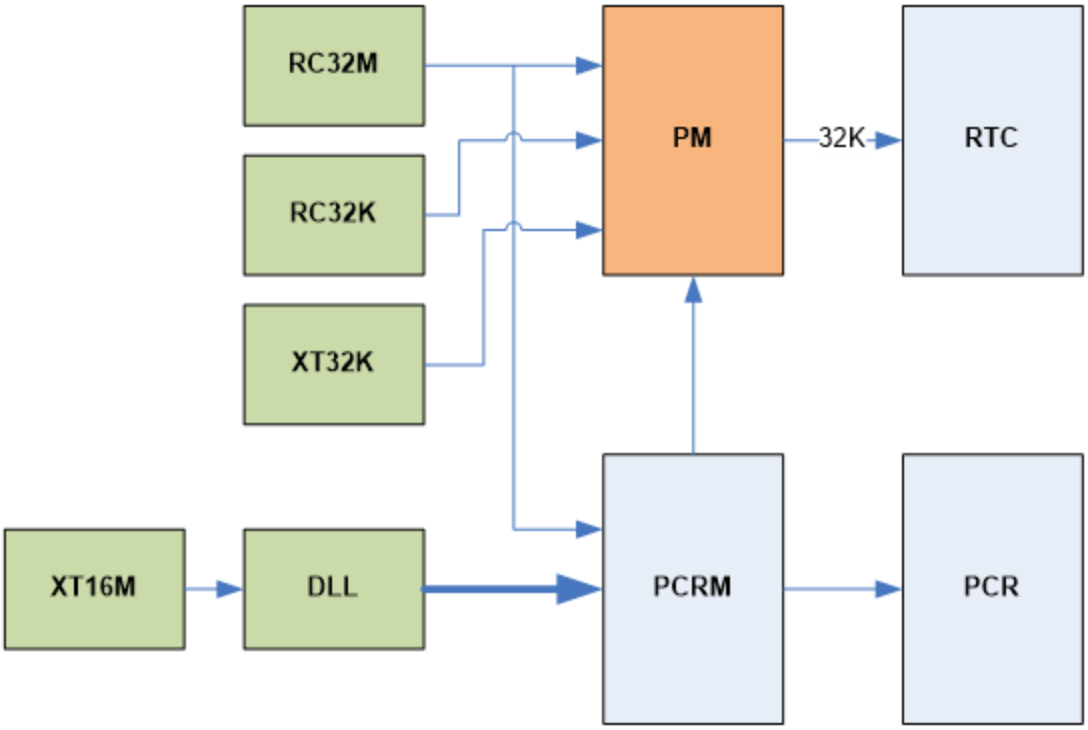


Figure 9: Clock management

There are two crystal clock sources: 16MHz crystal oscillator (XT16M) and 32.768kHz crystal oscillator (XT32k), of which the 32.768k crystal oscillator is optional. There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. If 32.768kHz crystal is not installed, RC32k oscillator would be periodically calibrated and used for RTC. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64/96MHz from the XT16M clock source.

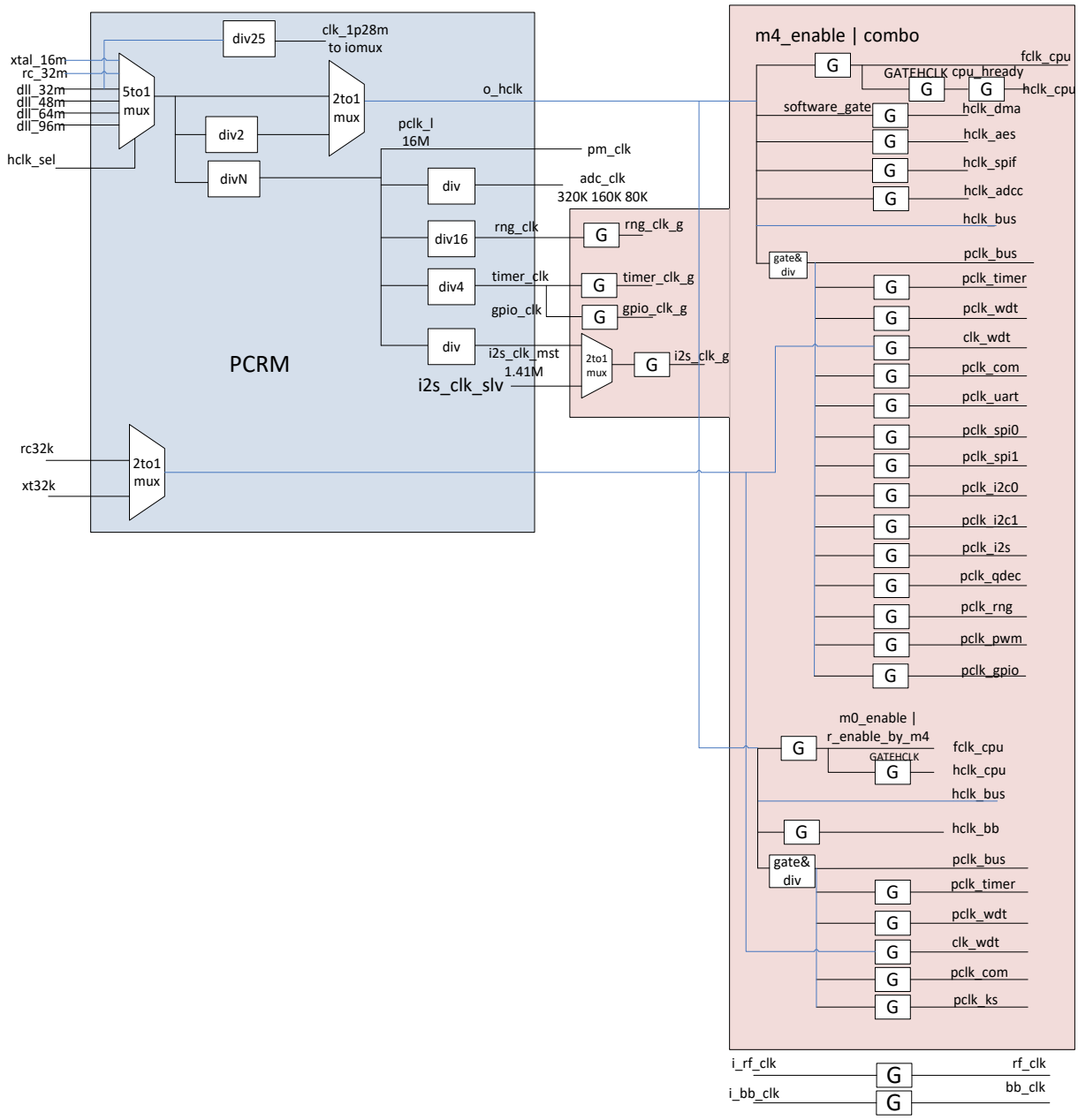


Figure 10: Clock structure diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to any of the physical I/O pads (I/O at die boundary). These peripheral modules include I2C 0-1, I2S, UART, PWM 0-5, SPI 0-1, Quadrature Decoder etc. However for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include JTAG, analog_ios, GPIOs and key scan.

Figure 11 below shows the IOMUX functional diagram.

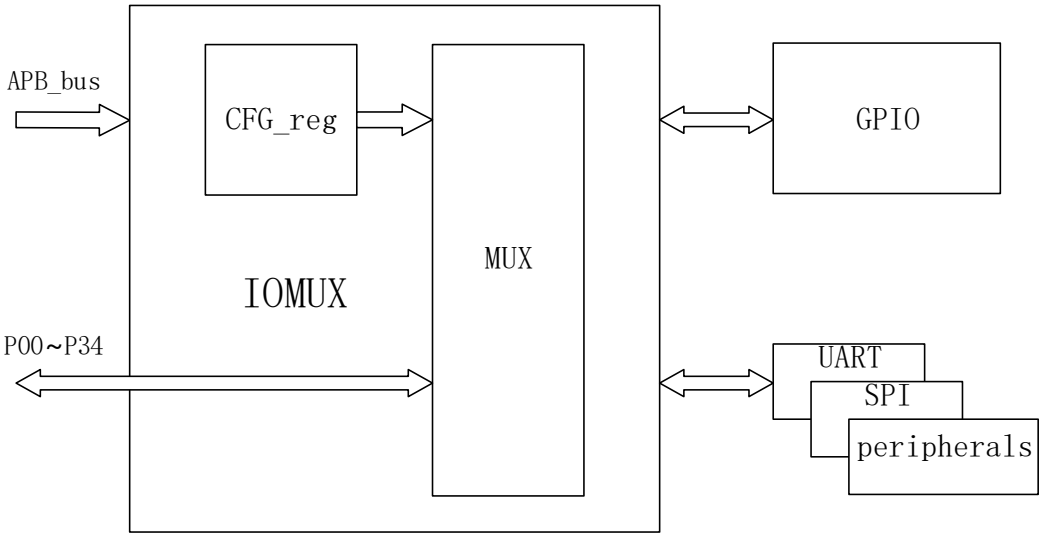


Figure 11: IOMUX structure diagram

There are 34 configurable pads which are from P00 to P07 and from P09 to P34. P08 pad is assigned for TM pin which is a test mode pin. The table blow shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C 0-1, I2S, UART, PWM 0-5, SPI 0-1, Quadrature Decoder, 1.28MHz clock and dmic_out.

Signal Name	IO	FULLMUX
iic0_scl	B	0
iic0_sda	B	1
iic1_scl	B	2
iic1_sda	B	3
i2s_sck	B	4
i2s_ws	B	5
i2s_sdo0	O	6
i2s_sdo1	O	35
i2s_sdo2	O	36
i2s_sdo3	O	37
i2s_sdi0	I	7
i2s_sdi1	I	38
i2s_sdi2	I	39
i2s_sdi3	I	40
uart_tx	O	8
uart_rx	I	9
pwm0	O	10
pwm1	O	11
pwm2	O	12
pwm3	O	13
pwm4	O	14
pwm5	O	15
spi_0_sck	B	16
spi_0_ssn	B	17

Signal Name	IO	FULLMUX
spi_0_tx	O	18
spi_0_rx	I	19
spi_1_sck	B	20
spi_1_ssn	B	21
spi_1_tx	O	22
spi_1_rx	I	23
chax	I	24
chbx	I	25
chix	I	26
chay	I	27
chby	I	28
chiy	I	29
chaz	I	30
chbz	I	31
chiz	I	32
clk_1p28m	O	33
adcc_dmic_out	I	34

Table 9: Peripheral IO mapped through IOMUX

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: JTAG, analog I/Os (ADC inputs), GPIO, and key scan. When they are enabled, their IOs are mapped to physical pads according to the following table (by default JTAG is enabled).

QFN48	QFN32					Name
0	√	GPIO_P00	jtag_dout	GPIO		mk_in[0]
1	√	GPIO_P01	jtag_din	GPIO		mk_out[0]
2	√	GPIO_P02	jtag_tm	GPIO		mk_in[1]
3	√	GPIO_P03	jtag_clk	GPIO		mk_out[1]
4		GPIO_P04	GPIO			mk_out[9]
5		GPIO_P05	GPIO			mk_in[10]
6		GPIO_P06	GPIO			mk_out[10]
7		GPIO_P07	GPIO			mk_in[11]
8	√	TEST_MODE				
9	√	GPIO_P09	GPIO			mk_out[4]
10	√	GPIO_P10	GPIO			mk_in[4]
11		GPIO_P11	GPIO		analog_io[0]	mk_out[11]
12		GPIO_P12	GPIO		analog_io[1]	mk_in[12]
13		GPIO_P13	GPIO		analog_io[2]	mk_out[12]
14	√	GPIO_P14	GPIO		analog_io[3]	mk_out[2]
15	√	GPIO_P15	GPIO		analog_io[4]	mk_in[2]
16	√	GPIO_P16	XTALI(ANA)	GPIO		mk_out[16]
17	√	GPIO_P17	XTALO(ANA)	GPIO		mk_out[17]
18	√	GPIO_P18	GPIO		analog_io[7]	mk_in[5]
19		GPIO_P19	GPIO		analog_io[8]	mk_in[13]

QFN48	QFN32					Name
20	√	GPIO_P20	GPIO		analog_io[9]	mk_out[5]
21		GPIO_P21	GPIO			mk_out[13]
22		GPIO_P22	GPIO			mk_in[14]
23	√	GPIO_P23	GPIO			mk_in[6]
24	√	GPIO_P24	GPIO			mk_out[3]
25	√	GPIO_P25	GPIO			mk_in[3]
26		GPIO_P26	GPIO			mk_out[14]
27		GPIO_P27	GPIO			mk_in[9]
28		GPIO_P28	GPIO			mk_out[8]
29		GPIO_P29	GPIO			mk_in[15]
30		GPIO_P30	GPIO			mk_out[15]
31	√	GPIO_P31	spi_t_ssn	GPIO		mk_out[7]
32	√	GPIO_P32	spi_t_rx	GPIO		mk_in[7]
33	√	GPIO_P33	spi_t_tx	GPIO		mk_out[6]
34	√	GPIO_P34	spi_t_sck	GPIO		mk_in[8]

Table 10: Peripheral IO mapped through IOMUX (special purpose)

In the IOMUX table above, the first column is the IO pad mapping in default mode, when no IOMUX function is selected and no special purpose peripherals such as analog IO, GPIO<0:3>, key scan, are enabled. In this mode, pin<0:3> are used for JTAG.

When analog IOs are enabled, pins<11:15>, <18:20> are connected to internal analog IOs. More specifically, analog_io<0:4><9> are connected to ADC inputs, analog_io<7,8> are connected to PGA inputs.

In JTAG mode, data output for JTAG test mode is mapped to P00; data input for JTAG test mode is mapped to P01; mode control input for JTAG test mode is mapped to P02; clock input for JTAG test mode is mapped to P03.

3.10 GPIO

The General Purpose I/Os are a type of peripheral that can be mapped to physical I/O pads and programmed by software. The flexible GPIO are organized as two PORTs. Among them, PortA has bi-direction 18 bit lines, e.g., GPIO_PORTA[17:0], while PortB has 17 bi-directional bit lines, e.g., PIO_PORTB[16:0]. With default setting, physical pads: P00-P17 are connected to PortA; Pads P18-34 are connected to PortB, when all GPIOs are enabled, as described in the IOMUX table in IOMUX section.

All PortA and PortB pins can be configured as bi-directional serial interface, by selecting as input or output direction, and their corresponding data can be either read from or written to registers. All PortA and PortB pins support wake-up, but only 18 PortA pins support interrupt. Also only PortA pins support debounce function.
Each GPIO pins can be pulled up to AVDD33 or pulled down to ground by adding pull up or pull down resistors to have default functions/states.

For more detailed info, please refer to “PHY62xx GPIO Application Notes”, in software SDK document folder.

#	QFN48	QFN32	Default MODE	Default IN_OUT	IRQ	Wakeup	ANA_IO
0	GPIO_P00	√	jtag_dout	OUT	√	√	
1	GPIO_P01	√	jtag_din	IN	√	√	
2	GPIO_P02	√	jtag_tm	IN	√	√	
3	GPIO_P03	√	jtag_clk	IN	√	√	
4	GPIO_P04		GPIO	IN	√	√	
5	GPIO_P05		GPIO	IN	√	√	
6	GPIO_P06		GPIO	IN	√	√	
7	GPIO_P07		GPIO	IN	√	√	
8	TEST_MODE	√					
9	GPIO_P09	√	GPIO	IN	√	√	
10	GPIO_P10	√	GPIO	IN	√	√	
11	GPIO_P11		GPIO	IN	√	√	ADC_CH1N_P11
12	GPIO_P12		GPIO	IN	√	√	ADC_CH1P_P12
13	GPIO_P13		GPIO	IN	√	√	ADC_CH2N_P13
14	GPIO_P14	√	GPIO	IN	√	√	ADC_CH2P_P14
15	GPIO_P15	√	GPIO	IN	√	√	ADC_CH3N_P15
16	GPIO_P16	√	XTALI(ANA)	ANA	√	√	
17	GPIO_P17	√	XTALO(ANA)	ANA	√	√	
18	GPIO_P18	√	GPIO	IN		√	
19	GPIO_P19		GPIO	IN		√	
20	GPIO_P20	√	GPIO	IN		√	ADC_CH3P_P20
21	GPIO_P21		GPIO	IN		√	
22	GPIO_P22		GPIO	IN		√	
23	GPIO_P23	√	GPIO	IN		√	
24	GPIO_P24	√	GPIO	IN		√	
25	GPIO_P25	√	GPIO	IN		√	
26	GPIO_P26		GPIO	IN		√	
27	GPIO_P27		GPIO	IN		√	
28	GPIO_P28		GPIO	IN		√	
29	GPIO_P29		GPIO	IN		√	
30	GPIO_P30		GPIO	IN		√	
31	GPIO_P31	√	**phyplus_spi_t_ssn**	IN		√	
32	GPIO_P32	√	**phyplus_spi_t_rx**	IN		√	
33	GPIO_P33	√	**phyplus_spi_t_tx**	OUT		√	
34	GPIO_P34	√	**phyplus_spi_t_sck**	IN		√	

Table 11: PHY62xx GPIO Application Notes

3.10.1 DC Characteristics

T_A=25℃, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 12: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with Bluetooth LE 5.2 protocol implementations.

- General modulation format
    - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
    - OQPSK with half-sine shaping
    - On-air data rates
    - 125kbps/250kbps/500kbps/1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
    - -103dBm@125Kbps GFSK
    - -98dBm@500Kbps GFSK
    - -97dBm@1Mbps BLE
    - -94dBm@2Mbps BLE
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 24-bit SysTick system timer, that extends the functionality of both the processor and the NVIC. When present, the NVIC part of the extension provides:

- A 24-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.
- See the ARMv7-M ARM for more information.

General purpose timers are included in the design. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers based on internal thermal noise. These random numbers are suitable for cryptographic purposes. The RNG does not require a seed value.

4.6 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.7 SPI (SPI)

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. SPI wrapper contains one SPI master and one SPI slave. They are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
1	0	SPI1 is master mode when set
0	0	SPI0 is master mode when set

Table 13: PERI_MASTER_SELECT Register bit definition (base address = 0x4000_302C)

4.8 I2C (I2c0, I2c1 Two Independent Instances)

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.9 I2S

I2S wrapper contains one I2S master and one I2S slave. They are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
3	0	I2S1 is master mode when set
2	0	I2S0 is master mode when set

Table 14: PERI_MASTER_SELECT Register bit definition (base address = 0x4002_302C)

4.10 UART (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin out and enables efficient use of

board space and signal routing.

4.11 DMIC/AMIC Data Path

The voice in interface supports one analog MIC (SAR-ADC) and two digital MIC (L+R), different output sample rate (64KHz, 32KHz, 16KHz and 8KHz), and different voice compress algorithm. For the Digital MIC, PDM signal is sampled at 1.28MHz(4x320KHz). L channel is sampled at raising edge, R channel is sampled at falling edge. For PCM-LOG and CVDS, output data rate is 64Kbps (8KHz x 8bit).

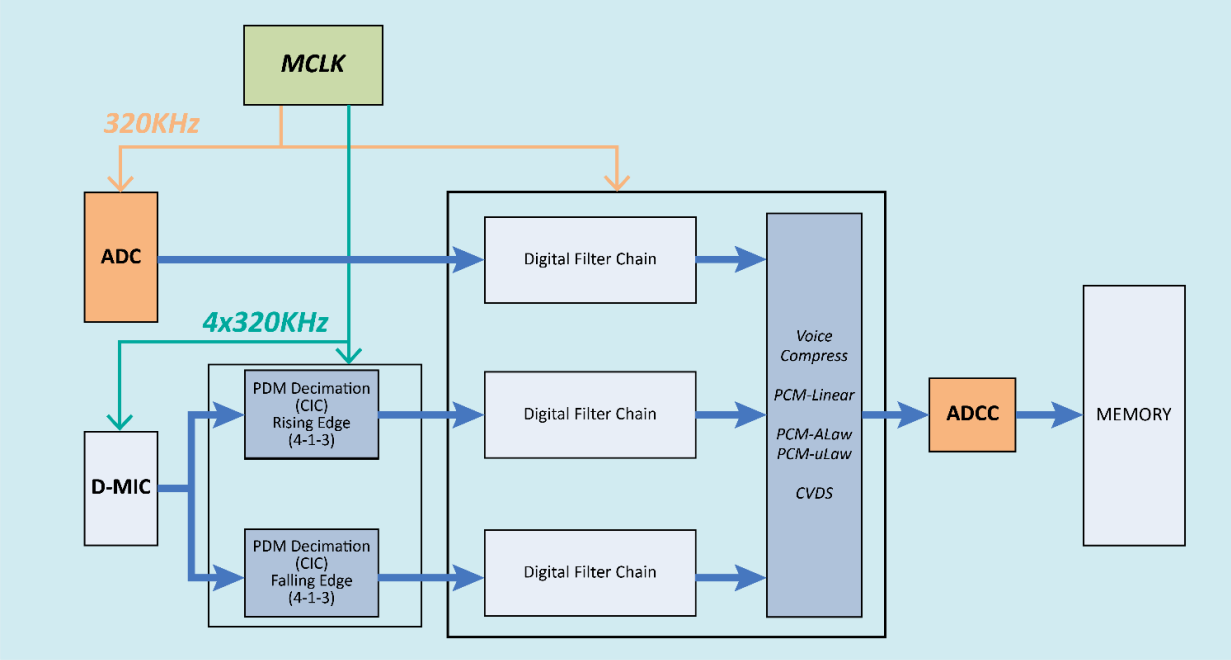


Figure 12: Block Diagram of Voice In Interface

4.11.1 Filter Chain Design

For D-MIC input, PDM Decimation (CIC) will convert the 1-bit PDM signal to 12 bit PCM signal. And the sample rate will be converted from 1.28MHz to 320KHz. The output data of the PDM Decimation will be connected to the Digital Filter chain.

For the A-MIC input, SAR-ADC will convert the signal to 12bit 320KHz digital samples. The Digital Filter chain will process the data same as the D-MIC path.

The Output sample rate of the Digital filter chain is programmable. 64KHz, 32KHz, 16KHz, 8KHz. The maximum value of the sample's bit-width is 16bit.

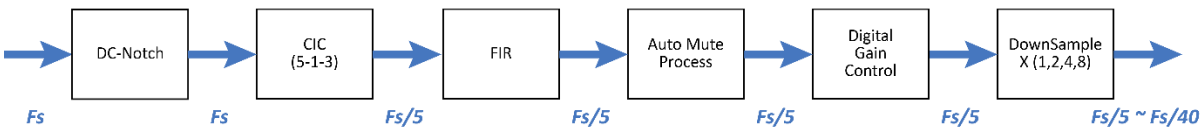


Figure 13: Digital Filter Chain

4.11.2 Auto Mute Process

Signal Level Estimate will check the input signal level with configurable window size. Mute threshold can be updated according to the signal level estimation or being configured by the register. There are two thresholds, one for MUTE_ON, another for MUTE_OFF. Gain step of MUTE_ON and MUTE_OFF can be configured individually.

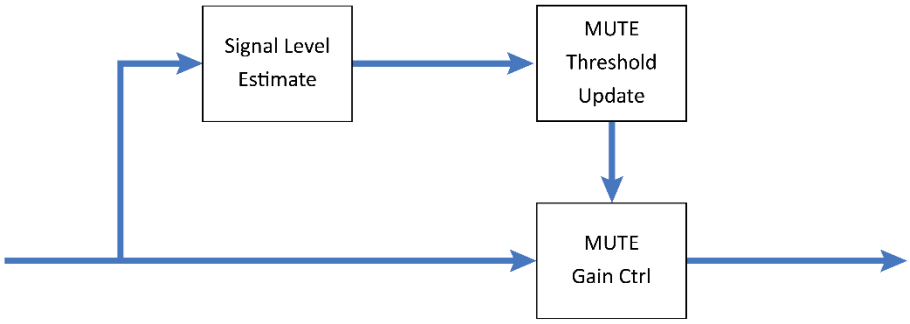


Figure 14: Auto Mute Process

4.11.3 Digital Gain Control

Digital gain is implemented by one Look up table. The gain error has been controled within 0.05dB.

4.11.4 Voice Compression

PCM-LOG support u-Law and a-Law. According to the ITU-G711 standard. The input data is 13~14bit @ 8KHz. The output data is 8bit @ 8KHz, 64Kbps. Also, it support 64Kbps CVSD according to the BT standard. Its Input is 16bit @64KHz, and its output is 1bit @ 64KHz. PCM-Linear is for the raw data without compression.

4.12 Pulse Width Modulation (PWM)

Phy62xx supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

Duty_cycle_PWM = N_threshold/N_top_count;

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following Figure 13, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers 0x4000_E000<0><4> to allow all PWM channels can be programmed. For details please refer to documents of PHY62xx register tables.

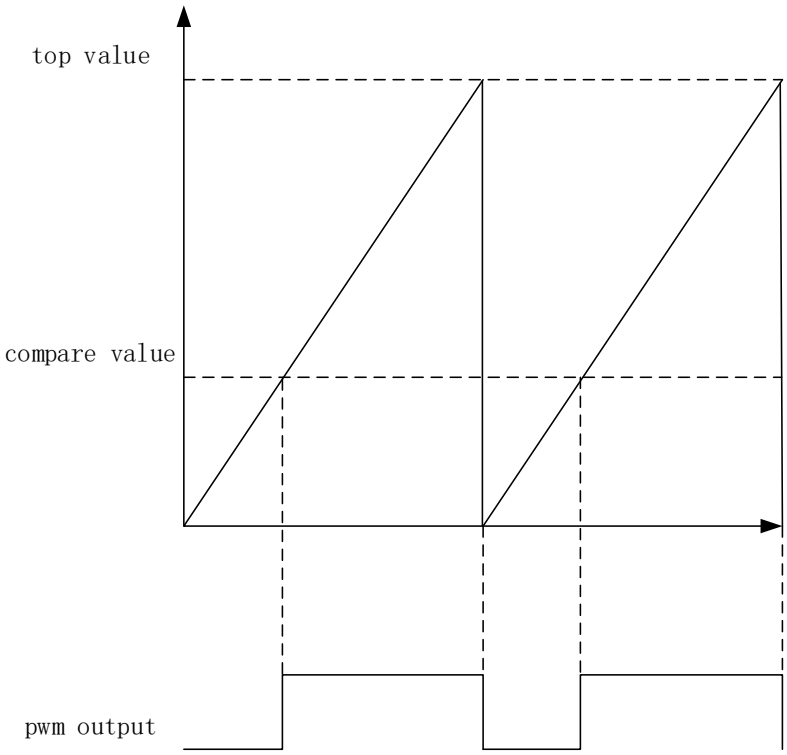


Figure 15: PWM operation

4.13 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals with input debounce filters. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The quadrature decoder has three-axis capability and index channel support. It can be programmed as 4x/2x/1x count mode.

4.14 Key Scan (KSCAN)

Keyscan supports key matrix with upto 16 rows by 18 columns. Each individual rows or columns can be enabled or disabled through register settings. GPIO pins can be configured to be used for key scan. A few key scan Parameters can be set through registers, including polarity (low or high indicating key pressed); support multi-key-press or only single-key-press; de-bounce time (the time duration a key press is deemed valid) from 0 to 128mS with 255us step.

A valid key press can trigger an interrupt when keyscan interrupt is enabled. After a keyscan interrupt

is serviced, writing 1 to the interrupt state register bit can clear the state bit.

The keyscan has a manual mode and an auto mode. For manual mode, when a keyscan interrupt is received, it is upo the MCU/software to scan the keyscan output pins and check the input pins, to determine which keys have been pressed. Manual mode is relatively slow and need CPU to process. On the contrary, in automode keyscan will automatically scan the output/input pins, and store the row/column info corresponding to the key pressed into read only registers, then trigger an interrupt for software to retrieve key press information.

4.15 Analog to Digital Converter (ADC) with Programmable Gain Amplifier (PGA)

The 12bit SAR ADC has total 10 inputs. Among them, there are two for PGA inputs, and two differential inputs for the on-chip temperature sensor. The other six inputs can be programmed to 3 pair differential inputs or six single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with a specific ADC clock rate. There is also an auto sweep mode, namely all enabled input channels can be swept automatically in order by the ADC and the converted data will be stored at corresponding memory locations.

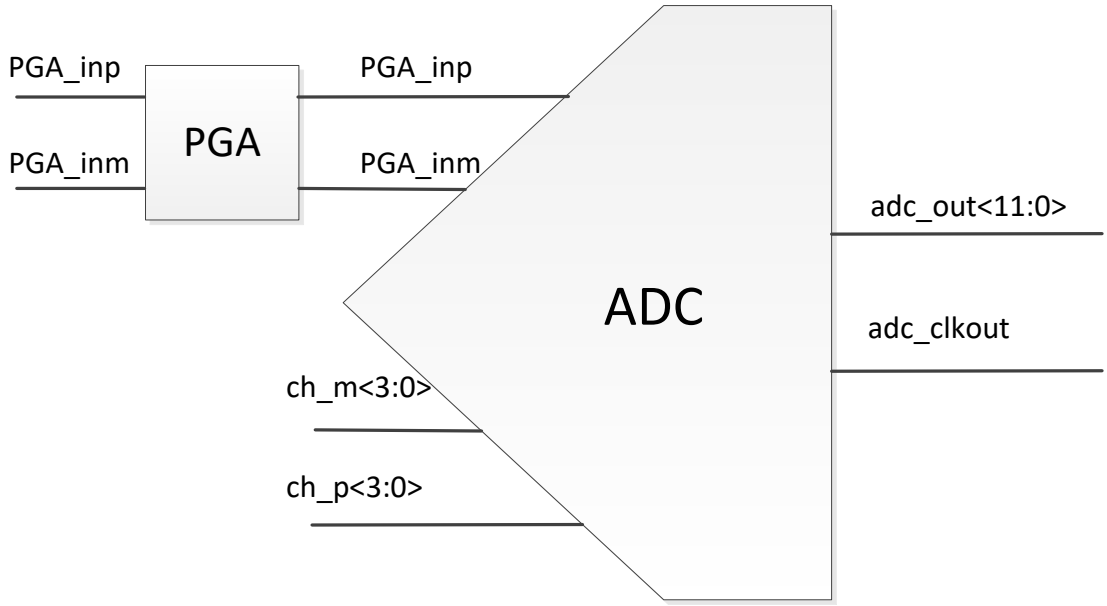


Figure 16: ADC

4.15.1 PGA Path

The PGA provides 42dB gain range from 0dB to 42dB in 3dB steps.

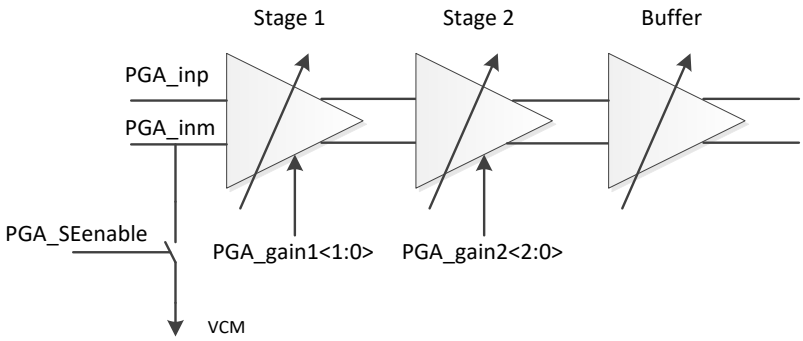


Figure 17: PGA path

pga_gain1<1>	pga_gain1<0>	Stage1 gain (dB)	pga_gain2<2>	pga_gain2<1>	pga_gain2<0>	Stage2 gain(dB)
0	0	0	0	0	0	0
0	1	12	0	0	1	3
1	0	24	0	1	0	6
			0	1	1	9
			1	0	0	12
			1	0	1	15
			1	1	0	18

Table 15: PGA gain

Set PGA_SEenable to “1”, PGA will be set to Single-ended mode by pulling the PGA into its Common-mode voltage.

4.15.2 ADC Path

By default the ADC is configured in manual mode. In this mode, the ADC clock rate can be configured to 80k/160k/320k sample per second. Select the pair of inputs and configure it to differential or singled-ended (positive or negative). By default it is differential. After enabling, the ADC will take samples with the configured clock rate and store the data to a channel dependent memory location. For each channel a memory size of 128Byte is allocated, when it is full an interrupt bit will be flagged. Each sample of 12bits takes 2 Byte memory space.

0x4000_F07C		Register Description
[4]	adc_ctrl_override	Set manual mode: 1: manual, 0: auto. Default 1
[3]	adc_tconv_sel	For auto mode only, adc conversion time sel: 0: 1.56us, 1: 2.34us
[2:1]	adc_clk_sel	For manual mode only, clksel: 00: 80k, 01: 160k, 10: 320k
[0]	max_rate_256k_320k	For auto mode only, max rate base: 0, 256k, 1, 320k
0x4000_F048		**Register Description**
[11]	adc12b_semode_enm	For manual mode only: 12 bit ADC signle-ended mode negative side enable. Bit<11> Bit<8> cannot both be 1; 1: Enable single-ended mode 0: Differential mode

[8]	Adc12b_semode_epm	For manual mode only: 12 bit ADC signle-ended mode positive side enable. Bit<8> Bit<11> cannot both be 1; 1: Enable single-ended mode 0: Differentail mode
[7:5]	Channel configure	For manual mode only: 12 bit ADC input channel select control bits. adc12_ctrl<3:1> Selected channel 000 PGA inputs, differential 001 Temperature sensing inputs, differential 010 input A, positive and negative 011 input B, positive and negative 100 input C, positive and negative
[3]	ADC enable	12b ADC power up control. 1: Power up ADC 0: Power down ADC

Memory start/end addresses	ADC channels
4005_0400 – 4005_047F	PAG inputs, differential
4005_0480 – 4005_04FF	Temperature sensing, differential
4005_0500 – 4005_057F	Input A, positive or differential
4005_0580 – 4005_05FF	Input A, negative
4005_0600 – 4005_067F	Input B, positive or differential
4005_0680 – 4005_06FF	Input B, negative
4005_0700 – 4005_077F	Input C, positive or differential
4005_0780 – 4005_07FF	Input C, negative

0x4005_003C	ADC interrupt status	Register Description
[7]		input C, negative
[6]		Input C, positive or differential
[5]		Input B, negative
[4]		Input B, positive or differential
[3]		Input A, negative
[2]		Input A, positive or differential
[1]		Temperature sensing, differential
[0]		PGA inputs, differential

0x4005_0038	ADC interrupt write clear	Register Description
[7]		input C, negative, write 1 to clear
[6]		Input C, positive or differential, write 1 to clear
[5]		Input B, negative, write 1 to clear
[4]		Input B, positive or differential, write 1 to clear
[3]		Input A, negative, write 1 to clear
[2]		Input A, positive or differential, write 1 to clear

0x4005_0038	ADC interrupt write clear	Register Description
[1]		Temperature sensing, differential, write 1 to clear
[0]		PGA inputs, differential, write 1 to clear

Table 16: ADC manual mode

ADC can also be configured into auto channel sweep mode by setting the “adc_ctrl_override” bit to 0, with which the enabled channels will be sampled in the configured order automatically. The ten ADC input channels can be configured by programming their corresponding registers. Their configurations include sampling time, enable/disable, differential/single-ended, and continuous sampling/single-shot, based on the following register table. The sampled data is stored in the corresponding memory locations as in manual mode.

0x4000_F06C	ADC_CTL0	Register Description
[31:16]	Temperature sensing, auto mode, differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	PGA inputs, differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x4000_F070	**ADC_CTL1**	**Register Description**
[31:16]	Inputs A, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input A, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x4000_F074	**ADC_CTL2**	**Register Description**
[31:16]	Input B, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

0x4000_F074	ADC_CTL2	Register Description
[15:0]	Input B, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one

		shot 1. For auto channel sweep mode only

0x4000_F078	ADC_CTL3	Register Description
[31:16]	Input C, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	Input C, positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

Table 17: ADC channel configurations

4.15.3 ADC Channel <3:0> Connectivity

PGA inputs	hardwired
temp sensing	hardwired
aio<0>	Input A negative
aio<1>	Input A positive
aio<2>	Input B negative
aio<3>	Input B positive
aio<4>	Input C negative
aio<9>	Input C positive

Table 18: ADC channel connectivity

Aio<9, 4:0> and PGA inputs(Aio<7:8>) can be selected through an analog Mux by programming aio_pass<7:0> or aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input A positive node.

0x4000_F020		Register Description

[13:8]	Attenuation ctrl	attn[5:0]. analogIO control for {aio<9>, aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass 10 attenuate to 1/4 11 NC
[5:0]	pass ctrl	pass[5:0]. analogIO control for {aio<9>, aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<11>/aio<0> gpio<12>/aio<1> gpio<13>/aio<2> gpio<14>/aio<3> gpio<15>/aio<4> gpio<16>/aio<5>/32K XTAL input gpio<17>/aio<6>/32K XTAL output gpio<18>/aio<7>/pga in+ gpio<19>/aio<8>/pga in- gpio<20>/aio<9>/mic bias

Table 19: analog Mux

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which PHY6212 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the PHY6212. **Table 20** specifies the absolute maximum ratings for PHY6212.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDMQF	Charged Device Model (QFN48, 7x7 mm package)		500	V
Flash memory				
Endurance			100 000	write/erase cycles
Retention			10 years at 40 °C	
Number of times an address can be written between erase cycles			2	times

Table 20: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that PHY6212 can operate within as defined in **Table 21**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA					
	Operating temperature (consumer)	-40	27	85	°C
	Operating temperature (Industrial)	-40	27	105	°C

Table 21: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	with internal DC-DC @3V		6.7		mA
Rx Only	with internal DC-DC @3V		6.7		mA

Table 22: Radio current consumption

7.2 Transmitter Specification

7.2.1 BLE TX

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
OBW for GFSK 500Kbps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
OBW for GFSK 125bps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
Error Vector Measure	Offset EVM for OQPSK modulation		0.02		
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 23: BLE Transmitter specification

7.3 Receiver Specification

7.3.1 BLE 1Mbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-97		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB

Parameter	Description	MIN	TYP	MAX	UNIT
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 24: BLE 1Mbps GFSK RX

7.3.2 BLE 2Mbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-94		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 25: BLE 2Mbps GFSK RX

7.3.3 BLE 500Kbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 500Kbps BLE ideal transmitter, 37 Byte BER=1E-3		-98		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-4		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/-1MHz, 37 Byte BER=1E-3		10		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/-2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/-3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/-4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		24		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte Ber=1E-3		-19		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 26: BLE 500Kbps GFSK RX

7.3.4 BLE 125Kbps GFSK RX

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 125Kbps BLE ideal transmitter, 37 Byte BER=1E-3		-103		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-1		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/-1MHz, 37 Byte BER=1E-3		-11		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/-2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/-3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/-4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB

Parameter	Description	MIN	TYP	MAX	UNIT
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		28		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-18		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 27: BLE 125Kbps GFSK RX

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 28: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus (ARM bus standard)
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus (ARM bus standard)
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port (ARM bus standard)
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SWD	Serial Wire DAP (ARM bus standard)
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 29: Glossary

9 Ordering information

9.1 Chip Marking Example

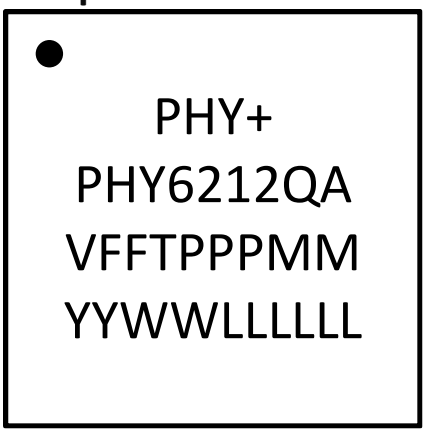


Figure 18: Chip Marking Example

9.2 Chip Marking Rule

<PHY+>
<PHY6212><XX>
<V><FF><T><PPP><MM>
<YY><WW><LLLLLL>

Figure 19: Chip Marking Rule

Abbreviation	Definition and Implemented Codes
<PHY+>	PHYPLUS MICROELECTRONIC
<PHY6212>	PHY6212 Product
<XX>	Package Type
<V>	Supply Voltage
<FF>	Flash Size
<T>	Operating Temperature
<PPP>	Product Information
<MM>	Manufacturer Information
<YY>	2-digital Year Code
<WW>	2-digital Week Code
<LLLLLL>	6-digital Wafer Lot Code

Table 30: Chip Marking Rule

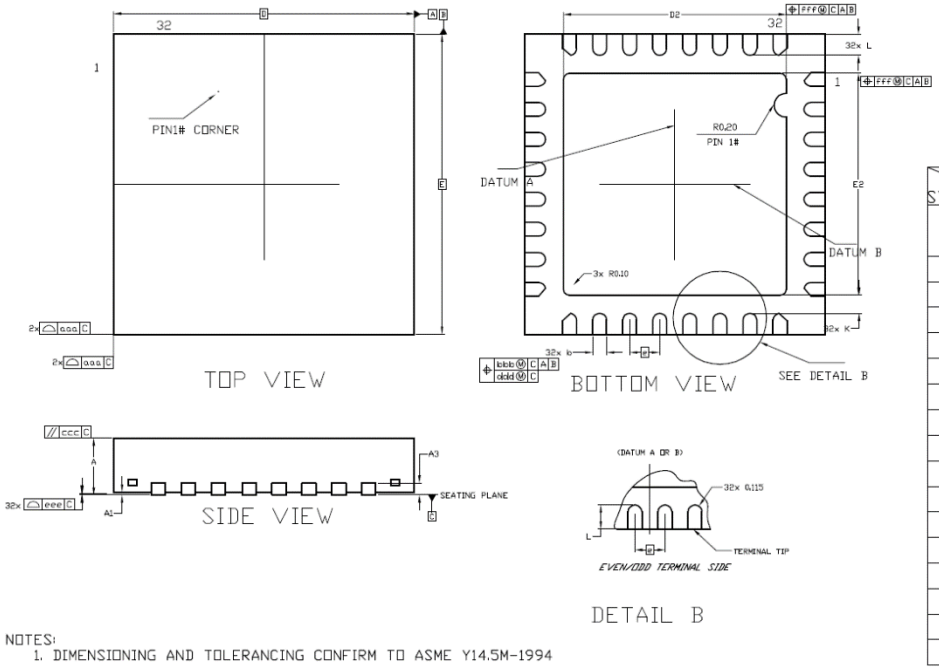
9.3 Order Code

Part No.	Package	Supply Voltage	Operating Temp. (°C)	Flash	Packing	Quantity (PCS/R)	MOQ (PCS)
PHY6212QA-W04I	QFN32 (5x5)	1.8~3.6V	-40~105	512KB	Reel	5000	5000
PHY6212QA-W04C	QFN32 (5x5)	1.8~3.6V	-40~85	512KB	Reel	5000	5000
PHY6212MAQA-UC	QFN32 (5x5)	1.8~3.6V	-40~85	512KB	Reel	5000	5000
PHY6212MAQA-PD	QFN32 (5x5)	1.8~3.6V	-40~85	512KB	Reel	5000	5000
PHY6212MAQA	QFN32 (5x5)	1.8~3.6V	-40~105	512KB	Reel	5000	5000
PHY6212MAQB	QFN48 (7x7)	1.8~3.6V	-40~105	512KB	Reel	2500	2500

Table 31: Order Code

10 Package dimensions

10.1 QFN32 package dimensions

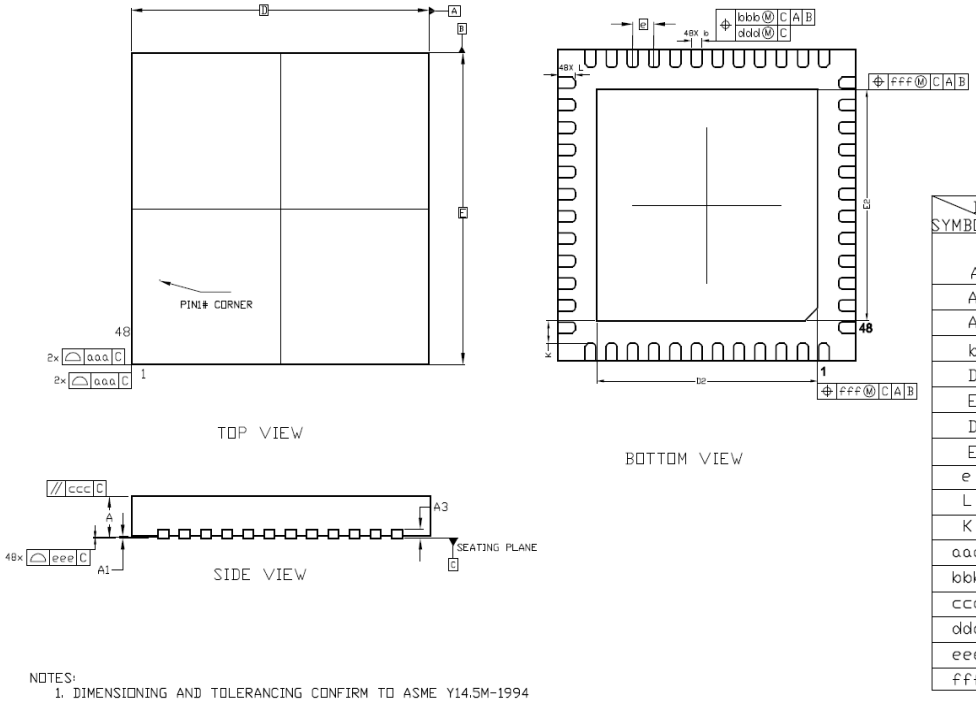


DIM / SYMBOL	MIN.	NOM.	MAX.
	0.70	0.75	0.80
A	0.85	0.90	0.95
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.18	0.23	0.28
D		5.00BSC	
E		5.00BSC	
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e		0.50BSC	
L	0.30	0.35	0.40
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 20: QFN32 package dimensions

Note: dimensions are in mm, angels are in degree.

10.2 QFN48 package dimensions



DIM / SYMBOL	MIN.	NOM.	MAX.
	0.70	0.75	0.80
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.20	0.25	0.30
D		7.00BSC	
E		7.00BSC	
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e		0.50BSC	
L	0.35	0.40	0.45
K	0.50	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 21: QFN48 package dimensions

Note: dimensions are in mm, angels are in degree.

11 Sample Application and Layout Guide

11.1 Sample Application

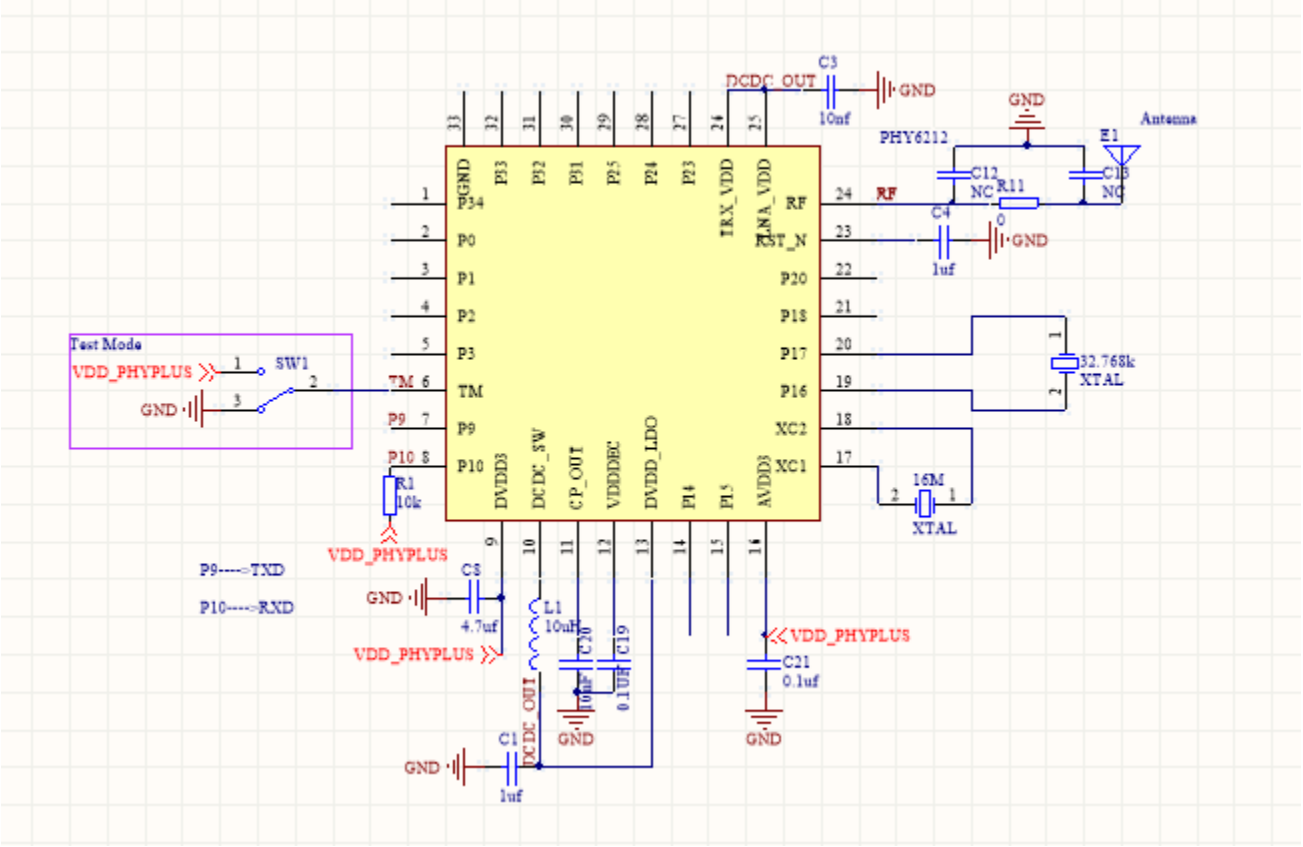


Figure 22: Sample application

11.2 Layout Guide

11.2.1 Placement

1. RF matching/Loop filter leading to antenna should be isolated from any other AC/DC signal as much as possible;
2. Xtal/OSC clock is a noise source to other circuits, keep clock trace as short as possible and away from any important area;
3. LDO's are sensitive and could be easily contaminated, care should be taken for the environment;
4. Antenna is the main RF radiation point, other important blocks should be shielded or away from this area.

RF traces

1. Define RF line width with given dielectric thickness (thickness of PCB dielectric layer to ground plain) to achieve 50ohm impedance; this is mainly for the RF line connecting to matching/loop filter and antenna.
2. Differential traces should be kept in the same length and component should be placed symmetrically;
3. Certain length of RF trace should be treated as part of RF matching.

11.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to the pin.
4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

11.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be “Ground ” layer , for both signal ground and RF reference ground , DO NOT put any other trace or plane on second layer, otherwise “antenna effect” will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for “signal ” layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

11.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

11.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.
2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace , the strong clock or RF signal would travel with power line.

11.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible , too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.